A. **Appendix for as1805 Frankenstein Assembler**

A.1 **Pseudo Operations**

A.1.1 ***Standard_Pseudo_Operation_Mnemonics***

End	END
File Inclusion	INCL INCLUDE
If	IF
Else	ELSE
End If	ENDI
Equate	EQU
Set	SET
Org	ORG
Reserve Memory	RESERVE RMB
Define Byte Data	BYTE DB FCB
Define Word Data	DW FDB WORD
Define String Data	FCC STRING
Define Character Set Translation	CHARSET
Define Character Value	CHARDEF CHD
Use Character Translation	CHARUSE

A.2 **Instructions**

A.2.1 ***Instruction_List***

Opcode	Syntax	Selection Criteria
ADC		
ADCI	'#' expr	
ADD		
ADI	'#' expr	
AND		
ANI	'#' expr	
B1	expr	
B2	expr	
B3	expr	
B4	expr	
BCI	expr	TS1805

Opcode	Syntax	Selection Criteria
BDF	expr	
BGE	expr	
BL	expr	
BM	expr	
BN1	expr	
BN2	expr	
BN3	expr	
BN4	expr	
BNF	expr	
BNQ	expr	
BNZ	expr	
BPZ	expr	
BQ	expr	
BR	expr	
BXI	expr	TS1805
BZ	expr	
CID		TS1805
CIE		TS1805
DACI	'#' expr	TS1805
DADC		TS1805
DADD		TS1805
DADI	'#' expr	TS1805
DBNZ	expr ',' expr	TS1805
DEC	expr	
DIS		

Opcode	Syntax	Selection Criteria
DSAV		TS1805
DSBI	'#' expr	TS1805
DSM		TS1805
DSMB		TS1805
DSMI	'#' expr	TS1805
DTC		TS1805
ETQ		TS1805
GEC		TS1805
GHI	expr	
GLO	expr	
IDL		
INC	expr	
INP	expr	
IRX		
LBDF	expr	
LBNF	expr	
LBNQ	expr	
LBNZ	expr	
LBQ	expr	
LBR	expr	
LBZ	expr	
LDA	expr	
LDC		TS1805
LDI	'#' expr	

Opcode	Syntax	Selection Criteria
LDN	expr	
LDX		
LDXA		
LSDF		
LSIE		
LSKP		
LSNF		
LSNQ		
LSNZ		
LSQ		
LSZ		
MARK		
NBR	expr	
NLBR	expr	
NOP		
OR		
ORI	'#' expr	
OUT	expr	
PHI	expr	
PLO	expr	
REQ		
RET		
RLDI	expr ',' '#' expr	TS1805
RLXA	expr	TS1805
RNX	expr	TS1805

Opcode	Syntax	Selection Criteria
RSHL		
RSHR		
RSXD	expr	TS1805
SAV		
SCAL	expr ',' expr	TS1805
SCM1		TS1805
SCM2		TS1805
SD		
SDB		
SDBI	'#' expr	
SDI	'#' expr	
SEP	expr	
SEQ		
SEX	expr	
SHL		
SHLC		
SHR		
SHRC		
SKP		
SM		
SMB		
SMBI	'#' expr	
SMI	'#' expr	
SPM1		TS1805

Opcode	Syntax	Selection Criteria
SPM2		TS1805
SRET	expr	TS1805
STM		TS1805
STPC		TS1805
STR	expr	
STXD		
XID		TS1805
XIE		TS1805
XOR		
XRI	'#' expr	

A.2.2 ***Selection_Criteria_Keywords***

TS1805	Instruction is only valid for the 1804A/1805A/1806A instruction sets.

A.2.3 ***Apostrophes*** The apostrophes in the syntax field are a notation used for the parser generator and are not put in the assembler source statement.

A.3 **Notes**

A.3.1 ***Instruction_Set_Selection*** The default is the 1805 instruction set. To restrict the instruction set, use the -p 1802 optional arguement on the command line, or rename or link the program file with a name containing the string 1802 (or just "02").

A.3.2 ***Register_and_Port_expressions*** The register and port numbers are specified as expressions. For registers, the value must be between 0 and 15 (1 and 15 for the LDN instruction). For input/output ports, the value must be between 1 and 7. The value must be computable when processed in the first pass. The SET and EQU statements can be used to setup symbols for registers and ports. It is recomended that a standard include file be setup to assign a set of symbols (like R0 to R15) for registers.

A.3.3 ***Branch_Target_Expression_Validity*** The "expression fails validity test" error message can occur if the destination of a short branch is not on the same page as the the last byte of the instruction. The "expression exceeds available field width" can also occur for this case. Usually the validity message occurs when the destination is at a lower page, and the width message occurs when the destination is at a higher page.

A.3.4 ***Immediate_Data*** The immediate data expressions for the RLDI (as well as the arithmetic and logic operations) are required to be on same line as the opcode.

A.3.5 ***Reserved_Symbols***

A.3.5.1 ***Standard_Reserved_Symbols*** AND DEFINED EQ GE GT HIGH LE LOW LT MOD NE NOT OR SHL SHR XOR and defined eq ge gt high le low lt mod ne not or shl shr xor

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