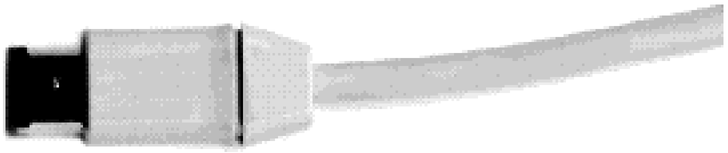
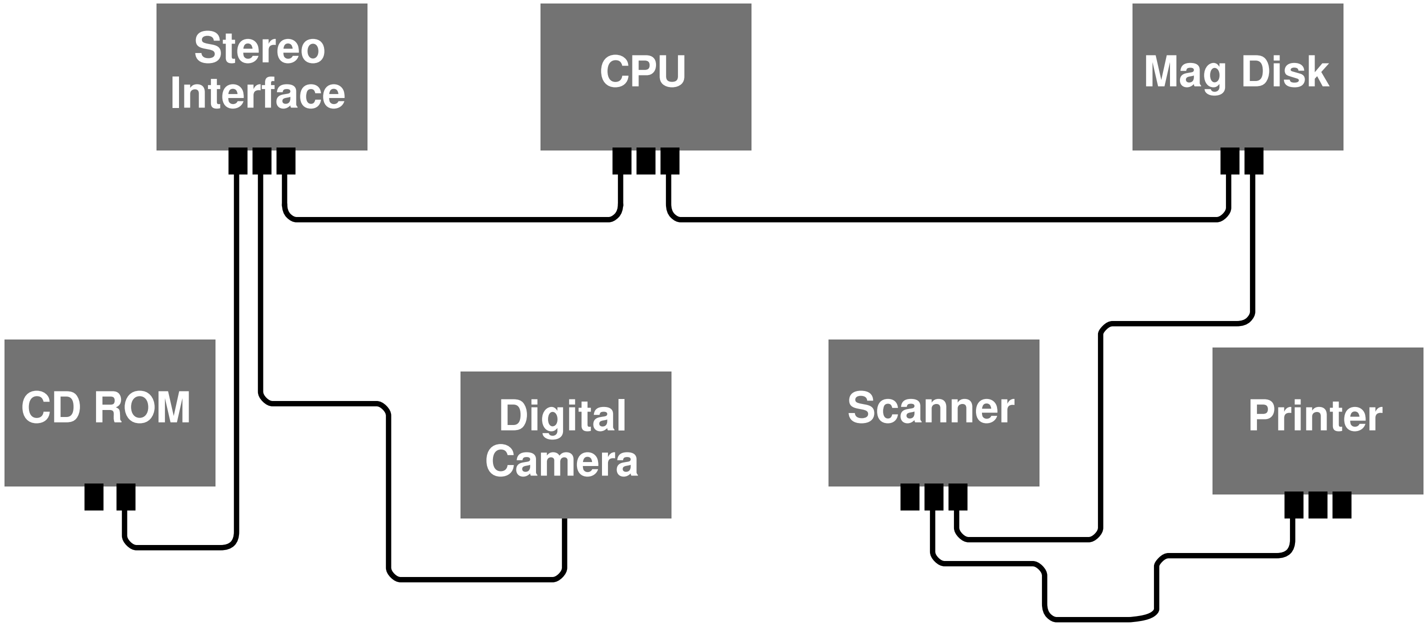
Serial Bus

Michael
Teener

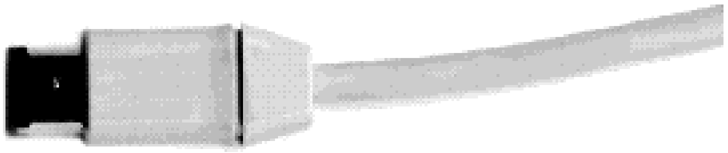
Plumbing Architect
408-974-3521
teener@apple.com

What is it?





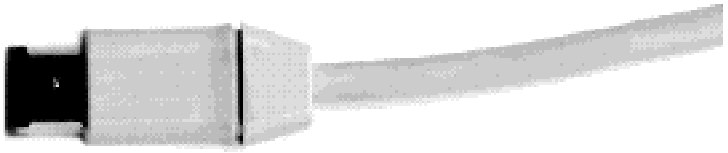
- Miniaturized ergonomic desktop bus
- Industry standard
- Provides the benefits of NuBus without slots
- Enables a new generation of QuickTime peripherals

Technical Details 

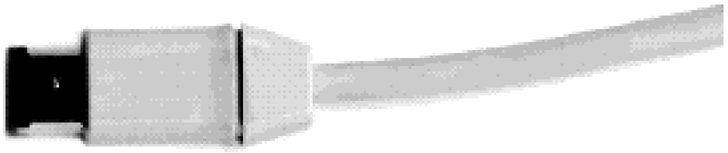
A small realtime connection that's faster than SCSI.

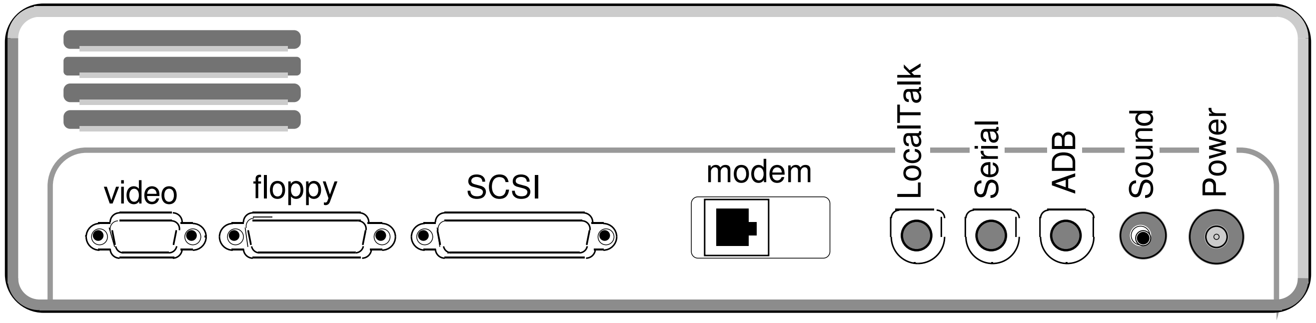
- **Easy to use:** hot plugging, no terminators or switches
- **Scalable:** ~100 Mbits/sec with growth path (2X, 4X)
- **Miniaturized:** small cable & connector at both ends
- **Realtime:** guaranteed latency for QuickTime™
- **Multimaster:** memory bus architecture with peer-to-peer transfers
- **System expansion:** a serial equivalent of NuBUS
- **Standard:** cross platform industry standard (IEEE P1394)

Key Benefits

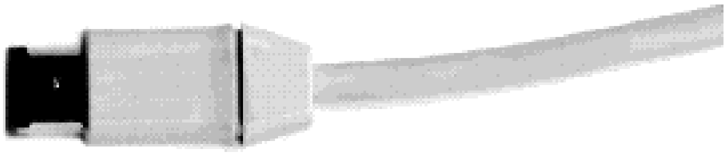


- **Provide a new class of desktop services**
  carry real-time data, e.g. audio and compressed video
  support peer-to-peer transactions between peripherals
  support more devices and more types of devices
- **Enhance existing I/O services**
  let devices move their data without burdening the CPU
  simplify software driver and controller models
- **Enable system miniaturization**
  consolidate most I/O functions into a single port
  permit attachment to small devices, e.g. microcamera

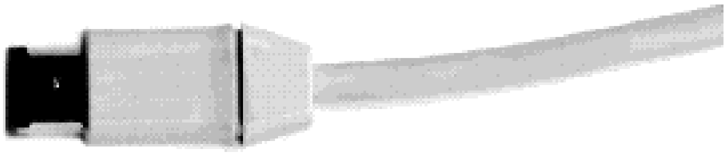
Background 



- **No I/O Integration**
  lots of PCB area, silicon & software
  no common architecture
- **Hard to change**
  no realtime transport
  performance not scalable

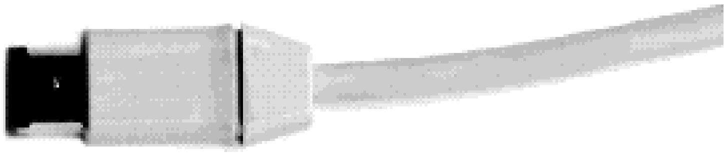
Goals 

- **Miniaturization**
  small cable & connector at both ends of wire
- **Integration**
  alternative to slots when space is a premium
  integrates power, control and data together
  fully digital and multimaster
- **Convenience**
  no terminator; no ID switches
  permits dynamic configuration

Goals (cont) 

- **Reliability**
  - 4.5 meter cables at fast/wide SCSI rates
  - true "plug-and-play" not "plug-and-pray"
  - meets EMC standards
- **Scalability**
  - performance scales with power consumption
  - permits mixed speeds over same cable plant
- **Value**
  - enables processing of streaming data
    - supports synchronization of multiple streams of data
    - always guarantees latency
  - ... at modest cost (comparable to today's SCSI)
  - ... with bandwith faster than "fast" SCSI

"Isochronous" ??

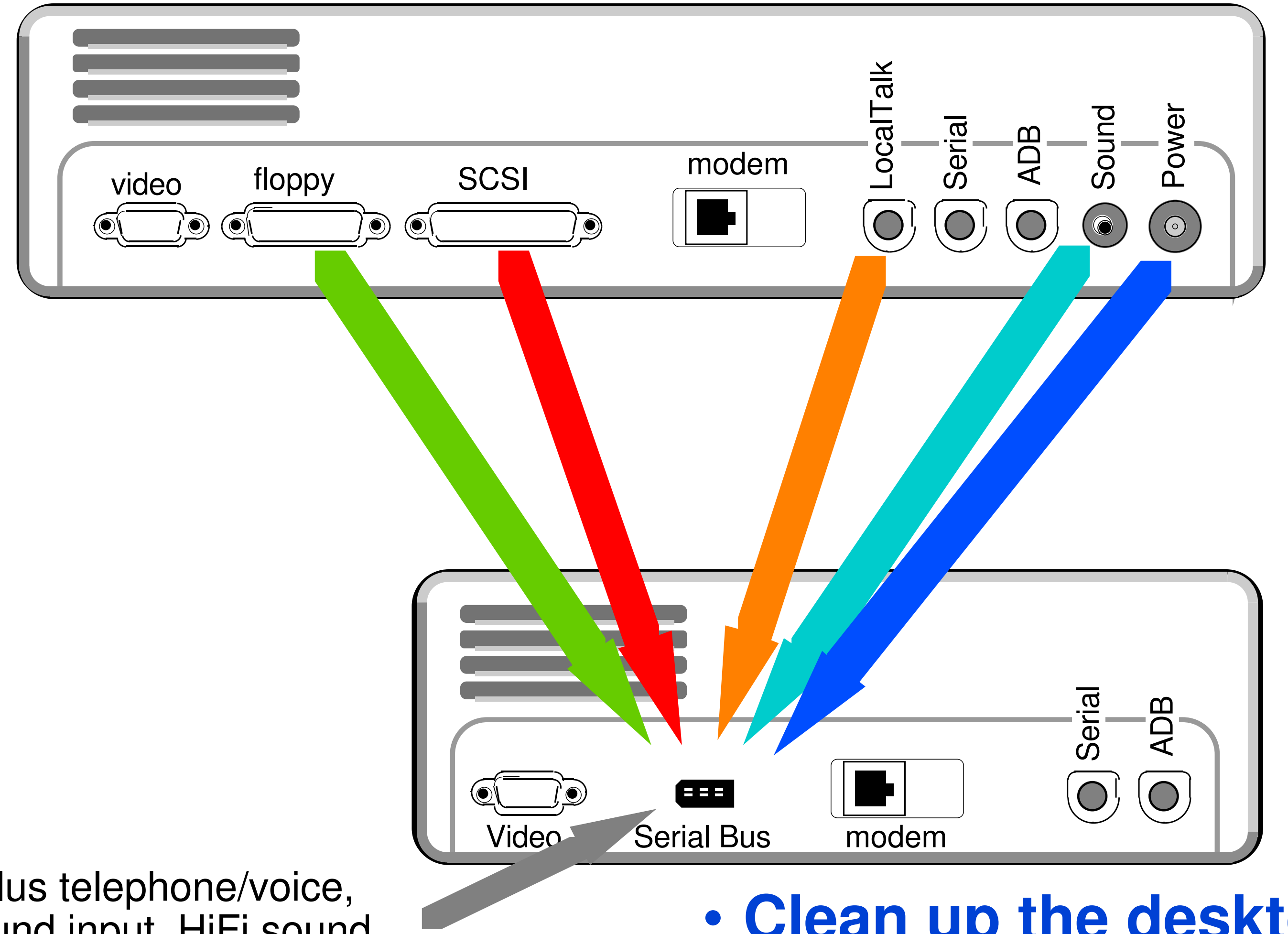


Iso (same) chronous (time)

- Uniform in time
- Having equal duration
- Recurring at regular intervals

Data Type	Sample size & rate	Bit rate
ISDN	8 kHz x 8 bits	64 kbps
CD	44.1 kHz x 16 bits x 2 channels	1.4 Mbps
DAT	48 kHz x 16 bits x 2 channels	1.5 Mbps
Video	15, 24, 25 or 30 fps	1.5 – 217 Mbps

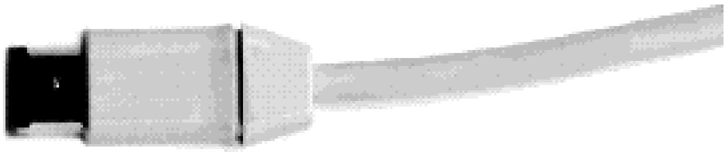
Goals (cont.)

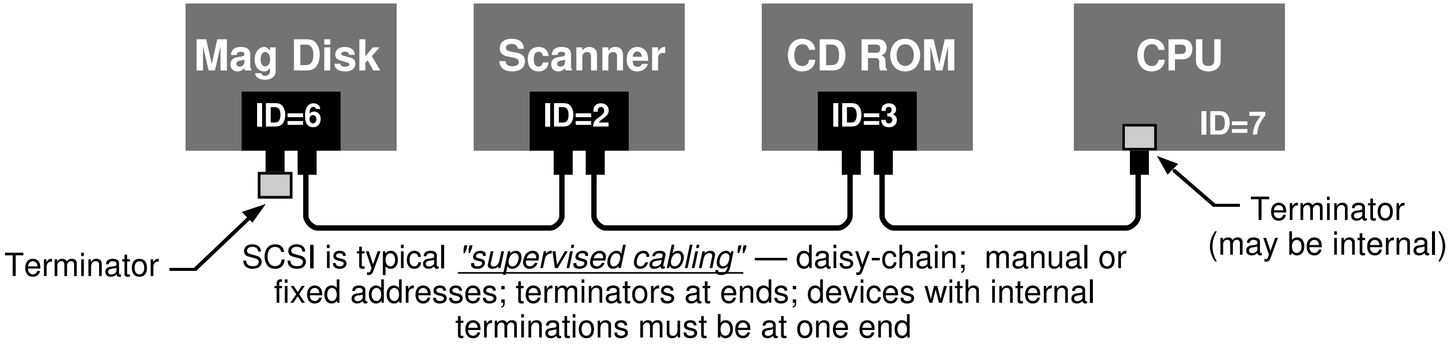


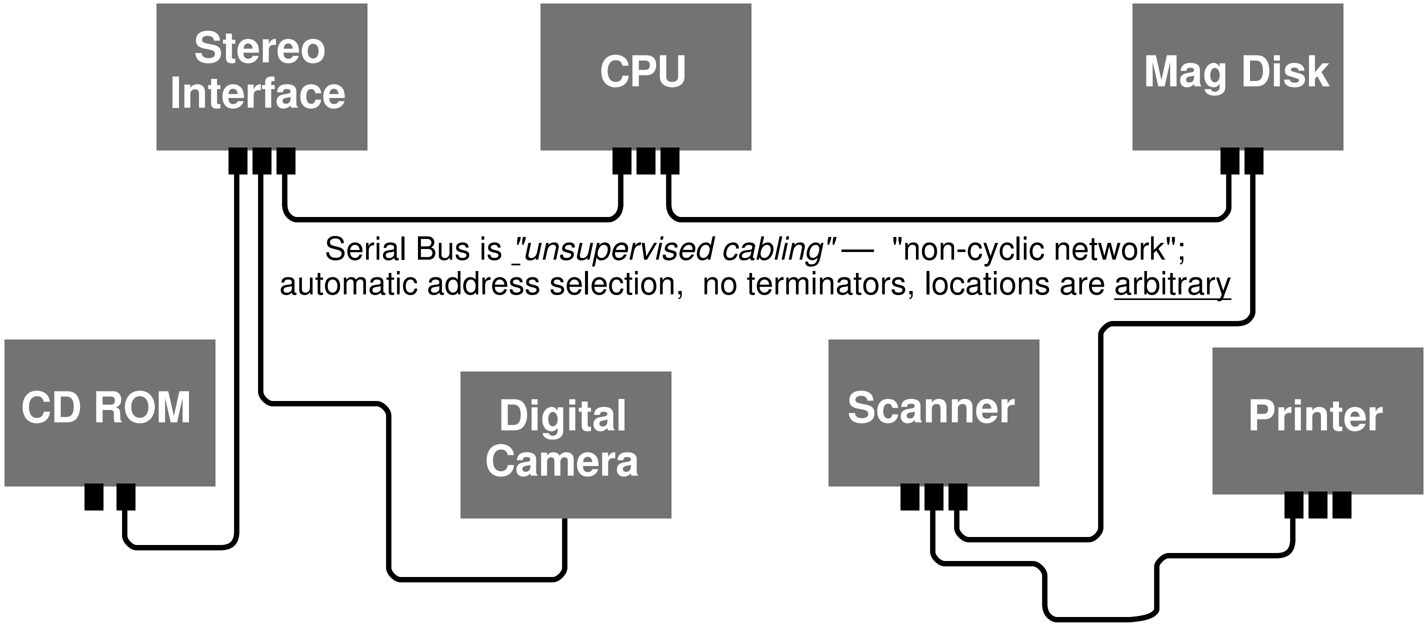
plus telephone/voice, sound input, HiFi sound, compressed video

- **Clean up the desktop cable mess!**

Unsupervised!

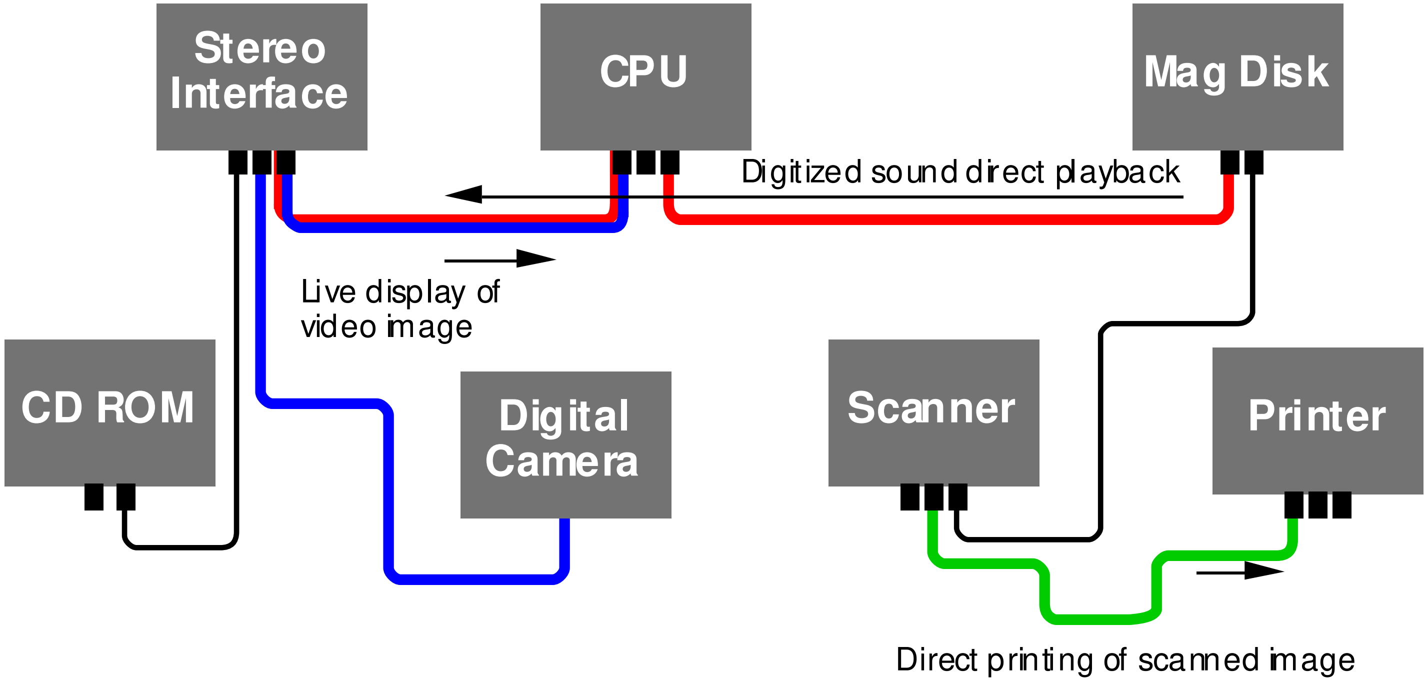




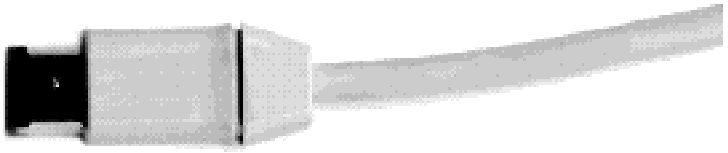


Data Paths

Full support for peer-to-peer I/O

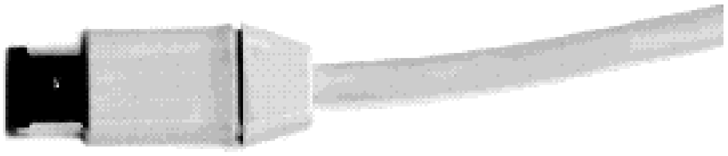


Applications



- **Electronic Imaging**
  - Printers
  - Scanners
- **Storage**
  - scalable disk arrays
  - media servers
- **Slot Replacement**
  - for portables (where adaptors can't be cards)
  - to optionalize LANs
- **Consumer Electronics**
  - portable peripherals
  - multimedia

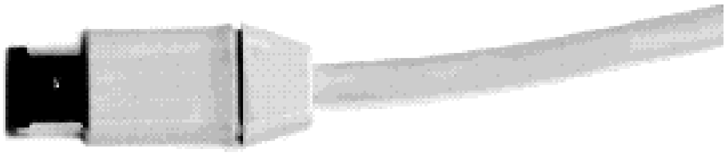
Protocols

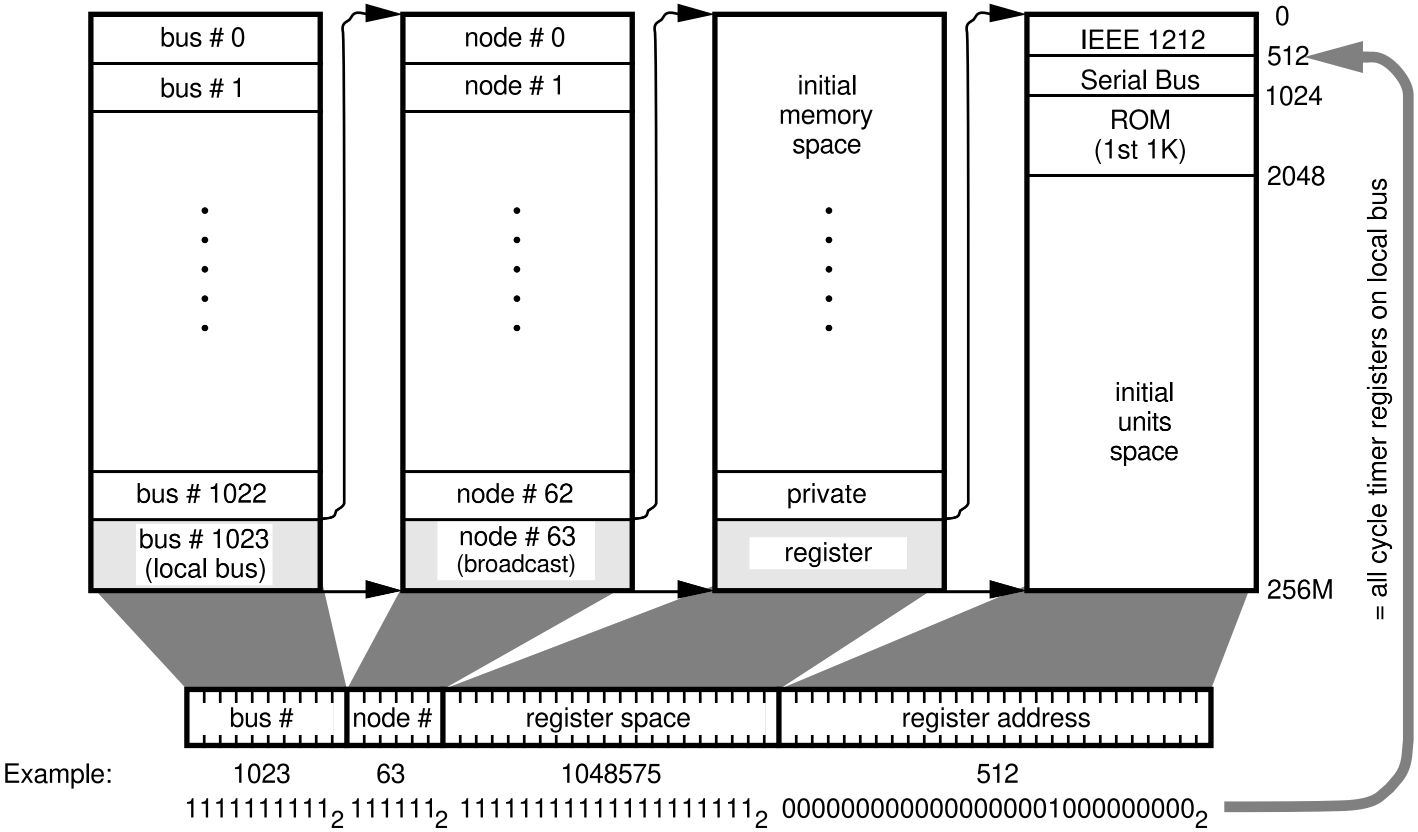


Based on emerging ISO standards

- **IEEE P1394 High Speed Serial Bus**
  "Memory-bus-like" logical architecture
- **IEEE 1212 CSR Architecture**
  Standardized addressing
  Well-defined control and status registers
  Standardized transactions
- **X3T9.2 SCSI-3 Serial Bus Protocol**
  Upgrade path for SCSI systems

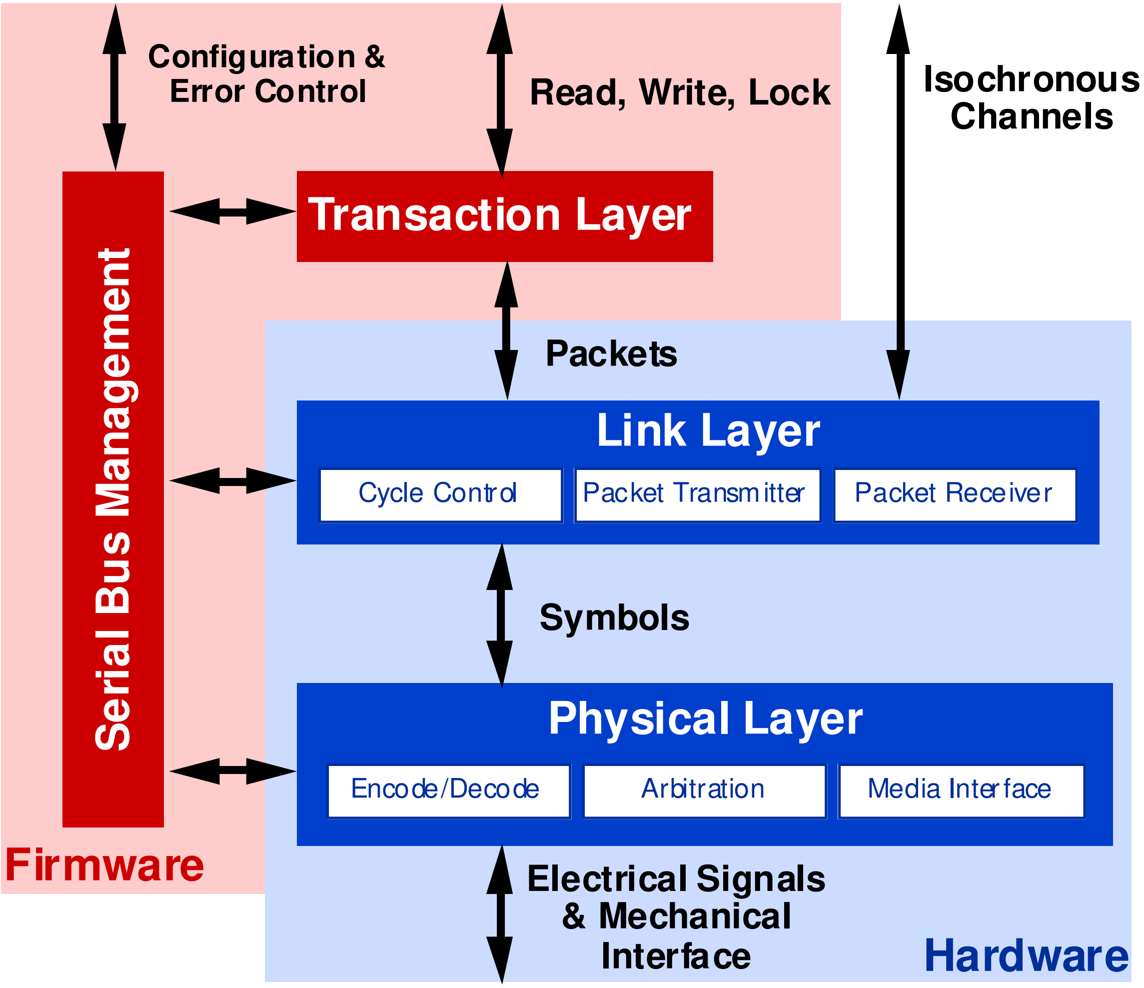
1212 Addressing

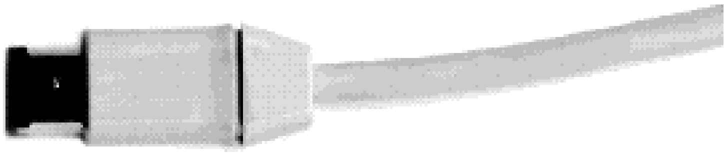


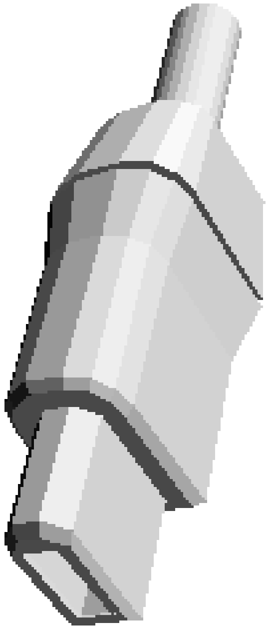


- **The serial bus uses 1212 "64-bit fixed" addressing**

Protocol Stack

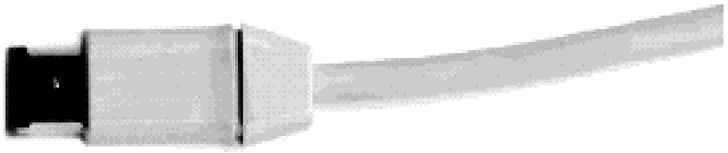


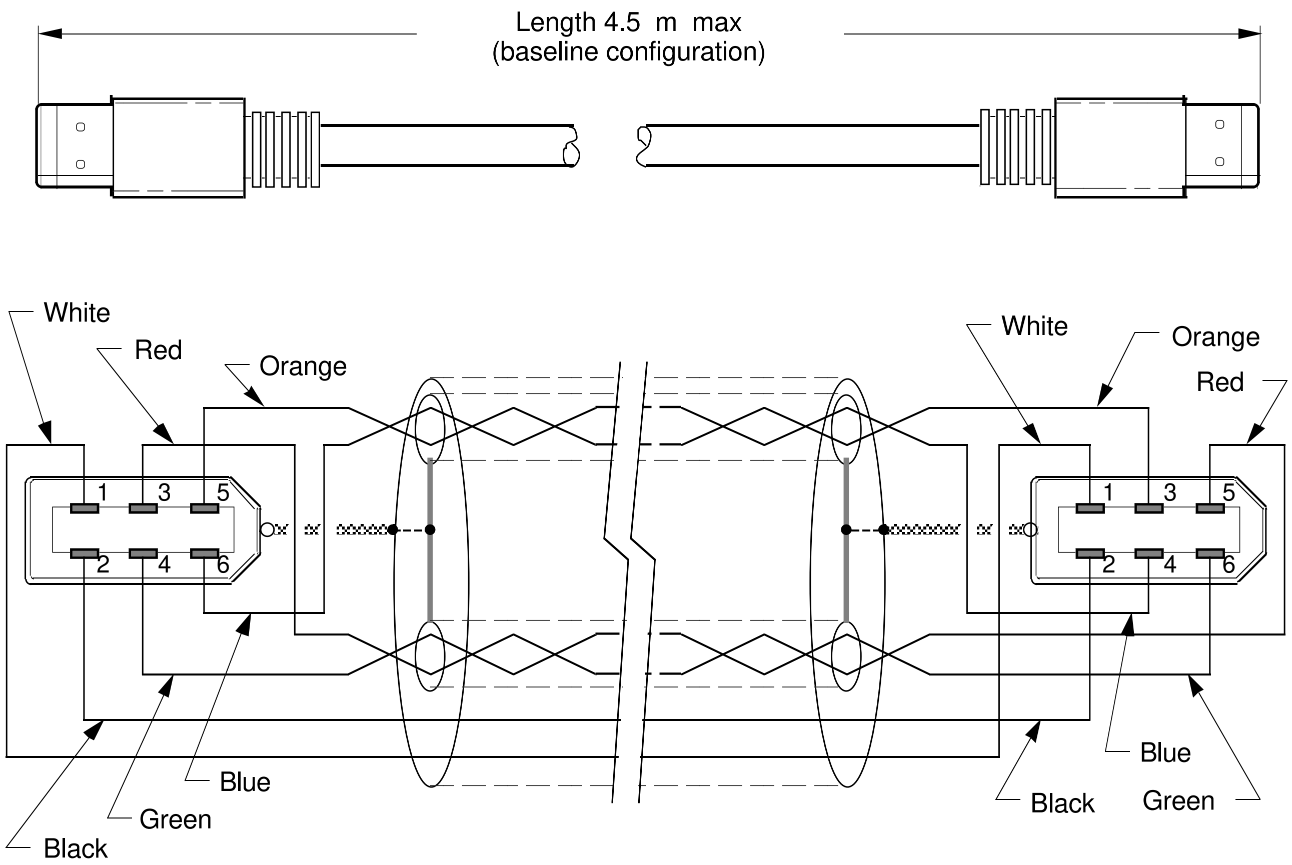
Cable Media 



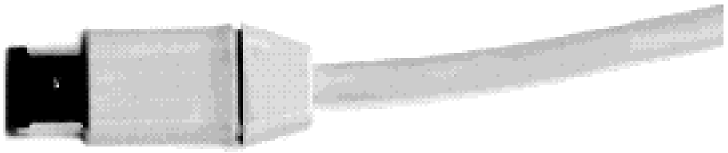
- **3-pair shielded cable**
  Two pairs for data, one for power
- **Small and rugged connector**
  Two sockets in the same area as one mini-DIN socket
- **CMOS transceiver**
  200 mv differential
  4 ma drive
  <800 ps worst case jitter

Cable Assembly



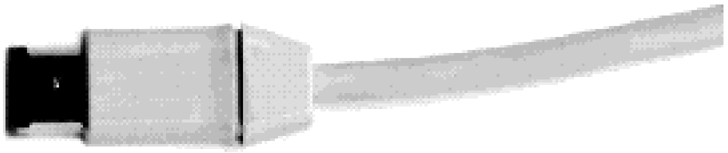


Cable Interface



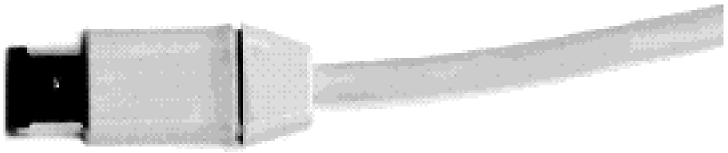
- **Live attach/detach**
  - System protected from power on/off cycling
  - Higher layers provide simple management
    - Remote power control
    - "I'm here!" message
- **Peripheral power**
  - 8 V to 40 V carried by cable
  - Total available power is system dependent
    - Power requirements declared during startup
  - Cable system allows up to 1.5 A (60 watts) per link
    - Devices can either source or sink power
    - Multiple power sources on one bus are supported

Physical Layer



- **98.304 Mbps half duplex data transport**
  - Data is reclocked at each node
  - DAT, ISDN & compressed video rate-compatible
  - 196.608, 393.216, ... Mbps growth paths
- **Data encoding**
  - "data-strobe" encoding gives 2x jitter tolerance
- **Fair and priority access**
  - Hierarchical handshake arbitration
  - Automatic assignment of addresses
  - Access opportunities equally allocated
  - Priority access for special purposes

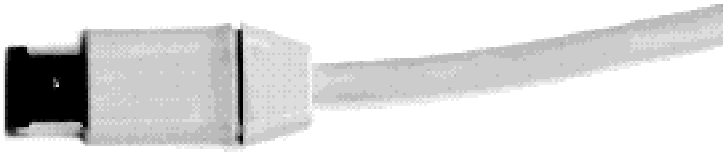
Link Layer



- **Flexible addressing under IEEE 1212**
  - Direct 64-bit addressing (48 bits per device)
  - Hierarchical addressing for up to 63 nodes on 1023 busses
  - Standardized register addresses
- **Flexible packet formats**
  - Optimized for 4-byte data
  - Optional variable-length packets

    Actual limit is 60 μsec per packet
    Yields 512 bytes @ 98 Mbit/sec, 1024 bytes @ 196 Mbit/sec
- **Immediate acknowledge**
  - Status code and optional data within 1 μsec
  - Non-hogging retry mechanism

Link Layer (cont.)



- **Isochronous transport**

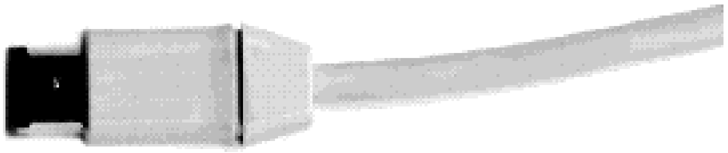
  Multiple "channels" each 125 µsec "cycle"

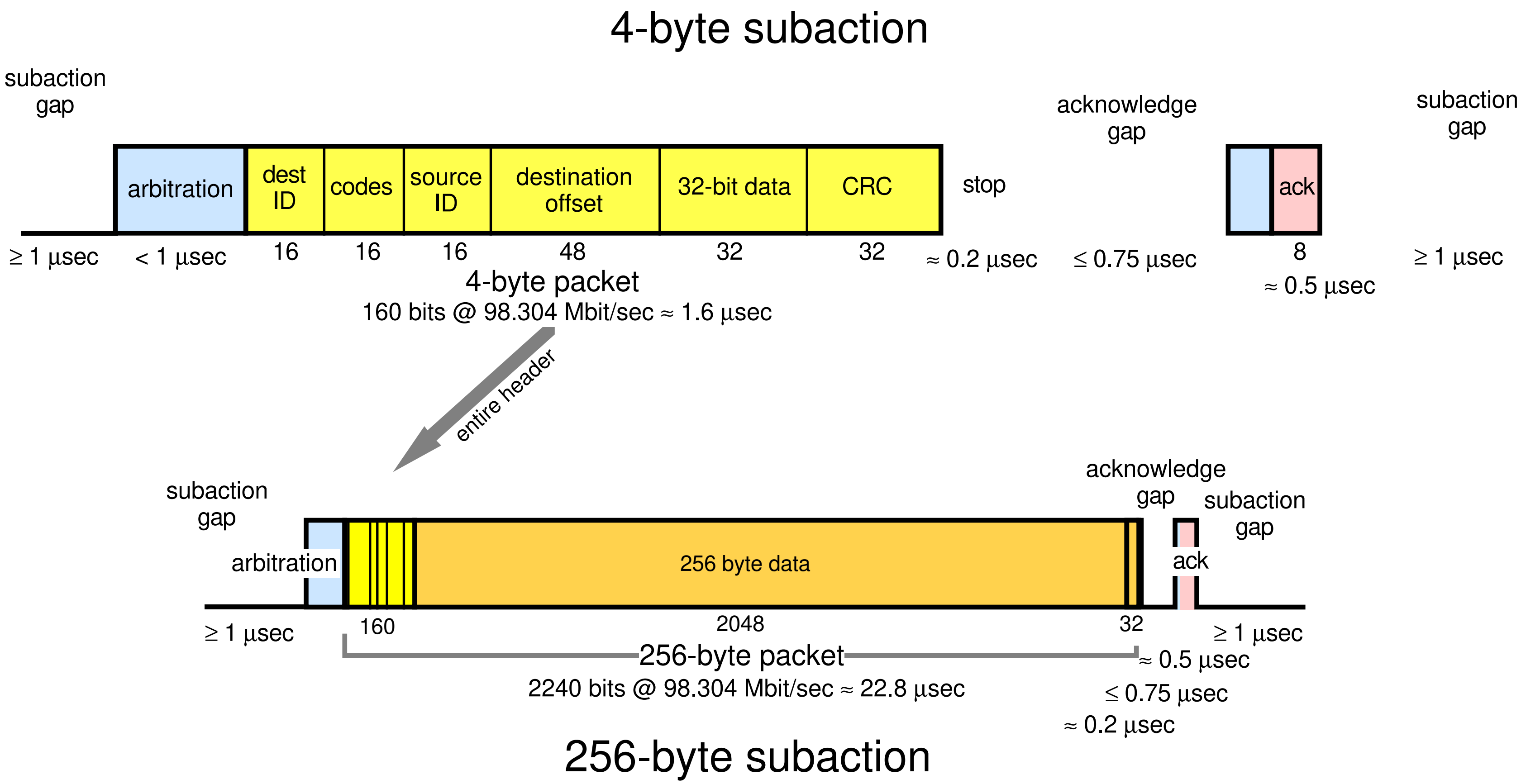
  41 ns max jitter in 125 µsec clock

  Variable channel size up to ≈1000 bytes/cycle

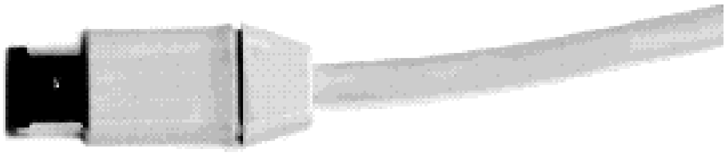
  - Up to ≈2000 bytes/cycle at 196 Mbps

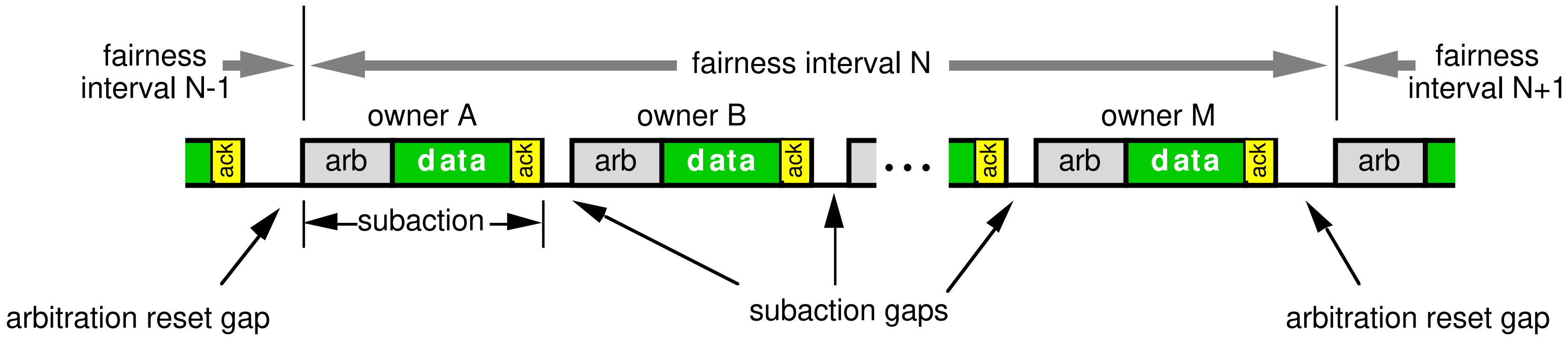
Example Packets





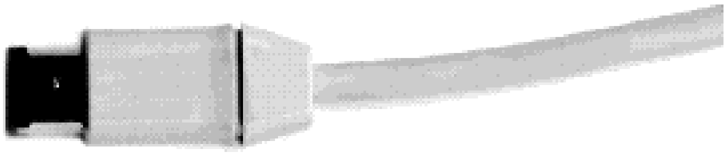
Fairness Cycle

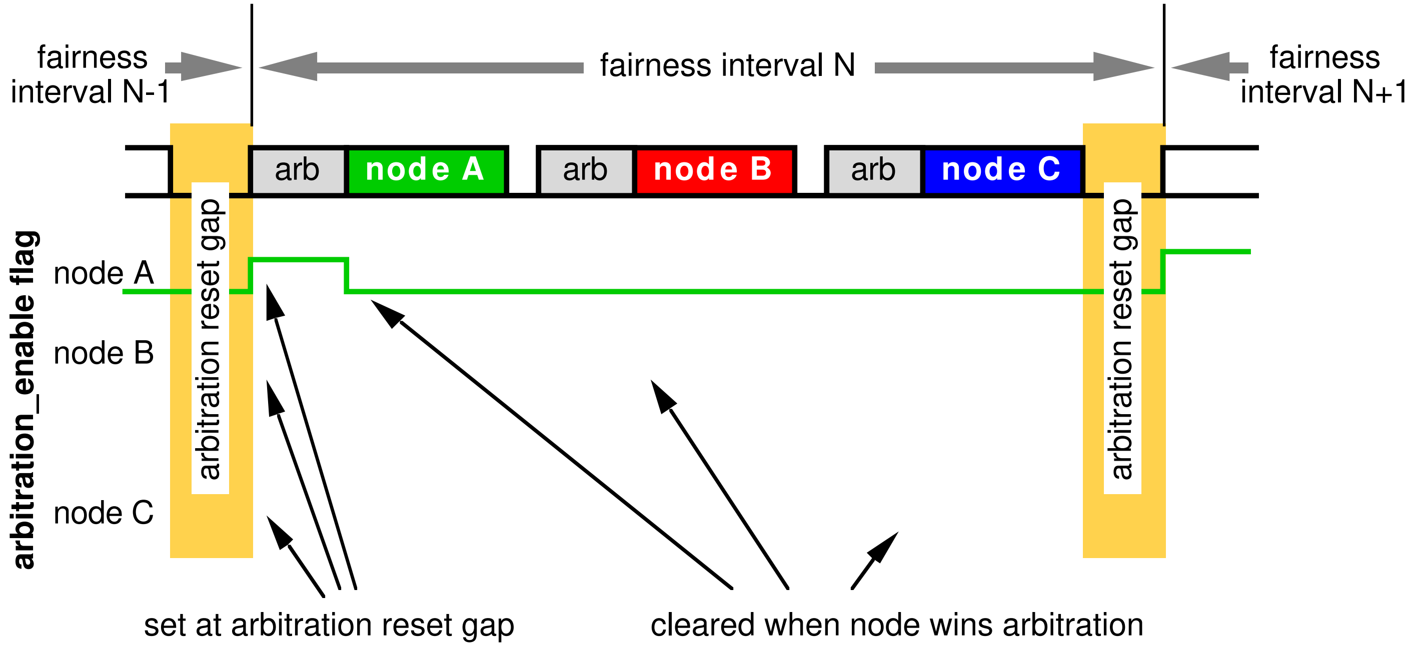




- Fairness interval is bounded by arbitration reset gaps
- Reset gaps are longer than normal subaction gaps

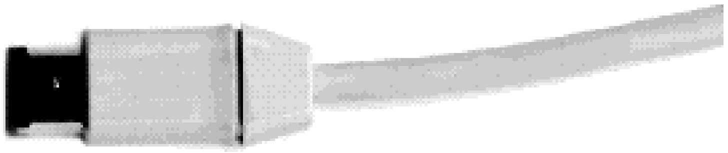
Fairness Arbitration

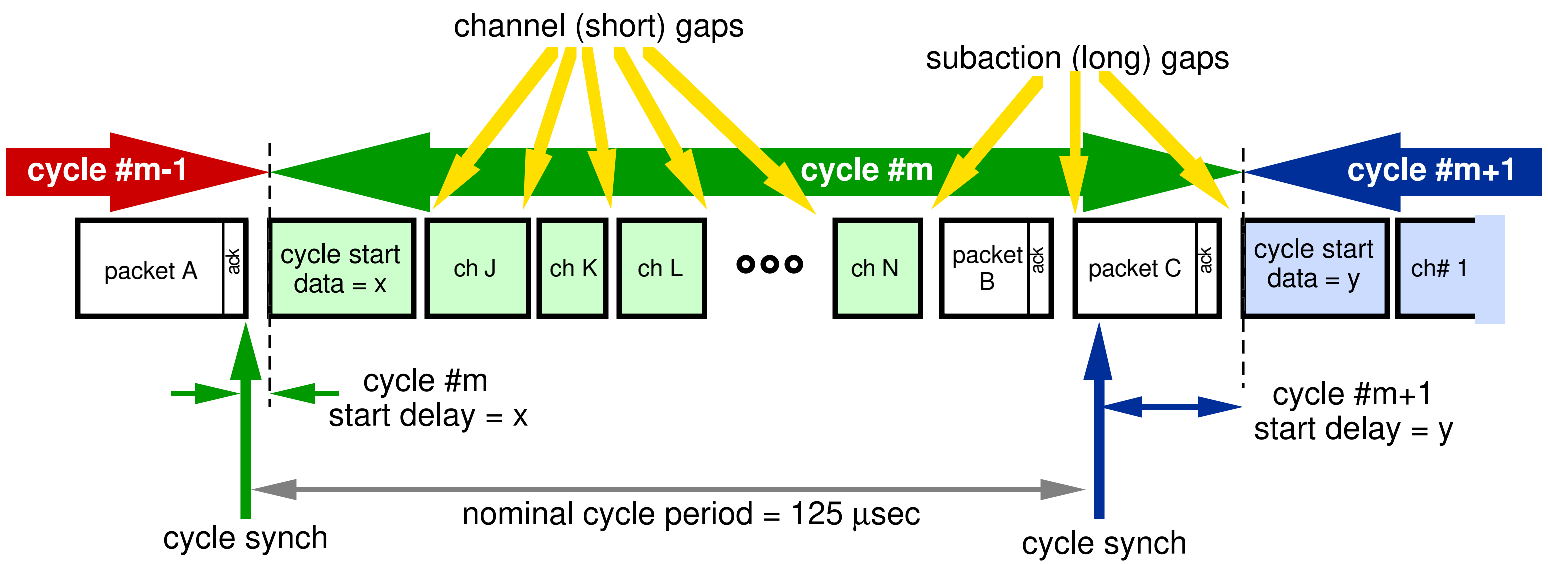




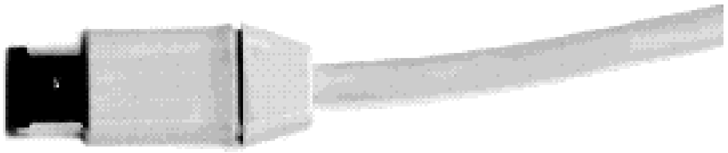
- **Each node gets one access opportunity each Fairness Interval**

Cycle Structure



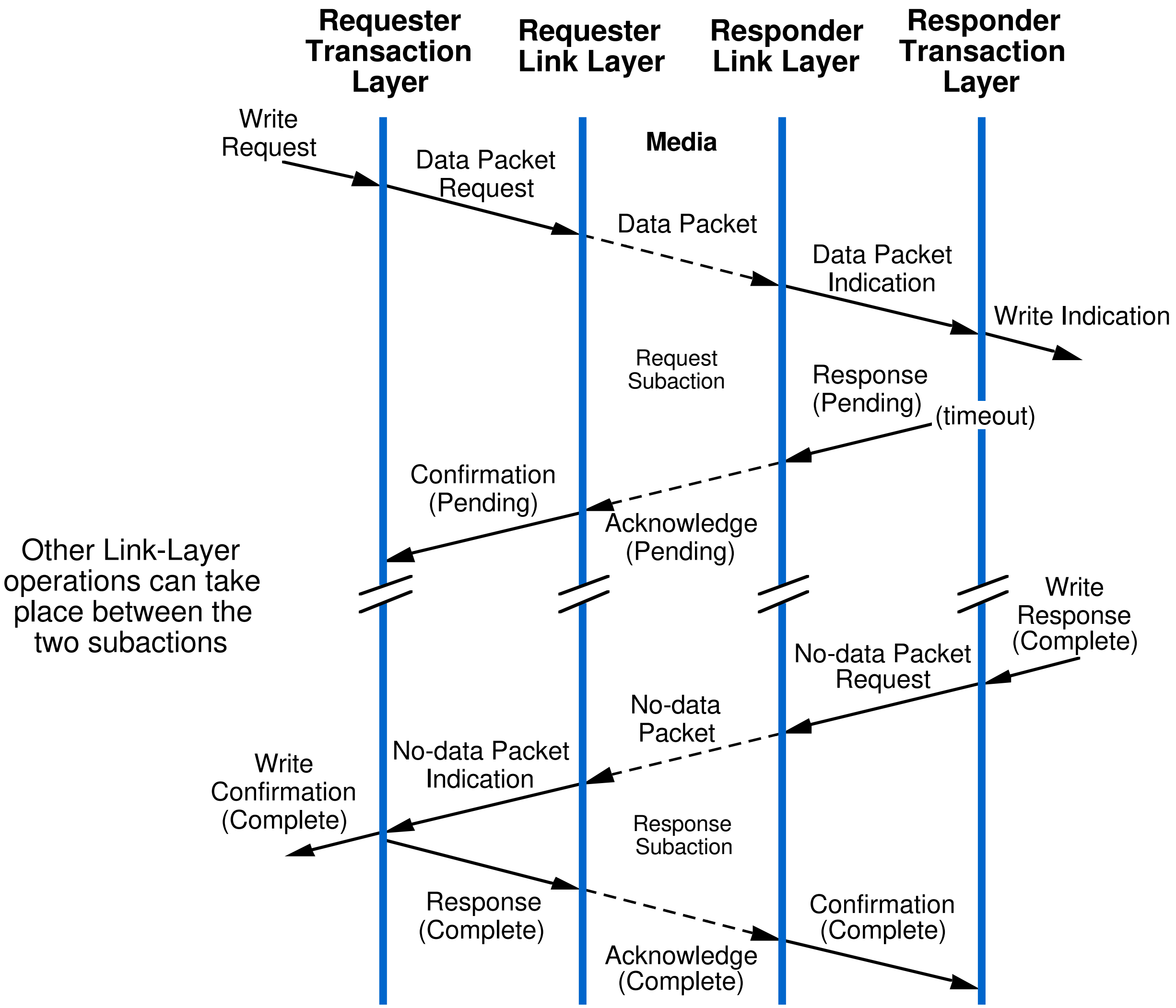


Transaction Layer

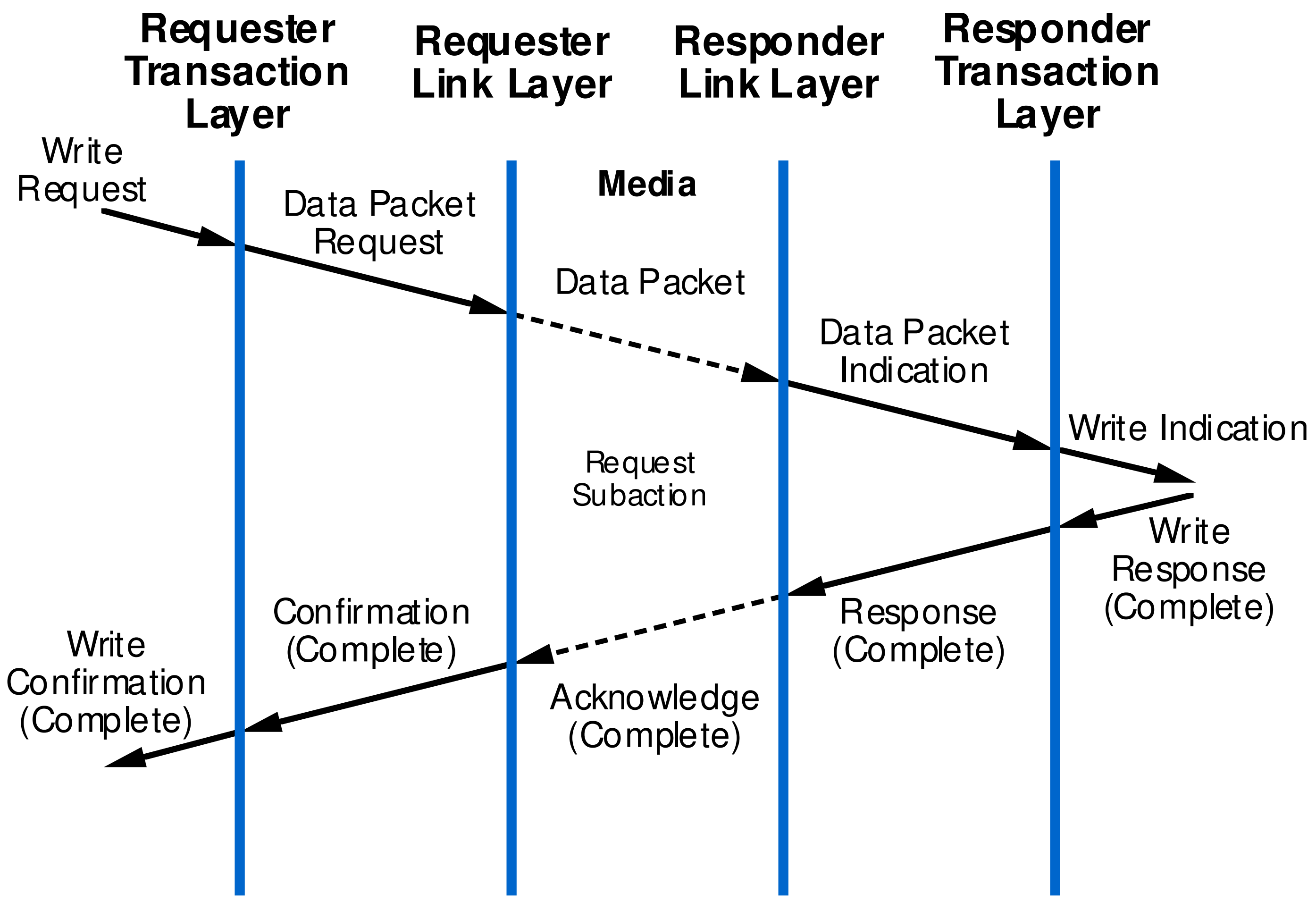


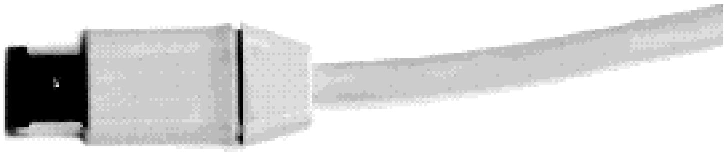
- **Multiple transaction types**
  - Optimized for 4-byte operations
  - Read and write quadlet are required
  - Variable-length block operations optional
  - Lock transactions optional
    Swap, Compare-and-swap needed for distributed DMA
- **Advanced management**
  - Automatic address assignment (no switches)
  - Standardized addresses from IEEE 1212 architecture
    command, status, interrupt, etc.
  - Configuration ROM from IEEE 1212 architecture
    device type, name, manufacturer, power requirements,
    capabilities, driver code

Split Transaction



Fast Transaction



Application Layer 

- **Configuration**
  - Automatic minimal configuration
  - Extensive self-identification possible
  - Software finishes configuration, possible user interaction
- **Bridges to existing devices**
  - SCSI bridge and software ... emulates SCSI manager
  - LAN bridge for peripheral sharing