Power-On Self Test

AMIBIOS provides all IBM standard Power-On Self Test (POST) routines as well as enhanced AMIBIOS POST routines. AMIBIOS POST supports CPU internal diagnostics. AMIBIOS POST checkpoint codes are accessible via the Manufacturing Test Port (I/O Port 80h). AMIBIOS checkpoint codes are documented in the *AMIBIOS Technical Reference.*

POST Phases

Every time the system is powered on, AMIBIOS executes two types of POST routines:

System Test and Initialization (test and initialize AMIBIOS for normal operations) and

System Configuration Verification (compare defined configuration with hardware actually installed).

BIOS Error Reporting

BIOS errors are reported in one of two ways:

If...	then...
the error occurs before the display device is initialized,	a series of beeps sound. Beep codes indicate that a fatal error has occurred. AMIBIOS Beep Codes are described on the next page.
the error occurs after the display device is initialized,	the error message is displayed. AMIBIOS error messages are explained on page 4. A prompt to press <F1> can also appear with displayed error messages.

Beep Codes

Fatal errors, which halt the boot process, are communicated through a series of audible beeps. If AMIBIOS POST can initialize the system video display, it displays the error message. Displayed error messages, in most cases, allow the system to continue to boot. Displayed error messages are described on page 4.

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry is faulty.
2	Parity Error	Parity error in the base memory (the first 64 KB block) of memory.
3	Base 64 KB Memory Failure	Memory failure in first 64 KB.
4	Timer Not Operational	A memory failure in the first 64 KB of memory, or Timer 1 is not functioning.
5	Processor Error	The CPU generated an error.
6	8042 - Gate A20 Failure	Cannot switch to protected mode.
7	Processor Exception Interrupt Error	The CPU on the CPU Card generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in AMIBIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS RAM has failed.
11	Cache Memory Bad — Do Not Enable Cache	The cache memory test failed. Cache memory is disabled. *Do not press <Ctrl> <Alt> <Shift> <+> to enable cache memory.*

Troubleshooting System Problems

If the Computer Beeps

If it beeps...	then...
1, 2, or 3 times...	reseat the memory SIMMs or DIPs. If the system still beeps, replace the memory.
6 times...	reseat the keyboard controller chip. If it still beeps, replace the keyboard controller. If it still beeps, try a different keyboard, or replace the keyboard fuse, if the keyboard has one.
8 times...	there is a memory error on the video adapter. Replace the video adapter, or the RAM on the video adapter.
9 times...	the BIOS ROM chip is bad. The system probably needs a new BIOS ROM chip.
11 times...	reseat the cache memory on the motherboard. If it still beeps, replace the cache memory.
4, 5, 7, or 10 times...	the motherboard must be replaced.

AMIBIOS Displayed Error Messages

If an error occurs after the system display has been initialized, the error message are displayed as follows:

```
ERROR Message Line 1
ERROR Message Line 2
    Press <F1> to continue
```

and the system halts. The system does not halt if *Wait for <F1> If Any Error* in Advanced Setup is *Disabled.*

```
RUN SETUP UTILITY.
```

can also appear. Press <F1> to run WINBIOS Setup if this message appears.

Error Message	Explanation
8042 Gate-A20 Error	Gate A20 on the keyboard controller (8042) is not working. Replace the 8042.
Address Line Short!	Error in the address decoding circuitry.
C: Drive Error	No response from drive C:. Run the AMIDiag Hard Disk Utility. Check the C: hard disk type in Standard Setup.
C: Drive Failure	No response from hard disk drive C:. Replace the drive.
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective. Run AMIDiag.
CH-2 Timer Error	An AT system has two timers. There is an error in timer 2.
CMOS Battery State Low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS Checksum Failure	CMOS RAM checksum is different than the previous value. Run WINBIOS Setup.
CMOS System Options Not Set	The values stored in CMOS RAM have been destroyed. Run WINBIOS Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected. Run WINBIOS Setup.
CMOS Memory Size Mismatch	The amount of memory found by AMIBIOS is different than the amount in CMOS RAM. Run WINBIOS Setup.
CMOS Time and	Run Standard Setup to set the date and time.

Error Message	Explanation
Date Not Set	
D: Drive Error	No response from drive D:. Run the AMIDiag Hard Disk Utility. Check the hard disk type in Standard Setup.
D: drive failure	No response from hard disk drive D:. Replace the drive.
Diskette Boot Failure	The boot diskette in drive A: cannot be used to boot the system. Use another boot diskette and follow the screen instructions.
Display Switch Not Proper	Some systems require a video switch be set to either color or monochrome. Turn the system off, set the switch properly, then power on.
DMA Error	Error in the DMA controller.
DMA 1 Error	Error in the first DMA channel.
DMA 2 Error	Error in the second DMA channel.
FDD Controller Failure	AMIBIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered down.
HDD Controller Failure	AMIBIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down.
INTR1 Error	Interrupt channel 1 failed POST.
INTR2 Error	Interrupt channel 2 failed POST.
Invalid Boot Diskette	AMIBIOS can read the diskette in floppy drive A:, but it cannot boot the system with it. Use another boot diskette and follow the screen instructions.
Keyboard Is Locked...Unlock It	The keyboard lock on the system is engaged. The system must be unlocked to continue to boot.
Keyboard Error	The keyboard has a timing problem. Make sure a Keyboard Controller AMIBIOS is installed. Set *Keyboard* in Advanced Setup to *Not Installed* to skip the keyboard POST routines.
KB/Interface Error	There is an error in the keyboard connector.
No ROM BASIC	Cannot find a proper bootable sector on either drive A: or C:. AMIBIOS cannot find ROM Basic.
Off Board Parity Error	Parity error in memory installed on an adapter card in an expansion slot. The format is: `OFF BOARD PARITY ERROR ADDR = (XXXX)` *XXXX* is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
On Board Parity Error	Parity error in motherboard memory. The format is: `ON BOARD PARITY ERROR ADDR = (XXXX)` *XXXX* is the hex address where the error occurred. Run AMIDiag to find and correct

Error Message	Explanation
	memory problems.
Parity Error ????	Parity error in system memory at an unknown address. Run AMIDiag to find and correct memory problems.

POST Memory Test

Normally, the only visible POST routine is the memory test. The screen that appears when the system is powered on is shown below.

```
AMIBIOS (C) 1995 American Megatrends Inc.
XXXXX KB OK


Hit <DEL> if you want to run SETUP




(C) American Megatrends Inc.
XX-XXXX-XXXXXX-XXXXXXXX-XXXXXX-XXXX-X
```

An AMIBIOS Identification string is displayed at the left bottom corner of the screen, below the copyright message. Press <Ins> during system boot to display two additional AMIBIOS Identification strings.

AMIBIOS Identification Strings show the options installed in AMIBIOS. You will need this information when calling for technical support.

Displaying Additional AMIBIOS ID Strings

Step	Action
1	Enable *Wait for <F1> If any Error* in Advanced Setup to *Enabled* before freezing the screen.
2	When a problem occurs, freeze the screen by powering on the system and holding a key down on the keyboard to cause a *Keyboard Error* message.
3	Copy the three lines and report this information to American Megatrends. Press <F1> to continue the boot process.

The following appears after POST completes:

```
Hit <DEL> if you want to run SETUP
```

Press <Del> to access WINBIOS Setup.

EISA BIOS Error Messages

An EISA AMIBIOS can generate additional error messages. None of these messages is fatal. The EISA AMIBIOS error messages are:

Error Message	Explanation
EISA CMOS Checksum Failure	The Checksum for EISA CMOS is bad. The battery for EISA CMOS RAM can be bad.
EISA CMOS Inoperational	A Read/Write error occurred in extended CMOS RAM. The battery may be bad.
Expansion Board Not Ready at Slot *X, Y, Z*	AMIBIOS cannot find the expansion board in Slot *X, Y*, or *Z*. Make sure the board is in the correct slot and is correctly seated.
Fail-Safe Timer NMI Inoperational	Devices that depend on the fail-safe NMI timer is not operating correctly.
ID Information Mismatch for Slot *X, Y, Z*.	The ID of the EISA Expansion Board in Slot *X, Y*, or *Z* does not match the ID in EISA CMOS RAM.
Invalid Configuration Information for Slot X, Y, Z.	The configuration information for EISA Expansion Boards *X, Y*, or *Z* is not correct. The board cannot be configured. Run the ECU.
Software Port NMI Inoperational	The software port NMI is not working.

ISA NMI Handler Messages

ISA NMI Message	Explanation
Memory Parity Error at *xxxxx*	Memory failed. If the memory location can be determined, it is displayed as *xxxxx*. If not, the message is *Memory Parity Error ????*.
I/O Card Parity Error at *xxxxx*	An expansion card failed. If the address can be determined, it is displayed as *xxxxx*. If not, the message is *I/O Card Parity Error ????*.
DMA Bus Time-out	A device has driven the bus signal for more than 7.8 microseconds.

EISA AMIBIOS NMI Error Messages

The EISA AMIBIOS can generate additional NMI messages that are specific to EISA systems.

EISA NMI Message	Explanation
BUS Timeout NMI at Slot *n*	There was a Bus Timeout NMI at Slot *n*.
(E)nable (D)isable Expansion Board?	Type E to enable the expansion board that had an NMI or D to disable it.
Expansion Board Disabled at Slot *n*	The expansion board in Slot *n* has been disabled.
Expansion Board NMI at Slot *n*	An expansion board NMI was generated from Slot *n*.
Fail-Safe Timer NMI	A fail-safe timer NMI has been generated.
Software Port NMI	A software port NMI has been generated.

AMIBIOS Configuration Screen

AMIBIOS displays a screen that looks similar to the following when the POST routines complete successfully.

```
AMIBIOS System Configuration (C) Copyright 1985-95 American Megatrends Inc.

Main Processor       : Pentium      Base Memory Size     : 640 KB
Numeric Coprocessor  : Present      Ext. Memory Size     : 7808 KB
Floppy Drive A:      : 1.2 MB ½     Display Type         : EGA/VGA
Floppy Drive B:      : 1.44 MB ¼    Serial Port(s)       : 3F8
ROM-BIOS Date:       : 07/15/95     Parallel Port(s)     : 378
```

POST Checkpoint Codes

When AMIBIOS performs the Power On Self Test, it writes diagnostic codes (checkpoint codes) to I/O port 0080h. If the computer cannot complete the boot process, diagnostic equipment can be attached to the computer to read I/O port 0080h. The following AMIBIOS POST checkpoint codes are valid for all AMIBIOS products with a core BIOS date of 7/15/95 (Enhanced).

Uncompressed Initialization Codes The uncompressed initialization checkpoint codes are listed in order of execution:

Checkpoint Code	Description
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
D1h	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h.The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BIOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.

Cont'd

POST Checkpoint Codes, Continued

Bootblock Recovery Codes The bootblock recovery checkpoint codes are listed in order of execution:

Checkpoint Code	Description
E0h	The onboard floppy controller if available is initialized. Next, beginning the base 512 KB memory test.
E1h	Initializing the interrupt vector table next.
E2h	Initializing the DMA and Interrupt controllers next.
E6h	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
EDh	Initializing the floppy drive.
EEh	Looking for a floppy diskette in drive A:. Reading the first sector of the diskette.
EFh	A read error occurred while reading the floppy drive in drive A:.
F0h	Next, searching for the AMIBOOT.ROM file in the root directory.
F1h	The AMIBOOT.ROM file is not in the root directory.
F2h	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3h	Next, reading the AMIBOOT.ROM file, cluster by cluster.
F4h	The AMIBOOT.ROM file is not the correct size.
F5h	Next, disabling internal cache memory.
FBh	Next, detecting the type of flash ROM.
FCh	Next, erasing the flash ROM.
FDh	Next, programming the flash ROM.
FFh	Flash ROM programming was successful. Next, restarting the system BIOS.

Uncompressed Initialization Codes The following runtime checkpoint codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Checkpoint Code	Description
03h	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05h	The BIOS stack has been built. Next, disabling cache memory.
06h	Uncompressing the POST code next.
07h	Next, initializing the CPU and the CPU data area.
08h	The CMOS checksum calculation is done next.
0Ah	The CMOS checksum calculation is done. Initializing the CMOS status register for date and time next.
0Bh	The CMOS status register is initialized. Next, performing any required initialization before the keyboard BAT command is issued.
0Ch	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0Eh	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0Fh	The initialization after the keyboard controller BAT command test is done.

Checkpoint Code	Description
	The keyboard command byte is written next.
10h	The keyboard controller command byte is written. Next, issuing the Pin 23 and 24 blocking and unblocking command.
11h	Next, checking if <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the *Initialize CMOS RAM in every boot* AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12h	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13h	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14h	The 8254 timer test will begin next.
19h	The 8254 timer test is over. Starting the memory refresh test next.
1Ah	The memory refresh line is toggling. Checking the 15 second on/off time next.
23h	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24h	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin.
25h	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27h	Any initialization before setting video mode will be done next.
28h	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2Ah	Bus initialization system, static, output devices will be done next, if present. See page 16 for additional information.
2Bh	Passing control to the video ROM to perform any required configuration before the video ROM test.
2Ch	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2Dh	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2Eh	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2Fh	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30h	The display memory read/write test passed. Look for retrace checking next.
31h	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32h	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34h	Video display checking is over. Setting the display mode next.
37h	The display mode is set. Displaying the power on message next.
38h	Initializing the bus input, IPL, general devices next, if present. See page 16 for additional information.
39h	Displaying bus initialization error messages. See page 16 for additional information.
3Ah	The new cursor position has been read and saved. Displaying the *Hit <DEL>* message next.
3Bh	The *Hit <DEL>* message is displayed. The protected mode memory test is about to start.
40h	Preparing the descriptor tables next.
42h	The descriptor tables are prepared. Entering protected mode for the memory test next.
43h	Entered protected mode. Enabling interrupts for diagnostics mode next.

Checkpoint Code	Description
44h	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45h	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46h	The memory wraparound test is done. Memory size calculation has been done. Writing patterns to test memory next.
47h	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.
48h	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49h	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4Bh	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4Ch	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4Dh	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4Eh	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4Fh	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50h	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51h	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52h	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53h	The memory size information and the CPU registers are saved. Entering real mode next.
54h	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57h	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58h	The memory size was adjusted for relocation and shadowing. Clearing the *Hit <DEL>* message next.
59h	The *Hit <DEL>* message is cleared. The *<WAIT...>* message is displayed. Starting the DMA and interrupt controller test next.
60h	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62h	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65h	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66h	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
67h	Completed 8259 interrupt controller initialization.
7Fh	Extended NMI source enabling is in progress.
80h	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81h	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82h	The keyboard controller interface test completed. Writing the command byte

Checkpoint Code	Description
	and initializing the circular buffer next.
83h	The command byte was written and global data initialization has completed. Checking for a locked key next.
84h	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85h	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86h	The password was checked. Performing any required programming before WINBIOS Setup next.
87h	The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88h	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89h	The programming after WINBIOS Setup has completed. Displaying the power on screen message next.
8Bh	The first screen message has been displayed. The *<WAIT...>* message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8Ch	Programming the WINBIOS Setup options next.
8Dh	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8Fh	The hard disk controller has been reset. Configuring the floppy drive controller next.
91h	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95h	Initializing the bus option ROMs from C800 next. See page 16 for additional information.
96h	Initializing before passing control to the adaptor ROM at C800.
97h	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98h	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99h	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9Ah	Set the timer and printer base addresses. Setting the RS-232 base address next.
9Bh	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9Ch	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9Dh	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9Eh	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2h	Displaying any soft errors next.
A3h	The soft error display has completed. Setting the keyboard typematic rate next.
A4h	The keyboard typematic rate is set. Programming the memory wait states next.
A5h	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7h	NMI and parity enabled. Performing any initialization required before

Checkpoint Code	Description
	passing control to the adaptor ROM at E000 next.
A8h	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9h	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
AAh	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
ABh	Uncompressing the DMI data and executing DMI POST initialization next.
B0h	The system configuration is displayed.
B1h	Copying any code to specific areas.
00h	Code copying to specific areas is done. Passing control to INT 19h boot loader next.

Bus Checkpoint Codes

The system BIOS passes control to different buses at the following checkpoints:

Checkpoint Code	Description
2Ah	Initializing the different bus system, static, and output devices, if present.
38h	Initialized bus input, IPL, and general devices, if present.
39h	Displaying bus initialization error messages, if any.
95h	Initializing bus adaptor ROMs from C8000h through D8000h.

Additional Bus Checkpoints While control is in the bus routines, additional checkpoints are output to I/O port address 0080h as word to identify the routines being executed. These are word checkpoints. The low byte of checkpoint is the system BIOS checkpoint where control is passed to the different bus routines.

The high byte of checkpoint indicates that the routine is being executed in different buses.

High Byte The high byte of these checkpoints includes the following information:

Bits	Description
Bits 7-4	0000 Function 0. Disable all devices on the bus. 0001 Function 1. Initialize static devices on the bus. 0010 Function 2. Initialize output devices on the bus. 0011 Function 3. Initialize input devices on the bus. 0100 Function 4. Initialize IPL devices on the bus. 0101 Function 5. Initiate general devices on the bus. 0110 Function 6. Initialize error reporting on the bus. 0111 Function 7. Initialize add-on ROMs for all buses.
Bits 3-0	Specify the bus 0 Generic DIM Device Initialization Manager. 1 Onboard System devices. 2 ISA devices. 3 EISA devices. 4 ISA PnP devices. 5 PCI devices.