Intel and IBM Microprocessors

PS/2®, ValuePoint™, ThinkPad® Megahertz	Paths	Standard Features
80386 SX L40, N51, CL57, 700T 35, 40, 55, 56, 57, 65 16, 20, 25, 33 MHz	16 Bit Data Path 32 Bit Processor 24 Bit Address Path	⇛ Address pipelining
80386 SL N45, 300 16, 20, 25 MHz	16 Bit Data Path 32 Bit Processor 24 Bit Address Path	⇛ Address pipelining ⚛ Power management
80386 DX 70, P70, 80 16, 20, 25, 33 MHz	32 Bit Data Path 32 Bit Processor 32 Bit Address Path	⇛ Address pipelining
80386 SLC 325T, N51, 56, 57, (Upgrade for 56, 57) 16, 20, 25 MHz	Same as 80386SX except **32 bit data path** between CPU and memory cache [1]	🖃 8 KB internal cache (2 way ; write-thru; w/ parity) ⇛ Optimized instructions ⇛ Address pipelining ⚛ Power management
80486 SLC 700, 700C, 710T 25 MHz	Same as 80386SX except **32 bit data path** between CPU and memory cache [1]	🖃 16 KB internal cache (4 way ; write-thru; w/ parity) ⇛ Optimized instructions ⇛ Address pipelining ⚛ Power management
80486 SLC2 53, 56, 57, 500, 720, 720/C (Upgrade for 56, 57, 700, 700C) 40/20, 50/25 MHz	Same as 80386SX except **32 bit data path** between CPU and memory cache [1]	🖃 Same as ***80486SLC*** above
80486 SLC3 56, 57 (Upgrade for 56, 57) 75/25, 60/20 MHz	Same as 80386SX except **32 bit data path** between CPU and memory cache [1]	🖃 Same as ***80486SLC*** above
Blue Lightning 50/25, 66/33 MHz 75/25 MHz	32 Bit Data Path 32 Bit Processor 32 Bit Address Path	🖃 16 KB internal cache (4 way ; write-thru; w/ parity) ⇛ Optimized instructions ⇛ Address pipelining ⚛ Power management
80486 SX 425SX, 433SX 76, 77, 85, 90, 95 16, 20, 25, 33 MHz	32 Bit Data Path 32 Bit Processor 32 Bit Address Path	🖃 8 KB internal cache (4 way set; write-thru) ⇛ Optimized instructions ⇛ Burst mode bus ⚛ Power mgmt (after Jun93)[2]
80486 SL 350, 350C, 750, 750Cs 750C, 750P 25, 33 MHz	32 Bit Data Path 32 Bit Processor 32 Bit Address Path ⌖ Math coprocssr possible (some SL's have integrated math co and some do not)	🖃 8 KB internal cache (4 way set; write-thru) ⌖ Math coprocessor ⇛ Optimized instructions ⇛ Burst mode bus ⚛ Power management
80486 DX 433DX, 70, 90 95, P75, 195, 295 25, 33, 50 MHz	32 Bit Data Path 32 Bit Processor 32 Bit Address Path ⌖ Math coprocessor std	🖃 8 KB internal cache (4 way set; write-thru) ⌖ Math coprocessor ⇛ Optimized instructions ⇛ Burst mode bus ⚛ Power mgmt (after Jun93)[2]
80486 DX2 450DX2, 466DX2, 77, 85, 90, 95 (Upgrade for 76, 77, 85, 425SX, 433SX, 433DX) 40/20, 50/25, 66/33 MHz	32 Bit Data Path 32 Bit Processor 32 Bit Address Path ⌖ Math coprocessor std	🖃 Same as ***80486DX*** above
Pentium ™ P60/D, 95 (Upgrade for 90, 95) 60, 66 MHz	64 Bit Data Path 32 Bit Processor 32 Bit Address Path ⌖ Pipelined math co std	🖃 8 KB internal instruction cache (2 way set; w/ parity) 🖃 8 KB internal data cache (2 way set; write-back or write-thru; with parity) ⌖ Math coprocessor ⇛ 2 execute units (superscalar) ⇛ Internal and external parity ⇛ Dynamic branch prediction ⇛ Optimized instructions ⇛ Address pipelining ⇛ Burst mode bus ⚛ Power management

ALL 386 SX PROCESSORS AND ABOVE

Modes	Addressable Memory	Operating Systems
REAL	1 MB	*DOS*
PROTECT	16 MB	*OS/2 1.3, Windows 3.X DOS Extenders*
NATIVE PROTECT	4 GB	***OS/2 2.X,*** *Windows NT DOS Extenders, AIX PS/2*
VIRTUAL 8086	Multiple 640 KB	***OS/2 2.X,*** *Windows 3.X, NT DOS Extenders AIX PS/2 DOS Merge*

The **386 SX** through the Pentium processor all offer the same modes which only means that applications run faster on a Pentium. Operating systems and applications written for the 386 family will be compatible with the 486 and Pentium processor.

The **386 SX** and all **SLC** processors can only address 16 MB of memory, although 64 TB of virtual memory, because of its 24 bit address path.

The **486 SLC2** and **486 DX2** run twice as fast internally (50 MHz) as externally (25 MHz).
The **486 SLC3** runs three times as fast internally (75 MHz) as externally (25 MHz).

Note 1: Although the**SLC's** have a 16 bit data bus like the **386 SX**, the memory cache is integrated on the processor chip (not external) so the memory cache transfers to the CPU in 32 bits. The SLC and Blue Lightning processors are developed and manufactured by IBM®.

Note 2: Effective June 1993, the **486 SX**, **486 DX**, and **486 DX2** (called 'SL Enhanced Intel486™ microprocessors') includes the **486 SL** power mgmt technology called System Management Mode (SMM).

Address pipelining: decodes next instruction's address while the current instruction is in progress.
Optimized instructions: instructions execute in fewer clock cycles.
Burst mode bus: for reads and writes from processor to memory; 4 back-to-back data transfers (usually in 5 cycles); 486 is 128 bits (16 bytes) and Pentium CPU is 256 bits (64 bits x 4; (32 bytes).
486SL: may or may not have integrated math coprocessor (can not determine via external appearance). IBM ThinkPad® 350/350C have no math coprocessor; ThinkPad 750 family does have a math coprocessor.
Intel® OverDrive™ Processor: with a single chip upgrade, gives 40% to 70% performance boost without modifying external system clock or memory subsystem. Three types:

1) Most 486 SX and 486 DX PC's can be upgraded to a 486 DX2 (168 or 169 pin).
2) Systems w/ 238 pin socket may be upgraded to 'Intel OverDrive processor with Pentium processor technology' chip expected in 1994 which will be based on Pentium processor technology. (Code name is **P24T**; 5.0 volts). Expected to increase performance of a 486 DX2 66/33 about 70%.
3) OverDrive processors are being developed for Pentium processor based systems. (273 pin; Code name is **P5T**).

(INTEL) Compiled by Roger Dodson, IBM. January 1994