Section 1 EPLD Receiver

Chapter 4 EPLD Receiver Introduction

The analog demodulation and synchronization system of figure 2.3 can be replaced with digital components. Digital components have the advantage of not drifting with temperature or age and have no tuneable parts. Digital components are generally re-programmable and can be configured for multiple tasks without changing the hardware design. Digital versions of its analog counterparts are readily available and are well matured. Digital Costas loop, phase locked loops, frequency translators and FIR and IIR filters are available to the system designer.

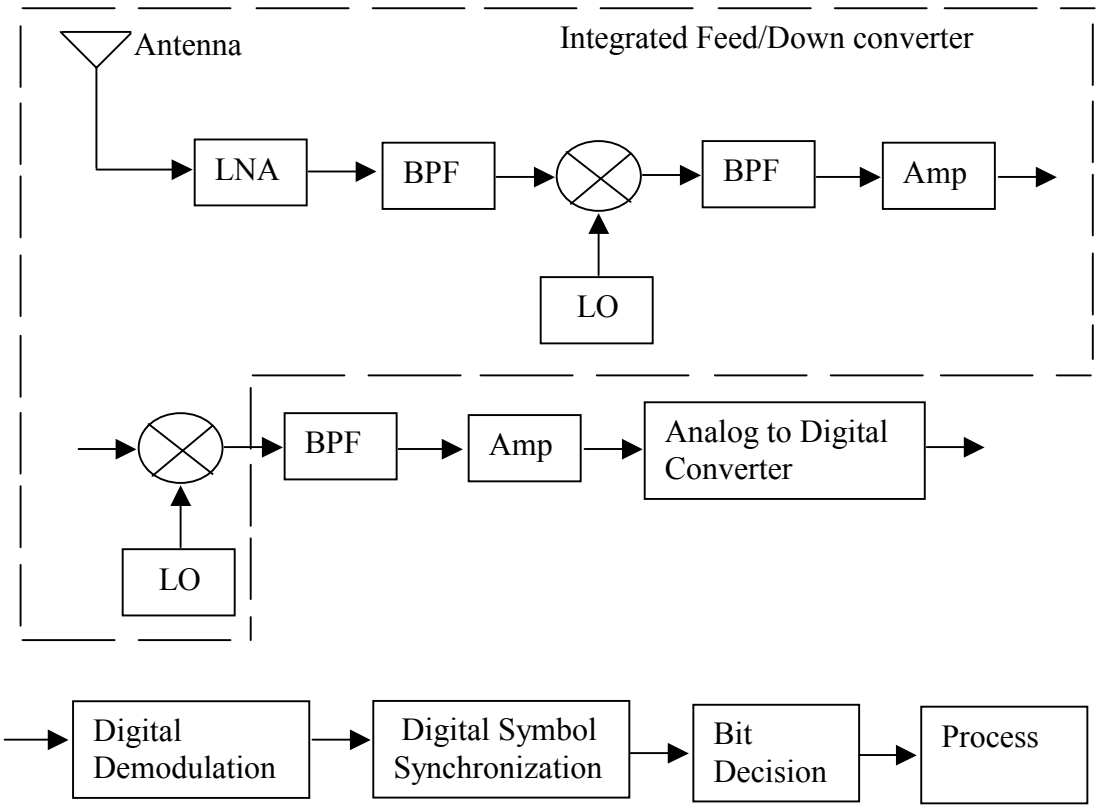

Figure 4.1. Digital Receiver Design

This design uses Electrically Programmable Logic Devices (EPLD) for the demodulation and synchronization. These devices are extremely flexible and use a hardware description language to describe to operation of the device.

3.1 DPSK Demodulator using Programmable Logic Devices

For optimum detection of differentially encoded PSK, a similar scheme to coherent PSK can be used. Except in this case the reference symbol is a delayed version of the received waveform, and not a known reference. The scheme shown in figure 4.2 requires a carrier recovery loop for optimum performance. The integrator also needs to be bit synchronized from the outset. This is complicated and prone to errors at low signal to noise ratios. The delay (T) is one bit period.

This method is only optimal for a wide-band transmitted signal. If the transmitted signal is bandpass limited, the bit error rate performance of the detection scheme in figure 4.2 is greatly reduced. Unfortunately, due to limited spectrum and power, it is not practical to transmit such a wide band signal. The GMS weather satellite has a transmit bandpass filter of 2MHz. The simulations in section 3.2 show degradation in performance of this detection scheme when transmitted in a band-limited channel.

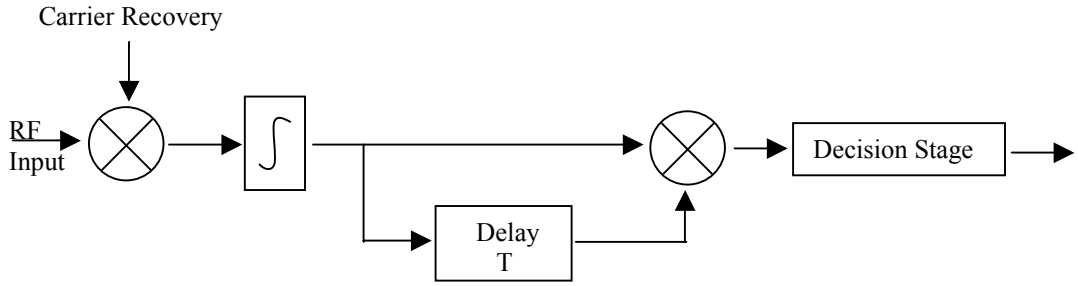

Figure 4.2. Coherent detection of differentially encoded PSK

A second technique that is sub-optimal compared to the above scheme, is to remove the carrier recovery synchronization and place the integrator after the delay and multiply stage. The input signal is now not required to be a baseband signal, as long

as the carrier frequency is an integer multiple of the bit rate. Although sub-optimal, this technique reduces the complexity involved in coherent detection. Figure 4.3 shows this technique.

This technique also suffers from the same degradation in error rate performance if the transmitted signal is band-limited.

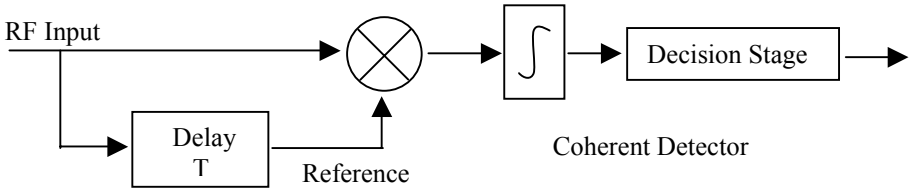

Figure 4.3. Differentially Coherent Detection

Theory of this detection method is presented below.
The input waveform, X(t), and the delayed waveform, Y(t), is:

$$\begin{aligned} X(t) &= \sin(\omega t) \\ Y(t) &= \sin(\omega t + \theta) \quad \theta = 0° \, or \, 180° \end{aligned} \tag{3.1}$$

The output of the multiplier:

$$\begin{aligned} Z(t) &= X(t) \times Y(t) \\ Z(t) &= \sin(\omega t) \times \sin(\omega t + \theta) \\ Z(t) &= \sin^2(\omega t) \times \cos(\theta) - \sin(\omega t) \times \cos(\omega t) \times \sin(\theta) \\ Z(t) &= \tfrac{1}{2}[1 - \cos(2\omega t)] \times \cos(\theta) - \tfrac{1}{2}\sin(2\omega t) \times \sin(\theta) \end{aligned} \tag{3.2}$$

For a DPSK system, the phase of the proceeding bit will be either zero of 180 degrees offset from the current phase. This simplifies the above equation since the second term will be zero.

$$Z(t) = \tfrac{1}{2}[1 - \cos(2\omega t)] \times \cos(\theta) \tag{3.3}$$

This results in a DC component and a large ripple. The ripple is at twice the carrier frequency, see figure 4.4. In figure 4.4, the received signal has first been band-limited. Differentially coherent detection also requires an integrator, shown in figure 4.3, which needs to be bit synchronized from the outset. This is not a problem as a

low pass filter can remove the high frequency component of the received signal and a standard symbol recovery phase locked loop can be used.

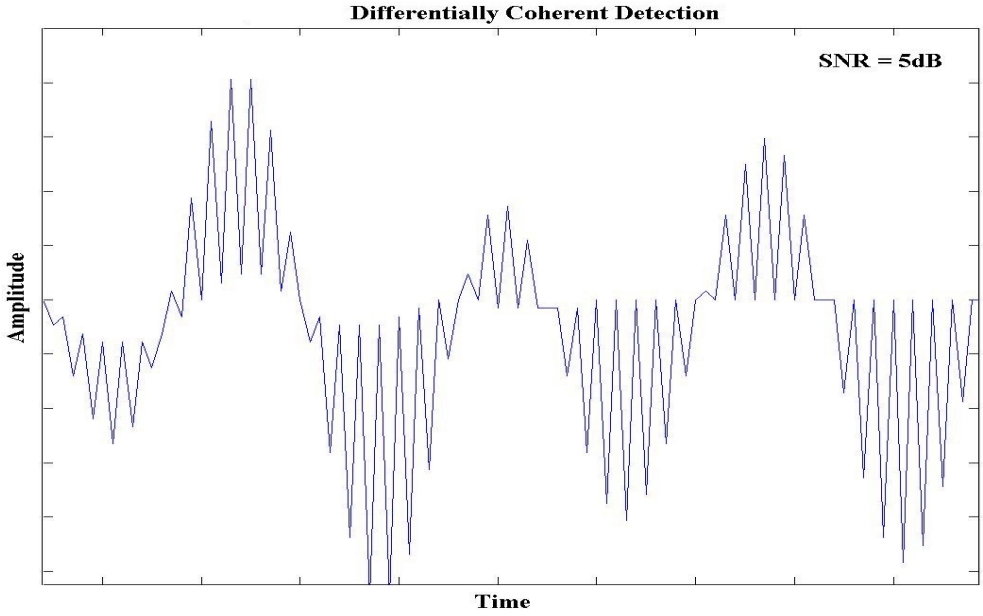

Figure 4.4. I only differential demodulation

A modification of this technique is present in this thesis. The above technique is simplified further by removing the integrator. The integrator is replaced with a sub-optimal Bessel low pass filter, figure 4.5. This design is justified in simulations in section 3.2. When the transmitted signal is band-limited, process gain associated with the integrator is greatly reduced. The noise rejection of the low pass filter offers a higher signal to noise ratio than the previous scheme. Note that this is only when the transmitted signal has been band-limited, this is the case in most practical systems. Figure 4.5 shows the proposed demodulator.

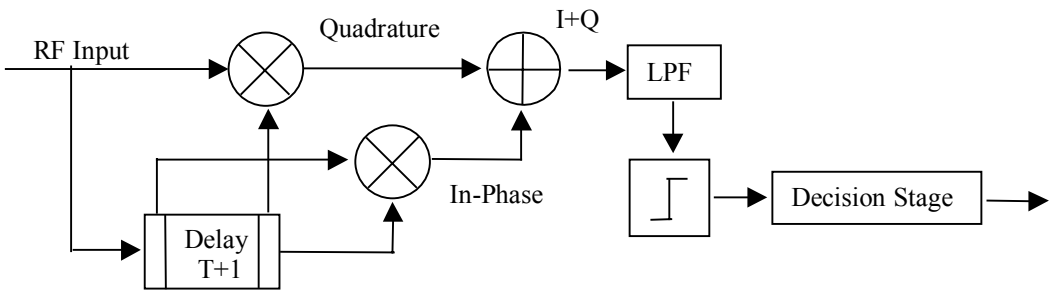

Figure 4.5. Digital Demodulator

$$
\begin{aligned}
Z_Q(t) &= \tfrac{1}{2}[1-\cos(2\omega t)]\times\cos(\theta) \\
Z_I(t) &= \tfrac{1}{2}[1-\sin(2\omega t)]\times\cos(\theta) \\
Z_{I+Q} &= 1-(\cos(2\omega t)+\sin(2\omega t))\cos(\theta) \\
Z_{I+Q} &= \cos(\theta)
\end{aligned}
\tag{3.4}
$$

This technique removes the ripple from equation 3.3, before the low pass filter stage by using the in-phase and quadrature components of the received signal. Equation 3.4 shows the output of the I&Q addition in figure 4.5. This demodulator is realized digitally with the use of Electrically Programmable Logic Devices (EPLD).

For the demodulator to combine in-phase and quadrature components to cancel the high frequency component of equation 3.3, each sample must be 90 degrees out of phase from the previous, when this is the case, equation 3.4 is correct. Therefore, the sample frequency is chosen such that there are a multiple of four samples per data period:

$$Fs = n\times 4\times 660KHz \ \ (n=1,2,3,etc) \tag{3.5}$$

Where 660 kHz is the bit-rate of the SVISSR and HiRID transmission. The intermediate frequency filter before the analog to digital converter, is of Bessel type, so the attenuation roll-off is slow. A sufficient sample frequency must be chosen so that the DPSK sidebands and noise are not aliased back into the first Nyquist band with any significant energy. A sample frequency of 10.56MHz (n=4) is chosen to meet this criteria. This provides 16 times oversampling. A fourth order Bessel bandpass filter has been chosen for the IF filter and provides sufficient attenuation before being aliased into the first Nyquist band.

An Intermediate carrier frequency is chosen so that after sampling the carrier will be mixed to the centre of the first Nyquist band.

$$Fc = k\times\frac{Fs}{4} \ \ (k=1,3,5,7,etc) \tag{3.6}$$

Selecting K being an odd multiple meets the requirement that each consecutive sample is 90 degrees out of phase. K is chosen to be seven, this gives an intermediate frequency of 18.48MHz. This frequency is sufficiently far away from the 10.56MHz sample clock so that the 18.48 – 10.56 MHz harmonic and other inter-modulation products are not mixed down into the first Nyquist band.

It can now been seen that from figure 4.6, that the two multiplier paths are out of phase by 90 degrees.

The output of the adder will have the following form

$$Z(t) = \sin(\omega t) \times \sin(\omega t + \theta) + \cos(\omega t + \alpha) \times \cos(\omega t + \theta + \alpha) \quad (3.7)$$

For differential binary phase shift keyed signals the phase change between symbols will be either zero or 180 degrees. Therefore, the above equation simplifies to.

$$\begin{aligned} Z(t) &= \sin^2(\omega t) + \cos^2(\omega t + \theta) = 1 \qquad \theta = 0° \\ Z(t) &= -\sin^2(\omega t) - \cos^2(\omega t + \theta) = -1 \quad \theta = 180° \end{aligned} \quad (3.8)$$

The symbol α is a phase rotation caused by a frequency error, ideally this will be very small. A carrier frequency error or sample frequency error will cause a ripple on the in-phase and quadrature signals.

The output of the adder will result in a baseband signal with no ripple (i.e. assume no frequency error). Figure 4.6 shows the effect of summing I and Q to produce the differentially demodulated waveform. Note that the input signal has been band-limited.

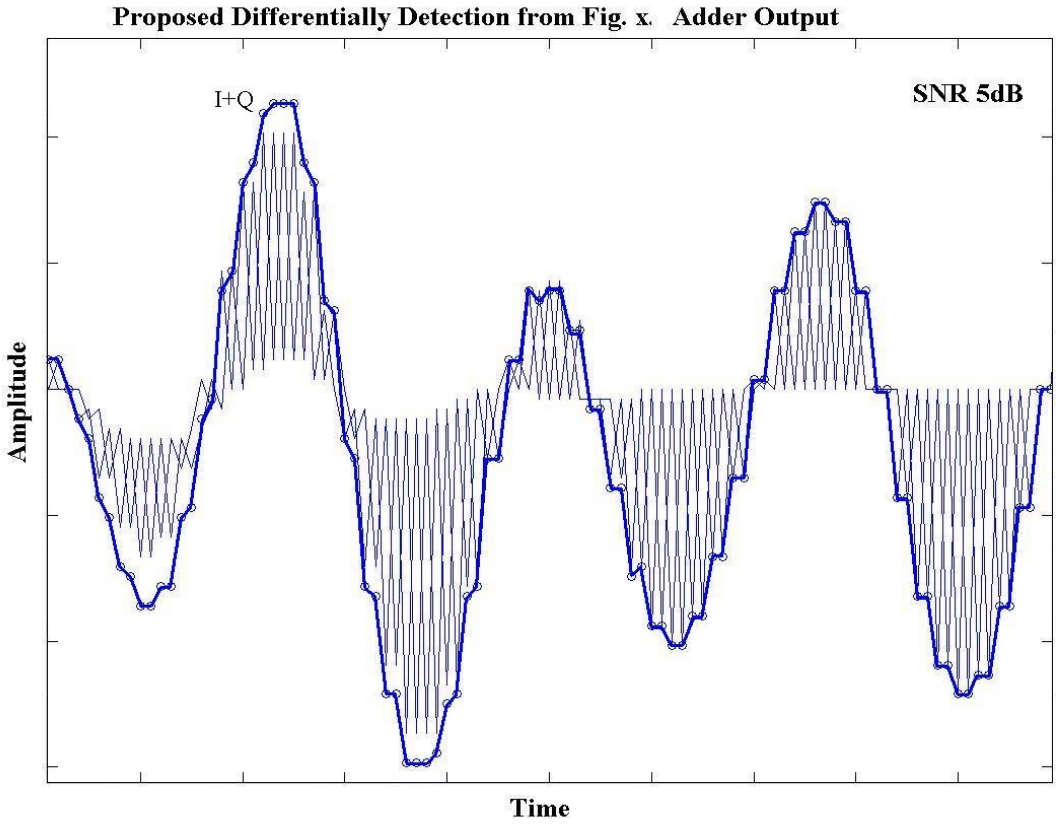

Figure 4.6. I+Q differential demodulation

The demodulator in figure 4.5 can further be simplified. One of the multipliers is redundant, figure 4.7 show the simplified demodulator, which is theoretically equivalent to the demodulator in figure 4.5.

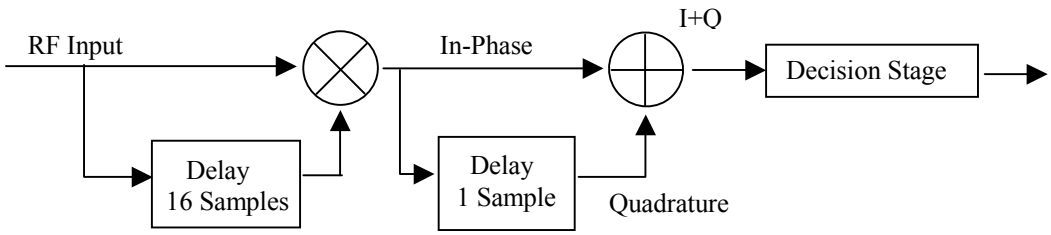

Figure 4.7. Simplified Digital Demodulator

The effect of a carrier frequency error and sample frequency can be simulated to show the degradation in the summer output. Figure 4.8 shows the tolerance of this BPSK demodulator to frequency errors, this figure is derived from equation 3.8.

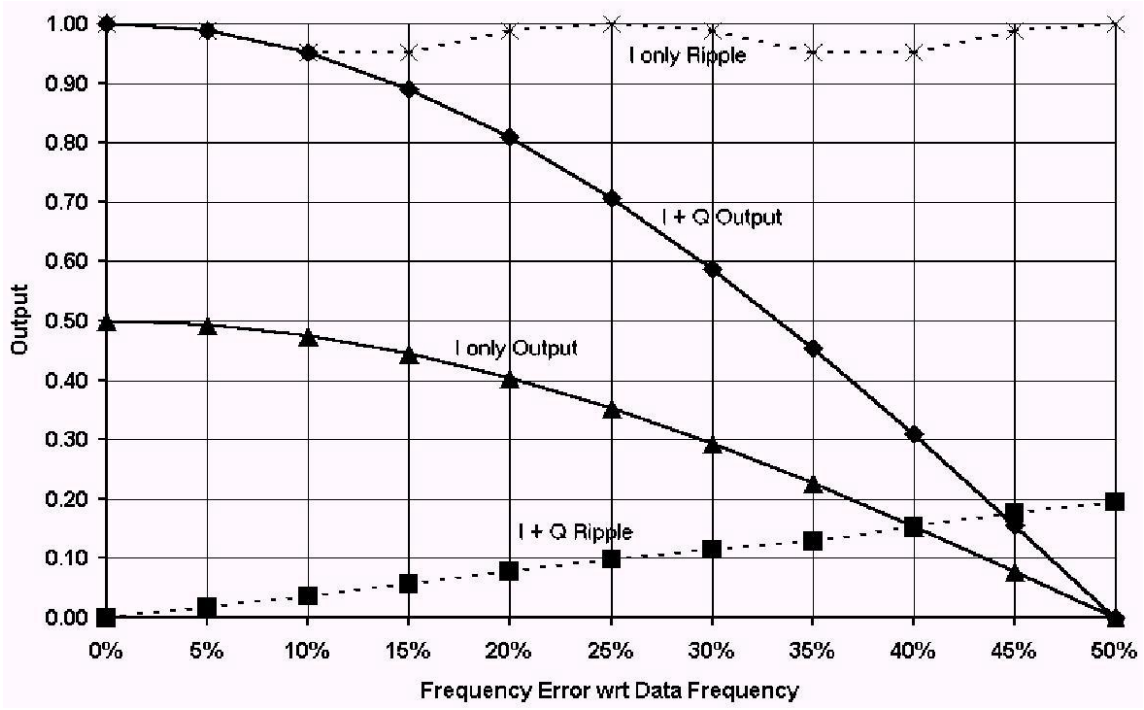

Figure 4.8. Effect of Frequency error on summation output. [4]

The I only output signal contains the high frequency ripple from equation 3.3, while the I+Q ripple is zero when there is no frequency error. As the frequency error increases, the I+Q ripple increases to 20% the output voltage at a frequency error of 50% the bit rate. The 3-dB point of the receiver is when there is a 25% frequency error, this is a severe error of 2.64 MHz at the 10.56 MHz reference clock. The proposed receiver can operate with no performance degradation using a 100-ppm reference crystal, this corresponds to a maximum frequency error of 0.01%. This is well within the stability achieved in a practical system.

3.2 Demodulator Simulations

3.2.1 Selecting IF and baseband filter bandwidths

A simulation of the proposed EPLD demodulator is required to select the Intermediate Frequency (IF) and baseband filters for optimal Bit Error Rate (BER).

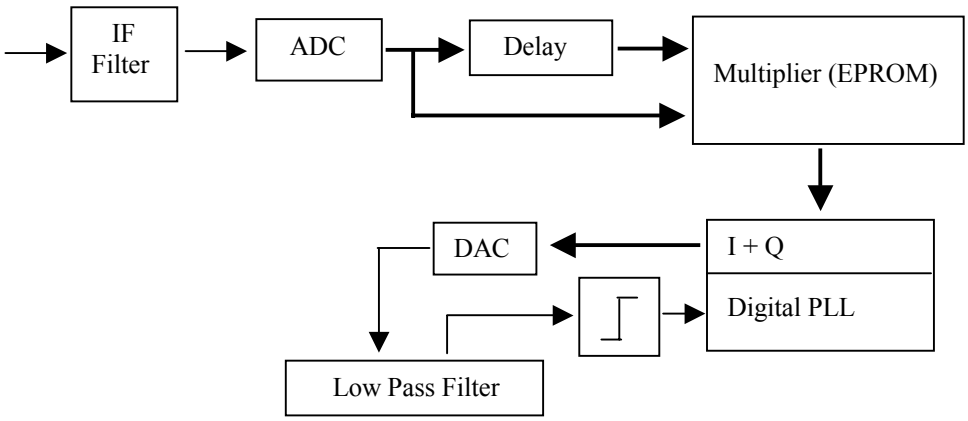

Figure 4.9. Digital Demodulator

The Baseband Low Pass Filter (LPF) is required to reduce wide-band gaussian noise but the filter also increases the zero crossing timing jitter introduced to the digital phase locked loop. The LPF filter bandwidth should be as wide as possible to reduce the timing jitter, then the IF filter is critical to reduce wide-band noise. A LC filter with a narrow bandwidth is quite difficult to make at 18.48MHz. A compromise from the simulations can be determined to find suitable filter bandwidths. The Nyquist bandwidth, Fs/2, is 5.28MHz. Care must be taken there is sufficient filter attenuation of the received signal before aliasing.

Filter Bandwidth combinations are tested for a 4^{th} order Bessel IF bandpass filter and 5^{th} order Bessel baseband LPF. Combinations of 40% to 110% of the bit rate are tested for both filters. Signal to noise ratios of 4, 6 and 8 dB are simulated to check the bandwidth requirements across various signal conditions.

Signal to noise ratio is determined by a 1024 tap FIR Blackman filter at the intermediate frequency with its bandwidth equal to the 2 x bit-rate. This is chosen as the reference because it can be measured on a spectrum analyser and a direct comparison to measured bit error rates can be determined. The actual signal to noise ratio is dependent on the filter bandwidths. The simulations are performed with 16 times oversampling, this is the same as the practical demodulator.

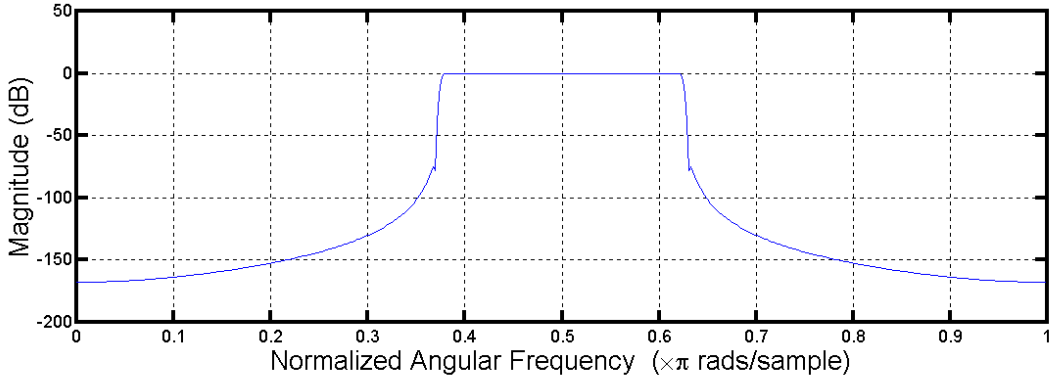

Figure 4.10. Blackman Filter for determining signal to noise ratio

Five simulations are performed for each of filter bandwidth combinations at various signal to noise ratio.

1 IF and Baseband filter bandwidths Vs. standard deviation of zero crossings

A contour plot represents the standard deviation of the zero crossings for each of the IF and baseband filter bandwidths. It is expected that as the filter rise-time decreases (wider bandwidth) the standard deviation would decrease. Filter bandwidth and rise-time are related by the following equation.

$$Rise\ Time = \frac{1}{\gamma \times Filter\ BW} \tag{3.8}$$

Where γ=2.88, Zverev [6], for a Bessel filter. Figure 4.11 shows the simulated results for a signal to noise ratio of 4dB.

This plot shows that the standard deviation of timing jitter is more dependent on the bandwidth of the intermediate frequency filter. An IF filter bandwidth of 60% of the bit-rate gives the best noise rejection performance, while allowing the baseband filter to be increased to reduce the standard deviation and timing jitter. Variation in the IF filter bandwidth gives more variation in the timing jitter standard deviation if the baseband filter is closer to the bit-rate. This plot is calculated for a very low signal to noise ratio of 4 dB. This SNR is not expected in the actual system, and the variation in standard deviation due to filter bandwidths will be less severe at higher SNR.

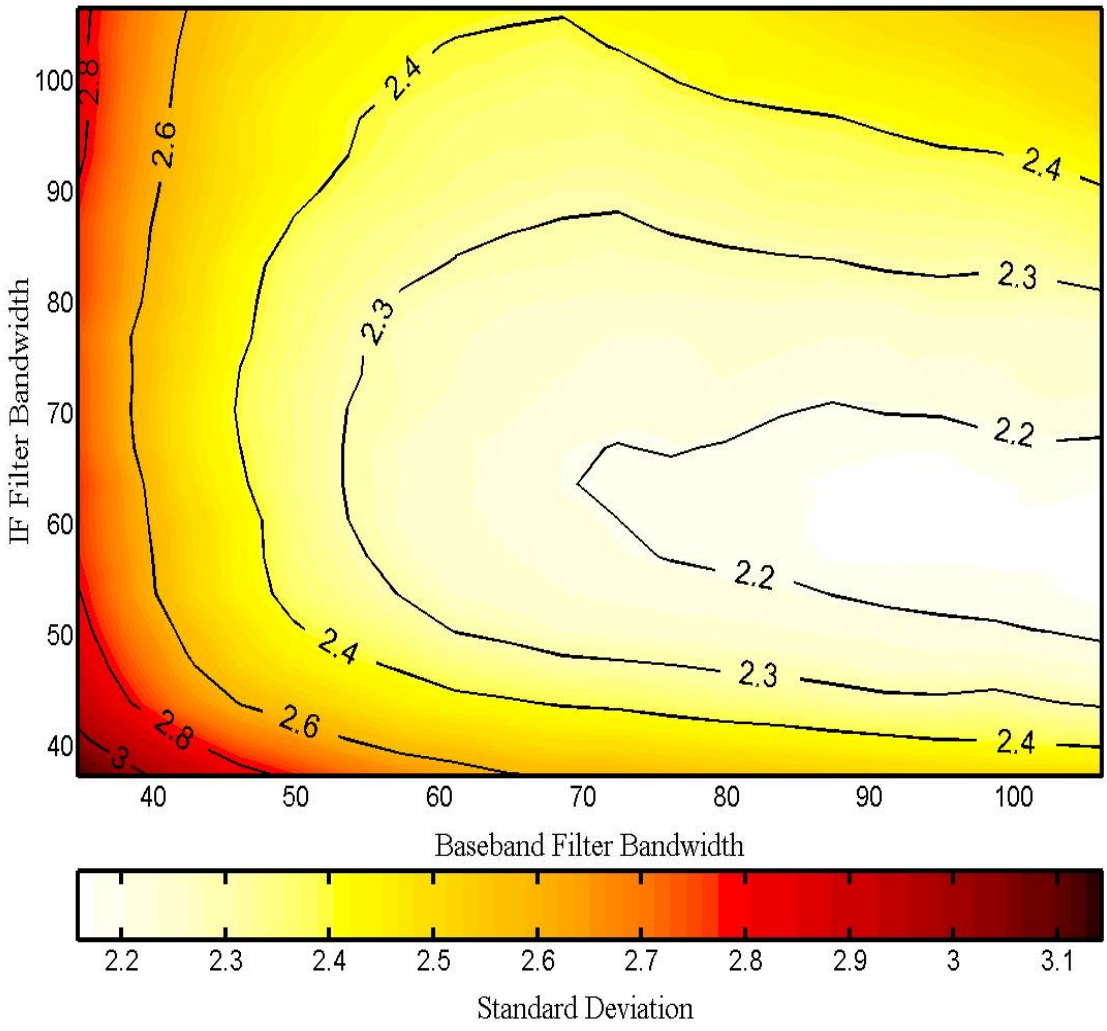

Figure 4.11. Filter Bandwidth Vs. Standard Deviation of timing jitter (4dB SNR)

2 IF and Baseband filter bandwidths vs. bit error rate with carrier noise

This is a contour plot with the y-axis being the IF filter bandwidth, x-axis the baseband filter bandwidth and contours are the bit error rate.

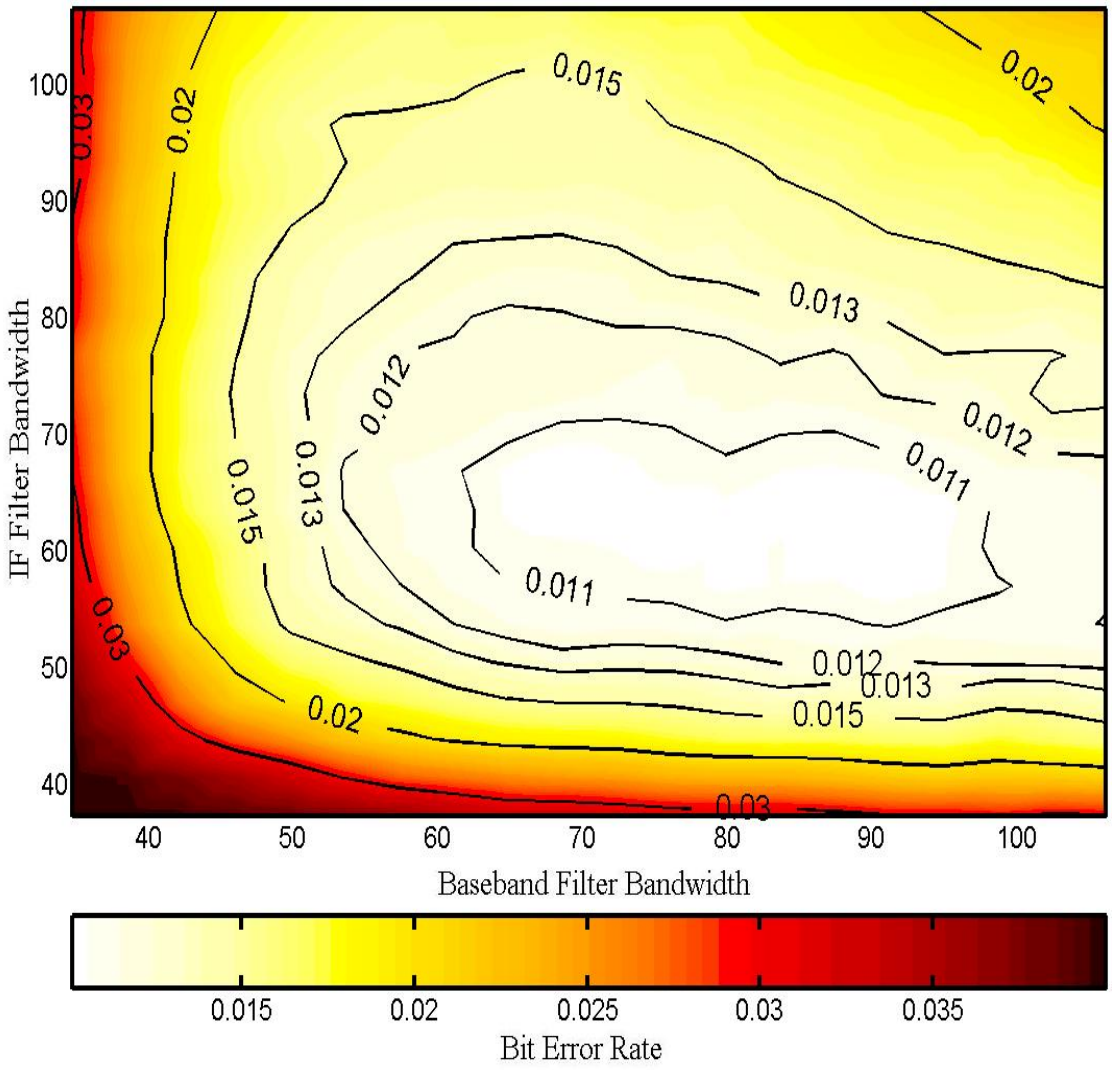

Figure 4.12. IF and Baseband filter bandwidth Vs. BER (with carrier noise)

The carrier noise is determined from the standard deviation of the zero crossings. The optimum sample selection point is in the middle of the filtered data (8 samples). Gaussian noise with a standard deviation equal to the standard deviation of the zero crossings is added to the sample being selected.

Figure 4.12 shows the effect of adding carrier noise. This plot follows the curves of the stand deviation of the zero crossings. This shows that the bit error rate is dependant on the zero crossing standard deviation of the received signal for low signal to noise ratios. As the SNR increases the standard deviation variation with bandwidth become less significant and bit error rate variations become less significant. This shows importance of the accurate filter bandwidths at low signal to noise ratios.

3 IF and baseband filter bandwidths vs. bit error rate, no carrier noise

This is a contour plot with the y-axis being the IF filter bandwidth, x-axis the baseband filter bandwidth and contours are the bit error rate.

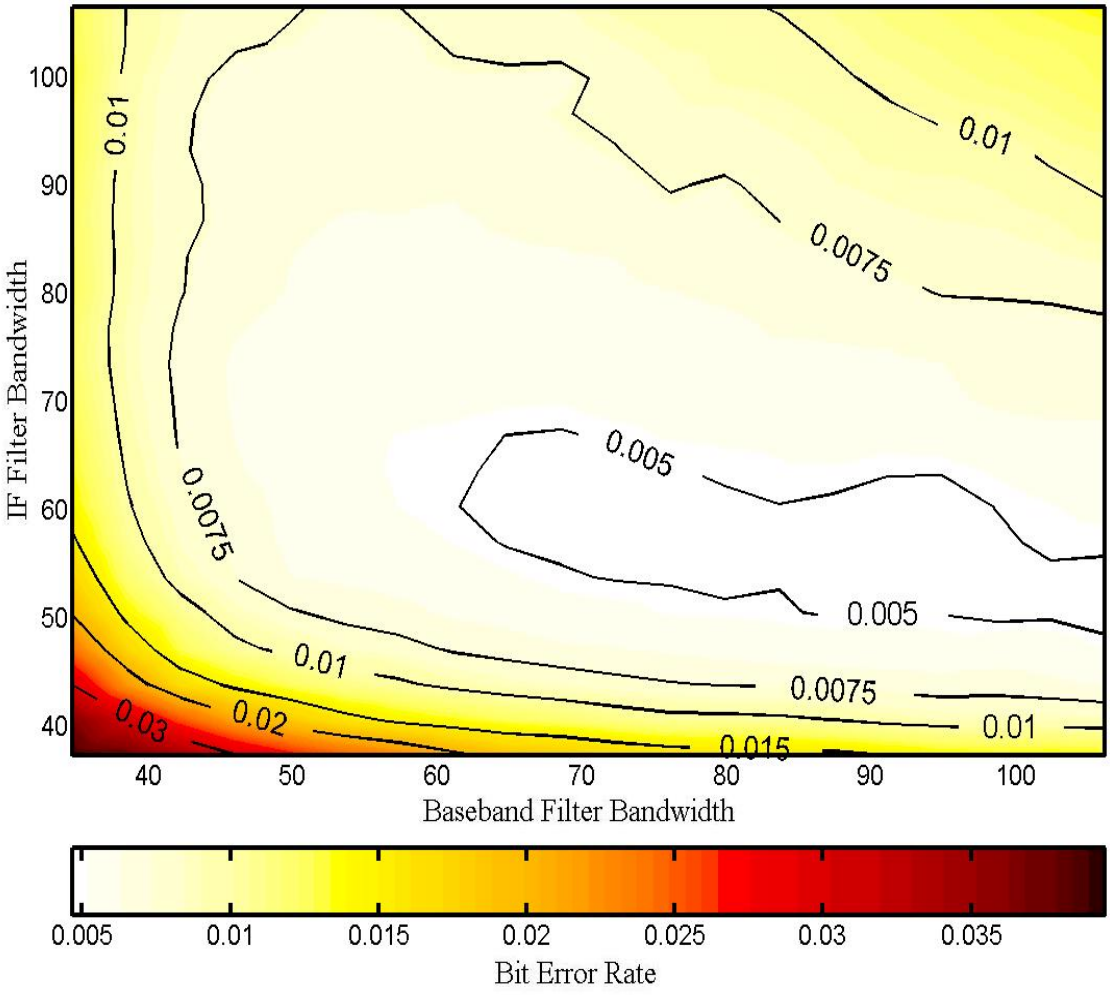

Figure 4.13. IF and baseband Filter Bandwidths Vs. BER (no carrier noise)

Figure 4.13 uses the same data as figure 4.12, but there has been no gaussian noise added to the sample selection, i.e. no timing jitter. All samples are selected at the optimum sampling point. This would occur under ideal synchronization circumstances. For the best bit error rate performance, the bandwidth of the intermediate frequency is critical. A bandwidth of 60% corresponds to 18.48MHz +/- 396KHz. This is very difficult to make as a LC filter. Very high inductor Q's and very accurate inductors are required for the narrow bandwidth. Therefore the baseband filter should be selected for best bit error rate performance independent of the bandwidth of the IF filter that can be made.

4 IF filter bandwidth vs. bit error rate (baseband filter BW = 70%)

This plot shows the variation of the bit error rate with the baseband filter bandwidth fixed at 70% of the bit-rate. A low pass filter of 462KHz is easier to make than the IF bandpass filter. The IF Filter ideal sync line represents the performance degradation with variation in IF filter bandwidth, under ideal synchronization and the bit selection taken before the baseband filter.

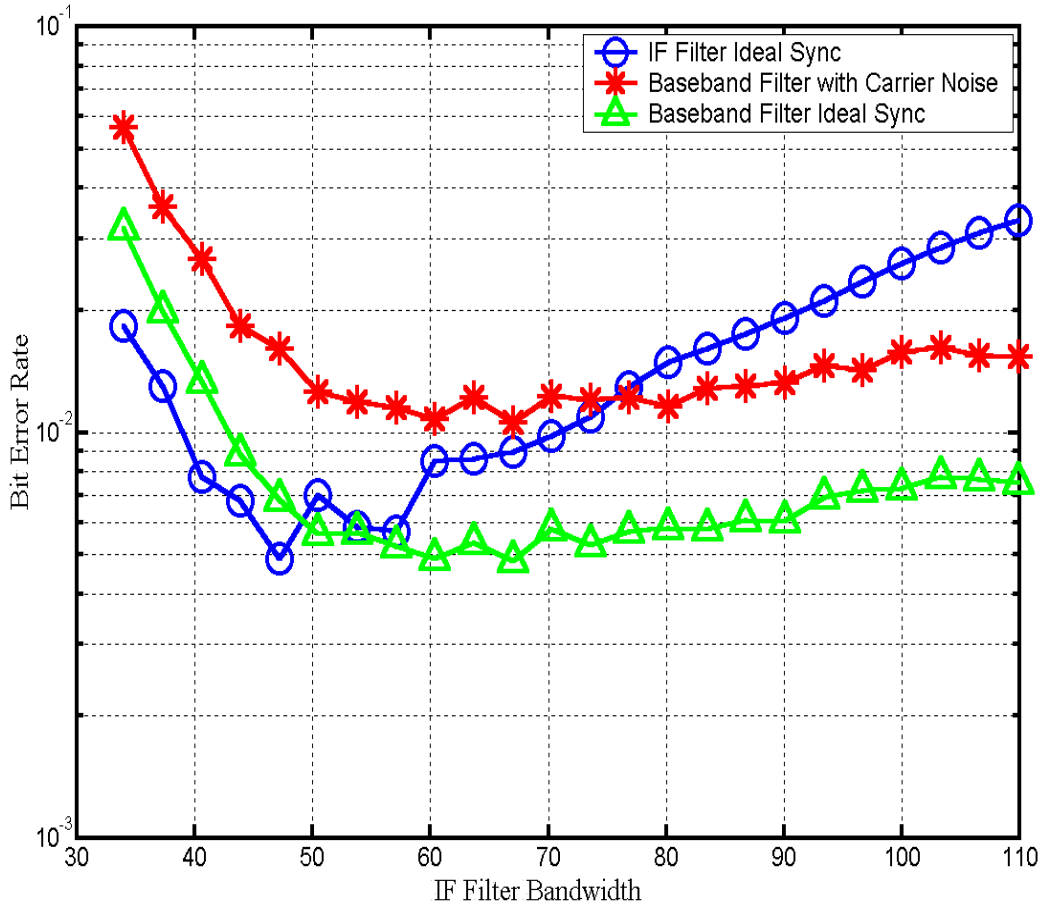

Figure 4.14. IF filter Bandwidth Vs. BER (baseband filter = 70% bit-rate)

The Baseband Filter Ideal Sync line of figure 4.14 shows the bit error rate performance under ideal synchronization and bit selection taken after the baseband low pass filter, with a baseband filter bandwidth of 70% the bit-rate. This shows that the bit error rate performance varies by 60% over the IF bandwidth range of 60% to 110%. The baseband filter with carrier noise line shows the same data but with noise added to the zero crossing selection samples. Even with noise, the performance variation is only 40% across an IF filter bandwidth range of 60-110%. The IF filter ideal Sync line show the performance of relying on the IF filter only for noise suppression, i.e. no baseband filter. Under this condition the IF filter bandwidth is critical and should be approximately at the Nyquist rate.

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5 IF filter bandwidth vs. bit error rate (with/without carrier recovery)

This plot shows the bit error rate Vs. IF filter bandwidth for a baseband filter bandwidth 70% of the bit rate. The ideal carrier recovery line shows the estimated performance of a receiver with a carrier recovery loop, i.e. Costas loop. Ideal carrier synchronization is assumed, the signal is then demodulated at baseband instead of at an intermediate frequency.

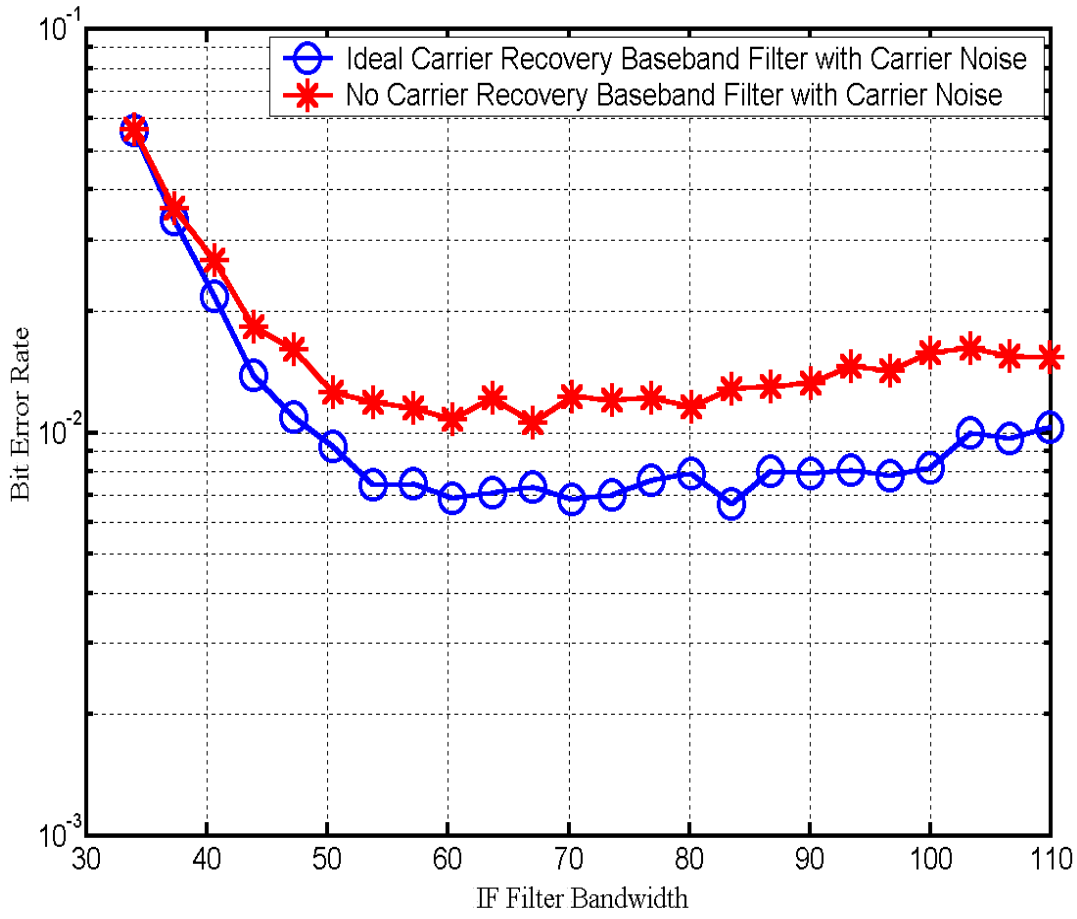

Figure 4.15. IF filter Bandwidth vs. BER

The no carrier recovery line shows the bit error rate performance of the demodulator if the signal at the input of the receiver is at an intermediate frequency, such that the signal is situated in the middle of the Nyquist band. No frequency offset of the intermediate frequency is used for these simulations. Both lines include the addition of carrier noise.

The bit error rate varies by 50% from the ideal baseband case. This is expected as the demodulator does not use ideal power combination for the I and Q samples.

3.2.2 Simulation Results

From the simulations, the baseband and IF filter bandwidths can be chosen. The bandwidths are chosen for optimum bit error rates, but the practicality of the intermediate frequency bandwidth must also be taken into account. IF filter bandwidths less than the bit-rate is difficult to make, they require very accurate and high Q inductors. For this reason, the intermediate frequency bandwidth is chosen to be as small as practical, approximately 80% the bit rate can be made.

The baseband filter bandwidth is now critical and needs to be set to 70% the bit rate for optimum performance. This bandwidth is realizable with a LC filter. Component values are reasonable and the filter is easy to make. The above simulation for signal to noise ratios 4,6 and 8 are included in appendix J. Matlab 5.3 code is in appendix K for reference.

By introducing another intermediate frequency stage at 70 MHz, a Surface Acoustic Wave (SAW) filter with a narrow bandwidth can be used to improve bit error rate. These filters are designed with a flat group delay and a steep roll-off, but they suffer from having a passband ripple and large insertion loss. A SAW filter with a bandwidth of 900 kHz is available, this corresponds to 68% of the baseband bit–rate. This could improve bit error rate performance by 20-30% at low signal to noise ratios in the system described above.

3.2.3 Comparison with other PSK and DPSK demodulation techniques

Once the filter bandwidths have been selected, a simulation is required to compare the proposed demodulator with other PSK and DPSK demodulation techniques. A comparison can be made with coherent PSK and DPSK. The transmitted GMS and MTSAT satellite signals are band-limited before being transmitted. The transmit bandwidth is less than 2MHz. The band limiting can also be simulated for a realistic comparison with coherent demodulators.

The effective demodulated signal to noise ratios is also determined for each technique. This shows the effective gain obtained from coherent receivers for wide-band and band-limited techniques.

The bandwidths of the intermediate and baseband filter have been determined from the previous simulations. IF filter bandwidth is +/-80% of the bit-rate, this is +/-528KHz. The baseband filter is 70% of the bit-rate, this is 462KHz. These filter bandwidths are now used to compare the proposed demodulator to standard Phase Shift Keyed demodulators.

The three standard demodulation techniques are coherent PSK, coherent DPSK and differentially coherent DPSK. The proposed demodulator is a variation of the last technique mentioned. The standard receivers are described in section 3.1 which use an integrate and dump filter.

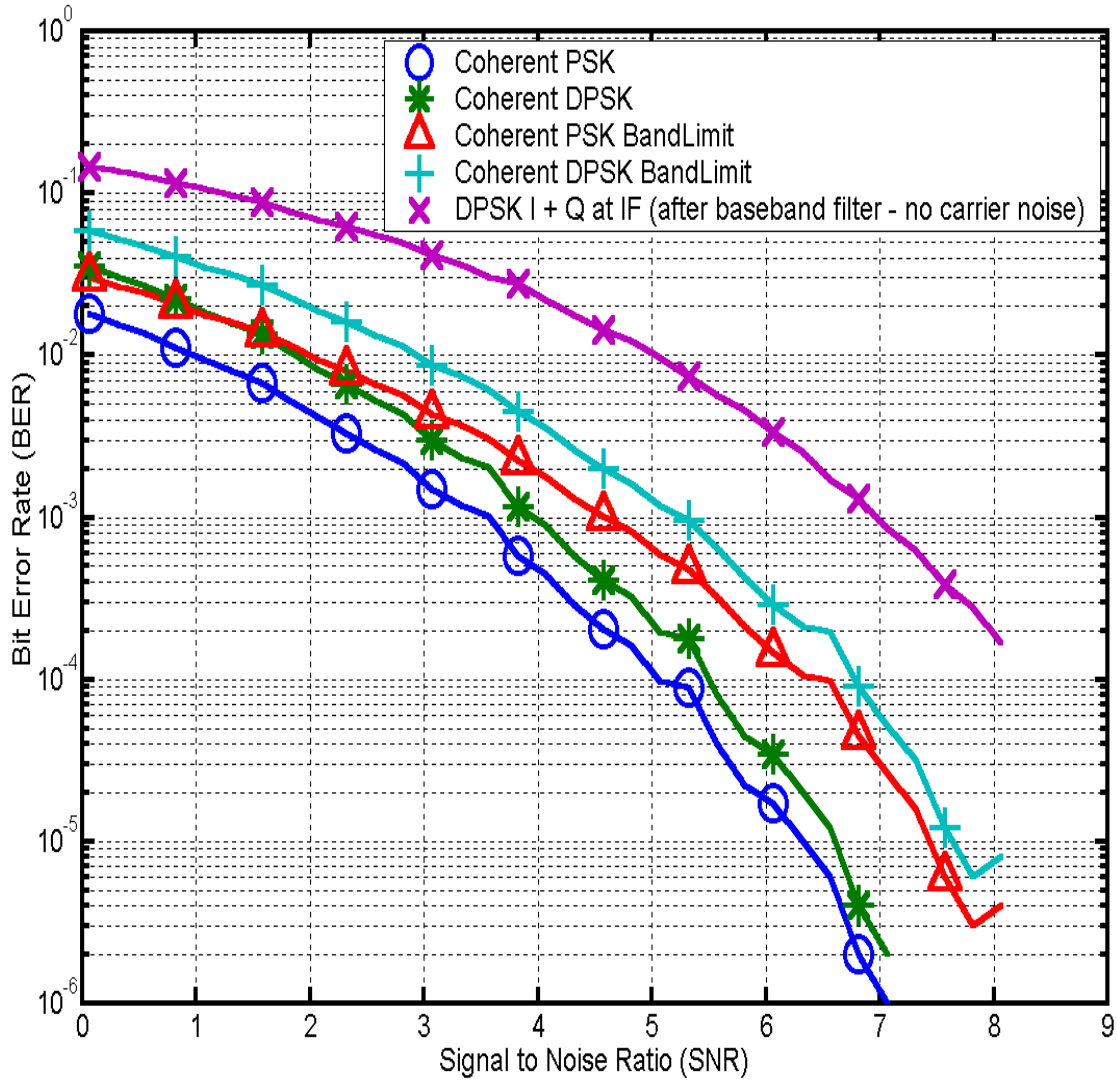

Figure 4.16. SNR Vs BER coherent phase shift keying

In a low signal to noise environment, it would be impossible, in practice, to achieve the above performance for a coherent receiver design. The coherent PSK and coherent DPSK plots in the above simulation is the result of ideal carrier and symbol synchronization. The band-limited PSK and DPSK plots are coherent PSK and DPSK but have a 2nd order Butterworth filter at 1.5 x the bit-rate. This filter simulates the transmit filter on the GMS/MTSAT satellite. The performance degradation due to the filter is most noticeable as the signal to noise ratio increases. A difference is greater than 1 dB at signal to noise ratios greater than 5 dB. This

band-limited coherent DPSK plot corresponds to the best possible bit error rate (BER) obtainable for the MTSAT system.

The DPSK I+Q plot in the above simulation is the proposed demodulator simulated using the selected filter bandwidths. This corresponds to the best obtainable BER for the proposed demodulator. The plot does not include carrier noise introduced by the digital phase locked loop or filters. The performance is approximately 2 dB worse than the band-limited coherent DSPK demodulator.

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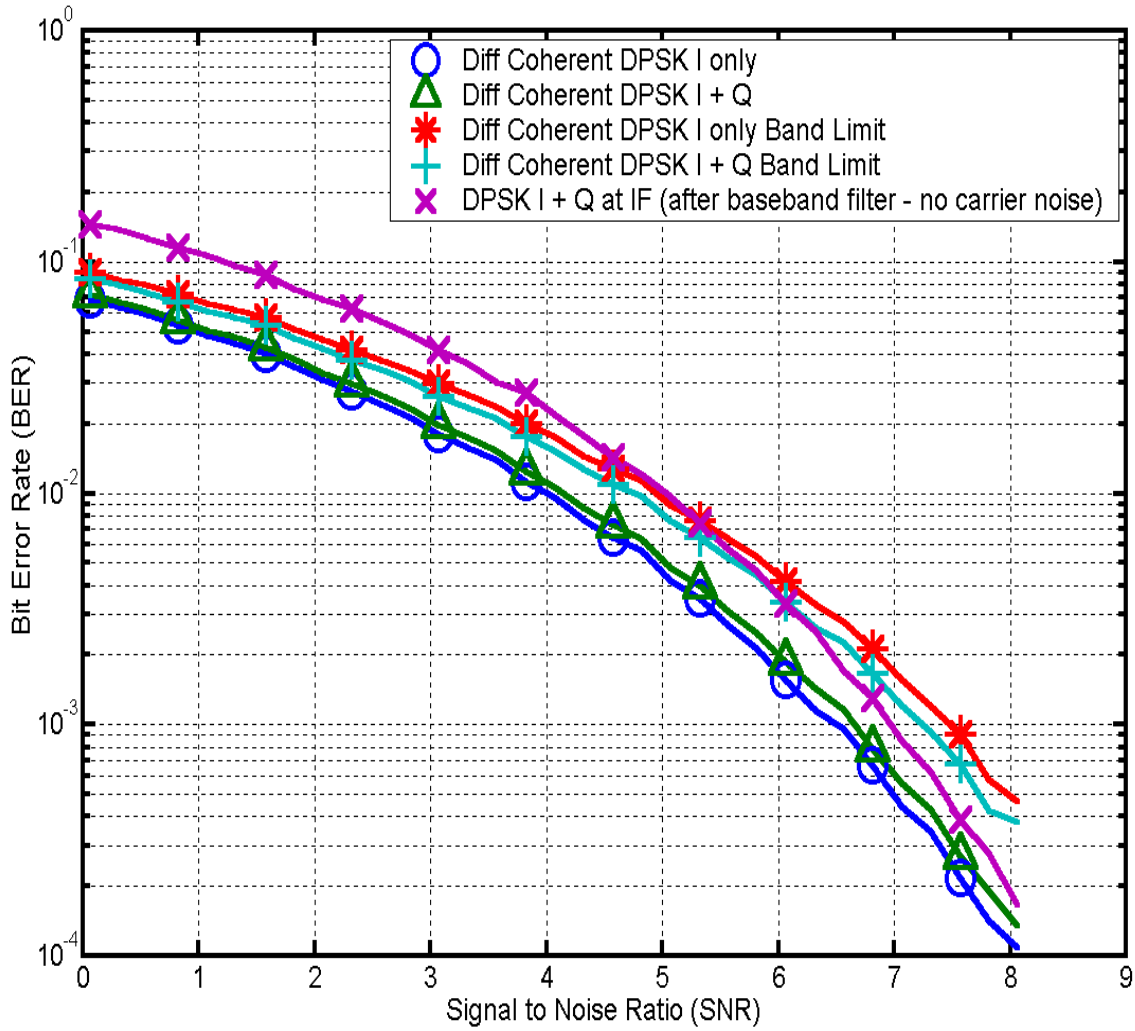


Figure 4.17. Differential Coherent Differential Phase Shift Keying

Figure 4.17 shows a comparison of ideal differential coherent DPSK and the proposed demodulator. The differential coherent demodulators are simulated at baseband while proposed demodulator is simulated at an intermediate frequency. The proposed demodulator approaches the ideal differential coherent DPSK at higher signal to noise ratios. The DPSK plot surpasses the performance of the practical GMS/MTSAT band-limited differential coherent DPSK demodulator after 5.5 dB signal to noise ratio. For all the plots, the I+Q plot slightly outperforms the I only simulation.

This shows that by selecting the correct IF bandpass and baseband filters, the integrate and dump differentially coherent receiver is not required for reliable reception.

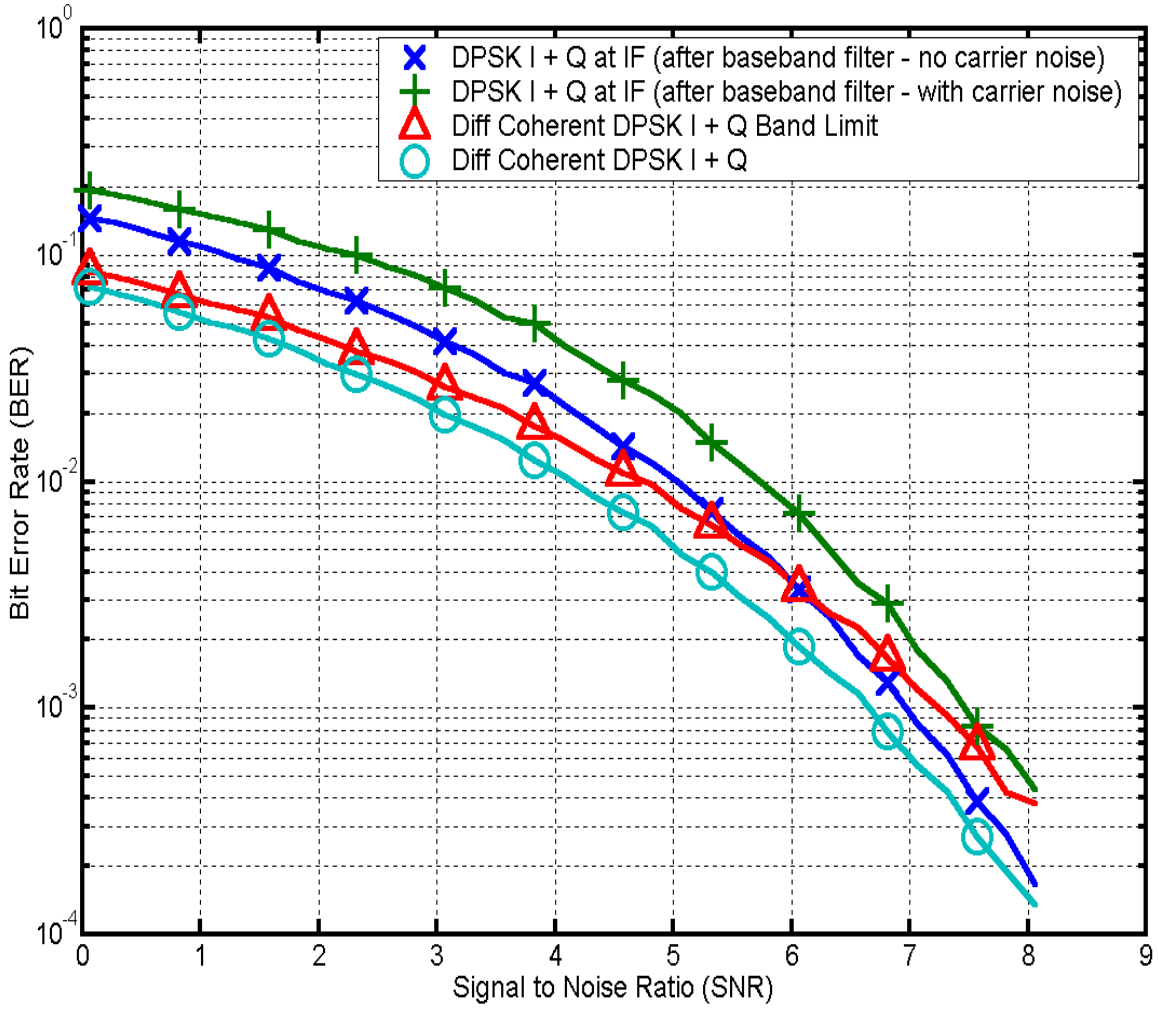


Figure 4.18. Differential coherent DPSK and DPSK demodulators

This simulation shows the performance of the differential coherent DPSK demodulator, band-limited differential coherent DPSK demodulator and the proposed demodulator with and without carrier noise (timing jitter). The degradation of the band-limited signal is about one dB at 7 dB SNR. This is due to a loss in the process gain of the integrate and dump filter. At approximately 5.5 dB the proposed DPSK I+Q demodulator surpasses the performance of the band-limited differentially coherent receiver. The proposed demodulator with carrier noise added to the bit selection point degrades the performance by 1 dB. The standard deviation of the carrier noise is determined form the simulation 1, figure 4.11. At 8 dB SNR the performance of the band-limited differentially coherent DPSK receiver and the proposed receiver with carrier noise is approximately the same. The differentially coherent DPSK receiver is an ideal case. This does not take into account the timing jitter associated with a symbol recovery phase locked loop.

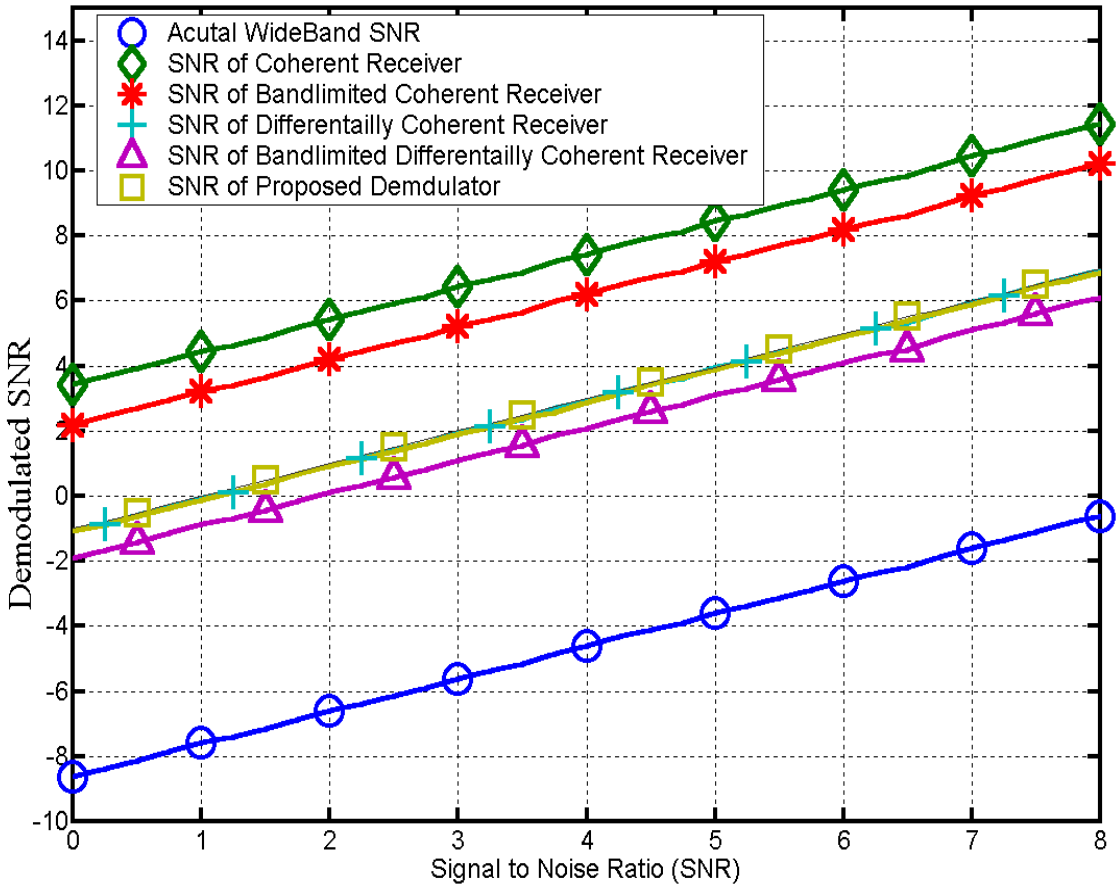


Figure 4.19. The Actual Signal to Noise Ratio of each of the Receivers

Figure 4.19 shows the demodulated signal to noise ratio seen be each of the receivers. The receiver design has an oversample rate of 16. Theoretically, this should provide a process gain of:

$$\begin{aligned} PG &= 10\log_{10}(Oversample\ Rate) \\ PG &= 10\log_{10}(16) = 12\ dB \end{aligned} \tag{3.9}$$

The actual wideband signal to noise ratio of the channel is shown in figure 4.19. From the simulations, the Coherent PSK receiver provides a process gain of 12 dB, which is as expected. If the received signal is band-limited with a 2^{nd} order Butterworth band-pass filter with a bandwidth of 1.5 x the bit rate, the signal to ratio seen by the coherent receiver drops by 2 dB. A differentially coherent receiver is sub-optimal. From figure 4.19 there is a 4-5 dB drop in the SNR seen by the receiver. This degrades the performance but simplifies the receiver, as no carrier recovery loop is required. Figure 4.19 also shows signal to noise ratio of the differentially coherent receiver with the received signal band-limited. The band-limiting filter is the same one that is used for the coherent receiver.

The proposed receiver in this thesis removes the integrate and dump filter from the differentially coherent receiver. Instead, the wide-band noise is reduced with the use of a bandpass and low pass filter. Figure 4.19 shows hat the receiver has a similar SNR as the differentially coherent receiver design. Matlab 5.3 code is available in appendix L for reference.

Chapter 5 EPLD Receiver Design

4.1 EPLD Demodulator and Synchronization Introduction

The simplified DPSK demodulator block diagram shown in figure 5.1 is to be implemented in hardware with inexpensive electrically programmable logic devices (EPLD).

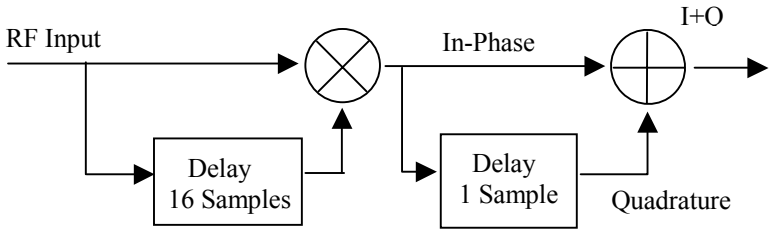


Figure 5.1. Demodulator Block Diagram

The Lattice Semiconductor's ispLSI 1032E is chosen for its price/density performance. Appendix E, gives an overview of the Lattice EPLD architecture.

Four 1032E EPLDs are required to implement the complete demodulator, digital phase locked loop, frame synchronization, FIFO control and parallel port communications. Figure 5.2 shows a block diagram of the complete DPSK receiver and synchronization.

An 8-bit Analog to Digital Converter (ADC) with a sample rate chosen to be 16 times the HiRID and SVISSR bit rate, is 10.56MHz. The density of the delay EPLD limits the oversampling rate. The eight bits per sample are sent to a Lattice 1032E EPLD that performs the one data period delay. One data period delay corresponds to 16 samples. The output of this EPLD provides the input to an EPROM programmed as a look up table to perform the multiplication of the current sample and the sample delayed by one data period. The multiplication is required to be completed within 94.7ns (the period of the 10.56MHz clock). This is achieved with a 512Kbit EPROM with a 60ns access time.

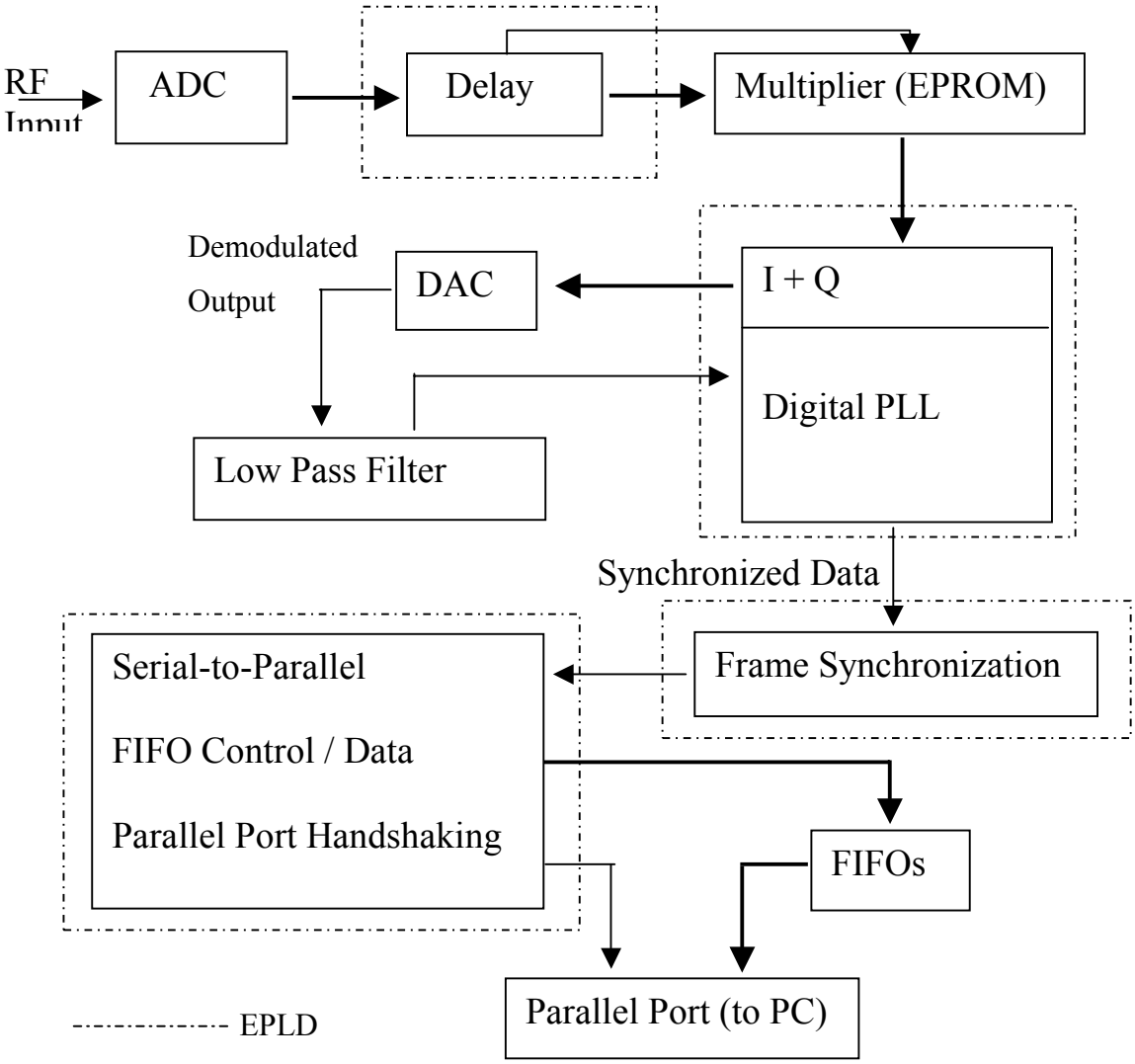


Figure 5.2. Complete receiver block diagram

The EPROM output connects to a second 1032E EPLD to perform the I and Q addition, one sample delay, and the digital phase locked loop. This EPLD also distributes the 10.56MHz clock to the ADC, DAC and delay EPLD.

A Digital to Analog Converter (DAC), figure 5.2, converts the output of the I and Q addition to the analog domain. The resulting waveform is a baseband NRZ (non-return zero) signal that has been differentially decoded, see figure 4.6. This signal is then low pass filtered with a 5^{th} order Bessel filter with the bandwidth determined

from simulations. A comparator with hysteresis is used to convert the filtered signal to TTL voltage levels.

The comparator output is connected to the second EPLD, which also performs the Digital Phase Locked Loop (DPLL) to rechover the symbol timing information. The clock generated from the DPLL is used to latch the data at the input of the digital phase locked loop into a register to be pass onto logic to perform frame synchronization and PN de-scrambling.

The frame synchronization detects the start of each frame and synchronizers the locally generated PN sequence with the header sector to perform the PN de-scrambling. Jumpers select which of the Infrared and Visible Channels are recovered and passed to the next EPLD for transmission to the PC.

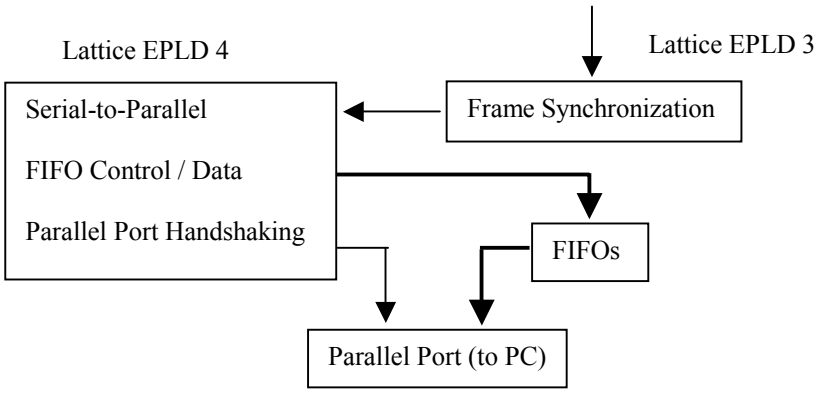


Figure 5.3. Receiver Frame Synchronization and PC interface

The fourth EPLD performs a serial-to-parallel conversion, FIFO control, and parallel port handshaking. The parallel port uses EPP hardware handshaking to improve throughput. The number of FIFOs is jumper selectable from one to four.

4.2 One-data-bit Delay EPLD Implementation

The delay EPLD uses the same 10.56MHz clock as the ADC. Samples are delayed by a grid of 16 x 8 D-Flip-Flops. There is 100% utilization in a 1032E EPLD. Using an EPLD of higher density can increase the oversample rate. The delay is one data bit period. The current sample and the sample delayed by 16 D-flip-flops are the input to and EPROM configured as a look up table multiplier.

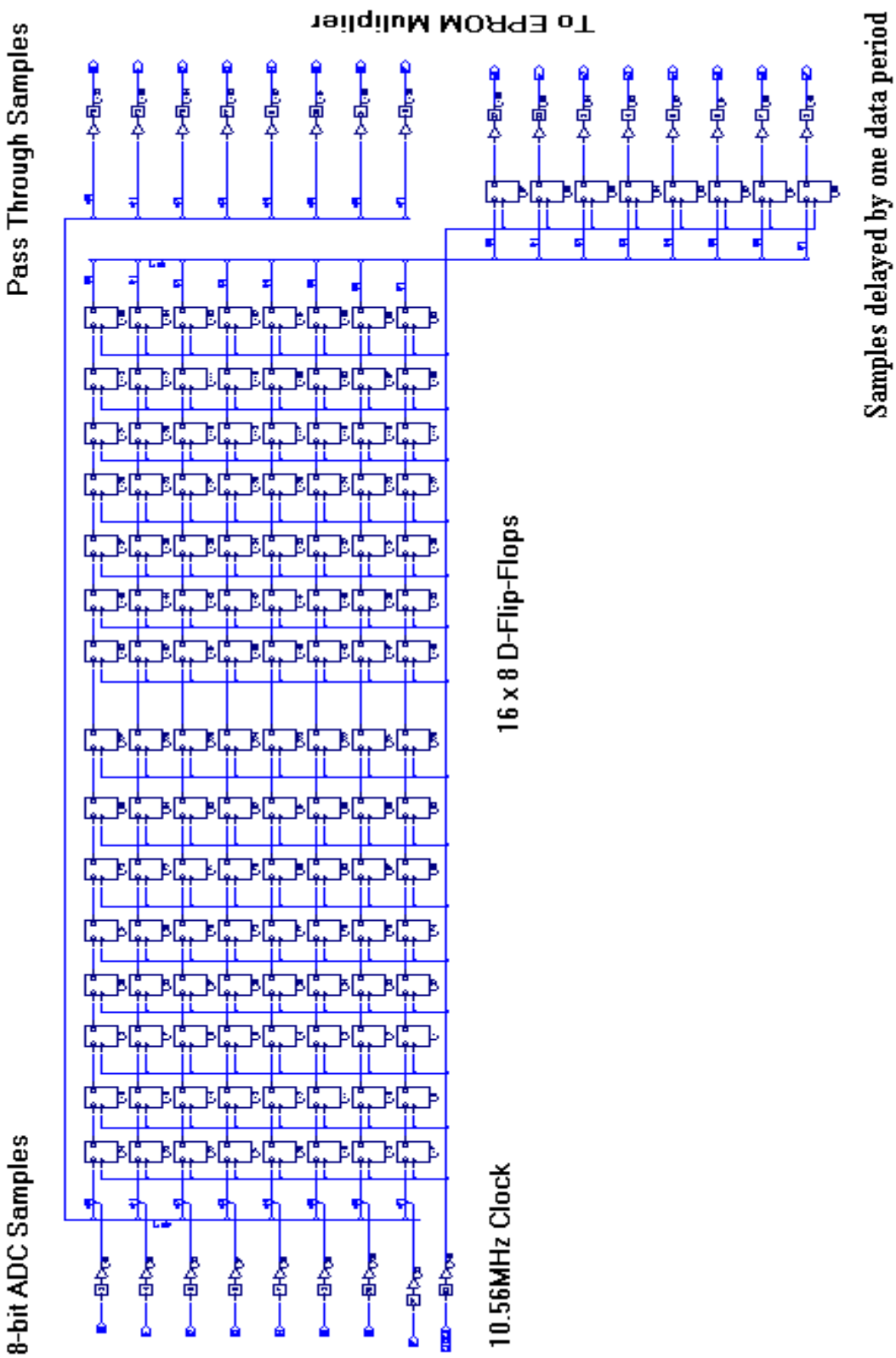


Figure 5.4. Delay EPLD Schematic

4.3 EPROM Look-Up-Table Implementation

The output of the ADC is not in a 2's complement format. Therefore the EPROM is not a straightforward multiplier. The EPROM stores 65536 bytes, this is the number of bytes required for a 8 x 8 bit multiplication. The multiplication output should be 16 bits, but the EPROM has only an 8-bit output. The output of the EPROM is to be in a 2's complement format to permit the subsequent addition to be performed easily. The transfer function required for this multiplication is:

$$\begin{aligned} &for(x = 0; x < 256; x++) \\ &\quad for(y = 0; y < 256; y++) \\ &\quad\quad z = {(x \times y)}/{128} - (x + y) + 255; \end{aligned} \tag{4.1}$$

Where x and y are the instantaneous and delayed inputs and z is the output of the EPROM.

4.4 Clock Distribution and I&Q Addition

This EPLD accepts a 21.12MHz reference clock. The reference clock is divided by 2 to ensure a 50% duty cycle. The 10.56MHz is now distributed to the ADC, delay EPLD, DAC, and is the reference used by the digital phase locked loop

The second EPLD implements a one-bit delay and the addition of a latched sample from the EPROM and the delayed sample, see figure 5.5. The output of the addition goes to a digital to analog converter and is low pass filtered before the decision stage.

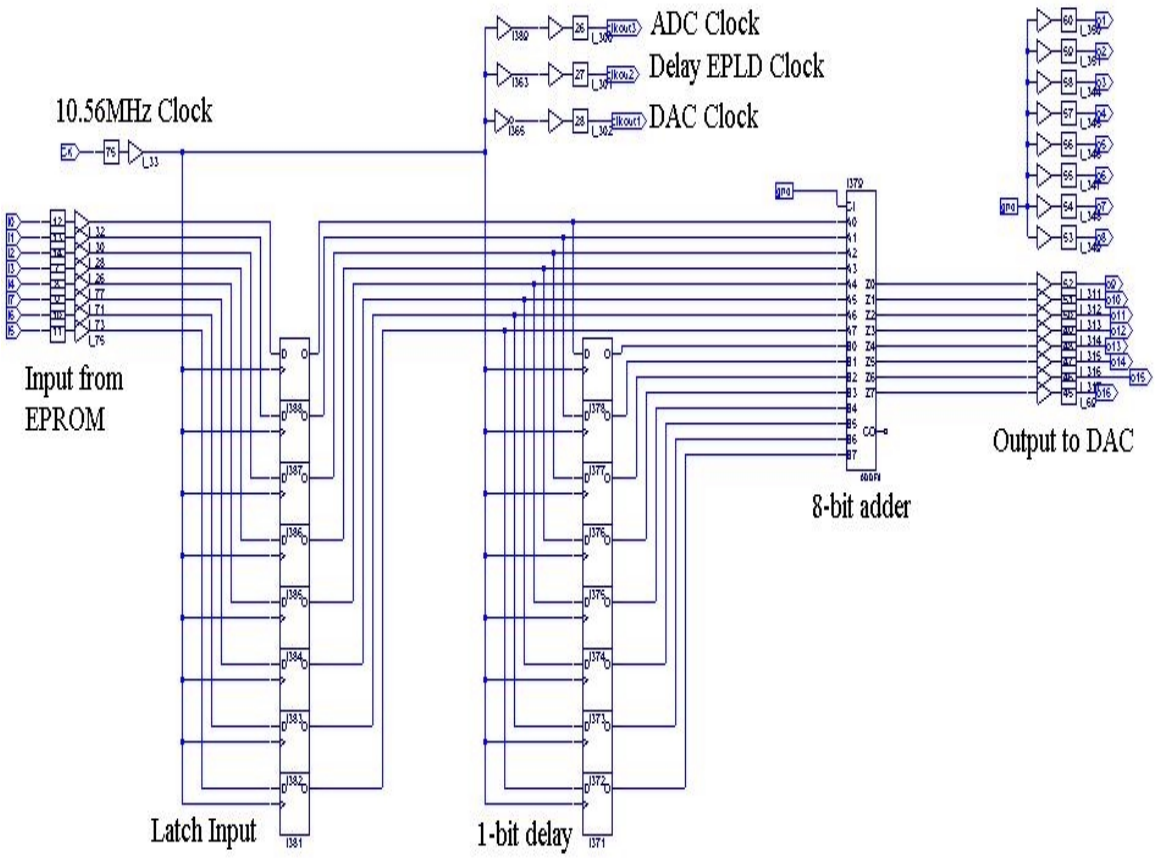
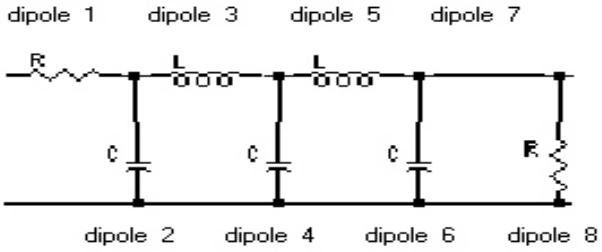


Figure 5.5. Clock Distribution and I&Q addition

This EPLD also performs the digital phase locked loop. This is discussed in detail in section 4.6

4.5 Low Pass Filtering of Received Data

The output of the DAC is low pass filtered with a 5th order of Bessel type, with a bandwidth of 462KHz. This bandwidth was determined from simulations for optimal Bit Error Rate (BER). The filter is designed with finite Q inductor values of 50. The software used to generate the filter is AADE Filter Design version 1.92.



DIPOLE 1
R=50.ohms

DIPOLE 2
C=1.201nF

DIPOLE 3
L=8.736uHy
Qu~50.

DIPOLE 4
C=5.539nF

DIPOLE 5
L=19.136uHy
Qu~50.

DIPOLE 6
C=15.559nF

DIPOLE 8
R=50.ohms

Figure 5.6. 5th Order Bessel Filter Design

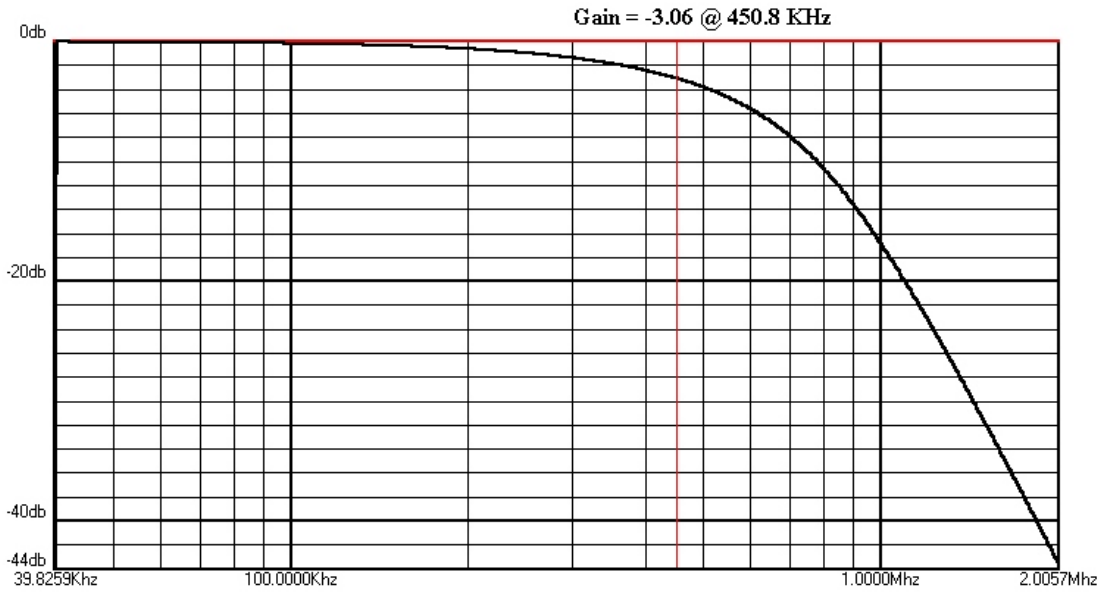


Figure 5.7. 5th Order Bessel Simulated Frequency Response

The output of the filter is converted to TTL voltage levels by a comparator with hysteresis. A small amount of hysteresis is included to prevent spurious responses due to noise. The hysteresis causes voltage dependant delay, which can be minimized with automatic gain control. This signal is now the input to the digital phase locked loop. The output of the filter also drives an AM peak detector, which determines the signal strength. This is then send back to the RF board for Automatic Gain Control (AGC).

4.6 Digital Phase Locked Loop

Several types of digital phase locked loops were investigated as part of this thesis, one design was presented at ISSPA conference [6]. The final design presented here is simpler and operates more reliably. A special phase detector is required, one that can lock onto random data.

The digital phase locked loop needs to be designed to operate in a low signal to noise ratios and a high timing jitter environment. The phase error for one sample offset from ideal is 22.5 degrees or 0.393 radians.

$$\sigma_e = 2\pi / N \tag{4.2}$$

where N is oversample rate and σe is the standard deviation of the timing jitter. The percentage error of the bit period is:

$$\sigma_e / T = 1 / N \tag{4.3}$$

where T is the bit period. For a standard deviation of 1 sample and an oversample rate of 16 the percentage error is 6.25%. From figure 2.7, this corresponds to a bit error rate performance degradation greater than 1 dB. This bit error rate degradation will increase at higher signal to noise ratios.

One way to improve the performance of the phase locked loop is to increase the oversample rate. The timing jitter is inversely proportional to the oversample rate. The current system uses 16 times oversample, this could be increased by using a higher density EPLD. This would improve the phase locked performance under all operating conditions.

The phase detector is of an edge detection type. If a rising or falling edge of the received data is detected an error counter is increment or decrement depending on the phase of the local reference clock. Once the error counter exceeds a threshold, the reference divide-by counter's modulus is changed. The output of the reference divide-by counter is the recovered clock phase synchronized to the received data.

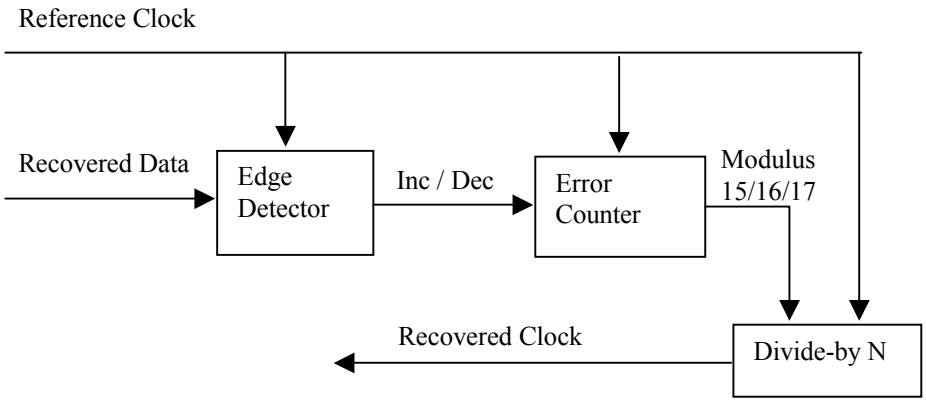


Figure 5.8. Block diagram of Digital Phase Locked Loop

The error counter sets the divide-by-N counter's modulus to either 15,16, or 17, depending on if there was an underflow or overflow of the error counter. The threshold of the error counter sets the bandwidth of the lock range of the phase locked loop, similar to equation 2.5.

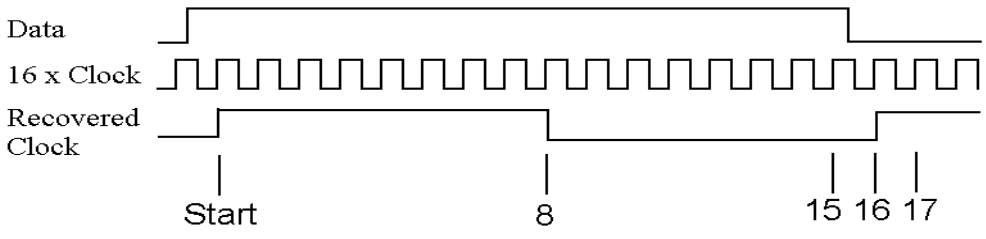


Figure 5.9. Digital Phase Locked Loop Operation

Figure 5.9 shows how the phase detector decides if there is a phase or frequency error. The detector only updates the error counter on two consecutive edges.

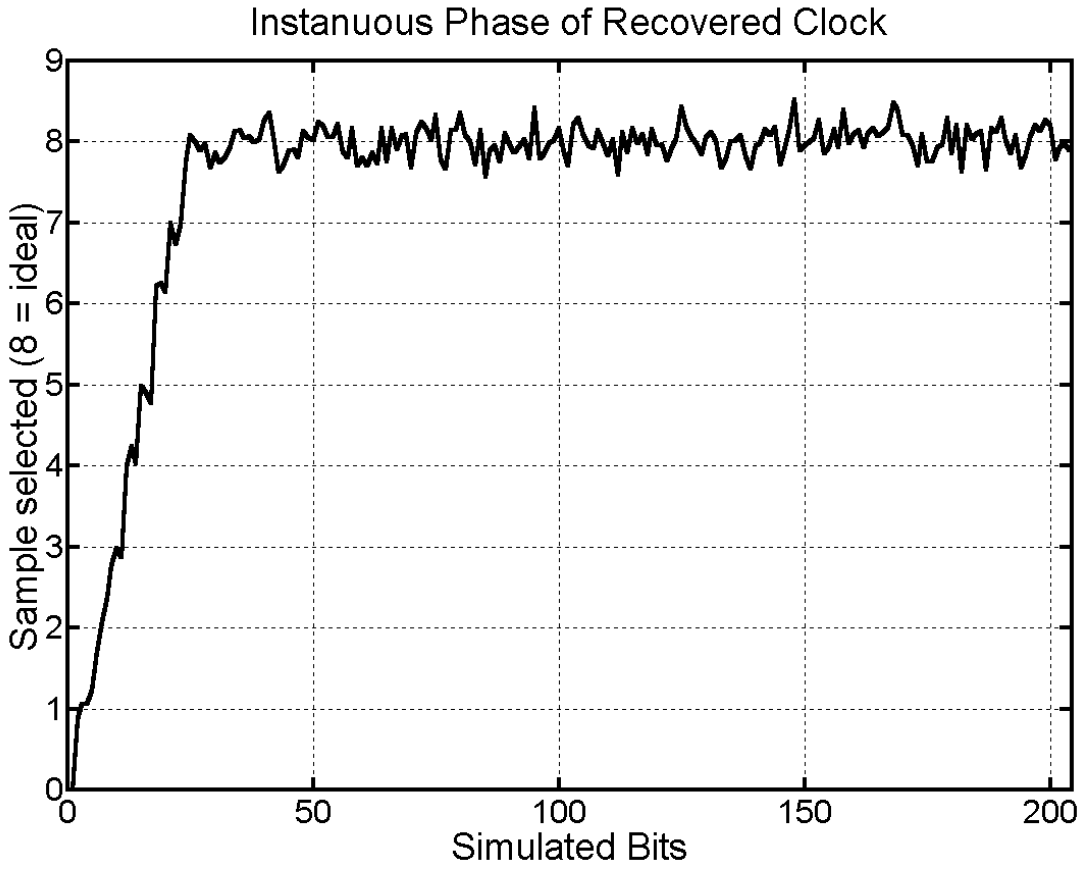


Figure 5.10. Digital Phase Locked Loop Step Response (SNR=6 dB)

Figure 5.10 shows the step response of the digital phase locked loop with noise (SNR=6 dB) added to the system. The detector starts 180 degrees out of lock, after approximately 30 data bit cycles, the recovered clock is phase locked to the incoming data.

Matlab 5.3 is used to check the effect of signal to noise ratio and frequency error on the timing jitter of the phase locked loop. Since the digital phase locked loop is an entirely digital design, the Matlab simulation should give an accurate performance indication. The Matlab 5.3 code is in appendix M for reference.

Figure 5.11 shows the timing jitter of the phase locked loop under a low signal to noise ratio (SNR=6 dB). There is also a reference clock frequency error of 3%. Figure 5.11 shows that most of the sample points lay within +/- 2 samples of ideal. Figure 5.12 shows a histogram of variation in sample points. The stand deviation for this set of data is 1.1547 samples, which corresponds to 25.9815 degrees. The standard deviation is also the RMS phase error for phase modulated systems. From [7] the table in appendix H, shows the corresponding signal to noise ratios for a given RMS phase error. For a RMS phase error of 25.98 degrees the effective signal to noise ratio is 6 dB. Appendix I, contains figures of the histogram and phase error for the digital phase locked loop at various signal to noise ratios.

Appendix A contains the design of the digital phase locked loop in an electrically programmable logic device (EPLD).

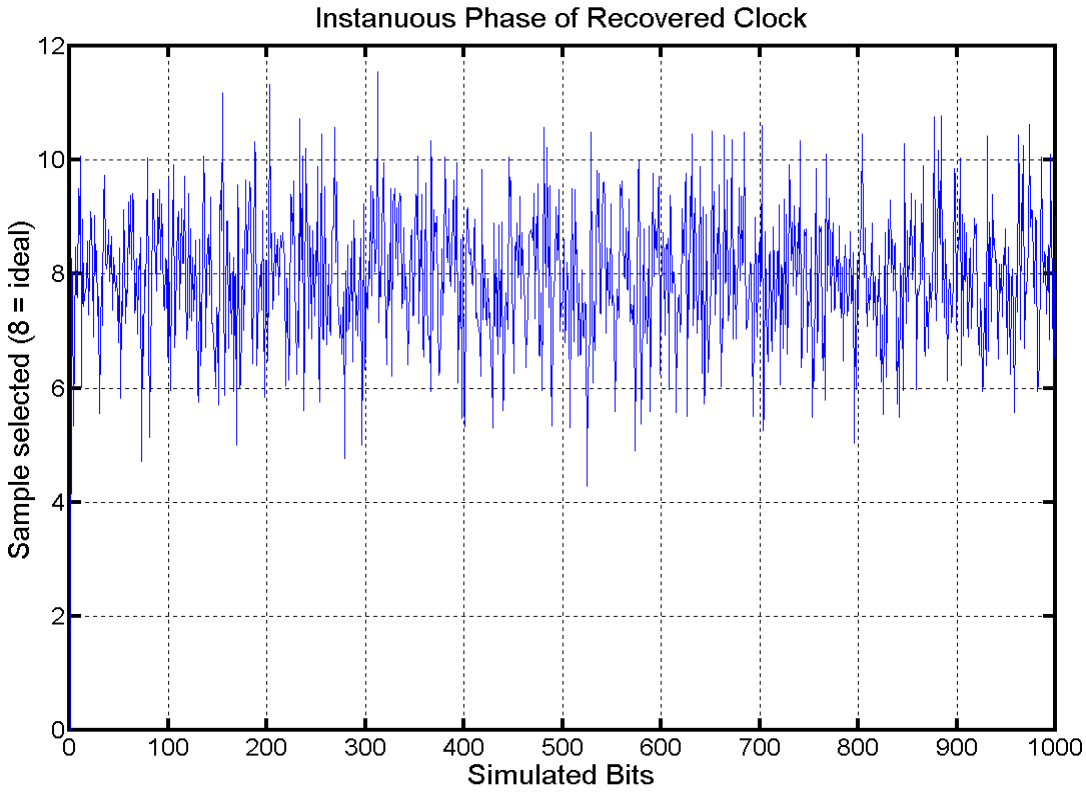


Figure 5.11. Sampling Instance of the Digital Phase Locked Loop

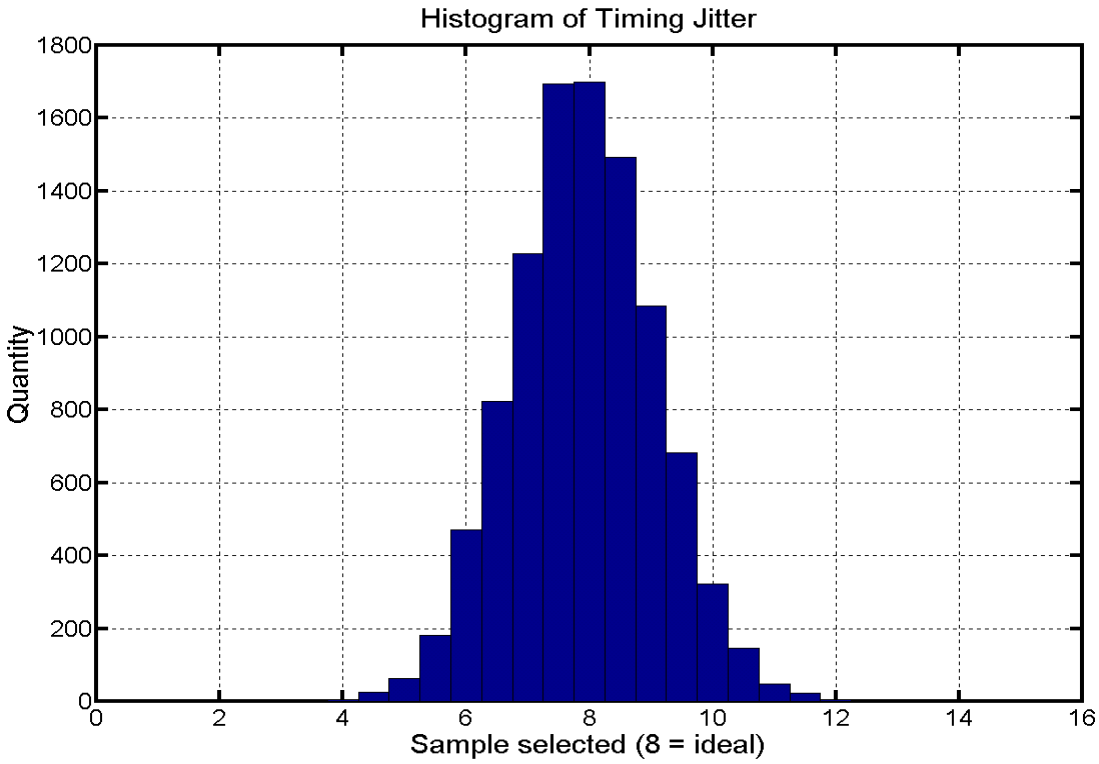


Figure 5.12. Histogram of the sampling instance

4.7 Frame Synchronization

The third EPLD accepts the 660KHz clock and data from the Digital PLL. Frame synchronization is achieved by detecting the SYNC code transmitted by the MTSAT (or GMS) satellite at the start of each frame. The SYNC code is 20,000 bits long and is derived from a 15-bit pseudo-random sequence generator. Fifteen consecutive ones in the serial shift registers of the pseudo-random sequence generator indicate the start of a frame. Piper [13] has performed a similar frame synchronization technique.

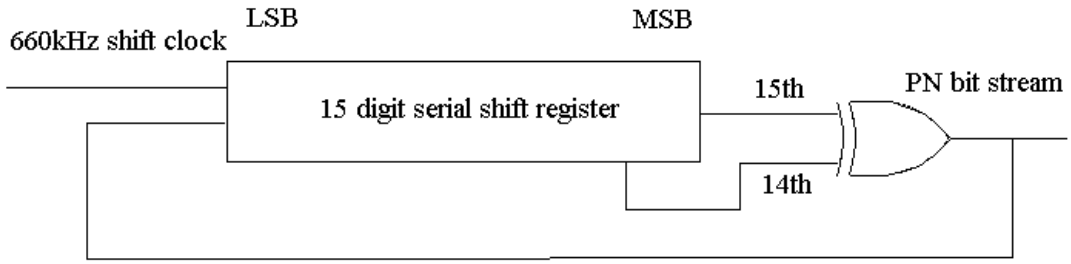


Figure 5.13. PN sequence generator

If the frame synchronization has not yet been achieved, received data is load directly into the PN sync serial shift register. The output of the PN generator's XOR gate is then compared to the incoming data. If the two are the same, the lock detection counter increments. If the data is different, the counter resets and starts counting again on the next successful comparison. The received Signal to Noise Ratio (SNR) is expected to be 8dB or greater. This gives an ideal Bit Error Rate (BER) of 1e-3 or 1 bit in error in every 1000 bits. If the SNR drops to 5dB the ideal BER is now 2e-2 or 1 bit error in every 50 bits. To make the frame synchronization reliable and robust to SNR ratio variations, the lock detection counter threshold should be small enough to still obtain lock under low SNR, and large enough to avoid false locks.

The next bit received after the header will be the start of the documentation section. If the frame synchronizer has obtained lock and detects all ones in the shift register,

the master frame counter will start. The first 20408 bits received are the documentation sector. This sector is always sent to the PC for processing. The IR (infra-red) and VIS (visible) sectors that are sent to the PC are jumper selectable. Received data being sent to the PC is converted into 8-bit parallel data then loaded into FIFOs to await transmission to the PC. Appendix B describes the operation of the frame synchronization EPLD.

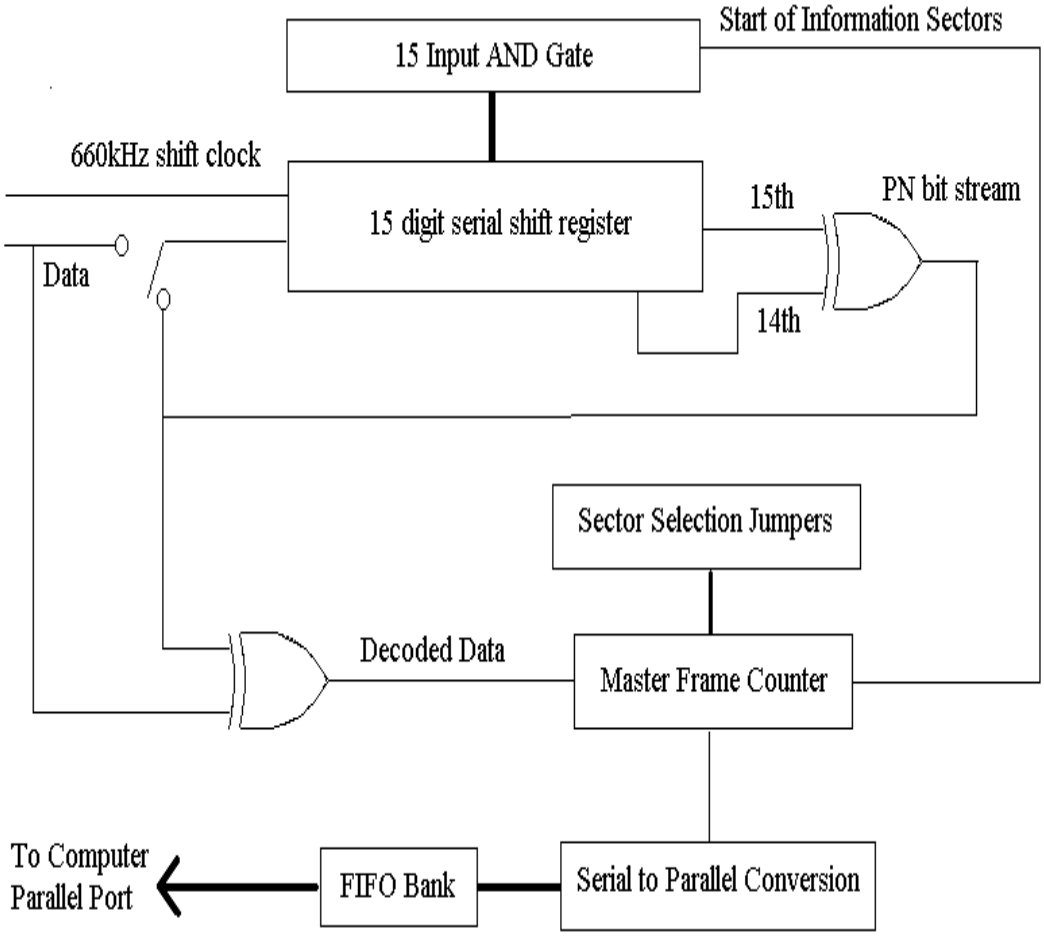


Figure 5.14. Frame Synchronization Block Diagram

4.8 Serial-Parallel Conversion and FIFO Control

The fourth and last 1032E EPLD contains the serial to parallel conversion, FIFO read and write control and the parallel port handshaking. Serial data from the previous EPLD is latched into an 8-bit serial shift register. Data is latched on the same clock as the frame synchronization hardware. When all eight shift registers are loaded, a 82.5 kHz, 660kHz divided-by 8, clock will latch the contents of the shift register onto the input bus of the FIFO. Before being latched, the data is byte-complemented with eight exclusive or gates.

When data is placed on the FIFO input data bus, a FIFO read control signal is generated. This continues until the end of the frame. When the frame synchronization EPLD obtains locks to the frame sync of the new frame, a FIFO reset pulse is generated and the PC is informed of the new frame start. This is to ensure the PC software always remains frame synchronized with the EPLD receiver hardware. Appendix C describes the operation of this EPLD in more detail.

4.9 EPP Parallel Port Handshaking

The parallel port handshaking protocol used for transmission from the FIFO to the PC is Enhanced Parallel Port (EPP). The EPP protocol is fast enough for the data transfer of SVISSR, HiRID, LRIT and HRIT and avoids system architecture dependence if the PC standards change, such as ISA bus being obsolete. This also allows the logger to be run from a Linux PC, Windows PC or MAC. Appendix D describes the operation of the EEP mode and the timing and software requirements.

4.9.1 Receiving Software

To verify the operation of the receiving hardware a data logger has been written for the Linux operating system. The receiving program first sets the parallel port to EPP Mode by writing 0x80h to the ECR. The control register is set for bi-directional data by writing 0x24h. This is all that is required to set up the parallel port in EPP mode. All that is required is to receive data from the EPLD demodulator board is to read from the EPP Data Port. If the demodulator does not respond within 10us by pulling the WAIT line high, the time-out bit in the Status Register of the EPP port will be set. To avoid EPP hang-up, control is sent back to the software, where another read can be made. To check if valid data has been read and not a time-out, the status register's time-out bit must be checked. If EPP timed-out then another read is sent, this continues until valid data is received. The demodulator writes data to the FIFO at a speed of:

$$\frac{8}{660kHz} = 12.12us \tag{4.5}$$

This is slower than the time-out period of EPP. Therefore care must be taken as the time-out bit will be continuously set after each read from the FIFO.

The start of a new frame is detected be reading pin 12 (spare pin in EPP). The demodulator board pulls this line low at the start of each frame. The line is then pulled high at the end. The high time is approximately 30ms. This is sufficient time for the software to detect the start of a new frame. Data received is written directly to a text file. Post processing software is required to extract the documentation and the image sectors.

Chapter 6 EPLD Receiver Schematic Design

5.1 Analog Input Schematic

The complete demodulator, digital phase locked loop, frame synchronization, FIFO and parallel port systems need to be integrated onto a single PCB. The Schematic and PCB design was done with Protel 99.

The analog input is first coupled through a 4:1 RF transformer from Minicircuits. The RF transformer offers some impedance matching to reduce the required input signal power level, and helps to lower distortion. The RF transformer, model ADT4-6WT, offers a 4:1 impedance transformation for a frequency range of 2-300 MHz with a 1 dB insertion loss. The AD9050 is a 10-bit analog to digital converter that has a maximum sampling frequency of 40 MSPS and an analog bandwidth of 100 MHz. The input voltage range is 1.024 Vpp with an input resistance of 5 KΩ.

$$\begin{aligned} P_{IN(MAX)} &= 10\log_{10}\left(V_{RMS}^{\,2}/R\right) + 30\ dBm \\ P_{IN(MAX)} &= 10\log_{10}\left(0.362^2/5000\right) + 30\ dBm \\ P_{IN(MAX)} &= -15.8\ dBm \end{aligned} \tag{5.1}$$

If the analog input is matched to 5 KΩ, the maximum input power required for full scale is -15.8 dBm.

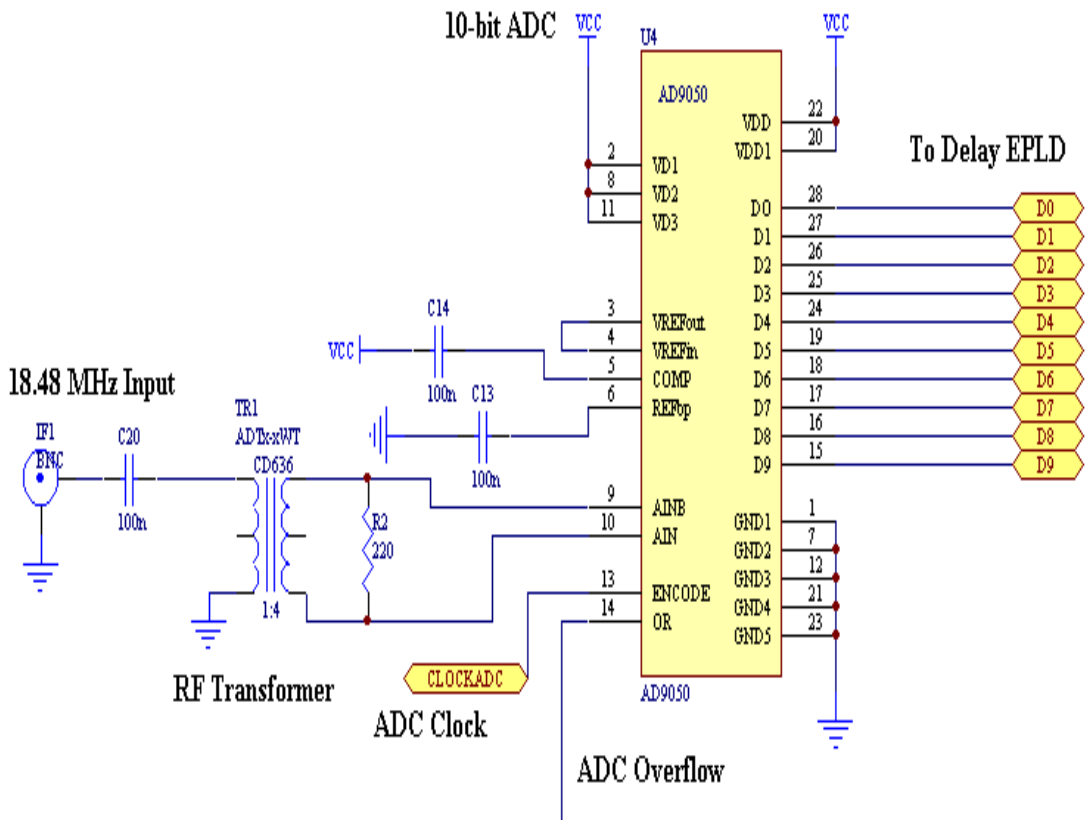


Figure 6.1. ADC Schematic

The RF transformer matches the 50Ω input to 200Ω. Therefore the required increase in input power for full scale is:

$$
\begin{aligned}
&P_{IN(Matched)} = xP_{IN(Unmatched)} \;\; dB \\
&x = 10\log_{10}\left(200/5000\right) \; dB \\
&x = -13.98 \;\; dB \\
&\therefore P_{IN(Unmatched)} = -1.82 \;\; dBm
\end{aligned}
\tag{5.2}
$$

Therefore for full-scale input, the maximum input power, adding 1 dB for transformer insertion loss, is –0.82 dBm. The 10.56 MHz ADC clock is distributed from the I+Q Addition and DPLL EPLD. The reference 21.12 MHz clock is divided-by two to ensure a 50% duty cycle.

5.2 Delay EPLD Schematic

The Delay EPLD is a lattice 1032E Electrically Programmable Logic Device. The Lattice EPLD architecture is described in Appendix E. The 1032E is a 84 pin PLCC package with 192 registers and 32 Global Logic Blocks (GLB) and a maximum operating frequency of 100 MHz. The array of 16 x 8 D Flip-flops uses 128 registers, but uses all of the GLBs. One of the EPROM multiplier inputs comes from data passed straight through the EPLD. The other one is delayed by sixteen 10.56 MHz clock cycles. The Lattice compiler offers an integrated timing analysis of the design. The expected delay for the eight pass through data pins is 16.3ns. The maximum delay through any of the register is 17.8ns, this limits the maximum operating frequency to 56MHz. Care must be taken that the EPROM has sufficient set-up time before the multiplied output is latched into the I+Q Addition EPLD. The delay EPLD runs from a 10.56MHz clock, which offers a 16 times oversampling. The design of the delay EPLD falls well with the specification of the Lattice EPLD being used.

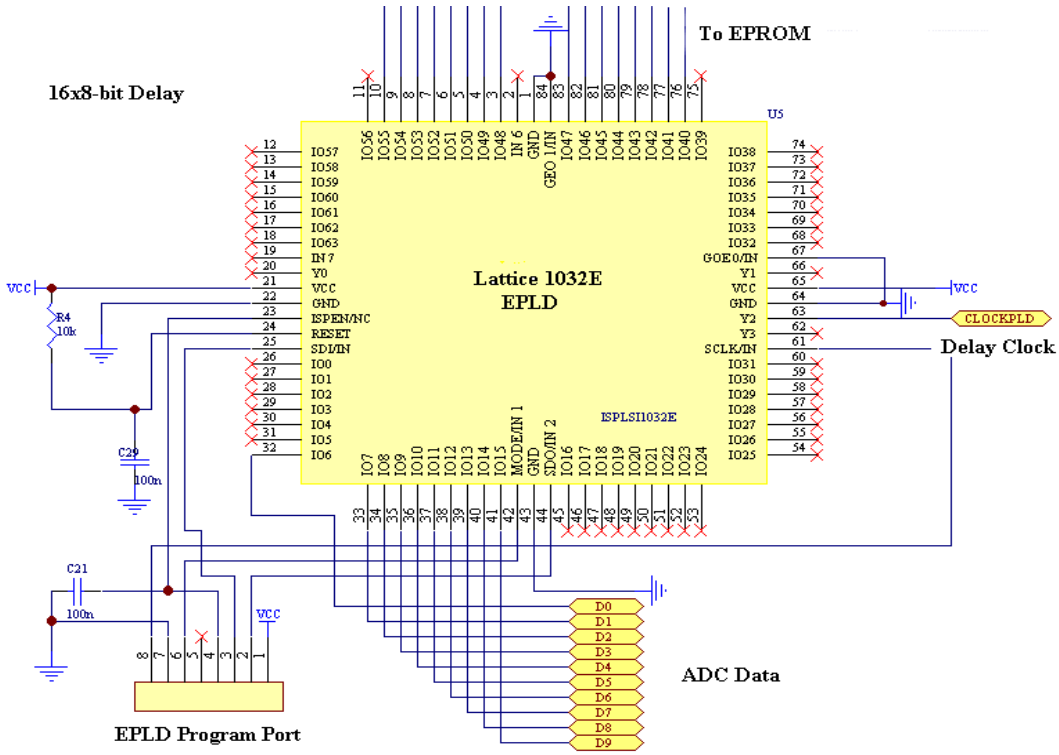


Figure 6.2. Delay Schematic

5.3 EPROM Multiplier

The multiplier in this design is required to operate at 10.56 million multiplications per second. An EPROM can perform this task cheaper and simpler than a DSP as eight bits resolution is sufficient. The EPROM is manufactured by Advanced Micro Devices (AMD). The AM27C512 is a 512 kbit Erasable Programmable Read Only Memory (EPROM) device in a 28-pin DIP package. The EPROM is organized into 64kbits x 8 bits. The 16 input pins allow an address range of 2^16 = 64kbits. 8 bits are stored at each address space, giving the 512kbits total EPROM memory size. The EPROM being used has an access time of 70ns. This limits the maximum frequency to 14MHz. The EPROM is thus running at 75% of maximum operating frequency.

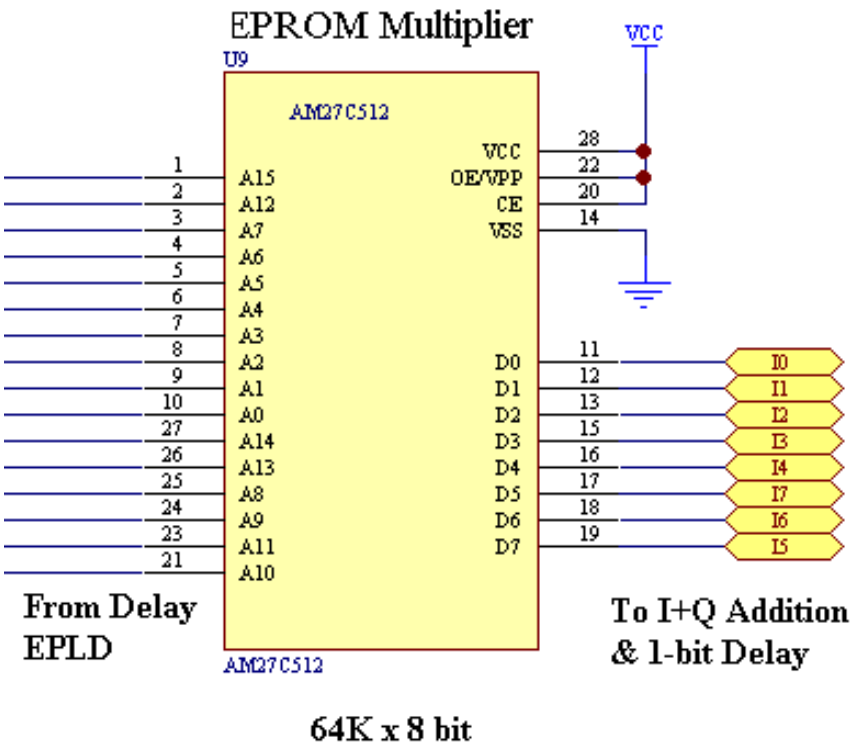


Figure 6.3. EPROM multiplier schematic

5.4 I+Q Adder and Digital PLL EPLD Schematic

The adder and digital PLL EPLD is a 1032E in a 84-pin PLCC package. The maximum operating frequency is 100Mhz. Data from the EPROM is latched on the rising edge of the 10.56MHz reference clock. The 21.12Mhz input clock is divided-by 2 to produce the 10.56 MHz reference clock with a 50% duty cycle.

From the Lattice compiler and timing analysis, this design uses 71 of the 192 registers and 21 of the 32 GLBs. The routing efficiency is 56%. The maximum delay through any of the delay registers is 12.7ns. Therefore the maximum operating frequency of the delay and the addition is 78 MHz. The digital phase locked loop is more complicated and is limited by the clock N counter. The maximum register delay is 20.4ns, making 49 MHz the maximum frequency that the phase locked loop can operate at. The design for this EPLD is running at 43% of maximum frequency. Blackburn and Kikkert [4] have shown that this design can be extended to demodulate Quadrature Phase Shift Keyed (QPSK). There is sufficient room in this EPLD to accommodate the additional adder circuitry.

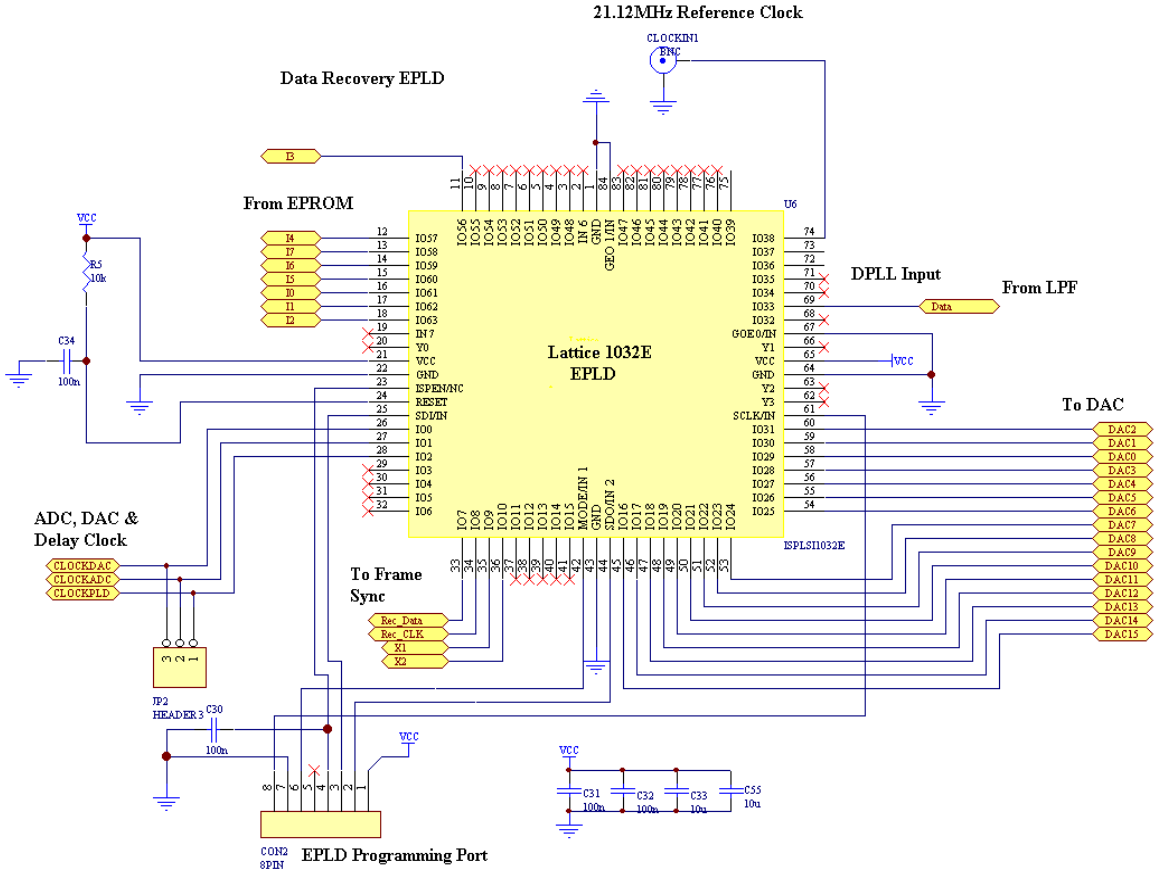


Figure 6.4. I+Q Addition and Digital PLL EPLD Schematic

5.5 DAC Schematic

The output of the I&Q addition is converted back to a continuous analog waveform with a 16-bit Digital to Analog Converter (DAC). The DAC being used is an Analog Devices part, model AD768. The AD768 has a maximum sampling frequency of 30 MSPS. The DAC clock is also the 10.56MHz reference clock derived from the 21.12MHz source. The output data will be at baseband and differentially decoded satellite data. The DAC output is a current sink. The maximum current drawn through the 50Ω output resister is set to 20mA. This produces a voltage with an output swing from 0 to –1 volts.

The DAC is then AC coupled into a high-speed Operational Amplifier (Op-Amp). The satellite data will not have a DC component as the signal is still encoded with the pseudo random noise sequence and byte complementing. This simplifies the comparator design as there will be no DC offset. The Op-Amp provides sufficient amplification such that the attenuation from the Low Pass Filter (LPF) does not effect the performance of the comparator.

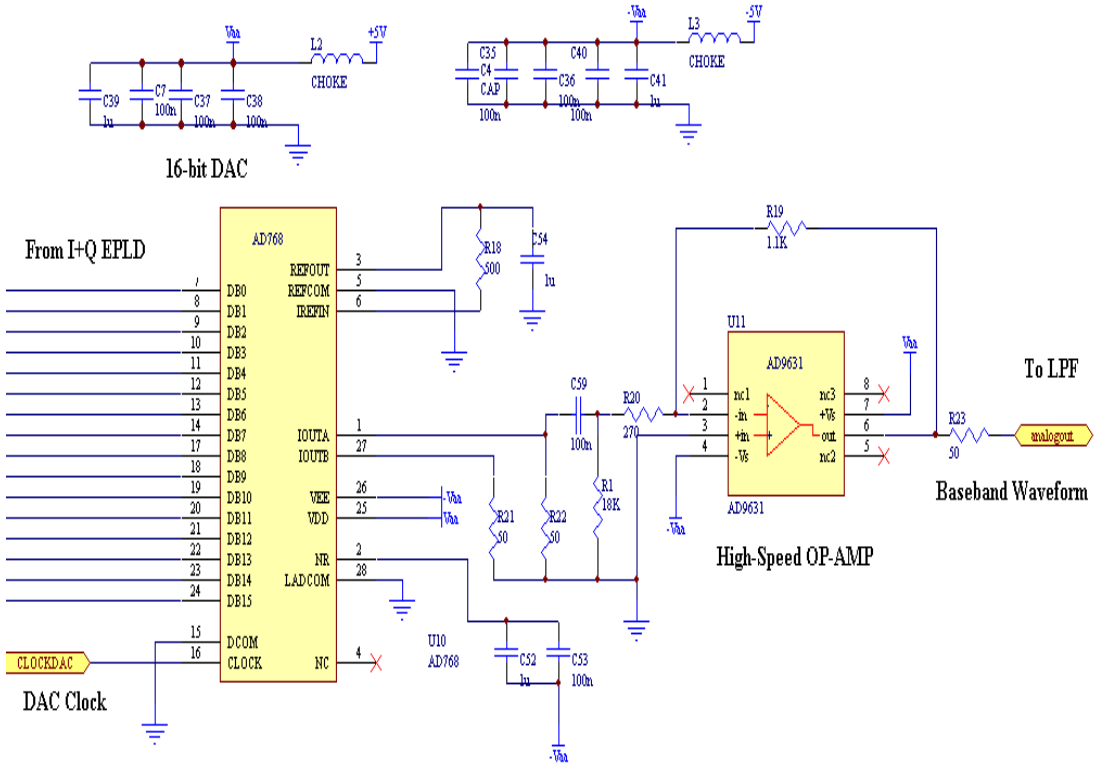


Figure 6.5. DAC Schematic

5.6 Low Pass Filter Schematic

The Low Pass Filter (LPF) design has been designed from simulations to give the optimal bit error rate performance. The filter is a 5th order Bessel design with a 50Ω source and load impedance. The large inductors are constructed from core formers with a variable ferrite core. The formers are from NEOSID, part number 60-731-64. This filter was designed in section 4.5.

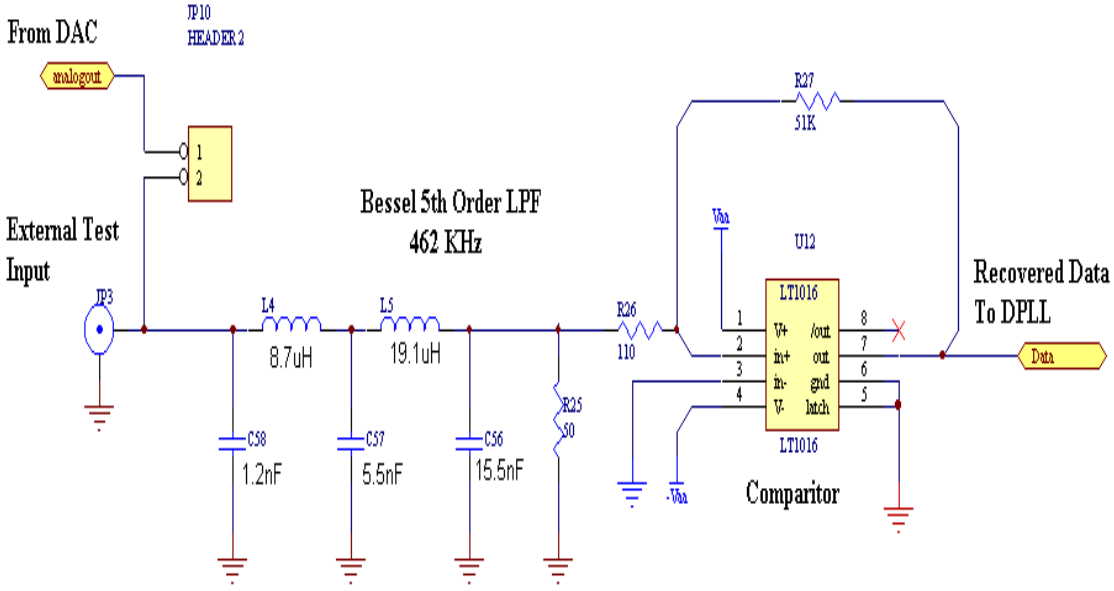


Figure 6.6. Low Pass Filter Schematic

5.7 Frame Synchronization Schematic

All the frame synchronization required is performed in one Lattice 1032E EPLD. It is a 84-pin PLCC package, with as speed rating of 100 MHz. The frame sync EPLD has two inputs from the digital phase locked loop, the data and clock signals. With the falling edge of the clock synchronized with a data transition. The sector selector header is a jumper that allows the users to select which of the IR and VIS sectors are transmitted to the PC for processing. Most of the EPLD register utilization is in the main frame counter. This is a 19-bit counter that is compared with the jumpers to select which of the frame sectors are transmitted to the PC.

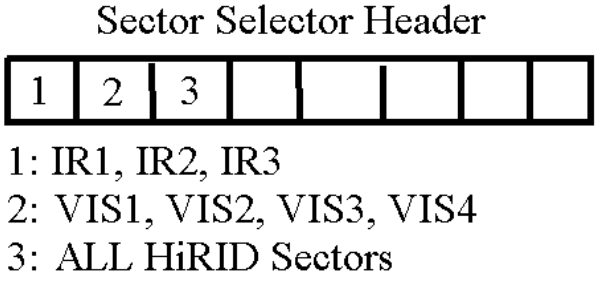


Figure 6.7. Sector Selector Header

This design uses 91 of the 128 Macrocells and 28 of the 32 GLBs. The routing efficiency is 82%. The maximum delay through any register is 26.9ns. This limits the maximum operating frequency to 37 MHz. The limitation is due to the propagation delay of the main frame counter. The frame synchronization operates at the bit-rate, so the operating frequency is less than 2% of the maximum frequency.

The serial data from the frame synchronization has been PN decoded. The serial data, various clocks and frame start and stop signals are passed to the FIFO and Parallel port control EPLD for further processing.

A Frame Lock Detect output line is supplied to drive a LED. This provides a visual indication the demodulator and frame synchronization is working. The locked detect is also available on the parallel port and is used by the Linux PC logger software.

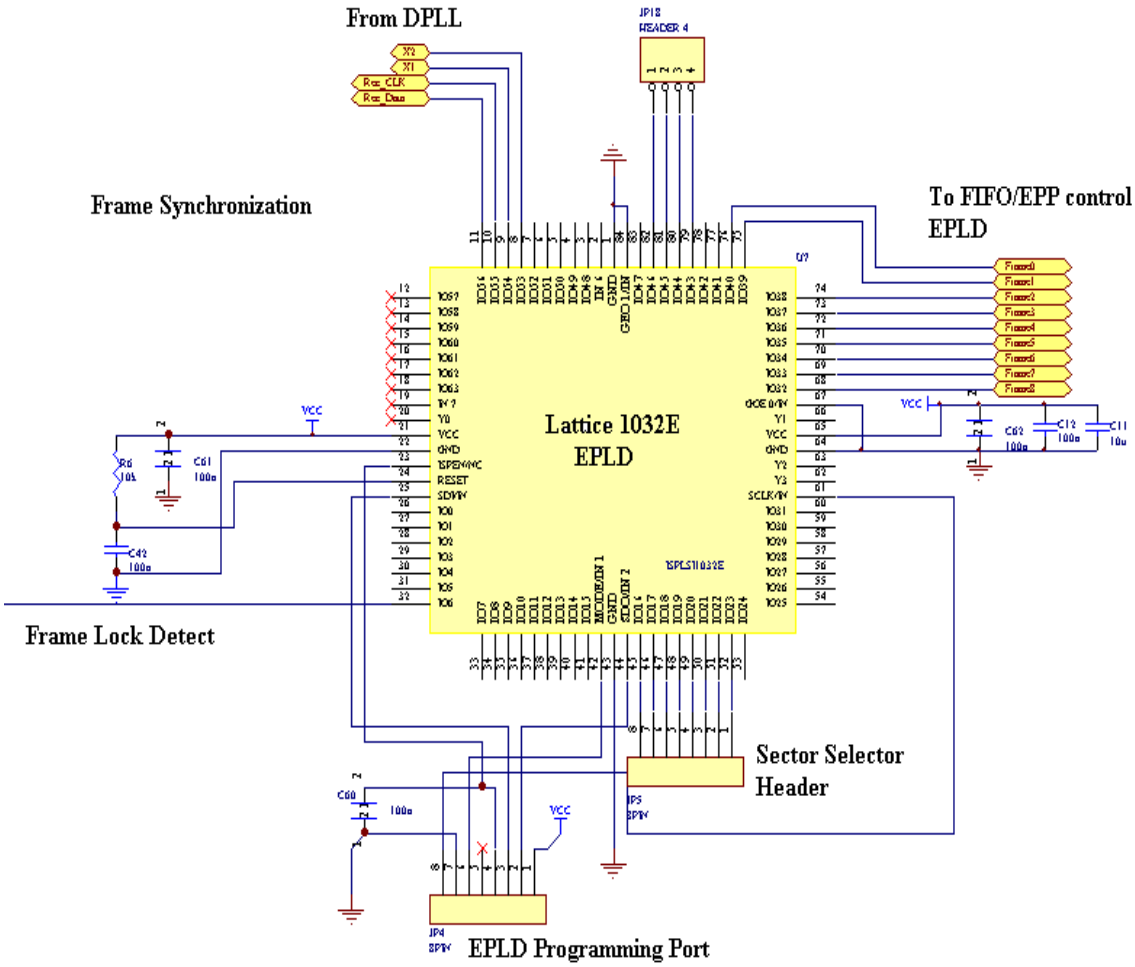


Figure 6.8. Frame Synchronization Schematic

5.8 FIFO and Parallel Port Data and Control

This device is also a Lattice Semiconductor's 1032E EPLD in a 84-pin PLCC package with a speed rating of 100 MHz. The data from the frame synchronization EPLD is converted into parallel data and byte complementing is performed before loading the data into the FIFOs. The parallel port protocol EPP is emulated to provide fast throughput to the PC.

The design uses 33 of the 128 registers and 9 of the 32 GLBs. This EPLD is under utilized, but was chosen for its price, density and speed performance. The routing efficiency is 92%. The clock of the serial to parallel shift register limits the

maximum delay. The maximum delay is 12.6ns, which limits the maximum operating frequency to 79 MHz. The shift registers operate at the bit-rate, which is 660 kbits/s. This is also less than 1% of the maximum frequency capability from the EPLD device.

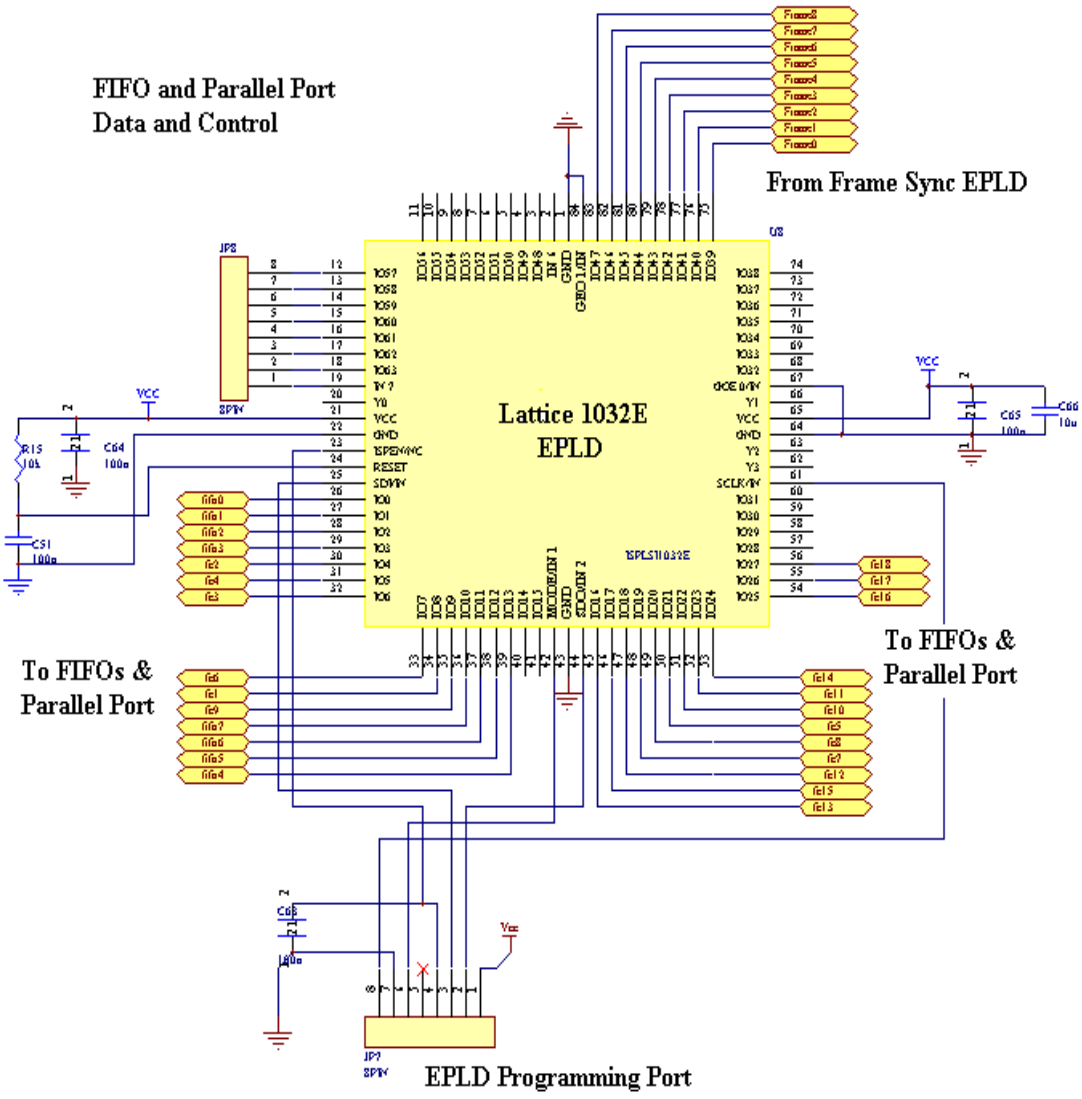


Figure 6.9. FIFO and Parallel Port Data and Control

The spare capacity of this EPLD can be used in the future to change the output interface from parallel port to USB or Firewire, if the need arises.

5.9 FIFOs and Parallel Port Header Schematic

The data has been converted to parallel and been byte complemented before being placed on the FIFO data input pins. The rate at which data is clocked onto the FIFO input pins is one eight the bit-rate, 82.5 Kbytes/s or every 12.12µs. The array of four FIFOs are set up in depth expansion mode. This increases the total FIFO depth to four times the individual FIFO depth. The FIFOs chosen are from Integrated Device Technology (IDT). The part number is IDT7204 with an access time of 65ns. The memory organization is 2 kbits deep x 9 bits wide. This device is pin compatible with larger density FIFO. This FIFO series supports densities up to 64 kbits deep. The rate at which data is written to the FIFO is of an order of magnitude slower than the access speed of the FIFOs, there are thus no problems with access times.

The parallel port header connects to a 25-pin D-connector compatible with standard parallel port cables available for the PC.

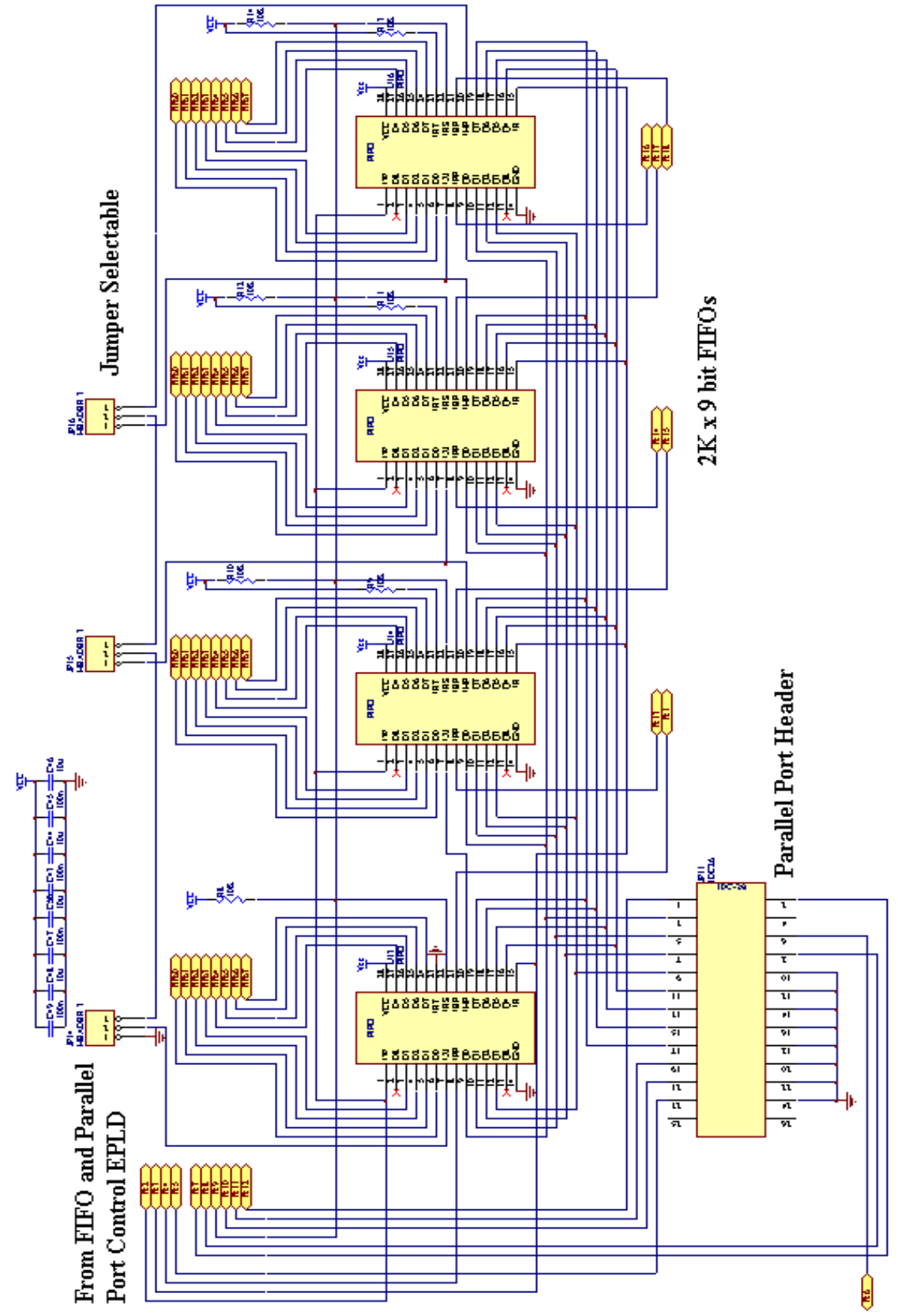


Figure 6.10. FIFOs and Parallel Port Header Schematic

5.10 AGC Control

AGC is required to keep the received signal power within a certain range. The range is determined from testing for optimal bit error rate in section 6.7. This AGC design is a simple AM peak detector and low pass filter. The DC voltage of the demodulated signal is passed to the RF board for gain control. Figure 6.11 shows the schematic of the AM peak detector and low pass filter.

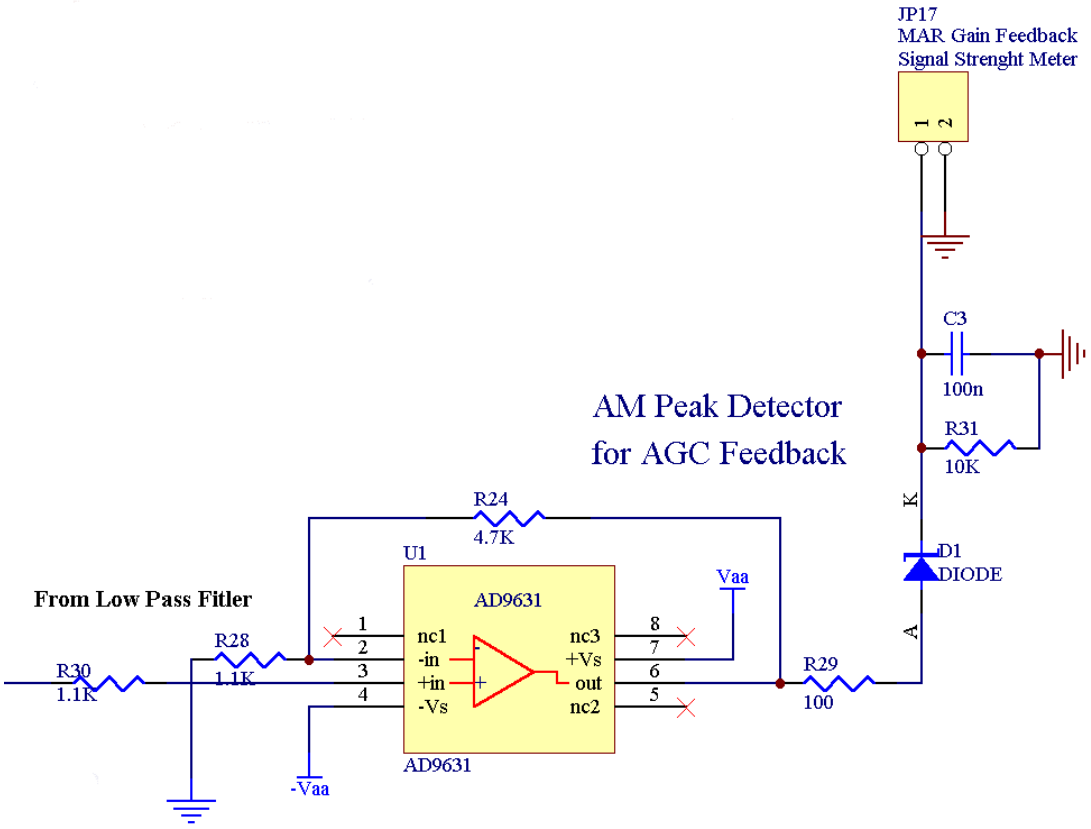


Figure 6.11. Schematic of the AGC Peak Detector and Low Pass Filter

The voltage at the output of the low pass filter needs to be measured for different input power levels. Figure 6.12 shows this relationship. When the input power level reaches 0 dB the voltage starts to flatten off. This represents the maximum input power of the ADC, past this point clipping will occur. A square relationship of input power to voltage exists up to the ADC power limit.

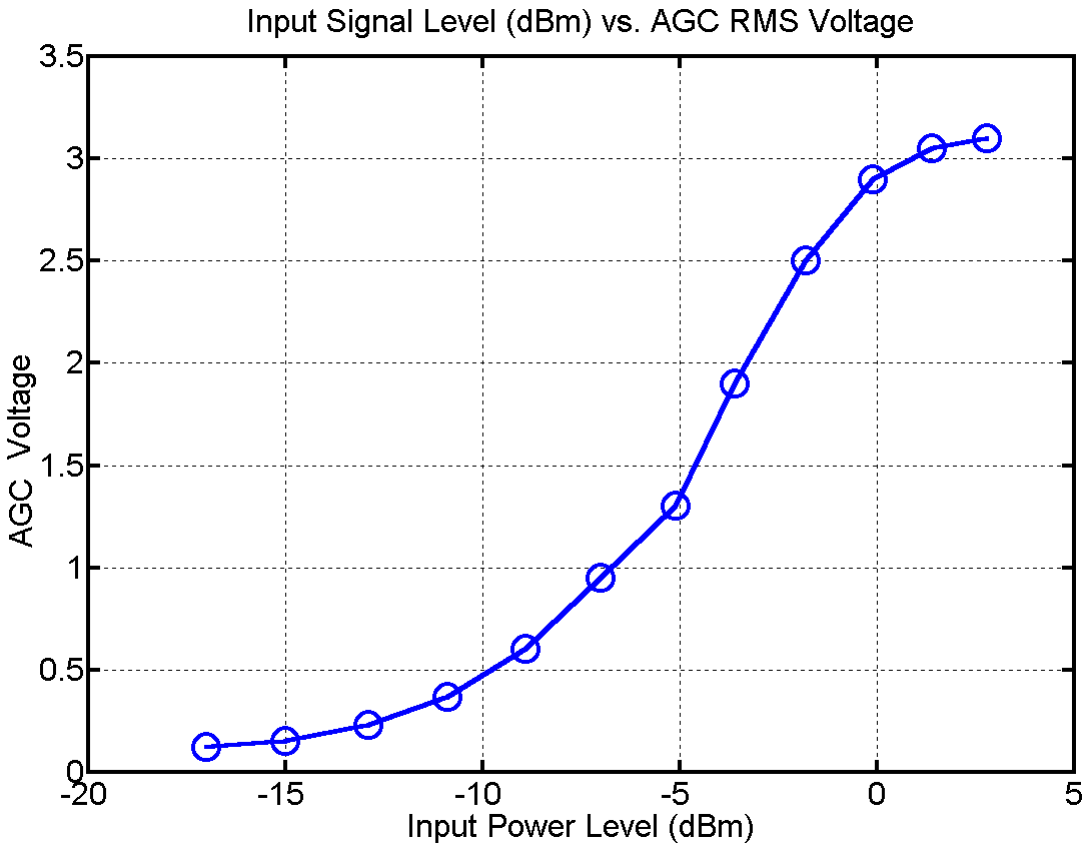


Figure 6.12. Input Power Level vs. AGC Control Voltage

5.11 Receiver PCB

Figure 6.13 shows the top overlay of the EPLD receiver PCB. This figure clearly marks the ADC, EPLDs, DAC, Low pass filter and FIFOs used in the receiver design. Figure 6.14 is photo of the completed EPLD receiver board.

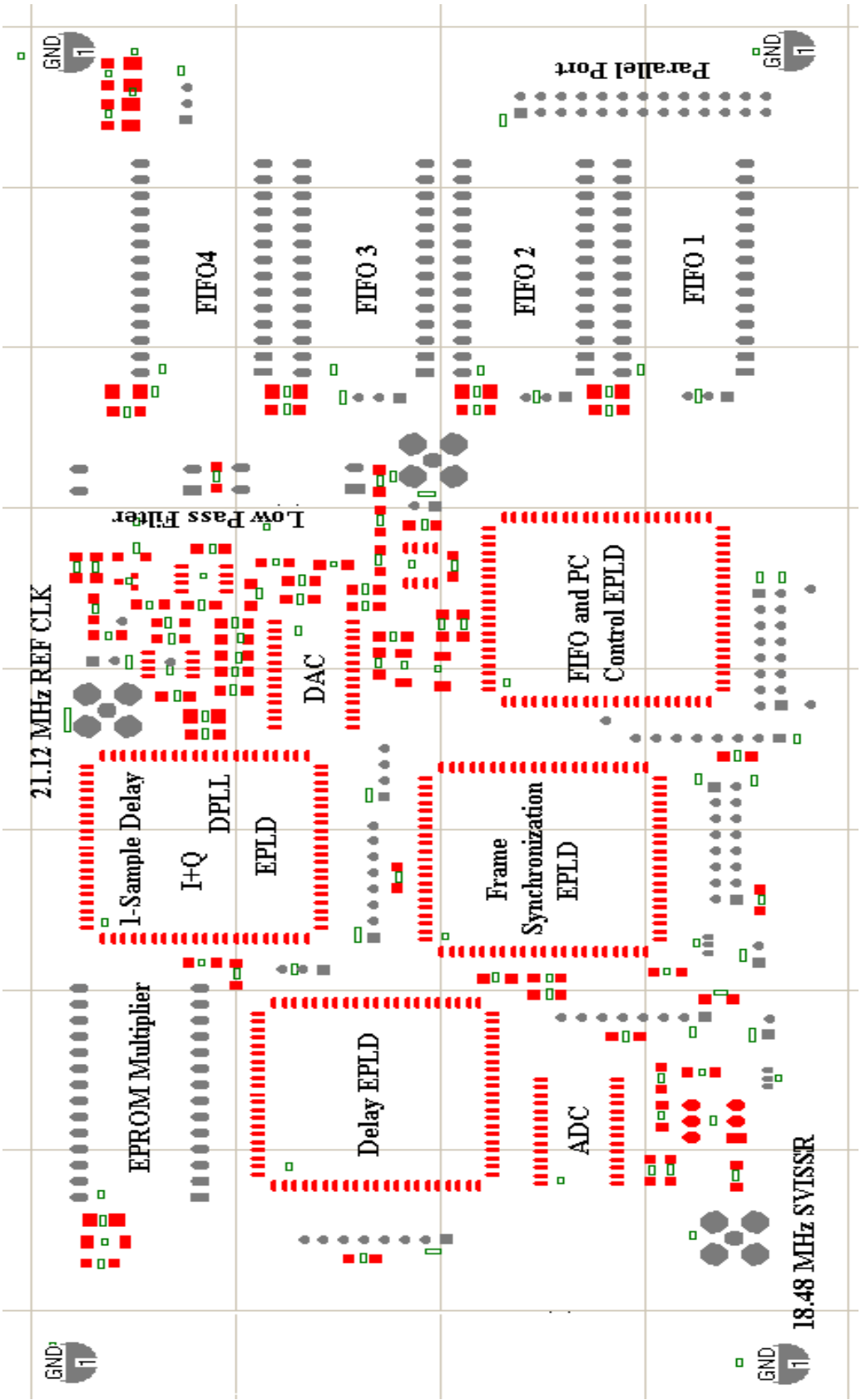


Figure 6.13. PCB Overlay of Important Components

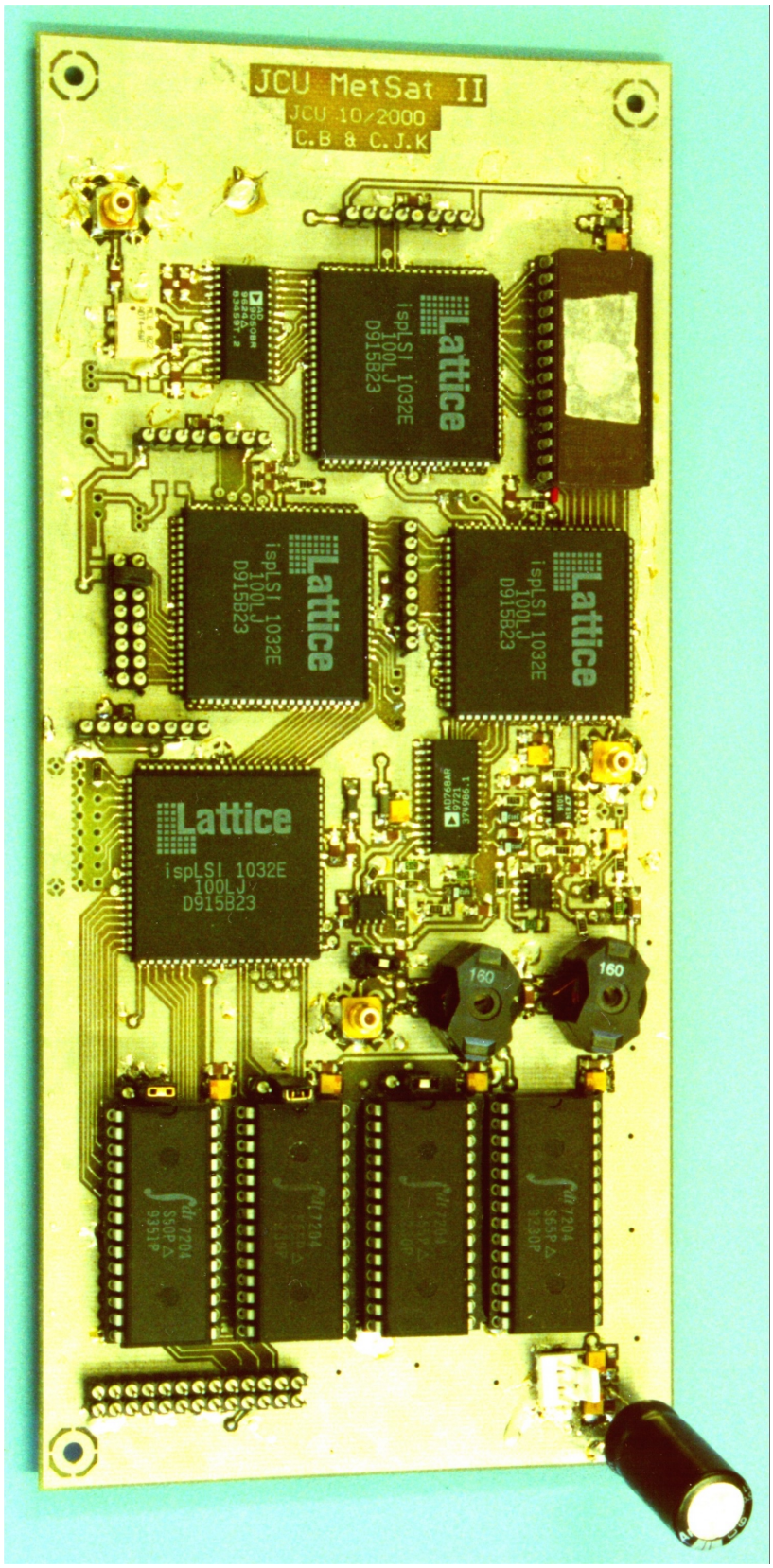


Figure 6.14. Picture of the EPLD receiver board

Chapter 7 EPLD Receiver Testing

6.1 Generating Test Data

A Lattice 1032E EPLD is used to generate a test sequence, which has the same properties as the GMS and MTSAT generated signals. Each generated frame starts with the same 20,000 bits of pseudo random sequence.

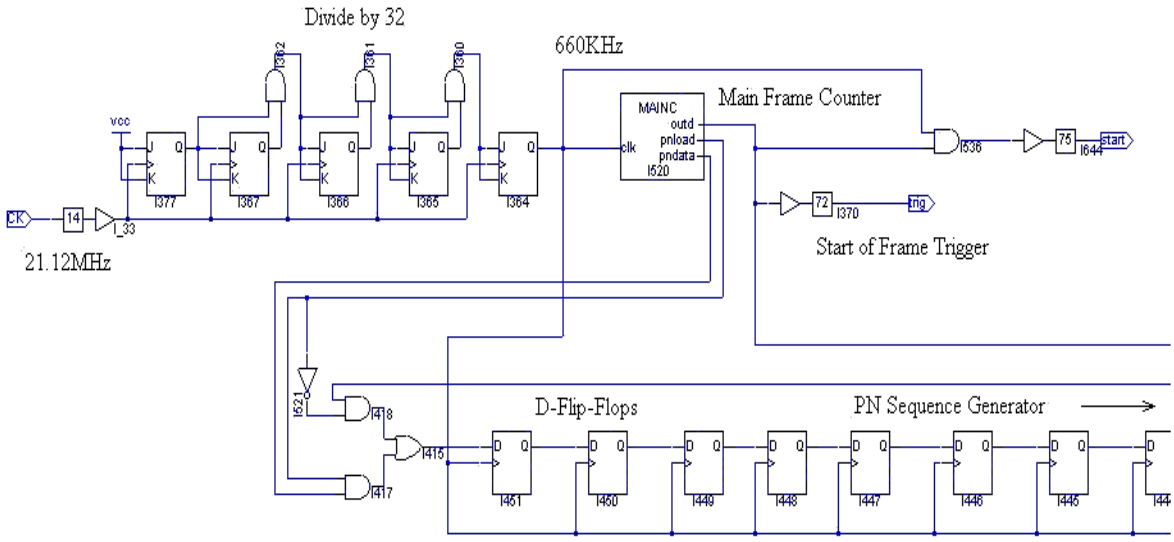


Figure 7.1. PN sequence generator

The EPLD demodulator board also uses a reference clock of 21.12MHz to avoid frequency errors. The reference clock is divided by 32 to produce the 660KHz clock used to generate the frame data. The frame count symbol contains the code to load the D-Flip-flops with the correct starting sequence so after 20,000 bits the header finishes with the correct sequence. The XOR feedback is disabled until all the start bits are loaded. Once all bits are loaded the feedback is connected and the GMS and MTSAT header sequence is generated.

```
"This module at the start of a frame loads the pseudo random sequence
"generator with the correct start bits.  Frame length is 2^19 = 524,288
" or 794ms.

MODULE mainc
        clk pin;
        [a0..a18] node istype 'reg';
        pnload pin;
        pndata pin;
        outd pin;
count = [a18..a0];  "19 bit frame counter

equations
        count := count.FB+1;  "Frame counter
        when (count<15) then            "Start of frame - disable xor feedback
                {pnload = 1;}
        else
                {pnload = 0;}
        when ((count==1)#(count==5)#(count==8)#(count==9)#(count==14))
then
                {pndata = 1;}
        else                            "load pn generator with start sequence
                {pndata = 0;}
        when (count>20014) then                 "end of header
                {outd = 1;}             "start encoding data with sequence
        else
                {outd = 0;}
        count.clk = clk;
END
```

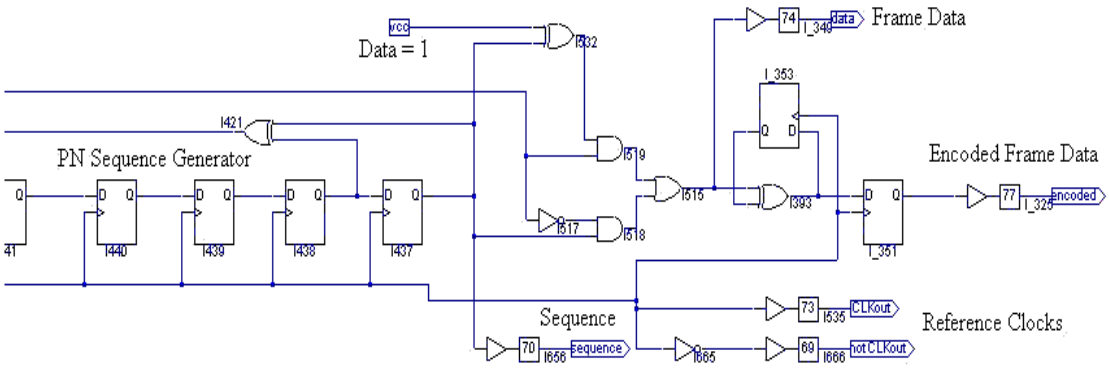


Figure 7.2. PN Sequence generator

Figure 7.3, is a photo of the SVISSR and HiRID frame generator board. Figure 7.4, is a capture of the start of a frame showing the pseudo random sequence and the differentially encoded data.

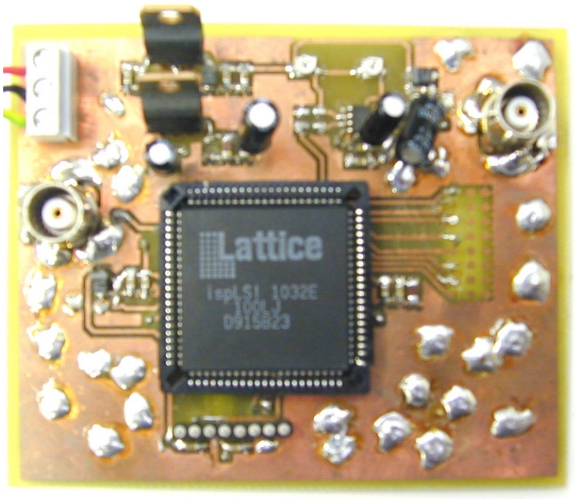


Figure 7.3. Photo Frame Generator Board

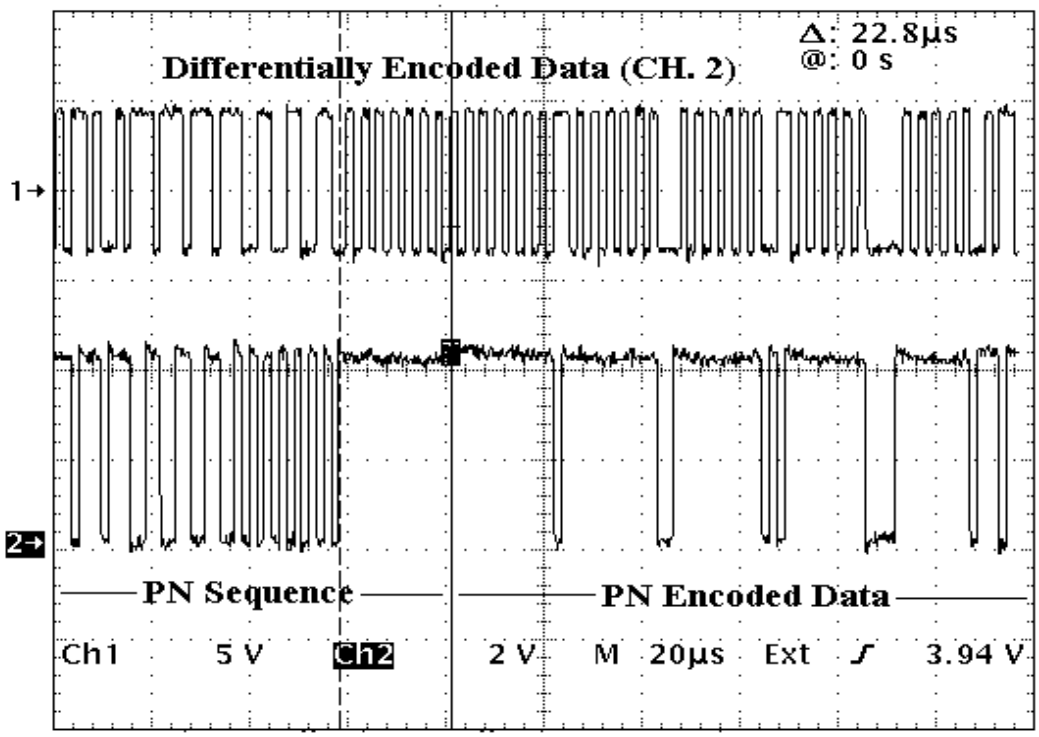


Figure 7.4. GMS and MTSAT generated frame

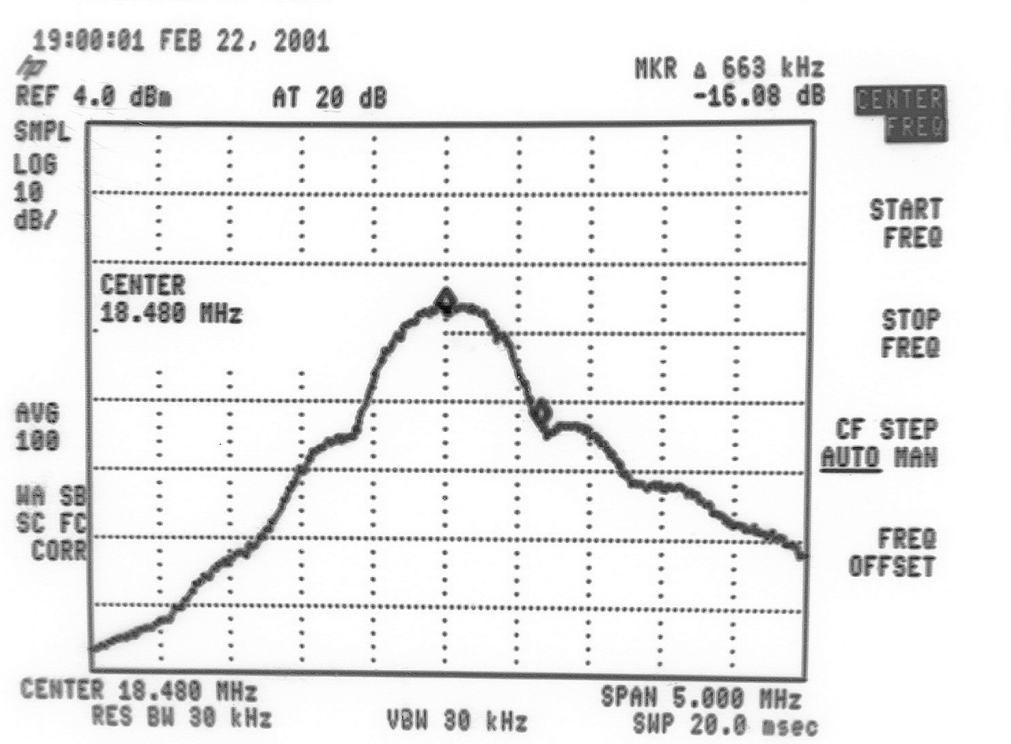


Figure 7.5. Generated GMS Spectrum at 18.48 MHz with a SNR of 10.6 dB.

Figure 7.5 shows the spectrum of the generated GMS signal using the test setup procedure described in 6.2. This spectrum is very similar to the received satellite signal.

6.2 Test Setup

A 18.48MHz carrier modulates the data generated by the SVISSR/MTSAT frame generator. The generator and demodulator are run from different clock sources, this allows testing frequency errors in the demodulator and digital phase locked loop.

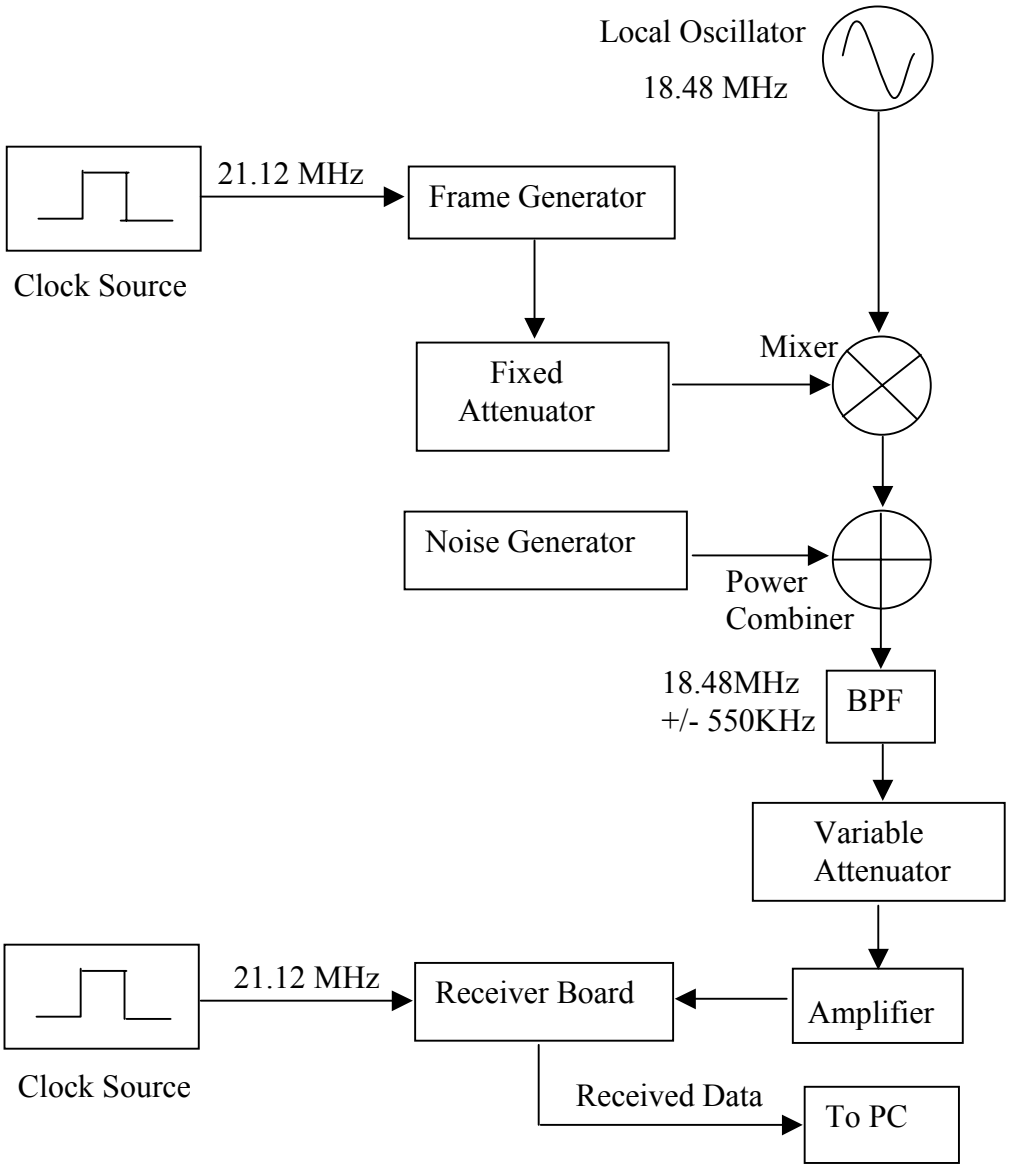


Figure 7.6. Block Diagram of the test setup

The test setup of the demodulator board is shown in figure 7.6. The attenuator after the frame generator board is to match the signal level into the mixer to simulate

received satellite signals. The bandpass filter is designed to meet the requirements for optimal bit error rate determined from the simulations and is the same as the one used in the RF receiver hardware. The signal is then amplified to the required signal level for optimal performance in exactly the same way as the receiving RF hardware. The test setup is thus configured to match the satellite transmission as close as possible. Table 7.1 lists the hardware required for the testing of the demodulator board.

Test Component	**Description**
Marconi 2041 Signal Generator	Clock Generator 21.12MHz
Marconi 2023 Signal Generator	Local Oscillator 18.48 MHz
Philips PM5193 Clock Source	Clock Generator 21.12 MHz
Agilent 33250A Function Generator	Noise Generator
20 dB + 3 dB Coax Attenuator	Fixed Attenuator
HP 8496B Attenuator	Variable Attenuator
Minicircuits MAR-8	Amplifier
Power Combiner	Custom
Bandpass Filter	Custom 18.48 MHz
Minicircuits SBL-3 Mixer	Mixer

Table 7.1. List of Components used for Demodulator testing

The power combiner is a Wilkinson power divider design with an RF transformer from Minicircuits, part number ADT1-1WT.

The method for measuring the signal to noise ratio is consistent with the technique in the simulation. The spectrum analyser from Hewlett Packard model number 8591E is used for all power measurements. The occupied bandwidth is measured for a centre frequency set to 18.48 MHz and bandwidth is set to 1.32 MHz. The resolution bandwidth is set to 13 kHz and video averaging of 100 sweeps is applied. The small resolution bandwidth relative to the bandwidth provides sufficient filtering so that

adjacent signal or noise outside of the 1.32 MHz bandwidth has little or no effect on the power measurements. The signal power and noise powers are measure separately and than combined for a signal to noise ratio. The combiner is properly terminated for each of the individual readings.

6.3 IF Filter Design

The IF filter is designed for a bandwidth of 2 x 80% (+/- 528 kHz) of the SVISSR bit-rate. A software package AADE Filter Design Program Version 1.92 is used to generate the 4th order Bessel band-pass filter. The filter is designed with input and output impedance of 50 Ohms and a finite inductor Q of 50 and all the component can be realised in practice.

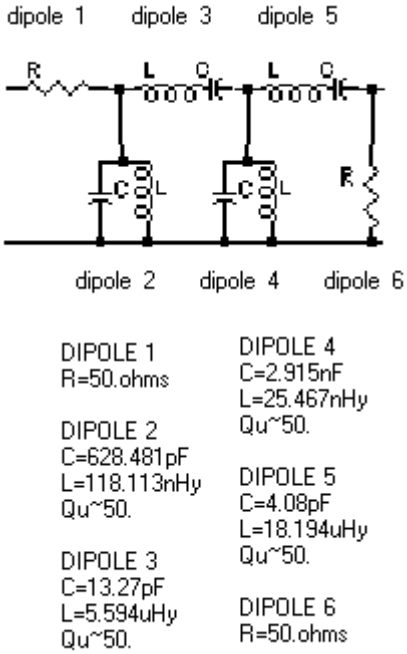


Figure 7.7. 18.48 MHz Bandpass Filter Design

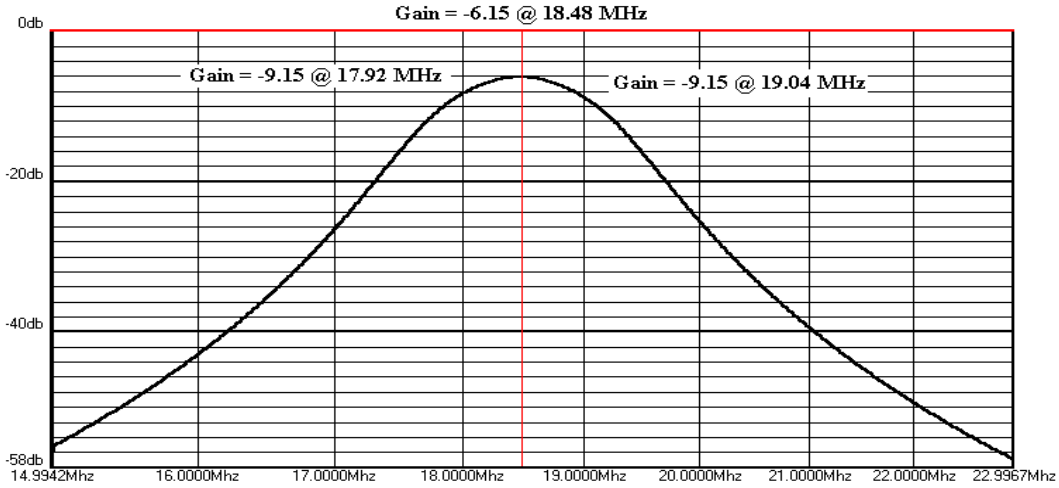


Figure 7.8. Bandpass Filter Frequency Response

The bandpass filter with the correct inductor and capacitor values should produce the frequency response shown in figure 7.8. The attenuation at +/-2.64 MHz (Nyquist bandwidth) is approximately 38dB. The actual frequency response of the bandpass filter is shown in figure 7.9.

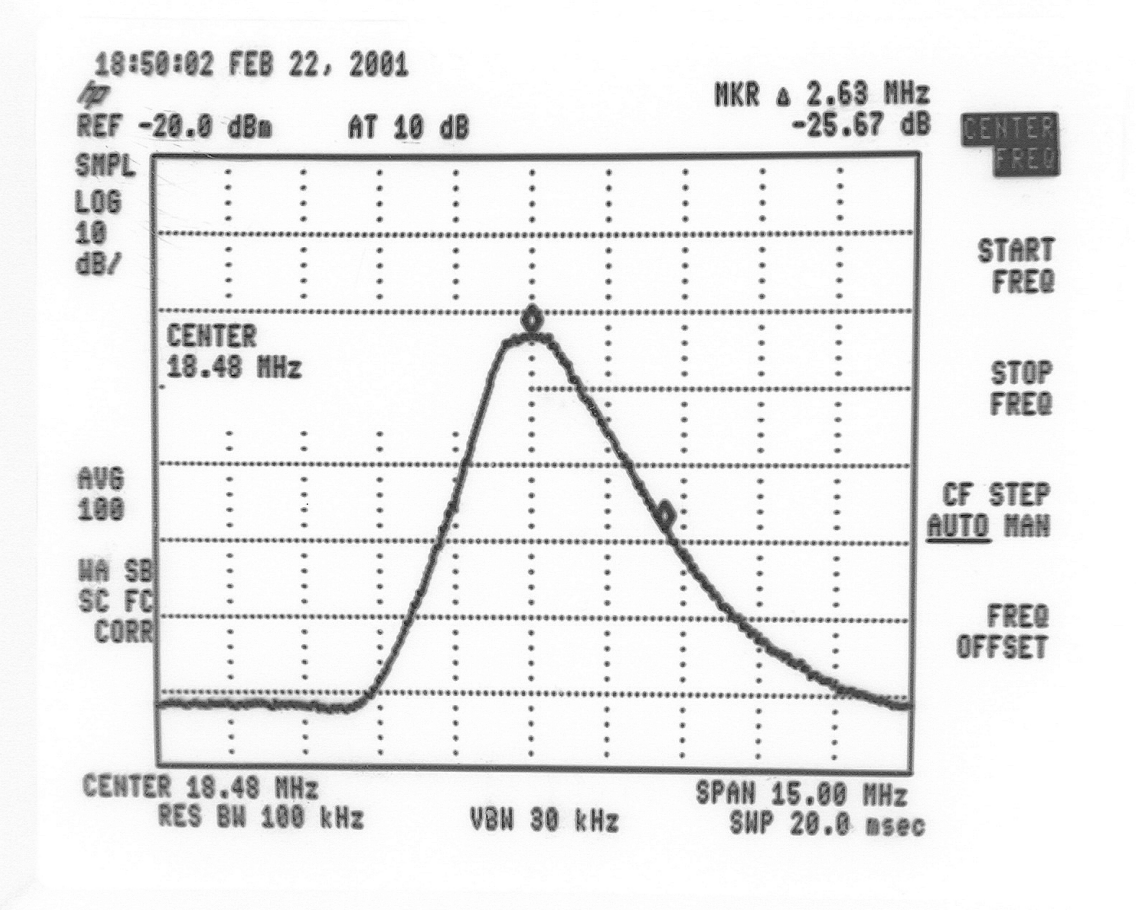


Figure 7.9. The Frequency Response of the IF Filter

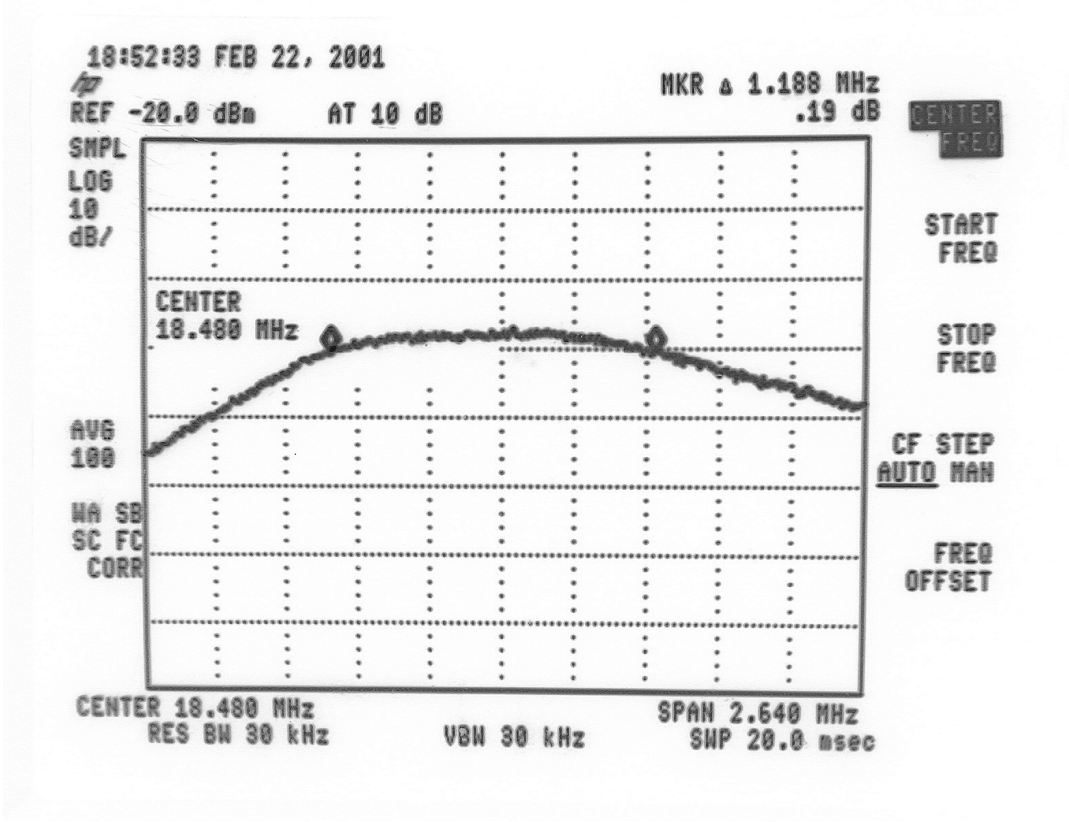


Figure 7.10. Shows a zoomed view of the passband of the IF bandpass filter.

6.4 Digital Demodulator

The demodulator section of the receiver board needs to be tested under various operating conditions. The output of the demodulator produces a baseband waveform that has been differentially decoded. The output of the digital to analog converter shown in figure 7.11, is the recovered waveform from a DPSK modulated waveform at 18.48 MHz.

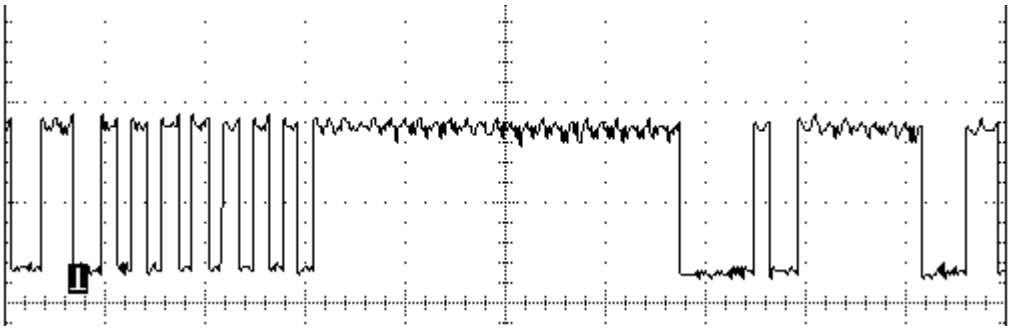


Figure 7.11. Demodulator Output with no added noise

Figures 6.12 show the output of the digital to analog converter under various signal to noise ratios.

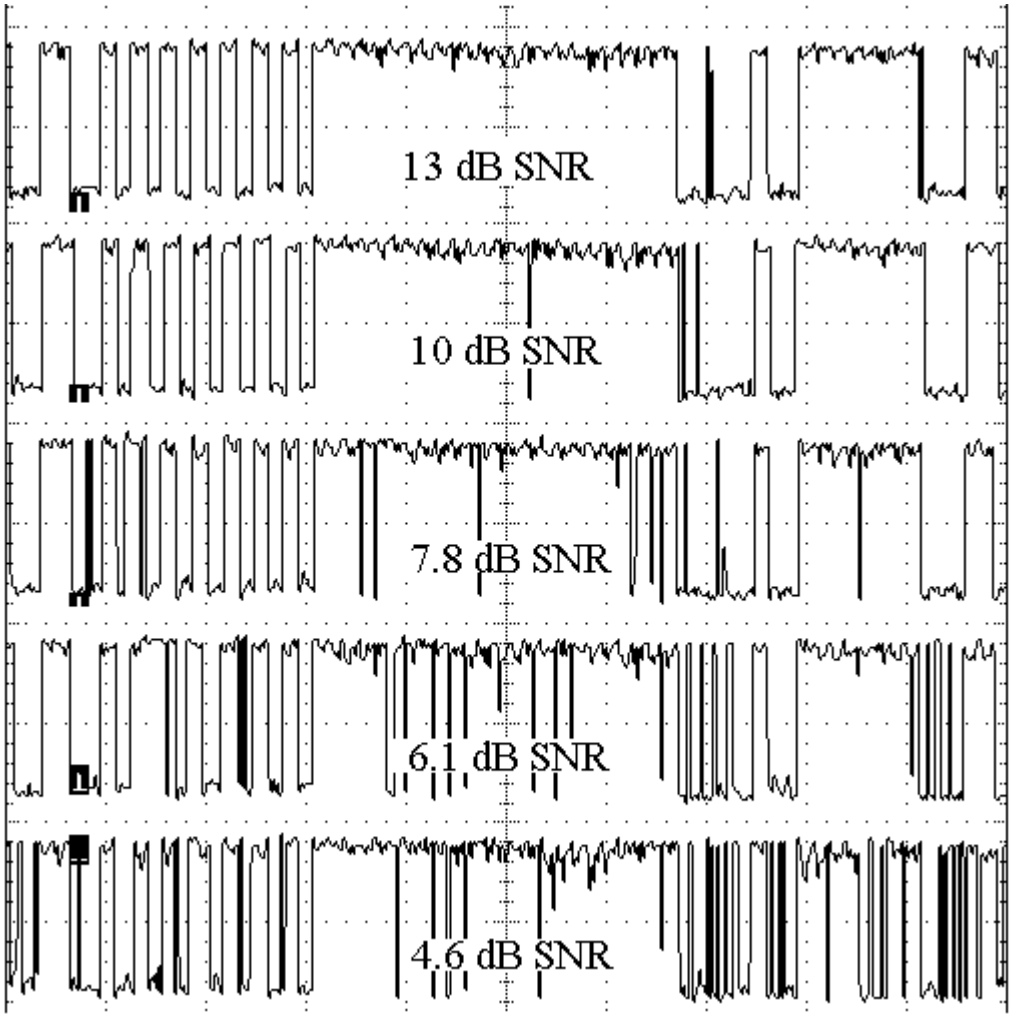


Figure 7.12. Demodulator Output with Noise

6.5 Low Pass Filtering

The design uses 16 times oversampling to reconstruct the above waveforms. Noise on the samples will cause many high frequency components up to half the sample rate, 5.28 MHz, on the recovered baseband signal. The low pass filter can attenuate most of frequency components above 70% the bit-rate. The filter bandwidth was determined from simulations in section 3.2. Figure 7.13, is the filtered demodulator output with no added noise.

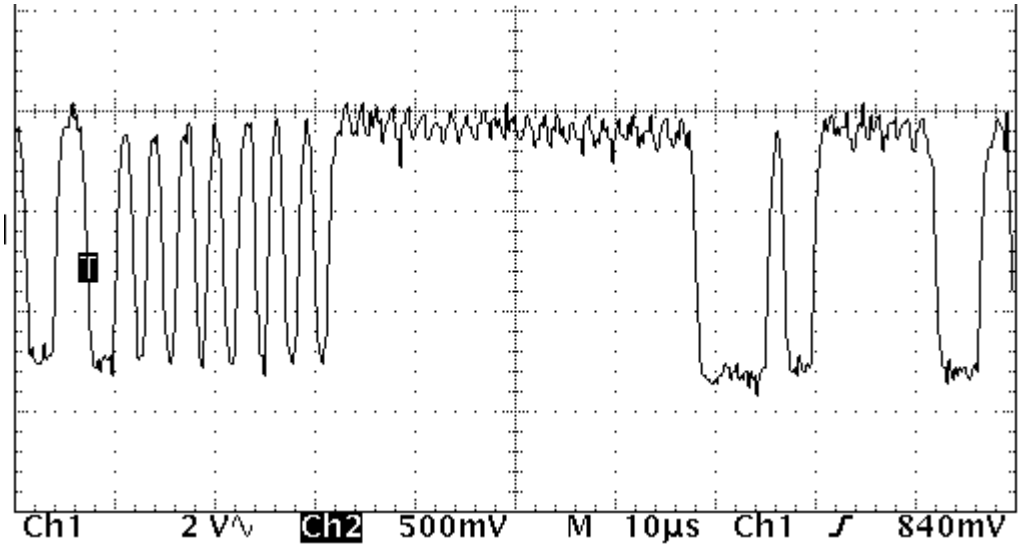


Figure 7.13. Low Pass Filter Output with no Noise

Figure 7.14 shows the effect of adding noise on the DPSK signal. As the signal to noise ratio decreases the bit transitions become obscured and are more susceptible to errors.

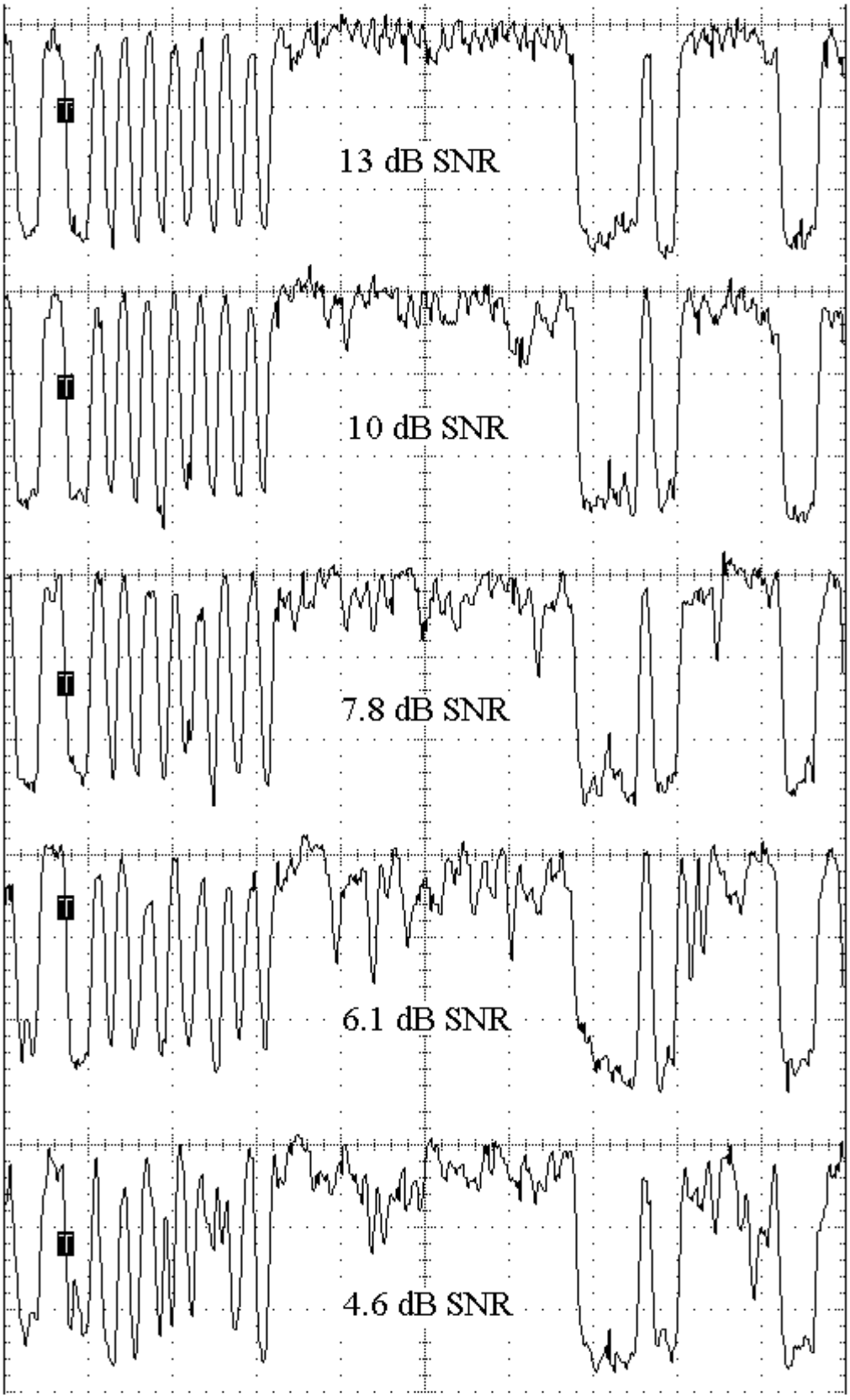


Figure 7.14. Low Pass Filter Output with Noise

The demodulator can also be tested for a reference clock frequency error. The satellite's bit-rate reference clock is susceptible to drifting due to manufacturing, temperature and age. The life of this satellite has been extended four years and this clock could drift outside the original design specification. The frequency accuracy is more likely to be limited by the reference crystal in the receiver. The receiver's crystal stability is likely to be an order of magnitude worse than the satellite crystal. For a 100ppm crystal, the maximum receiver reference crystal error is 1 kHz.

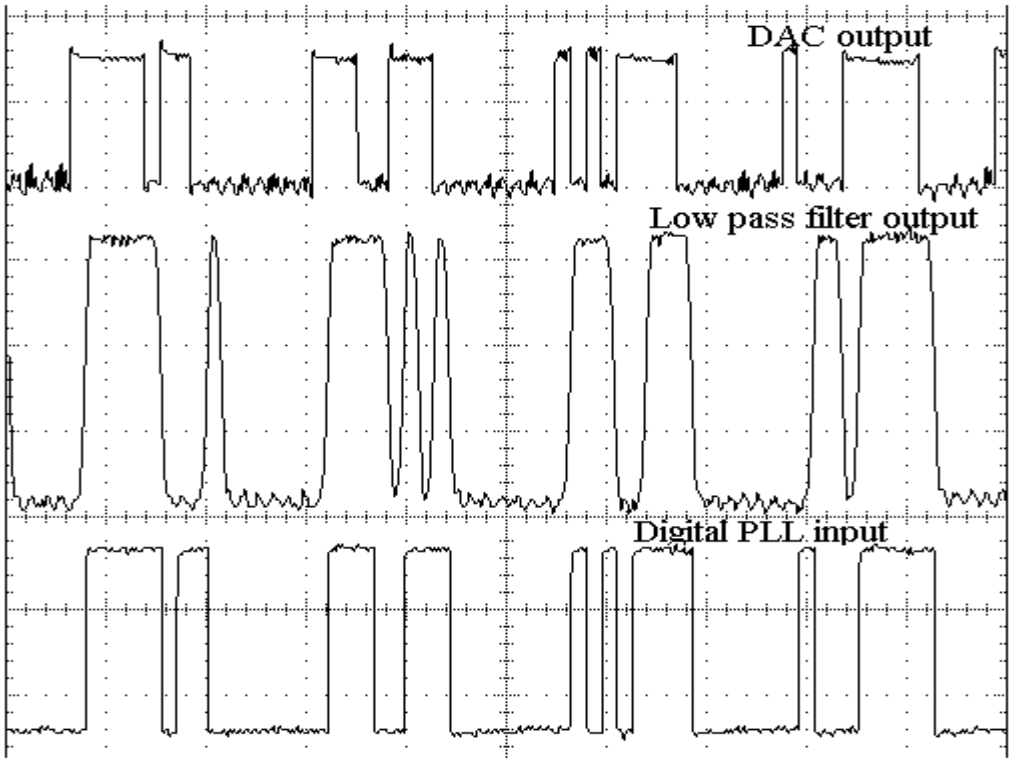


Figure 7.15. 0 Hz Error (Ideal)

Figure 7.15 shows the effect of reference clock frequency error on the output of the demodulator. The first waveform is the output of the demodulator, then next is the output of the low pass filter, and the last waveform is the input to the digital phase locked loop. Figure 7.16-18 shows the effect the frequency error on the performance of the demodulator.

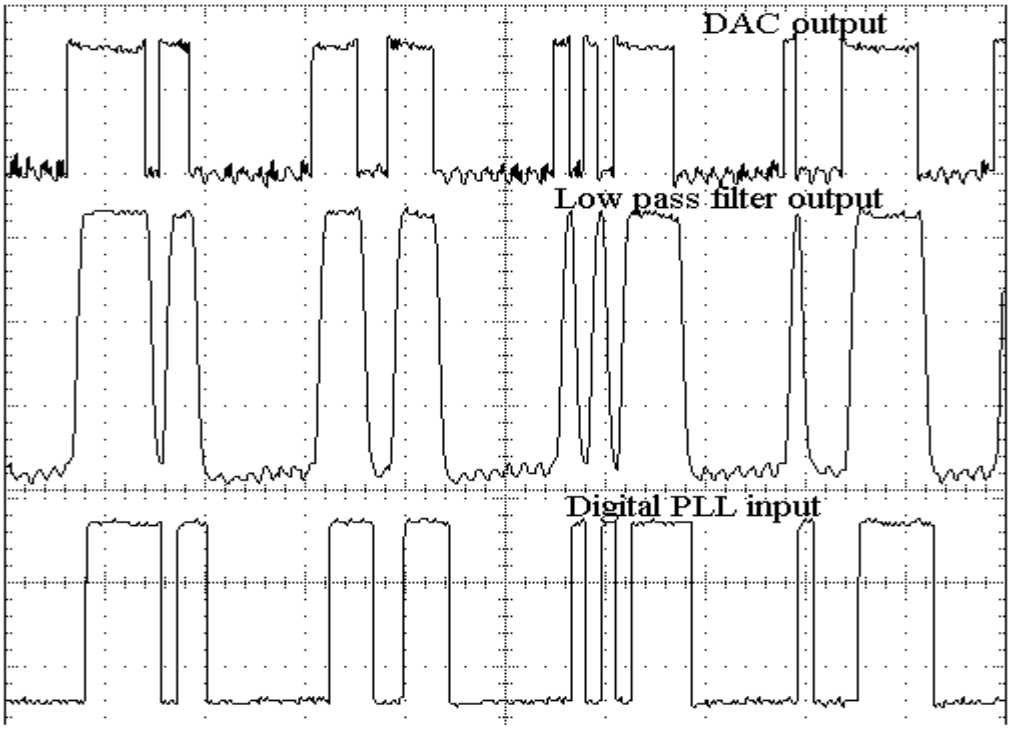


Figure 7.16. 10KHz frequency offset

For frequency errors less than 25 kHz there seems no degradation in the demodulator output. As the frequency error increases the demodulator output produces high frequency transition errors. This will limit the bit error rate. This shows that expensive and high satiability reference crystals are not required for the operation of the demodulator.

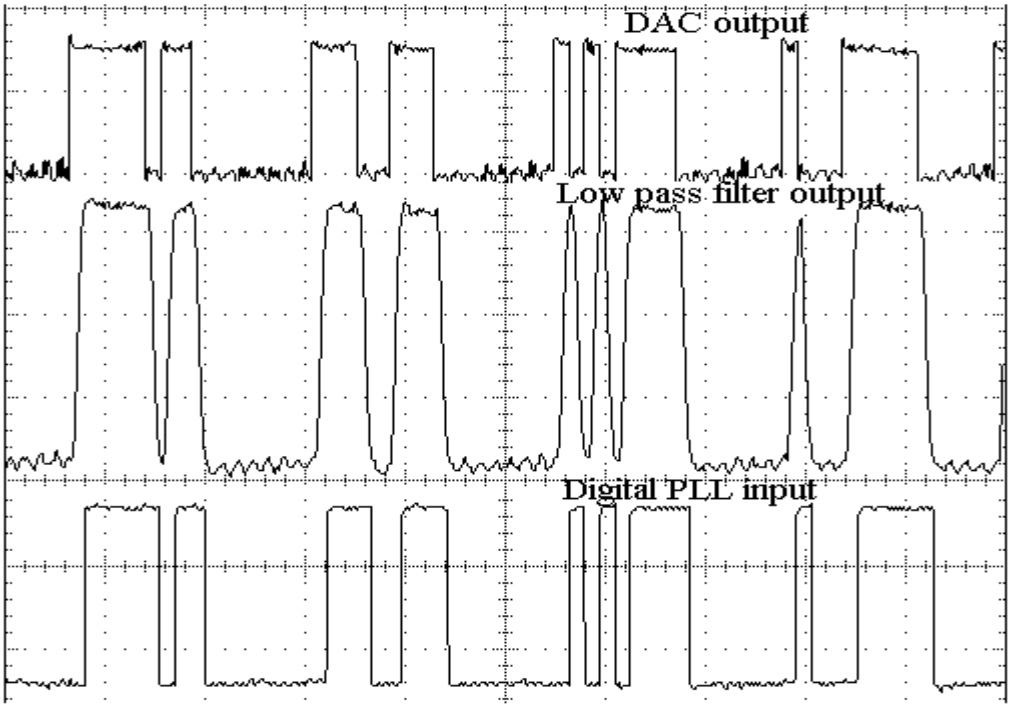


Figure 7.17. 25KHz frequency offset

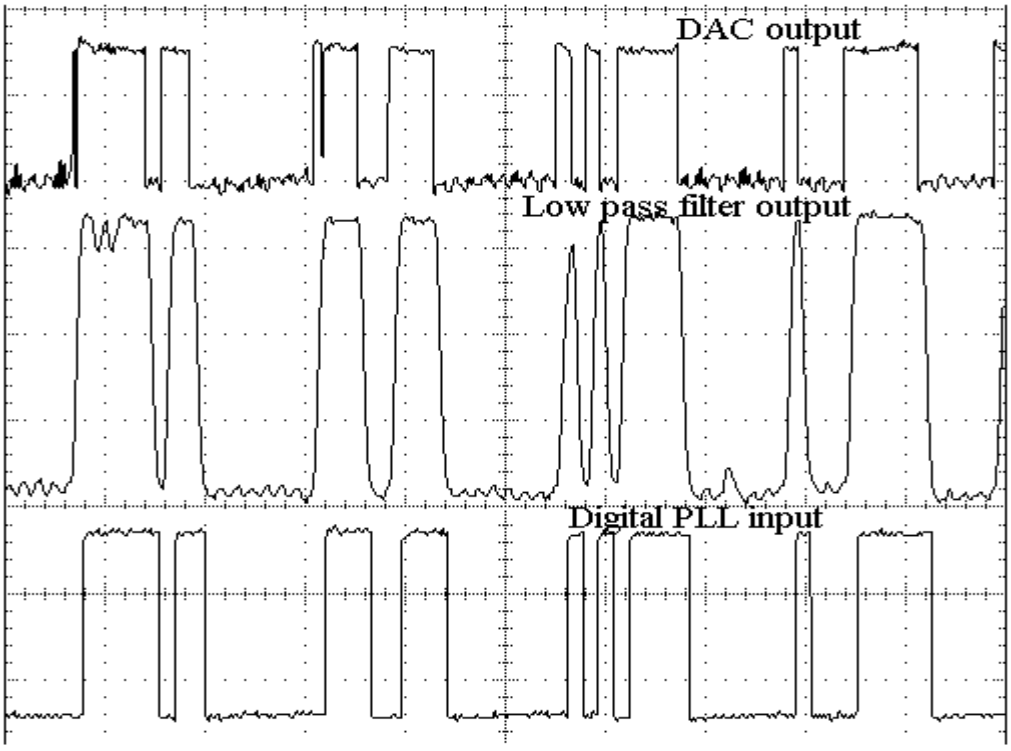


Figure 7.18. 40KHz frequency offset

6.6 Digital Phase Locked Loop

The output of the low pass filter is the converted to TTL levels with a comparator. The comparator includes hysteresis to help reduce the susceptibility of noise on the bit transitions. The digital phase locked loop outputs the recovered clock and the latched data at the correct sampling instance. An eye diagram is a measure of the locking ability of the phase locked loop. Figure 7.19 shows the eye diagram for the demodulator board. The analog output is measured at the output of the low pass filter flowing the digital to analog converter.

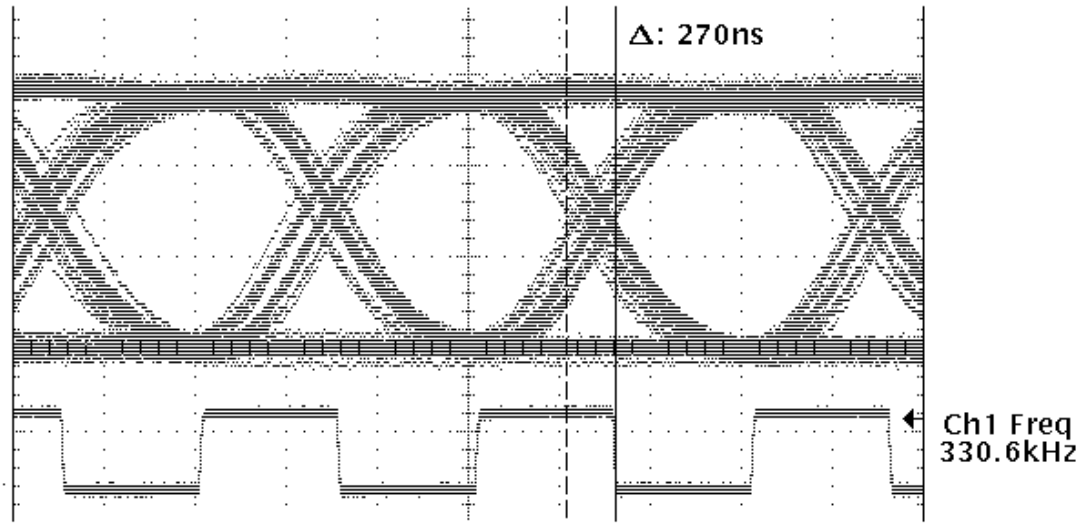


Figure 7.19. Eye Diagram with no frequency error or added noise

The timing jitter is expected from simulations and is due filtering. The measured timing jitter is approximately 270ns, which is approximately 3 samples or 66 degrees. This timing jitter is larger than predicted in the simulations, and is due to non-ideal realization of the bandpass and low pass Bessel filters, quantization errors due to rounding in the EPLDs and noise introduced through the power supply and ground loops. The system is designed to operate at signal to noise ratios below 13 dB, so the degradation in bit error rate due to timing jitter at high signal to noise ratios are not critical for this design. Figure 7.20 show the eye diagrams for the digital phase locked loop under various signal to noise ratios. The figure also measures the timing jitter for each of the signal conditions.

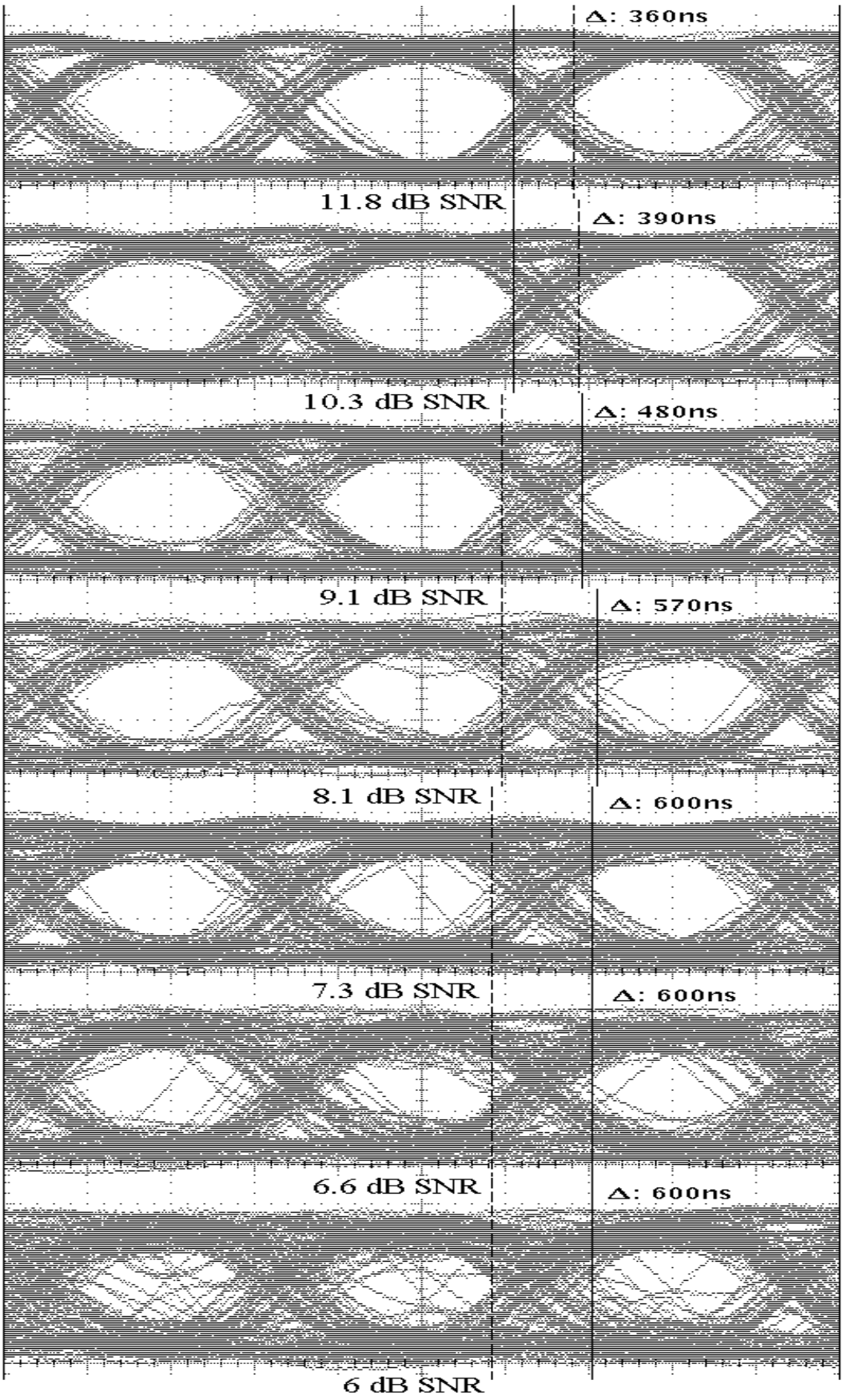


Figure 7.20. Eye Diagram with added Noise

The Digital Phase Locked Loop can also be tested with the same reference crystal frequency error. Figure 7.21 shows the effect on the eye diagram of a 10 kHz frequency error.

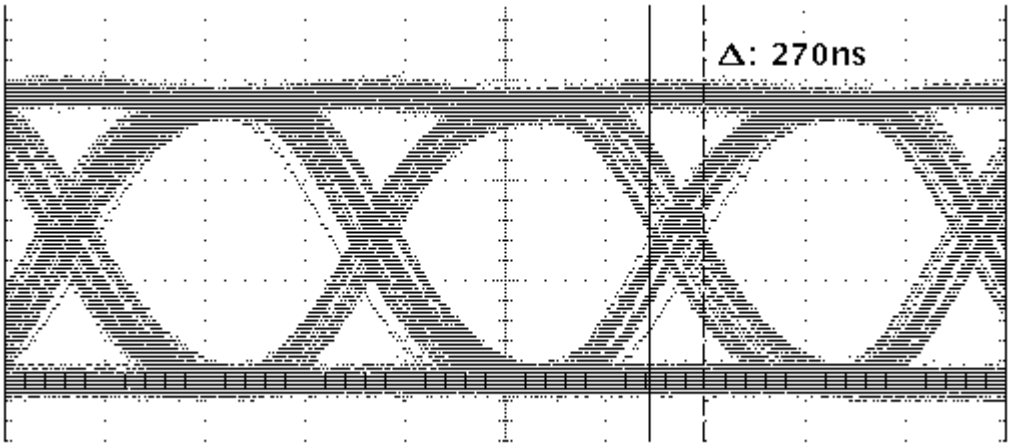


Figure 7.21. Eye Diagram Frequency Error = 10KHz

For frequency error less than 25 kHz the timing jitter of the recovered clock only increases by 10ns. This shows that the performance of the phase locked loop will not degrade with the use of low stability reference crystals. Figure 7.22 show the eye diagram under various frequency errors.

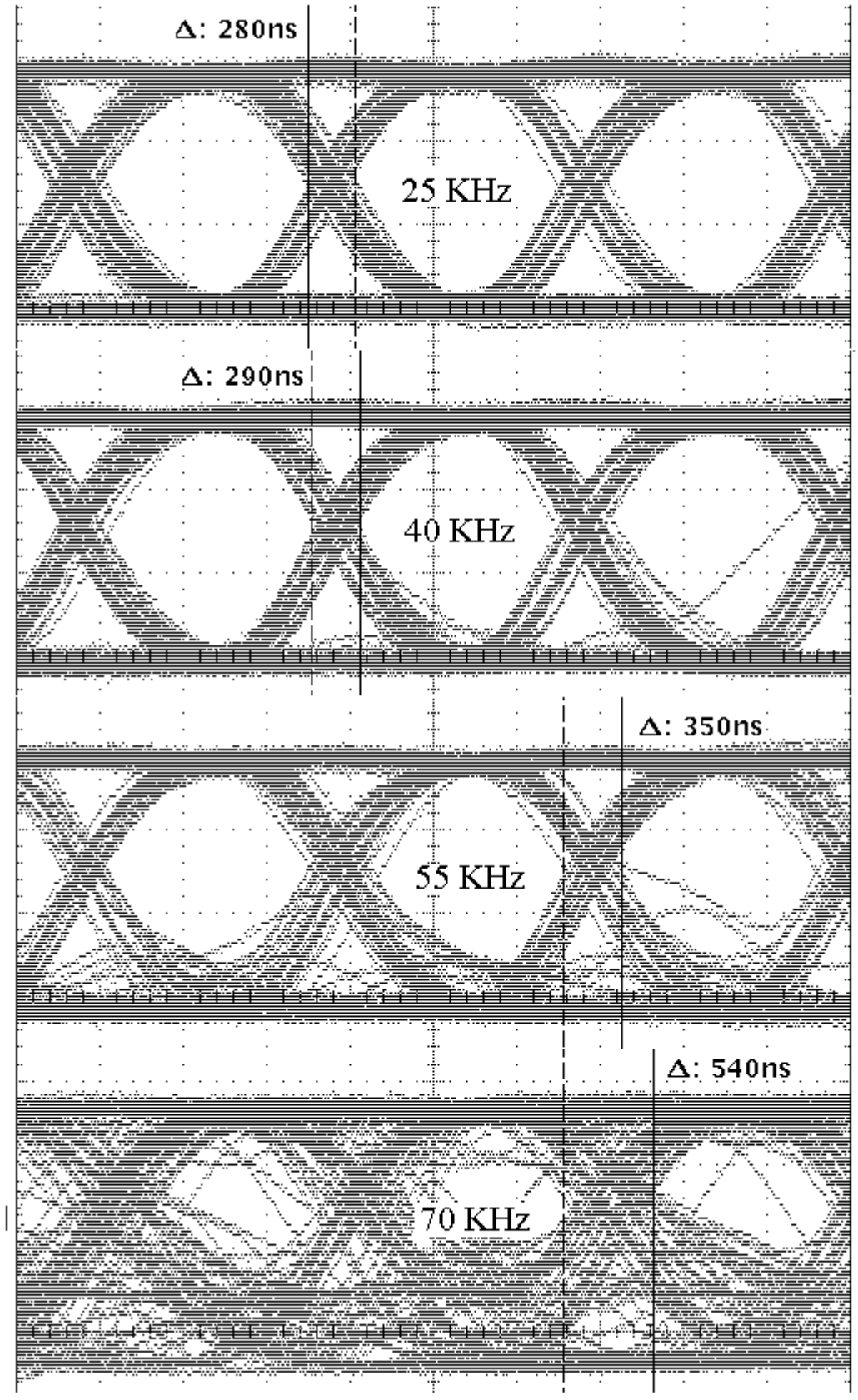


Figure 7.22. Eye Diagram with Frequency Errors

6.7 Bit Error Rate Testing

This compares the theoretical simulation with the measured bit error rate. Figure 7.23 shows the measured bit error rate and expected bit error rate from simulations. The measured performance gives a 1 dB worse performance. This is partly due to the higher than expected timing jitter on the DPLL recovered clock, almost 3 samples. With a high timing jitter, the performance of the demodulator at high signal to noise ratios will further reduce performance. Part of the problem could be attributed to the physical anomalies in the design of analog components. The 18.48 MHz filter is very susceptible to variations in component values. This alone could be the major contributor to loss of performance in the measured BER tests. The analog components DAC, LPF and comparator will also add to the timing jitter. The LPF is susceptible to non-ideal components and the comparator requires hysteresis to reduce noise on the DPLL input. This hysteresis will be another contributor to the timing jitter.

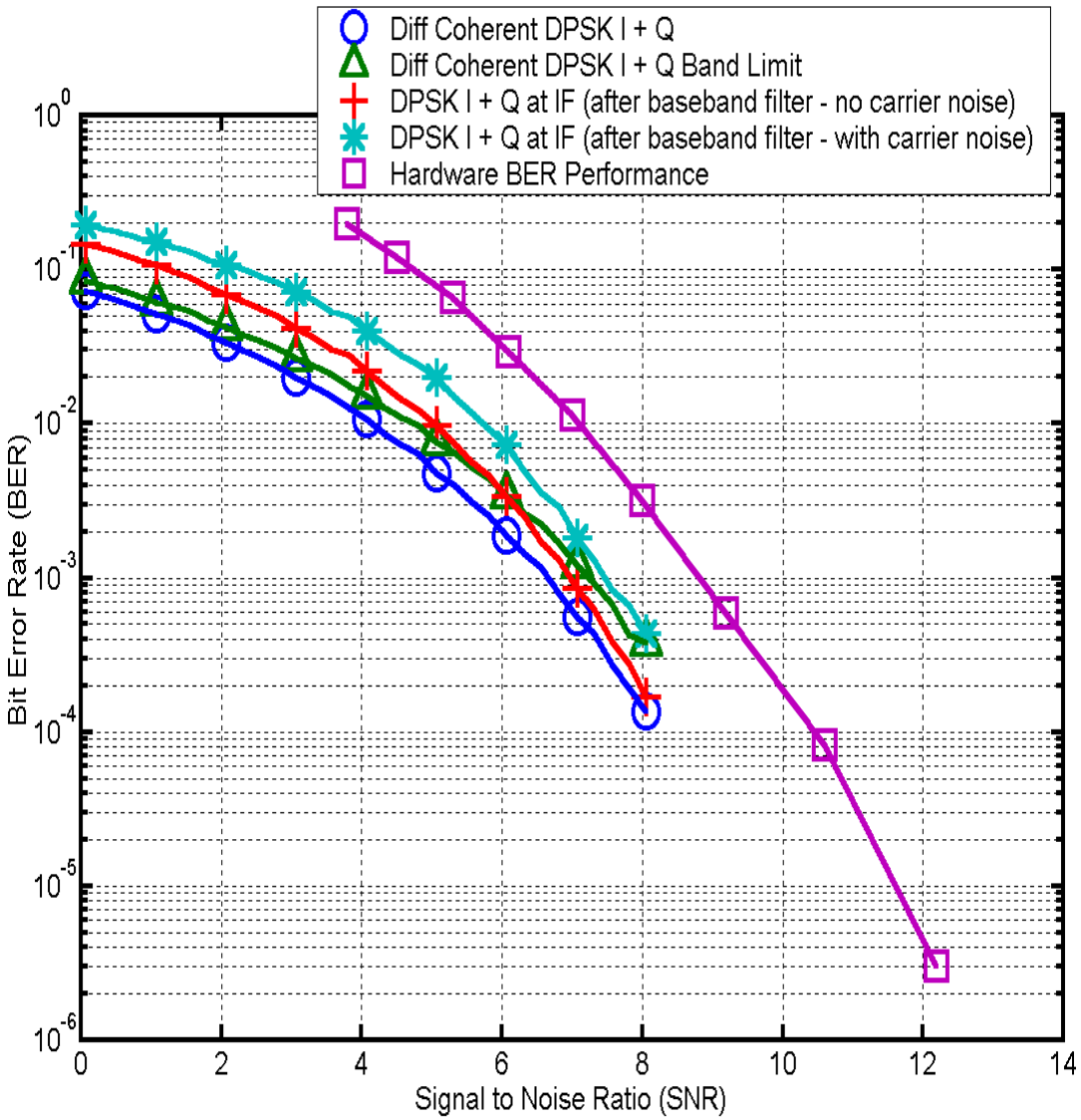


Figure 7.23. Demodulator and DPLL BER performance comparison

The coherent receivers require a wide-band signal for optimal performance. The band-limited receiver suffers 1 dB degradation from ideal. If timing jitter from the symbol recovery loop is also incorporated in the differentially coherent simulation the performance would expect to drop be at least 1 dB. This makes to the measured BER approximately 1-1.5 dB worse than the differentially coherent receiver design.

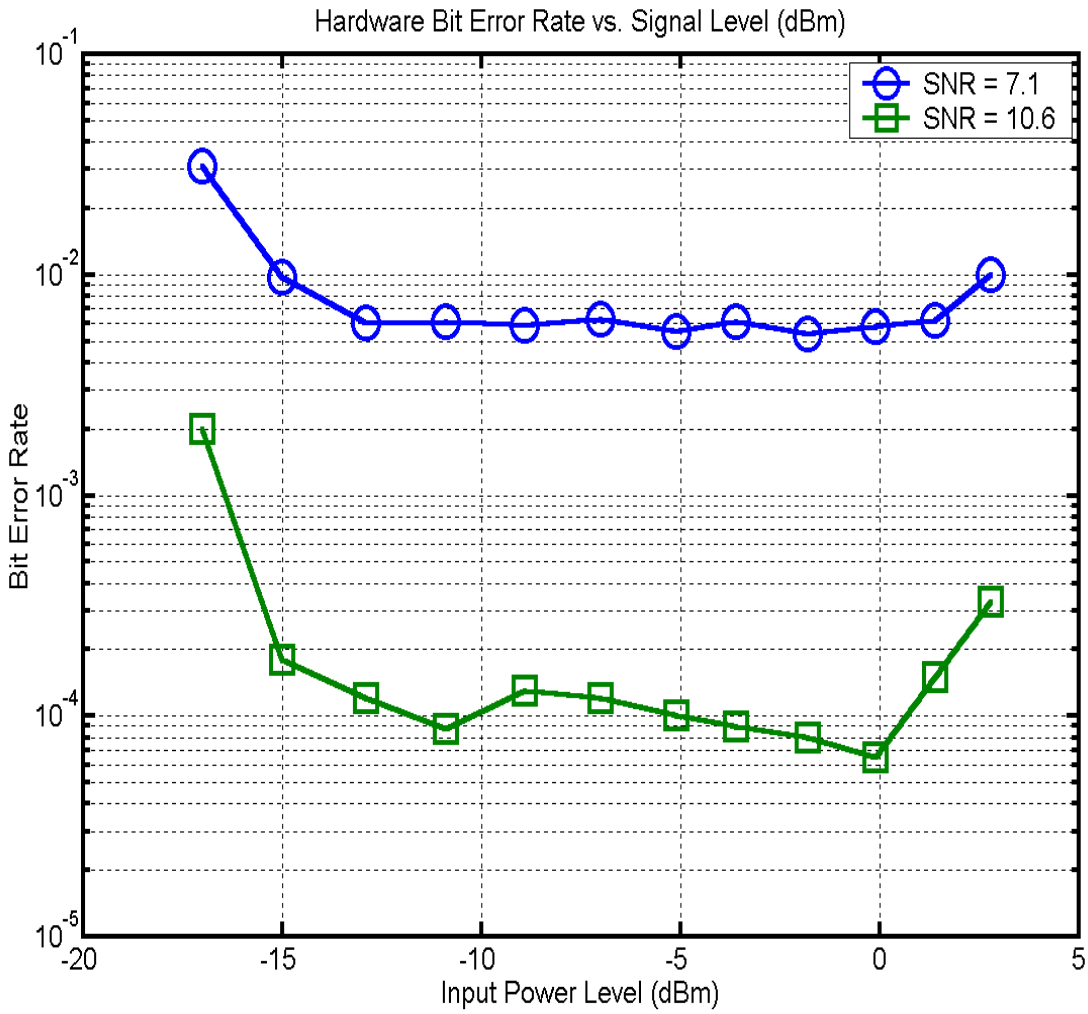


Figure 7.24. Signal level Vs. Bit error Rate

The BER is tested over a range of input signal levels to test performance. Figure 7.24, show the BER for various signal to noise ratios and input power levels. The EPLD receiver can successfully receive data over a 15 dB dynamic range. The receiver can operate reliably with the ADC driven 3 dB into clipping. This results reduces the requirements of the AGC for accurate gain control. AGC may not even be required, as the GMS-5 signal rarely suffers from large fades. At the 1.7 GHz transmission signal fades due to rain are not significant.

6.8 Frame Synchronizer Performance

The frame synchronization is designed to achieve reliable locking under low signal to noise ratios. The frame synchronization works successfully down to a signal to noise ratio of 4 dB.

Below a SNR of 4 dB the BER is very high, greater than 1e-1, and reliable synchronization is not possible for this design. The frame synchronization exceeds the required performance of the receiver.

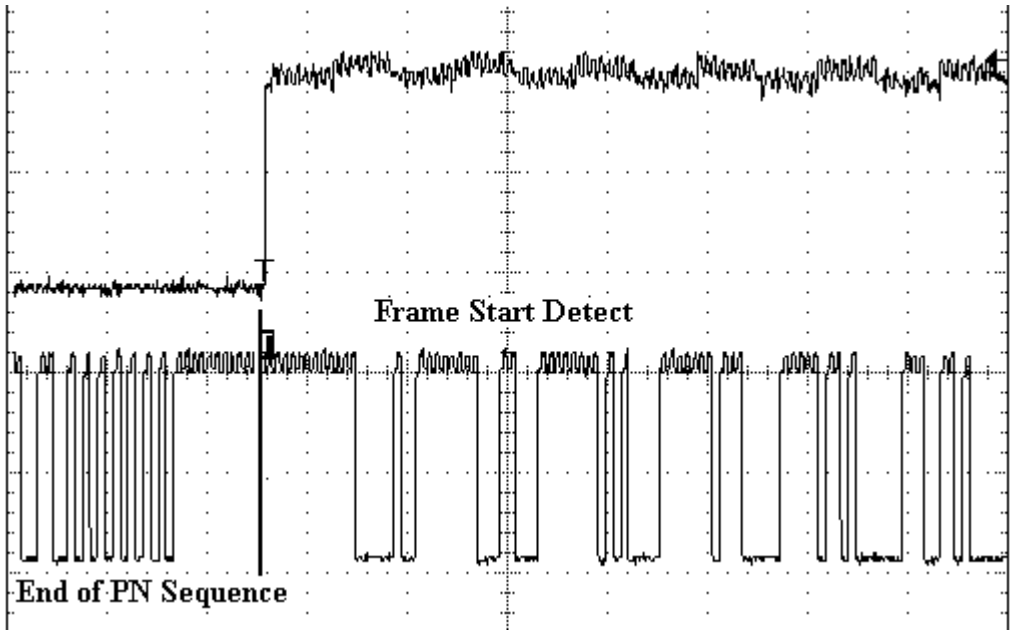


Figure 7.25. Frame Start Detection

Figure 7.25 shows that successful frame synchronization is achieved and the start of the information sectors are successfully detected. Figure 7.26 shows the performance of the frame synchronization under various signal to noise ratio conditions.

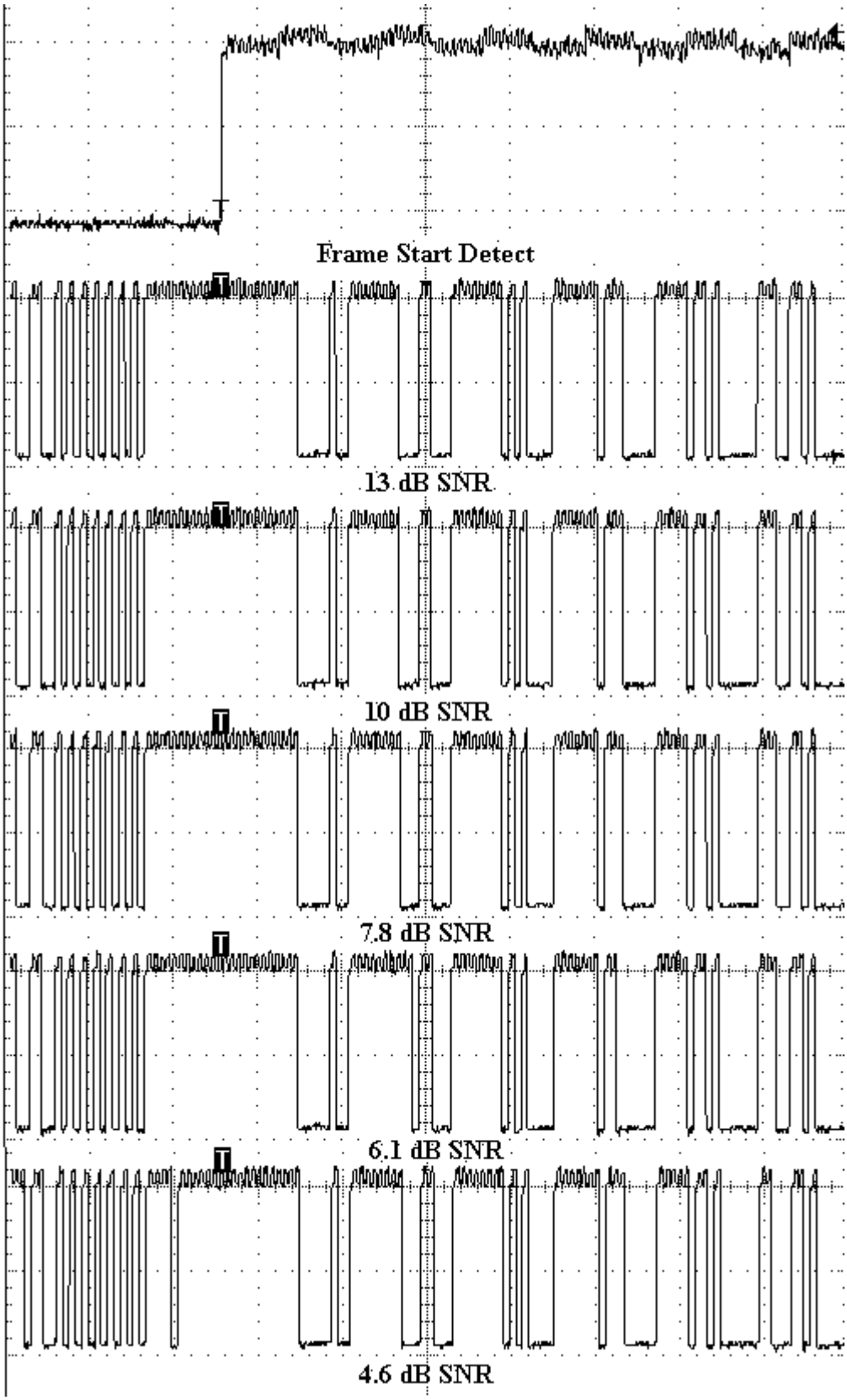


Figure 7.26. Frame Synchronization with added Noise

Chapter 8 Receiving Satellite Images

7.1 Receiving SVISSR Images

The received GMS-5 WEFAX signal is transmitted at a frequency of 1687.1 MHz. The SVISSR signal is transmitted only 3.9 MHz higher at 1691 MHz. The two systems are never transmitting at the same time, so there is no inter-channel interference. The current JCU MetSat system has the first stage of the RF signal down mixing and amplifier infrastructure in place and is not required to be replaced.

The signal received after the down mixing and amplification is centred on 137.5 MHz for WEFAX and 133.6 MHz for SVISSR. When GMS-5 is replaced with MTSAT-1R in 2003 the HiRID system will transmit at the same frequency as the GMS-5 SVISSR system.

7.2 Hardware Set-up for receiving GMS-5 SVISSR images

The power of the received signal at 133.6 MHz with a 3 metre satellite dish is about –120 dBm. Amplification and down mixing is required to produce a signal at 18.48 MHz with an input power level between –15 dBm and 0 dBm. This signal power level has been determined from testing to give the optimal bit error rate.

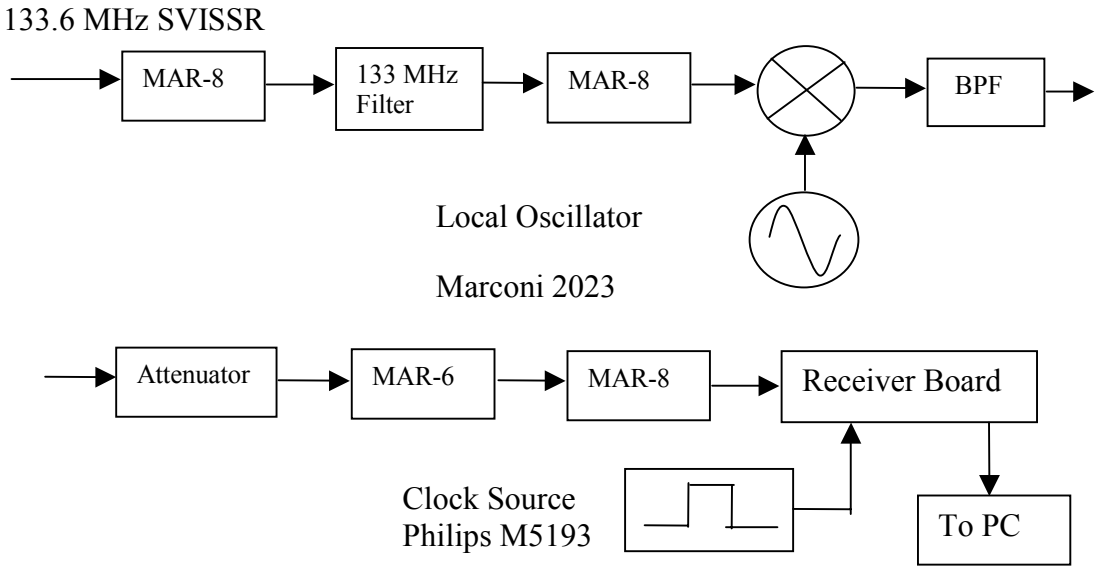


Figure 8.1. Test Setup to Receive SVISSR Images

The list of equipment used for the RF down mixing and amplification from 133.6 MHz to 18.48 MHz is as follows.

Amplifier	Minicircuits MAR-8
Amplifier	Minicircuits MAR-6
Amplifier	Minicircuits MAR-6
Amplifier	Minicircuits MAR-8
Local Oscillator	Marconi signal generator model 2023
Clock generator	Philips programmable function generator model PM5193
Filter	Helical Filter centre frequency 133 MHz
Attenuator	Hewlett Packard variable attenuator model 8496B

Table 8.1. Test equipment used to receive GMS-5 SVISSR signals

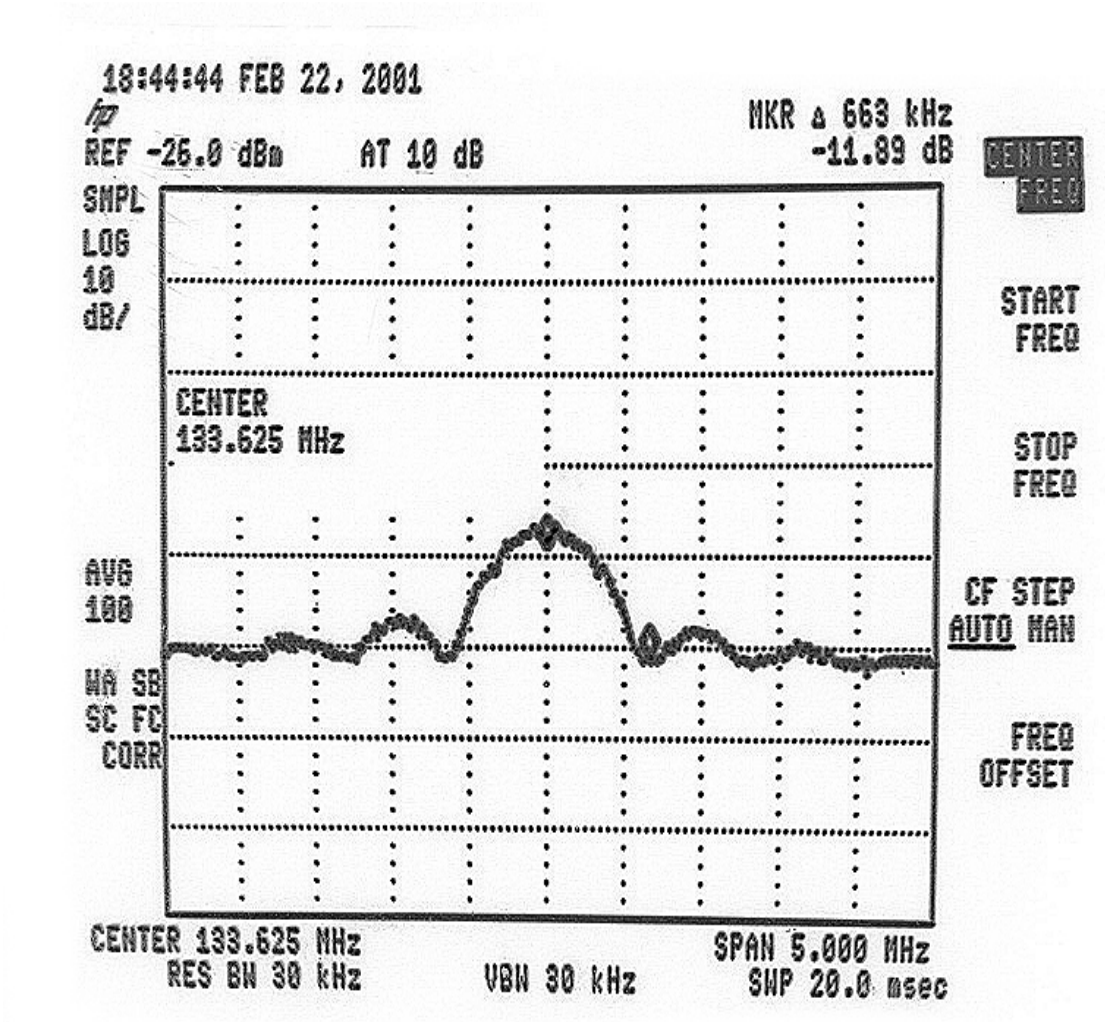


Figure 8.2. GMS Signal at 133.6 MHz

Figure 8.2 shows the received GMS-5 SVISSR signal at 133.6 MHz. This is after a Low Noise Amplifier (LNA) and oscillator being used for the current MetSat system has mixed and amplified the GMS-5 signal.

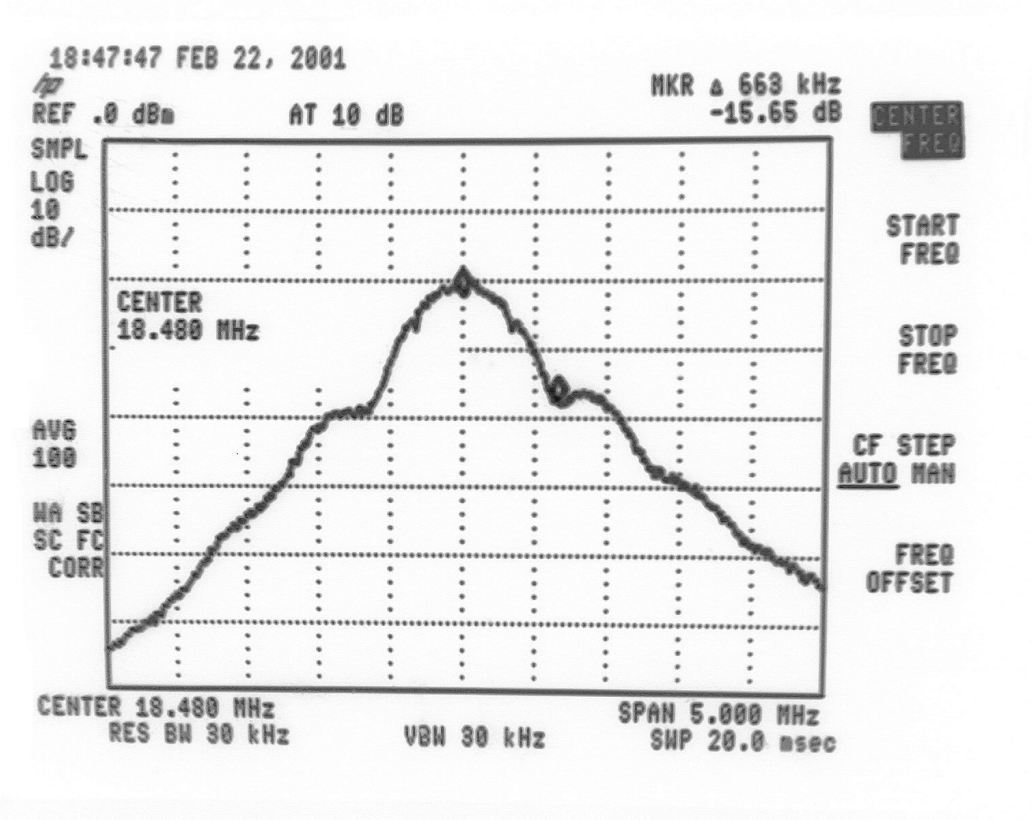


Figure 8.3. GMS Signal at 18.48 MHz

Figure 8.3 shows the GMS-5 SVISSR signal after being amplified, mixed and filtered at 18.48 MHz. The received signal power can be measured for an occupied bandwidth using a built-in function of the HP8591E spectrum analyser. This is same technique to measure signal to noise ratio in the simulations. The channel power is first measured while there is no SVISSR signal. This gives a measure of the channel noise power. The channel noise power (NP) was measured to be:

$$NP = -50.1\,dBm$$

Next the received signal and noise power (SNP) of the channel can be measured.

$$S + NP = -39.5\,dBm$$

From the above two results the signal power can be extracted and the signal to noise ratio can be calculated.

$$SNR = 10.2\,dB$$

Therefore the measured signal to noise ratio of the received GMS-5 SVISSR signal is 10.2 dB

7.2 Software Set-up for receiving GMS-5 SVISSR images

The receiving software is written in “C” for the Red Hat Linux operating system. The parallel port is setup in EPP mode by writing directly to the registers described in Appendix D. The parallel port is then polled to check if a new byte has been received or the start of a new frame. The start of a new frame is detected by receiving a high on a spare pin of the parallel port. This keeps the software synchronized with the start of each frame, in case synchronization is lost in a frame. This software will continue to receive frames until user intervention. The receiving software is used for testing the receiver board and used for logging images. Appendix N lists the receiving software.

7.3 Post Processing Software

The user, at the end of the received dissemination, launches the post processing software. The software extracts and generates the greyscale infrared or visible images in the standard Windows bitmap image format. The images that are generated depend on the jumper settings on the EPLD receiver PCB, see section 5.7.

7.4 Bitmap Image Format

Bitmap files are stored in a device-independent bitmap (DIB) format that allows Windows and other operating systems to display the bitmap on any type of display device. The term "device independent" means that the bitmap specifies pixel colour in a form independent of the method used by a display to represent colour. The default filename extension of a Windows DIB file is .BMP.

Each bitmap file contains a bitmap-file header, a bitmap-information header, a colour table, and an array of bytes that defines the bitmap bits. The bitmap-file header contains information about the dimensions, compression type, and colour format for the bitmap. The colour table, defined as an array of RGB structures, contains as

many elements as there are colours in the bitmap. The colours in the table should appear in order of importance. This helps a display driver render a bitmap on a device that cannot display as many colours as there are in the bitmap.

The bitmap bits, immediately following the colour table, consist of an array of BYTE values representing consecutive rows, or "scan lines," of the bitmap. Each scan line consists of consecutive bytes representing the pixels in the scan line, in left-to-right order. The number of bytes representing a scan line depends on the colour format and the width, in pixels, of the bitmap. If necessary, a scan line must be zero-padded to end on a 32-bit boundary. The scan lines in the bitmap are stored from bottom up. This means that the first byte in the array represents the pixels in the lower-left corner of the bitmap and the last byte represents the pixels in the upper-right corner. Appendix O contains a listing of the post processing software.

Once on the bitmap format, the images can be subsampled and converted to memory efficient formats like JPEG. Figure 8.4 shows the greyscale infrared IR 1 channel. Figure 8.5 shows a false colour image generated by combining infrared IR 1 & IR 2 and visible VIS 1 channels.

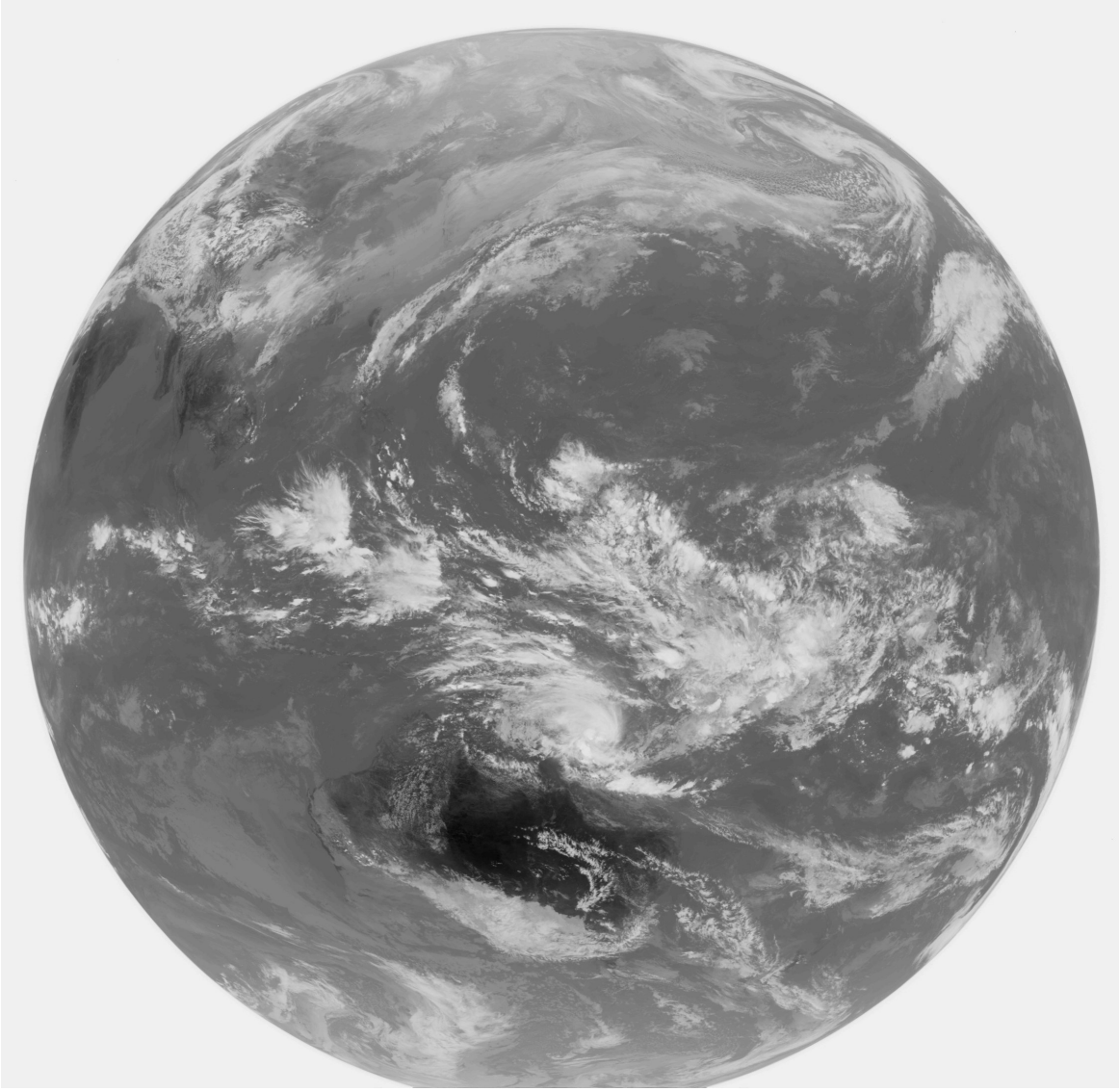


Figure 8.4. SVISSR High Resolution Infrared IR 1 Image

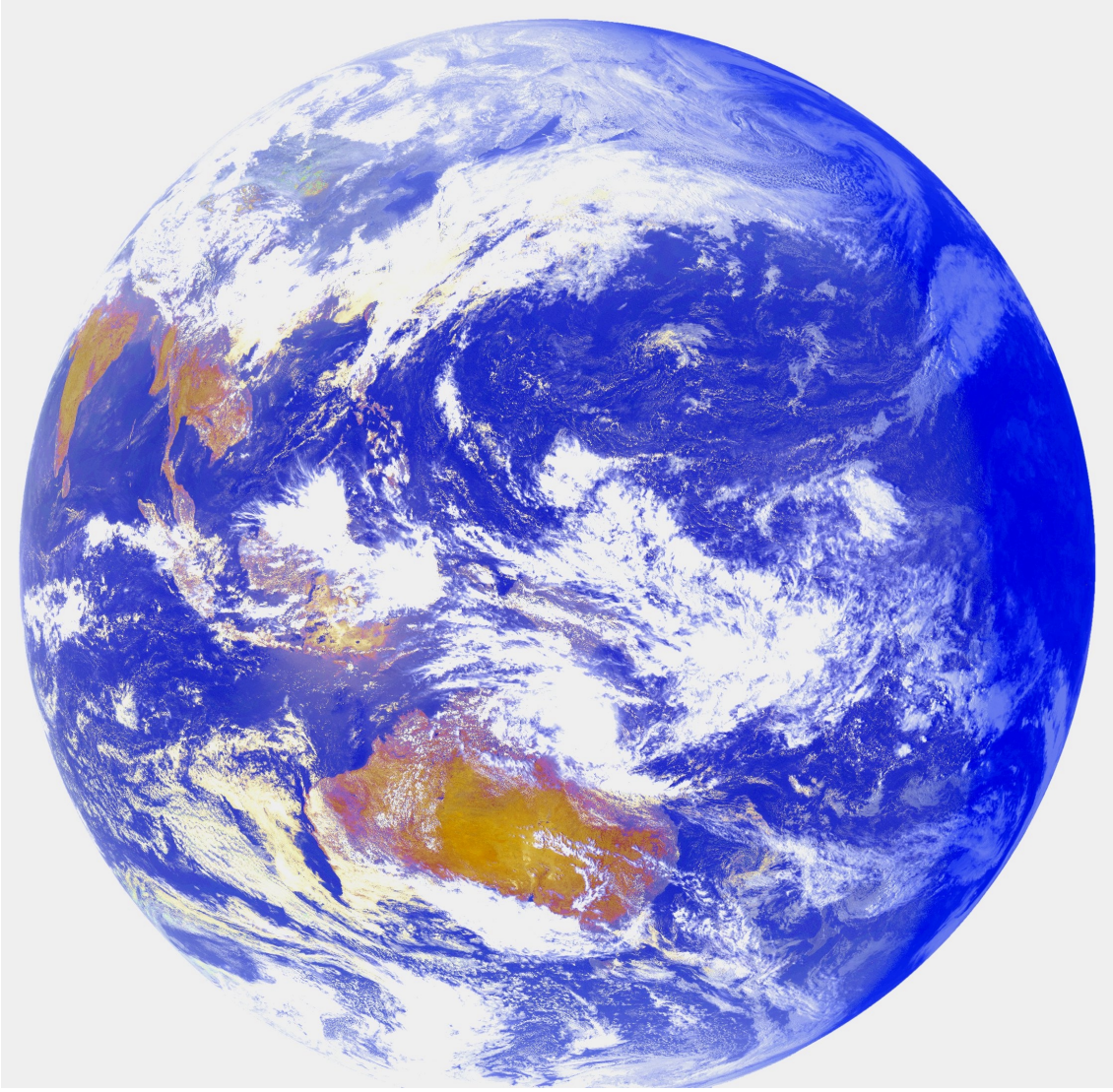


Figure 8.5. SVISSR High Resolution False Colour Image

Chapter 9 RF Board Design

8.1 RF Board

An RF Board is required to replace the test equipment used in figure 8.1. The RF board has a similar block diagram, see figure 9.1. A MAR-6 amplifier first amplifies the received SVISSR signal, then bandpass filtered with a 133 MHz commercial filter with a 2 MHz bandwidth. The signal is then amplified with a MAR-8 amplifier before being mixed down to 18.48 MHz with a commercial mixer from Minicircuits. The bandpass filter has been designed in section 6.3 for optimal bit error rate performance. A fixed attenuator is used to reduce the maximum signal power level into the final stages of the RF board. A MAR-6 followed by an MAR-8 amplifies the received signal up to a power level that is acceptable for the EPLD receiver board, see section 6.7 for input power level requirements.

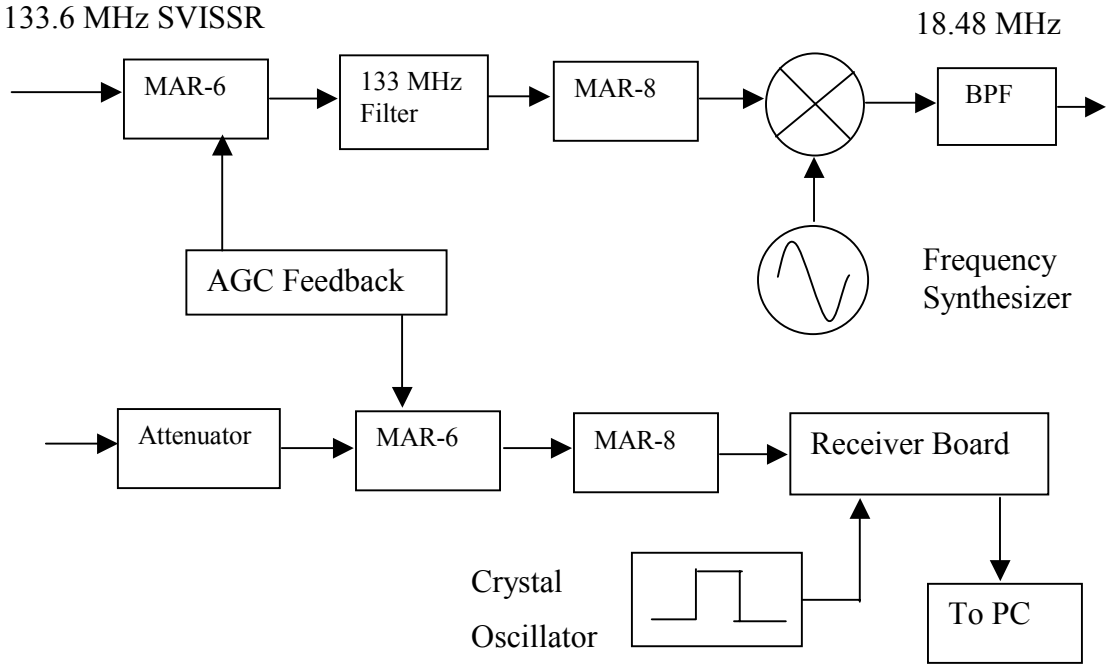


Figure 9.1. RF Board Block Diagram

The Automatic Gain Control (AGC) is a AM peak detector and low pass filter on the EPLD receiver board. Figure 7.24, section 6.7, shows the bit error rate performance

with variation in input signal power levels. AGC is required so that any received signal power variations can be compensated without the loss in bit error rate performance. Due to the 15 dB dynamic range of the EPLD receiver the AGC may not be required.

The mixer clock source is from a frequency synthesizer IC. This is IC is programmed via an on-board PIC micro-controller from Microchip. The crystal oscillator is a commercial fixed TTL clock generator. It is designed to have a centre frequency of 21.12 MHz and an accuracy of 100 ppm.

Appendix F contains the complete design of the RF Board, schematics and PCB.

Chapter 10 EPLD Receiver Improvements

9.1 Filter Improvements

The bandwidth of the intermediate frequency (IF) filter at 18.48 MHz is difficult to construct and could be the source of many tuning problems in the EPLD receiver design. One improvement would be to add an extra IF stage at 70 MHz. This bandpass filter could be a narrow bandwidth Surface Acoustic Wave (SAW) filter. SAW filters are manufactured with high predictability to have a narrow bandwidth and a sharp roll-off. A SAW filter is available with a bandwidth of 900 kHz at a 70 MHz centre frequency. SAW filters do suffer because of a high insertion loss and passband ripple. This design amendment would require another mixer, MAR amplifier and a fixed crystal oscillator. This would add to the cost of the EPLD receiver but the requirements of the 18.48 MHz bandpass filter would be reduced to an anti-aliasing filter that would not require such precise components. The EPLD receiver would then operate at 68% bandpass filter bandwidth, figure 4.12, this could improve the bit error rate by 20%-30%.

9.2 EPLD Integration

One way of improving performance is to eliminate as many of the analog components on the receiver board. The digital to analog converter, low pass filter and comparator adds noise and distortion that contribute to the loss of performance.

To remove these components the low pass filter would have to be digitally in an EPLD. With today's high performance and high density EPLDs and FPGAs, all the function of the receiver board could be integrated into a single chip. The current design was implemented for the best price performance. Thus Lattice EPLDs filled this criteria. The project could not justify the expensive outlay for a high performance FPGA or EPLD when high integration is not a design criterion.

EPLDS and FPGAs from Xilinx and Altera provide similar architecture to the lattice EPLDs, but also contain multiplication and memory blocks. With these extra blocks, the filter and multiplier can be implemented in silicon and remove the need for external components.

The number of EPLD registers required by the current design is:

Description	**Registers**
Delay EPLD	128
I+Q Delay and DPLL	71
Frame Synchronization	91
FIFO and Parallel Port	33
Total Registers	**323**

Table 10.1. Table of Registers used in Receiver Board

A low density of the Altera Flex 10K devices contains 50,000 gates as compared with the Lattice 1032E EPLD, which has only 6,000 gates. Those 50,000 gates can be configured into 2880 logic elements (registers). There are also 40,960 bits of dual-port memory.

The number of registers required to implement the multiplication, the low pass filter and a FIFO can be estimated.

Description	**Registers**
8-bit 16 tap FIR filter	597
16-bit multiplier with 3 stage pipeline	592
Total Registers	**1189**

Table 10.2. Register Required for Altera Implementation

The on-board dual port memory can be configured as a FIFO. With 40,960 bits of memory, a 5 K x 8 bit FIFO can be configured. The complete design would require a minimum of 1512 registers to be implemented in a single device. The Flex 10K50E contains 2880 registers, this will leave 1368 registers for other uses. Even with only 50% routing efficiency, 2268 registers would be required. This would leave 612 registers free.

With the free registers the number of bits used can be increased from 8-bits to 10- or 12-bit, depending on the ADC. This would improve the dynamic range of the EPLD receiver. The oversampling rate could also be increased, this would improve the timing jitter from the digital phase locked loop.

This design would also have the advantage of a linear phase filter and removal of the digital to analog converter and comparator. This device is expensive but all components in the current design, except the analog to digital converter, are redundant. This design would also expect an improvement in performance closer to the theoretical limit.

The speed of FPGA does also offer a substantial speed advantage when compared to a digital signal processor. The Altera Flex architecture can be optimised to perform an 8-tap FIR filter at 100 MSPS, due to the pipelining architecture, FIR filters with higher order taps can also be performed at 100 MSPS. The multiplication can operate at a maximum speed of 20 MSPS. Both of these speed specifications exceed the requirements of the EPLD receiver design. Figure 10.1 shows a block diagram of the Altera FPGA solution. All the components, except the ADC, on the EPLD receiver board could be replaced with a single FPGA. The price and availability of the Altera FPGA devices make this solution unattractive. One advantage of writing code in VHDL and ABEL is that the code and EDIF files are compatible between manufacturers, so if an Altera FPGA was to be used, only minimal changes to the code would be required.

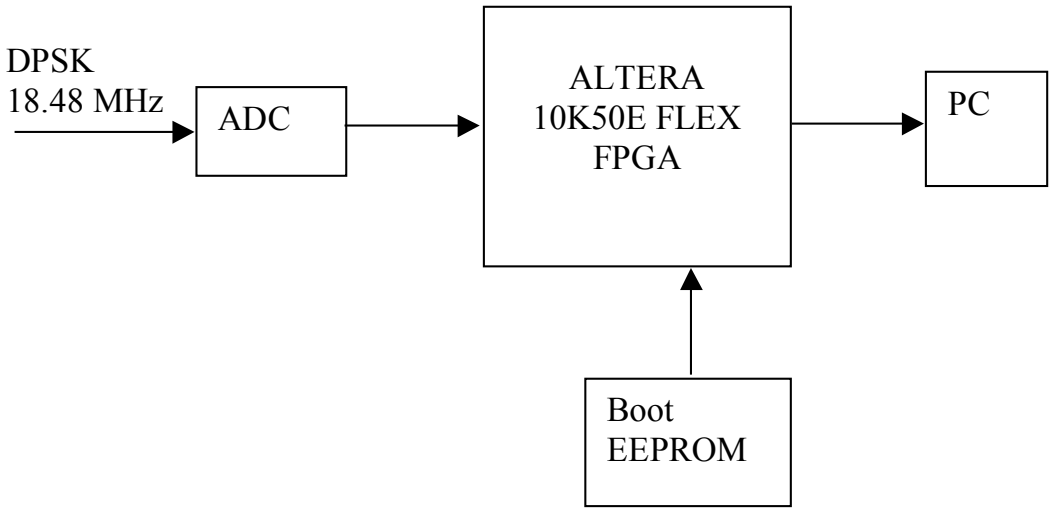


Figure 10.1. Altera FPGA realization of EPLD receiver