

### Basic Concepts: Instruction Execution

Each SPARC instruction is one word long (32-bits)

Info is encoded into each instruction.

01001101 10101010 10111001 00101101

**OpCode Register**

**Literal Data**

Instructions are stored in memory with data.

Instructions are always word aligned.

Registers

“PC” - the program counter

The “fetch-increment-execute” loop:

```

PC = 0
loop
  instr = MEMORY [PC]
  PC = PC + 4
  Execute instr...
    • fetch operands
    • perform computations
    • store results (includes modifying PC)
endLoop
    
```

### Machine Architecture Variations

#### Stack Architectures

Easy to compile to  
Lots of memory accesses  
Used mostly for interpreters

```

LVALUE z
PUSH x
PUSH y
ADD
ASSIGN
    
```

#### Accumulator Architectures

One general purpose register

```

LOAD x
ADD y
STORE z
    
```

#### CISC / Two-Operand Architectures

Several general-purpose registers  
Two operand fields in instructions  
The result overwrites one operand

```

LOAD x, R3
ADD y, R3
STORE R3, z
    
```

#### RISC / Load Store / Three-operand Architectures

Lots of general-purpose registers  
Instructions have 3 operand fields  
Each instruction is either  
Computation  
Memory access

```

LOAD x, R1
LOAD y, R2
ADD R1, R2, R3
STORE R3, z
    
```

Operands for computation must be in registers  
Many instructions execute in a single clock cycle

## SPARC Registers

### General-Purpose Registers

32 registers  
 32-bits (4bytes) each  
 Divided into 4 sets of 8 registers

*Well, okay to assume 32-bits...*

**Global** %g0, %g1, ... %g7  
**Local** %l0, %l1, ... %l7  
**In** %i0, %i1, ... %i7  
**Out** %o0, %o1, ... %o7

Available operations:  
 Integer arithmetic: add, sub, mul, div, cmp  
 Logical: and, or, not, shift-left, shift-right

### Floating-Point Registers

32 registers %f0, %f1, ... %f31  
 Available operations:  
 Floating-point arithmetic: add, sub, mul, div, cmp  
 Integer-to-floating conversion

## Other Registers

### Program Counter (PC)

32-bits

### Integer Condition Code Register

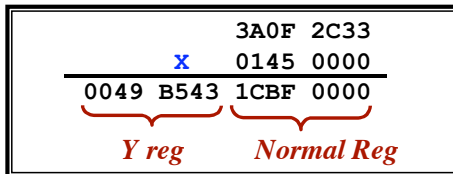
4-bits  
 For integer operations

### Floating-Point Condition Code Register

4-bits  
 For floating-point operations

### “Y” Register

32-bits  
 Used for integer multiply  
 and divide operations



### Other Registers

Lots - ignore them



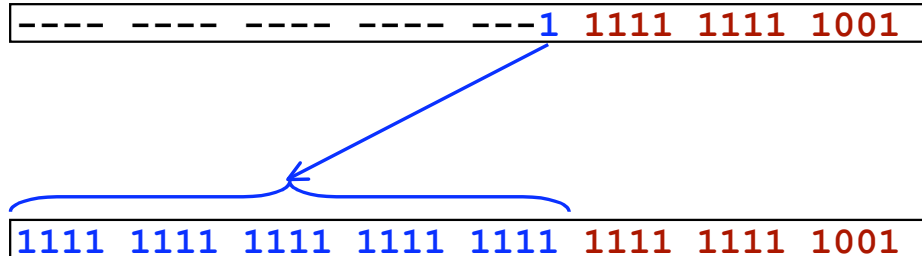
### 13-Bit Immediate Values

The instruction includes a 13-bit signed value.

Range: **-4096 .. 4095**

This value is “sign-extended” to 32-bits.

Example:



### Notation

**sub**      **reg1, reg2\_or\_immed, regD**

**reg1, reg2, regD:**

Any one of the 32 general-purpose integer registers (5 bits)

**immed**

13-bit signed integer value

Must be between -4096 and 4095

Signed-extended to 32-bits before being used

Syntax: Full “C”-like expressions

Character literals	'm'	}	<i>All equal</i>
	"m"		
Hex	0x6d		
Decimal	109		
Octal	0155		
Expressions	64 + (3 * 'm')		
Symbols	x		<i>← Assembly-time constants, not runtime variables!</i>

### Assembler Syntax

One instruction per line  
 Labels - on same line, or on line alone

Spaces are okay, but not normally used

```

label:
    sub    %g3,%g5,%g7    ! Comments
    add    %g7,56,%g7    !
    add    %12,34,%12    !
    
```

{ Tab
{ Tab
{ Tab

Example

```

ld      myVal,%12      ! myVal = myVal + 78
add     %12,78,%12    ! .
st      %12,myVal      ! .
    
```

Note the Commenting style

The destination is always on the right.

(Not quite legal SPARC)

### Instructions

<p><u>Arithmetic</u></p> <pre> add sub Signed { smul         { sdiv Unsigned { umul          { udiv     </pre> <p><u>Logical</u></p> <pre> and or xor andn orn xnor     </pre> <p><u>Shifting</u></p> <pre> sll srl sra     </pre>	<p><i>These do not modify the condition code Register.</i></p>	<p><u>Arithmetic</u></p> <pre> addcc subcc smulcc sdivcc umulcc udivcc     </pre> <p><u>Logical</u></p> <pre> andcc orcc xorcc andncc orncc xnorcc     </pre> <p><i>Will set:</i>  <i>Z=1</i>  <i>if result is zero</i>  <i>N=1</i>  <i>if result is neg</i>  <i>etc.</i></p>	<p><i>These do modify the condition code register.</i></p>
--	--	---	--

Logical Functions

and  
 or  
 xor = x != y  
 andn = x and (not y)  
 orn = x or (not y)  
 xnor = x = y

x	y	and	or	xor	andn	orn	xnor
0	0	0	0	0	0	1	1
0	1	0	1	1	0	0	0
1	0	0	1	1	1	1	0
1	1	1	1	0	0	1	1

*These instructions work on all 32 bits at once:*

```
and    %g4, %g5, %g6

%g4 → 0011 1100 ... 1010
%g5 → 1010 1101 ... 1001
%g6 → 0010 1100 ... 1000
```

To turn on bits in a word...

Use the “or” instruction and a “mask” word

```
or    x, mask, result
```

Turn on bits in x wherever the mask has a 1 bit

<i>Example: Turn on every other bit in 3A0F</i>			
0011 1010 0000 1111	←	3A0F	
0101 0101 0101 0101	←	mask	
0111 1111 0101 1111	←	result	

To turn off bits in a word...

Use the “and” instruction and a mask

```
and   x, mask, result
```

Turn off bits in x wherever the mask has a 0 bit

To flip (or “toggle”) bits in a word...

Use the “xor” instruction and a mask

```
xor   x, mask, result
```

Change the bits in x wherever the mask has a 1 bit

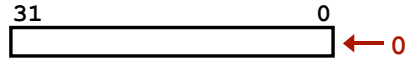
### Shifting Instructions

#### sll

“Shift Left Logical” <<

```
sll reg1, reg2_or_immed, regD
```

Number of bits 0..31



A fast way to multiply by  $2^N$ ...

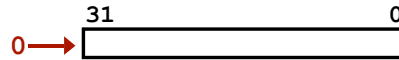
*Example:* Multiply by 32 (=  $2^5$ )

```
sll x, 5, result
0000 0000 0000 0011 = 3
0000 0000 0110 0000 = 64+32 = 96
```

#### srl

“Shift Right Logical” >>>

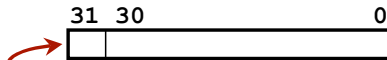
```
srl reg1, reg2_or_immed, regD
```



#### sra

“Shift Right Arithmetic” >>

```
sra reg1, reg2_or_immed, regD
```



A fast way to divide by  $2^N$ , rounding toward  $-\infty$ ...

```
sra x, N, result
```

### Testing

```
cmp reg1, reg2_or_immed
```

Compare operand1 to operand2

Set integer condition codes accordingly

The next instruction will normally be a conditional branch

*Example:*

```
cmp %g3, 73 ! if x <= 73 goto loop
ble loop ! .
```

*Branch if the condition codes indicate  
 $op1 \leq op2$*

## How to turn high-level code into assembly code:

```
if (x >= 73) && (y < 98) then
  b = c + d
endif
```

### Step 1: Convert LOOPS and IFs into GOTOs (possibly reversing the tests):

```
if x<73 then goto elseLabel
if y>=98 then goto elseLabel
b = c + d
elseLabel:
```

Assume:

```
x in %l3
y in %l2
b in %g3
c in %g4
d in %g5
```

### Step 2: Turn into assembly code.

Keep the operand order and tests the same!

```
cmp    %l3,73      ! if x >= 73
bl     elseLabel  ! .
cmp    %l2,98      ! . and y < 98
bge    elseLabel  ! .
add    %g4,%g5,%g3 ! b = c + d
elseLabel:        ! endif
```

*NOTE: The comments look like source code, including indentation!*

## Unconditional Branch (the “goto” instruction)

```
ba label
```

## Conditional Branches

### For Signed Values

```
bl  label
ble label
bg  label
bge label
```

### For Unsigned Values

```
blu label
bleu label
bgu  label
bgeu label
```

### Equality Testing

```
be  label    <same>
bne label    <same>
```



The Condition Code Register

4 bits:

**N** 1 = negative  
**Z** 1 = zero  
**V** 1 = overflow  
**C** 1 = carry out

Set after arithmetic operations

**addcc, subcc, ...**

Reflect the result

Instructions to test the bits individually

<u>Instruction</u>	<u>Will branch if...</u>
<b>bneg label</b>	<b>N=1</b>
<b>bpos label</b>	<b>N=0</b>
<b>bz label</b>	<b>Z=1</b>
<b>bnz label</b>	<b>Z=0</b>
<b>bvs label</b>	<b>V=1</b>
<b>bvc label</b>	<b>V=0</b>
<b>bcs label</b>	<b>C=1</b>
<b>bcc label</b>	<b>C=0</b>

The Delay Slot**Due to pipelining...****All branch instructions take 1 extra instruction to go into effect**

*The instruction following the branch is executed  
before the branch happens!!!*

## The Delay Slot

### Due to pipelining...

**All branch instructions take 1 extra instruction to go into effect**

*The instruction following the branch is executed before the branch happens!!!*

Option 1: Put a “nop” instruction in the “delay slot”

```

cmp    %13,73
bl     elseLabel
nop

```

## The Delay Slot

### Due to pipelining...

**All branch instructions take 1 extra instruction to go into effect**

*The instruction following the branch is executed before the branch happens!!!*

Option 1: Put a “nop” instruction in the “delay slot”

```

cmp    %13,73
bl     elseLabel
nop

```

Very tricky to do correctly!

Option 2: Figure out how to put a real, useful instruction in the “delay slot”.

```

ld     myVar,%13      ! var = var - 1
sub    %13,1,%13     ! .
st     %13,myVar      ! .
cmp    %13,73        ! if var < 73
bl     elseLabel     ! . goto elseLabel
nop

```

## The Delay Slot

### Due to pipelining...

**All branch instructions take 1 extra instruction to go into effect**

*The instruction following the branch is executed before the branch happens!!!*

**Option 1:** Put a “nop” instruction in the “delay slot”

```

cmp    %13,73
b1     elseLabel
nop

```

*Very tricky to do correctly!*

**Option 2:** Figure out how to put a real, useful instruction in the “delay slot”.

```

ld     myVar,%13      ! var = var - 1
sub    %13,1,%13     ! .

cmp    %13,73        ! if var < 73
b1     elseLabel     ! . goto elseLabel
st     %13,myVar     ! . (delay)

```

- Figuring out how to rearrange the code to fill the delay slot is difficult & error-prone
- Study Chapter 2 (in “Paul”) for examples.
- Project 7:
  - You can practice filling the delay slots
  - Get the program right first!!!
- Our Compiler
  - Will not make this important optimization.
- See how smart the “C” compiler is.

### Optimizing Assembly Code

A typical loop:

```
while x1 <= 17 do
  x1 = x1 + x2;
  x3 = x3 + 1;
end
```

Assume variables in registers:

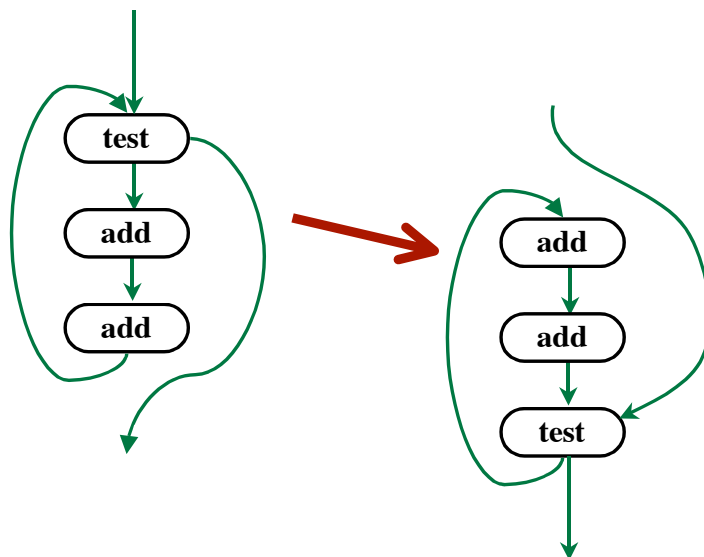
```
x1 => %11
x2 => %12
x3 => %13
```

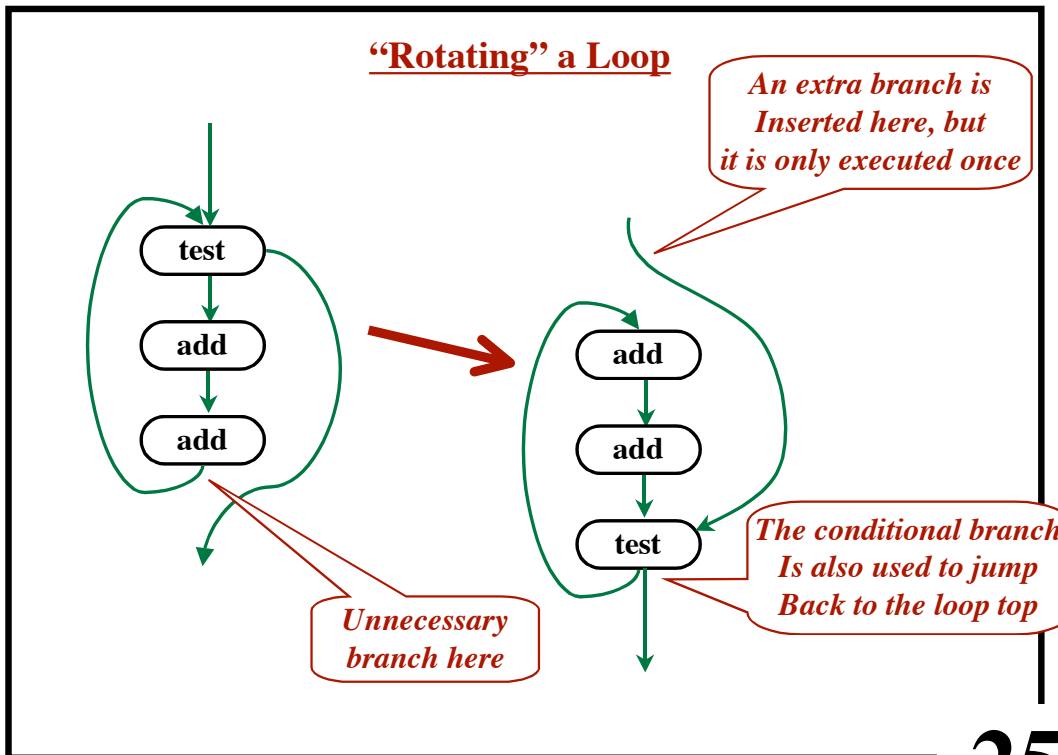
Translation into SPARC:

```
test:
  cmp    %11,17
  bg     done
  nop
  add    %11,%12,%11
  add    %13,1,%13
  ba     test
  nop
done:
```

*Execution Time:  
N\*7*

### “Rotating” a Loop





### Optimizing Assembly Code

A typical loop:

```

while x1 <= 17 do
  x1 = x1 + x2;
  x3 = x3 + 1;
end
    
```

Assume variables in registers:

```

x1 => %11
x2 => %12
x3 => %13
    
```

Translation into SPARC:

```

test:
  cmp    %11,17
  bg     done
  nop
  add    %11,%12,%11
  add    %13,1,%13
  ba     test
  nop
done:
    
```

*Execution Time:*  
 $N*7$

### Optimizing Assembly Code

A typical loop:

```

while x1 <= 17 do
  x1 = x1 + x2;
  x3 = x3 + 1;
end
    
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Assume variables in registers:

```

x1 => %11
x2 => %12
x3 => %13
    
```

Translation into SPARC:

```

test:
  cmp    %11,17
  bg     done
  nop
  add    %11,%12,%11
  add    %13,1,%13
  ba     test
  nop
done:
    
```

```

ba     test
nop
loop:
  add    %11,%12,%11
  add    %13,1,%13
test:
  cmp    %11,17
  ble   loop
  nop
    
```

*Execution Time:  
N\*5*

### Optimizing Assembly Code

A typical loop:

```

while x1 <= 17 do
  x1 = x1 + x2;
  x3 = x3 + 1;
end
    
```

Assume variables in registers:

```

x1 => %11
x2 => %12
x3 => %13
    
```

Translation into SPARC:

```

ba     test
loop:
  cmp    %11,17
  add    %11,%12,%11
  add    %13,1,%13
  cmp    %11,17
test:
  ble   loop
  nop
    
```

```

ba     test
nop
loop:
  add    %11,%12,%11
  add    %13,1,%13
test:
  cmp    %11,17
  ble   loop
  nop
    
```

*Execution Time:  
N\*5  
(1 cycle saved, total)*

How to fill a delay slot

```

ble    target
nop
mul    ...
...
div
target: add    %10,%11,%12
sub    ...

```

*Copy the target instruction into the delay slot, and branch to 2nd instruction*

```

ble    target
add    %10,%11,%12
mul    ...
...
div
add    %10,%11,%12
target: sub    ...

```

How to fill a delay slot

```

ble    target
nop
mul    ...
...
div
target: add    %10,%11,%12
sub    ...

```

*Copy the target instruction into the delay slot, and branch to 2nd instruction*

```

ble    target
add    %10,%11,%12
mul    ...
...
div
add    %10,%11,%12
target: sub    ...

```

Problem:

*The "add" is executed even when the branch is NOT taken!*

Solution:

*"Annulled Branches"*

## Annulled Branches

### Assumption:

- Loops end with a conditional branch
- The branch is back to the loop-top
- Loops execute many times
- Goal: Speed up highly repetitive loops
- The branch is taken more often than not
- Goal: Optimize the “branch-is-taken” case

### Approach:

- Execute the delay instruction when branch is taken
- Add some support for the case when branch not taken  
May execute a little slower, but...

## Annulled Branches

One bit in conditional branch instructions

*The “annul” bit*

If the bit is “0” (The branch is not “annulled”)

The instruction in the delay slot is always executed.

**Syntax:**

**bge**      **label**

If the bit is “1” (The branch is “annulled”)

**Branch Taken**

Instruction in delay slot is executed

**Branch Not Taken**

Instruction in delay slot is NOT executed

**Syntax:**

**bge, a**      **label**



## Optimizing Assembly Code

### A typical loop:

```

while x1 <= 17 do
  x1 = x1 + x2;
  x3 = x3 + 1;
end

```

### Translation into SPARC:

```

      ba    test
      cmp   %11,17
loop:
      add   %11,%12,%11
      add   %13,1,%13
      cmp   %11,17
test:
      ble  loop
      nop

```

### Assume variables in registers:

```

x1 => %11
x2 => %12
x3 => %13

```

### Execution Time:

 $N*4$ 

```

      ba    test
      cmp   %11,17
loop:
      add   %13,1,%13
      cmp   %11,17
test:
      ble,a loop
      add   %11,%12,%11

```

## Pseudo-Ops

```

.byte    35      ! 0x23
.half    35      ! 0x0023
.word    35      ! 0x00000023

```

### The value can be specified many ways (hex, decimal, ascii, expressions,...)

```

.word    0x3a0f12d8
.half    (123+0x0F00)<<5
.byte    'a'

```

### A list of values may be used:

```

.word    25,78,0x44000000+'a'    ! fills 3 words

```

### Floating-Point values may be placed in memory:

```

.single  0r12.34    ! 4-byte floating point value
.double  0r+1234e-2 ! 8-byte floating-point value

```

### Labels will often be used:

```

myVar: .word    0xffffabcd

```

```
.ascii    "abcdef"
```

*Will initialize N bytes of storage, filling it with character data.*

*“C” strings are terminated with 0x00.*

```
.asciz    "abcdef"
```

*Will initialize N+1 bytes of storage, putting 0x00 after the final byte.*

```
.skip     3500
```

*Will skip 3500 bytes, leaving them uninitialized.*

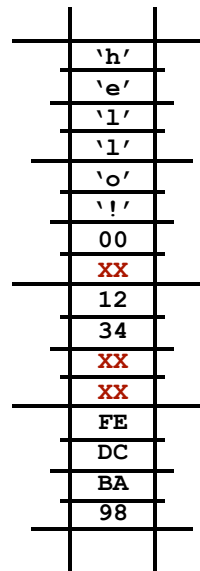
### The “align” Pseudo-Op

```
.align    2
.align    4
.align    8
```

*Will skip as many bytes as necessary to get onto the indicated alignment boundary.*

*Example:*

```
.asciz    "hello!"
.align    2
.half     0x1234
.align    4
.word     0xfedcba98
```



## Symbols

Each label is a symbolic name for an address

```

loop:  ...
      ...
      ba    loop
      nop

```

By default, each symbol is local to one “.s” file.

---

```

.global  symbol

```

Makes “symbol” available to the linker and debugger as an “external symbol”.

```

.global  main
main:   ...

```

To use an externally defined symbol, nothing special is needed.

```

call    printf

```

The assembler will not complain if “printf” is not defined in this .s file.

The linker will resolve the symbol.

If not defined in any .o file ⇒ Linker error: “unknown symbol”

## Segments (in Unix)

**.data** ← Put most data here  
Will be placed in read-write pages

**.text** ← Put code and constant data here  
Will be read-only pages

**.bss** ← Put uninitialized data here  
Read-write pages will be allocated

## Unix Commands

```
gcc myProg.s -c
```

Looks at the .s extension  
Calls assembler  
-c means produce a “.o” file

```
gcc myProg.o ...plus other .o files... -o myProg
```

Looks at the .o extensions  
Calls the linker  
“-o **xxx**” means produce an executable with name “xxx”

```
myProg
```

Loads the program into memory and executes it.

```
gcc -S samplePgm.c
```

To see what the “C” compiler produces.  
Creates “samplePgm.s”

## Integer Multiplication and Division

### No multiply or divide instructions in early versions of SPARC

Place operand 1 in %o0  
Place operand 2 in %o1  
Call a subroutine  
Find the result in %o0

#### Example:

```
ld    x,%o0      ! z = x * y
ld    y,%o1      ! .
call  .mul       ! .
nop                    ! .
st    %o0,z      ! .
```

Signed and Unsigned Versions

#### Available subroutines:

```
.mul }
.umul } %o0 x %o1 => %o0
.div  }
.udiv }
.rem  } %o0 + %o1 => %o0
.urem }
```

**Loading / Storing / Moving**

```
ld    address, regD
st    reg1, address
mov   reg1, regD
```

} *Data always moves to the left*

These each move one word (32 bits).  
 “reg” and “regD” may be any integer register.

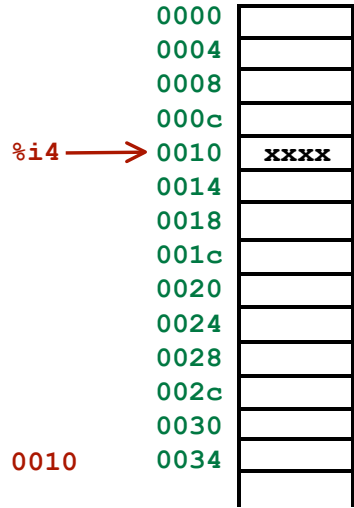
Address

- [reg]
- [reg+offset]
- [reg+reg]

Examples

```
ld    [%i4], %i6
```

*%i4 = 0010*



**Loading / Storing / Moving**

```
ld    address, regD
st    reg1, address
mov   reg1, regD
```

} *Data always moves to the left*

These each move one word (32 bits).  
 “reg” and “regD” may be any integer register.

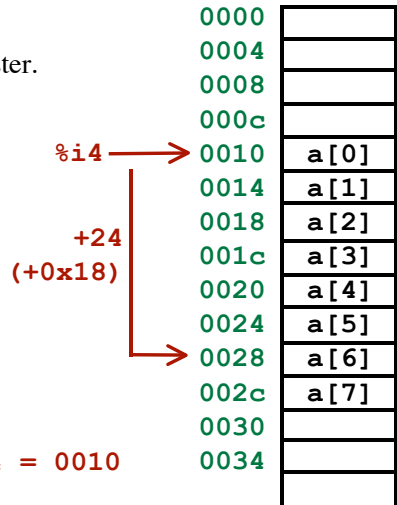
Address

- [reg]
- [reg+offset]
- [reg+reg]

Examples

```
ld    [%i4], %i6
ld    [%i4+24], %i6
```

*%i4 = 0010*



*A constant 13-bit value*

Loading / Storing / Moving

```
ld    address, regD
st    reg1, address
mov   reg1, regD
```

} *Data always moves to the left*

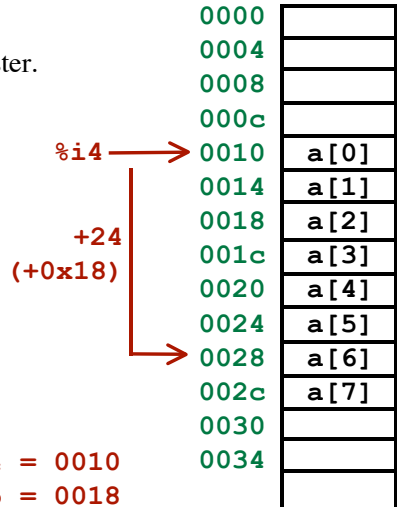
These each move one word (32 bits).  
 “reg” and “regD” may be any integer register.

Address

```
[reg]
[reg+offset]
[reg+reg]
```

Examples

```
ld    [%i4], %i6
ld    [%i4+24], %i6
ld    [%i4+%i5], %i6
```



```
%i4 = 0010
%i5 = 0018
```

%g0

Special register: %g0

Reading from it?  
 Always zero

Writing to it?  
 Data is discarded

### Synthetic Instructions

`mov reg_or_immed, regD`

*Programmer codes this*



`or %g0, reg_or_immed, regD`

*Assembler produces this*



`not reg1, regD`



`xnor reg1, %g0, regD`



`cmp reg1, reg2_or_immed`



`subcc reg1, reg2_or_immed, %g0`

### Loading Immediate Data into a Register

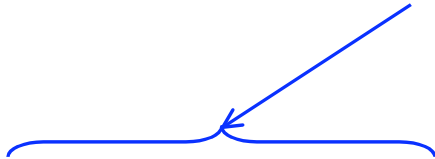
Option 1:

`mov reg_or_immed, regD`

The immediate value will be encoded in 13 bits.  
 ... And sign-extended to to 32-bits when used.  
 The range:  
 -4096 .. 4095

-----1 0000 0101 0111

1111 1111 1111 1111 1111 0000 0101 0111



The “sethi” Instruction

```
sethi    immed_22, regD
```

A 22-bit value included in instruction

Loaded into the high-order (most significant) 22 bits of regD

The low-order 10 bits are cleared (to zero)

Built-in macros in the assembler

```
%hi ( X )
```

Returns the high-order 22 bits of X

```
%lo ( X )
```

Returns the low-order 10 bits of X

Option 2:

```
sethi    %hi (value) , regD
```

```
or       regD, %lo (value) , regD
```

The “set” Synthetic InstructionOption 3:

```
set      value, regD
```

Any 32-bit value

Expands into two instructions

```
sethi    %hi (value) , regD
```

```
or       regD, %lo (value) , regD
```

Example:

```
set      myVar, %14
ld       [%14], %15
```



### The “set” Synthetic Instruction

Option 3:

set            value, regD

Any 32-bit value  
Expands into two instructions

sethi        %hi(value), regD  
or            regD, %lo(value), regD

Example:

```
set   myVar, %14
ld    [%14], %15
```

The Delay Slot

```
cmp     ...
ble     loopLabel
add     ...
sub     ...
```

The “delay slot”

Do not put “set” in the delay slot.

Actually, for some values, “set” will expand to only one instruction.  
Still, do not put “set” in the delay slot.

### Synthetic Instructions

Shorthand

What Gets Assembled

tst	reg	orcc	reg, %g0, %g0
clr	regD	or	%g0, %g0, regD
btst	reg_or_immed, reg	andcc	reg, reg_or_immed, %g0
bset	reg_or_immed, regD	or	regD, reg_or_immed, regD
bclr	reg_or_immed, regD	andn	regD, reg_or_immed, regD
btog	reg_or_immed, regD	xor	regD, reg_or_immed, regD
mov	reg_or_immed, regD	or	%g0, reg_or_immed, regD
not	reg1, regD	xnor	reg1, %g0, regD
cmp	reg1, reg2_or_immed	subcc	reg1, reg2_or_immed, %g0
nop		sethi	0, %g0

Mask, with selected bits set to 1

## Registers

### *Four groups of 8 registers each*

Global	%g__
Local	%l__
In	%i__
Out	%o__

### Local %l0, %l1, %l2, ... %l7

Used by this routine any way it wants

Will be saved automatically during subroutine calls

### Global %g0, %g1, %g2, ... %g7

%g0 is special (= zero), can not be modified

Used for “global” data, visible to all routines

Not saved during subroutine calls

### In %i0, %i1, %i2, ... %i7

### Out %o0, %o1, %o2, ... %o7

Used in passing parameters to/from subroutines.

The “Calling Conventions”

Efficient parameter passing

## SPARC Calling Conventions

Consider calling a subroutine

The “*caller*” calls the “*callee*”.

From the perspective of the current routine...

### “In” Registers

Arguments to this routine are found in

%i0,	%i1,	%i2,	...	%i5
↑	↑	↑	...	↑
arg1	arg2	arg3	...	arg6

Fewer than 6 arguments? Use only as many as needed.

Additional arguments? Must be passed on the stack.

This routine will put the “returned value” into %i0 before returning (if any)

### %i6

Has a special name: %fp (the “frame pointer”)

### %i7

Has a special use

Holds a pointer to the “call” instruction which called this routine

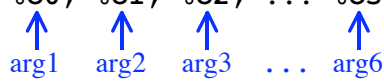
Will be used by the “return” instruction

## SPARC Calling Conventions

### “Out” Registers

Used to pass arguments to routines we will call.

Just before the “call”, arguments to the subroutine are put into

$\%o0, \%o1, \%o2, \dots \%o5$   


Fewer than 6 arguments? Use only as many as needed.

Additional arguments? Must be passed on the stack.

If the callee returns a value...

This routine will find it in  $\%o0$

### $\%o6$

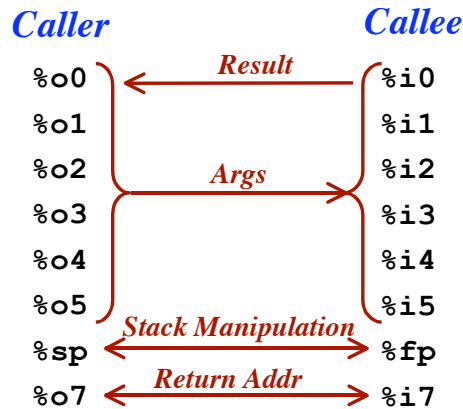
Has a special name:  $\%sp$  (the “stack pointer”)

### $\%o7$

Has a special use

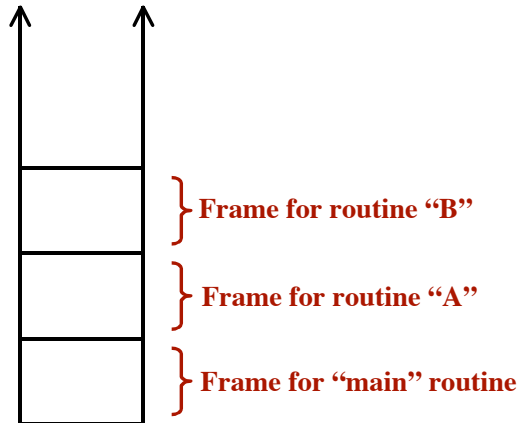
When a “call” instruction is executed...

the address of the “call” instruction will be placed in  $\%o7$



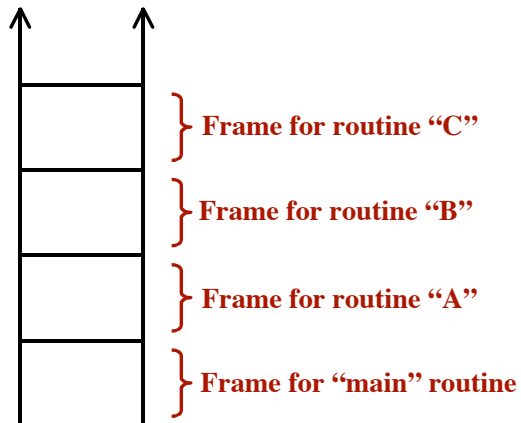
### Subroutine Calling Stack

Local variables for each routine...  
kept in the stack frame  
(Also called “activation record”)  
The stack of frames is located in main memory



### Subroutine Calling Stack

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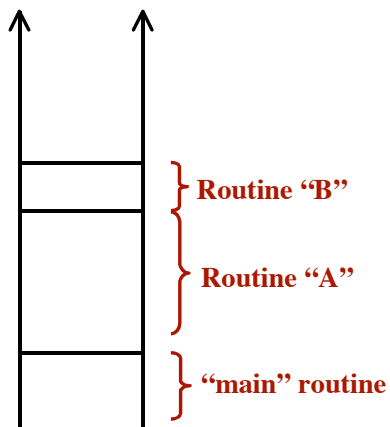
### The SPARC Idea

Goal:

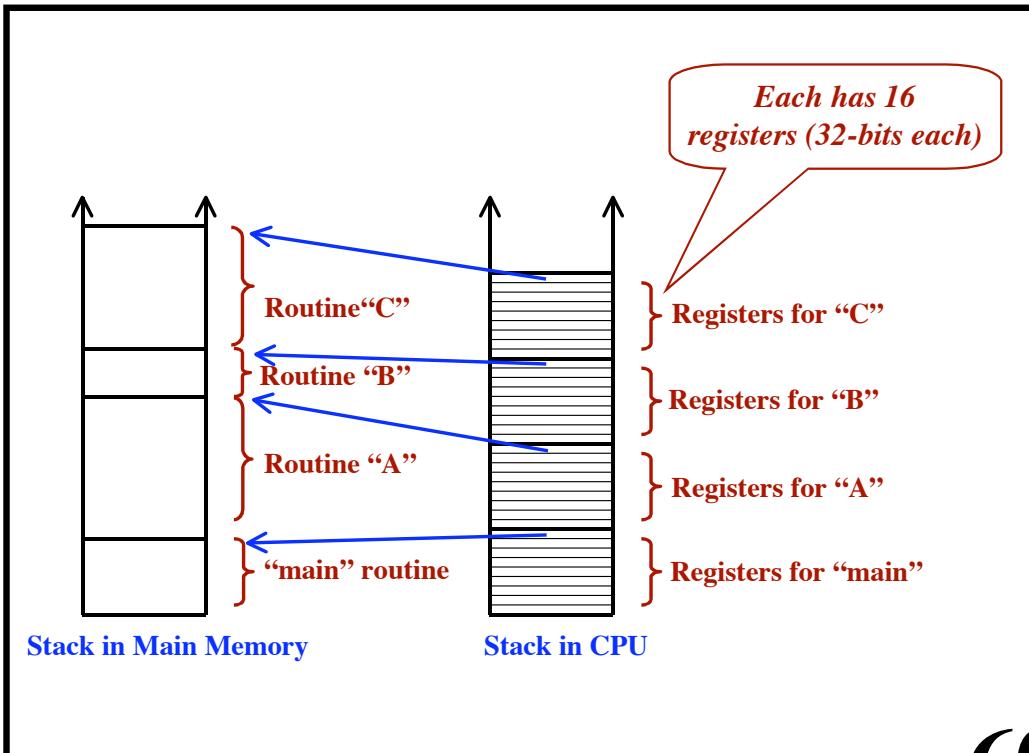
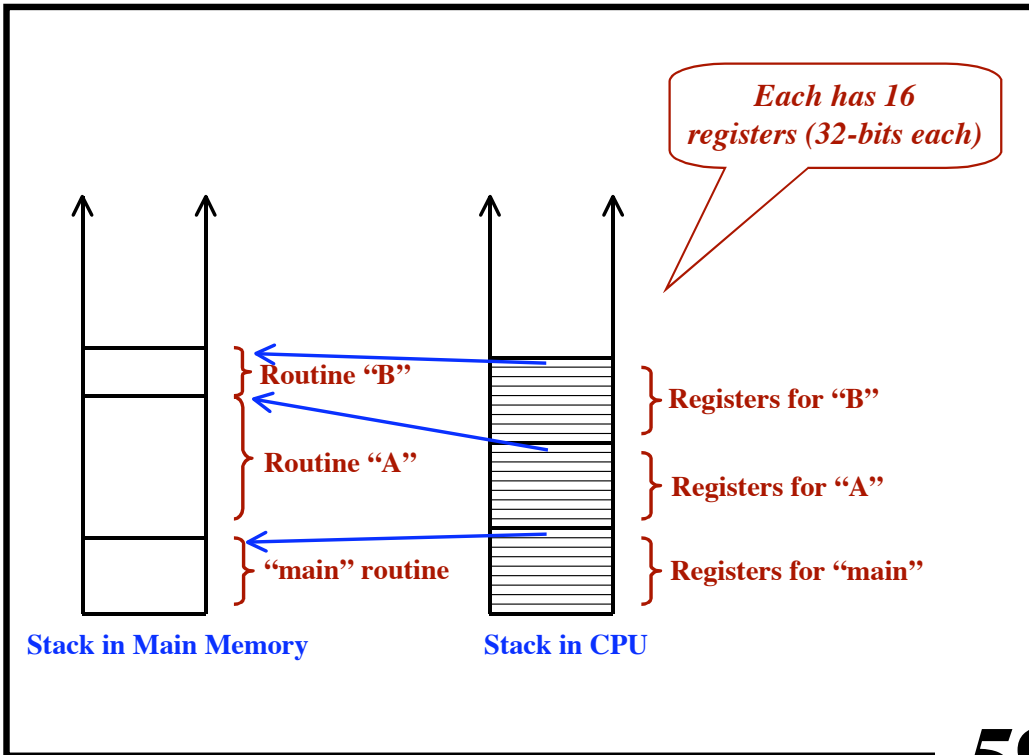
- Fast subroutine calling
- Keep the calling stack in registers
  - But each frame has a different size...

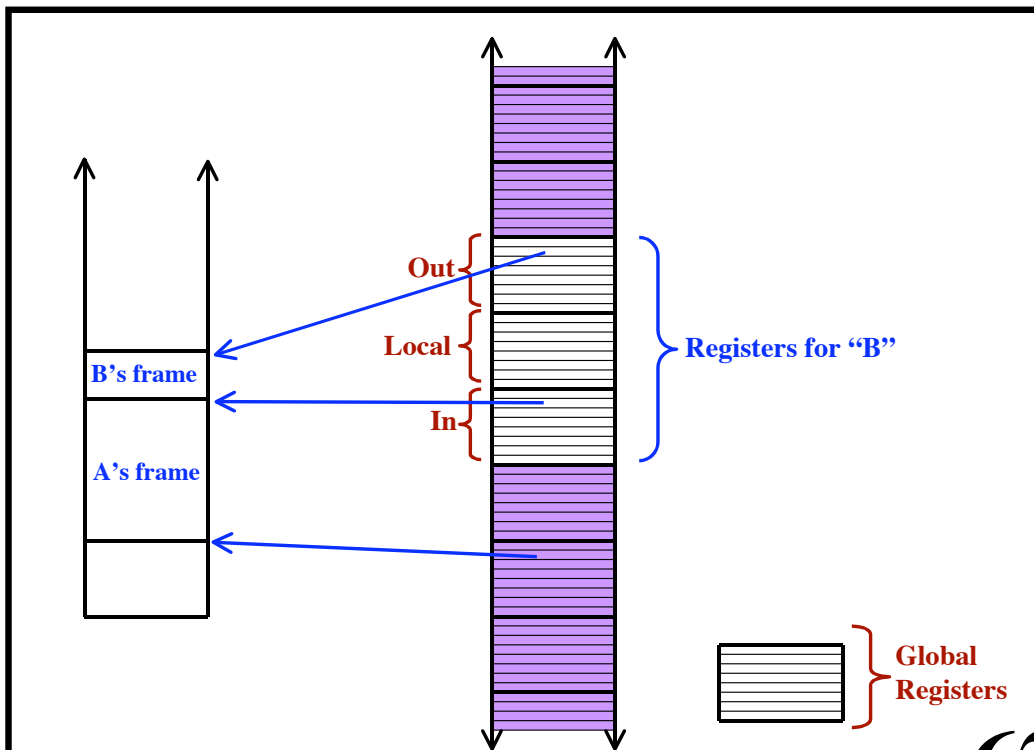
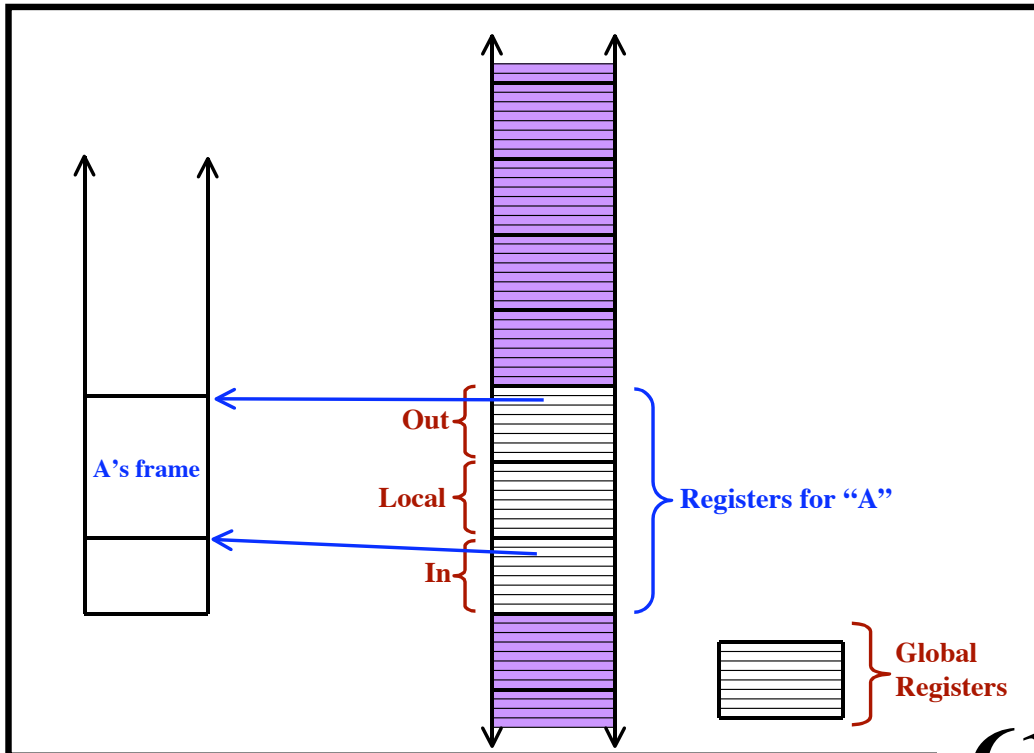
Idea:

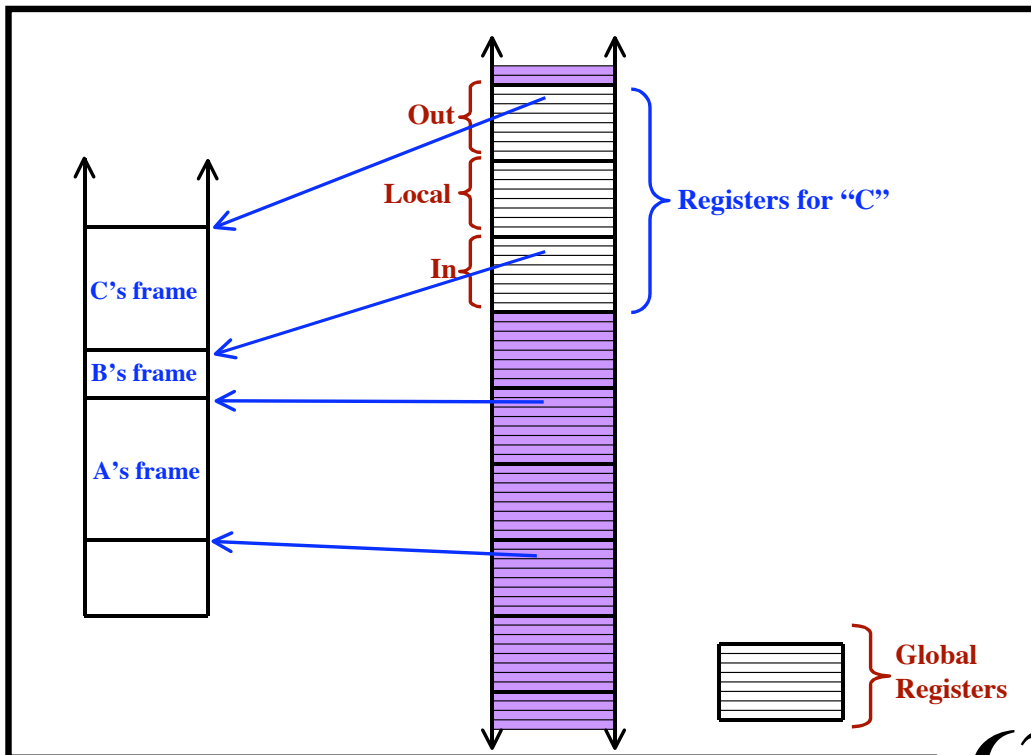
- Cache part of the frame in registers
- Create a stack of frames in the CPU
  - Avoid main memory most of the time!!!



Stack in Main Memory







- Lots of on-chip registers
- Each routine gets a new set of 16 registers  
Access to stack (i.e., to main memory) is reduced
- Arguments can be passed in registers  
(Most of the time)
- Return addresses are stored in registers (on-chip)
- Relevant instructions  
`call`  
`ret`  
`save`  
`restore`

These instructions  
manipulate the  
register stack

<i>Typical Usage</i>	
...	
<code>call</code>	<code>foo</code>
...	
<code>foo:</code>	
<code>save</code>	...
...	
<code>restore</code>	...
<code>ret</code>	