SiliconGraphics
Computer Systems

SGI Digital Video

Specification
(Version 1.1)

August 18, 1995

SILICON STUDIO™

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Revision History

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Unnumbered (1.0)	Original Issue	October 1, 1993
1.1	Added description of Indy Video (34 pin) Digital Video connector	August 18, 1995

SGI Digital Video Specification

This document defines the electrical specifications of the SGI Digital Video standard and the mechanical interface to the digital video port. This interface is used for transporting digital video information either into or out of Silicon Graphics machines. There are currently three implementations of this interface. Two of them are external connections to SGI products - an input only implementation as used by the IndyCam digital camera on the Indy workstation, and an input/output implementation as found on the Galileo, Indy Video, Indigo^2 video add-in products and the Cosmo Compress Motion JPEG compression card. The third implementation is the internal connection used to connect the Indy Video and Cosmo Compress boards together. This specification covers all three of these variations.

General Description

SGI Digital Video provides an interface for moving digital video information into and/or out of a Silicon Graphics workstation. The full implementation provides two digital ports - one, an input only port, and the other capable of either input or output (but not simultaneously). The interface also provides an I^{2}C interface for controlling external devices. The IndyCam port on the Indy workstation only provides the ability to input digital video data. Figure 1 shows a diagram of the interface.

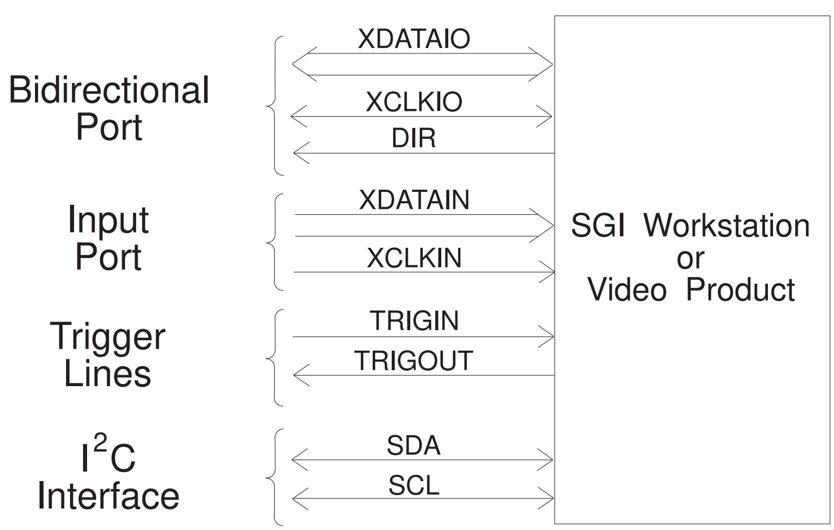

Figure 1 SGI Digital Video Interface

The SGI Digital Video interface is nearly identical to that specified in the definition of the CCIR 601 Digital Video Specification. There are two differences between the CCIR 601 interface and the Digital Video Port. The first exception is that the data lines in the SGI Digital Video interface are implemented as single-ended TTL level signals rather than differential ECL signals. The second exception is that not all of the systems or products with SGI Digital Video connections support pixel sampling at 13.5 MHz as specified by CCIR 601. These systems may only be capable of supporting square pixel sampling. This is discussed more completely in *Digital Video Sampling on page 7*.

Mechanically, the connection to SGI Digital Video port is made via a 60 pin high density connector or a 34 pin high density flat cable type connector. This connector may be included as part of the workstation system (Indy, for example) or may be included as part of an add-in option board (Galileo, for example).

SGI Digital Video Signals

The SGI Digital Video interface consists of two 8 bit (per component) video ports and associated clocks, a signal that defines the direction of data for the bidirectional port, trigger in and trigger out signals, and data and clock signals for the I^2C interface bus. Table 1 shows a listing of these signal groups. A definition of each of the signals follows.

Table 1 SGI Digital Video Signals

Signal(s)	Description
XDATAIO.[0-7]	Bidirectional Port Video Data Lines
SPARE[AB]IO	Additional I/O Data Lines (reserved)
$\overline{\text{XCLKIO}}$	Bidirectional Port Clock
DIR_SEND/_REC	Bidirectional Port Direction
XDATAIN.[0-7]	Input Port Video Data Lines
SPARE[AB]IN	Additional Input Data Lines (reserved)
$\overline{\text{XCLKIN}}$	Input Port Clock
$\overline{\text{TRIGIN}}$	Trigger Input
$\overline{\text{TRIGOUT}}$	Trigger Output
SDA_SEND/_REC	I^2C Data
SCL_SEND/_REC	I^2C Clock
+12V_SEND/_REC	+ 12 Volt output/input
+5V_SEND/_REC	+ 5 Volt output/input
-12V_SEND/_REC	- 12 Volt output/input

XDATAIO.[0-7]: These 8 data lines contain the video data that is either going into, or coming out of the Silicon Graphics Video port. For each of the signals there is a corresponding return line with the suffix "_RET". The signal and it's return line should be implemented as coax pairs to minimize interference. Data on these lines are at TTL levels. Signal XDATAIO.7 is the Most Significant Bit.

SPARE[AB]IO: These two signals are intended for future expansion. They are currently unused. They should not be used for the present time, but for forward compatibility, cables should include these connections. Each of the signals has a corresponding return line with the suffix "_RET". See *SGI Digital Video Cable Connections* for more information on the cable connections.

$\overline{\mathrm{XCLKIO}}$: This signal is used to clock in (or out) the data on the bidirectional port. Depending on the state of the DIR signal, the clock should be provided by the external device in the case of input, or is provided by the system in the case of output. This clock signal has it's own return line, $\overline{\mathrm{XCLKIO\_RET}}$.

DIR_SEND/_REC: DIR_SEND is an output signal from the port defining the direction of data for the bidirectional port. When this signal is 0 the port is an input port. When it is 1, the port is configured as an output port. DIR_REC is the signal connection used to receive the DIR_SEND signal at an external device. This signal default state is “0”, or input.

XDATAIN.[0-7]: These 8 data lines contain the video data that is going into the input port. This port does not support data output. As with the XDATAIO signals, each of these signals has its corresponding return line, denoted by the “_RET” suffix. Signal XDATAIN.7 is the Most Significant Bit.

SPARE[AB]IN: These two signals are intended for future expansion. They are currently unused. They should not be used for the present time, but for forward compatibility, cables should include these connections. Each of the signals has a corresponding return line with the suffix “_RET”. See *SGI Digital Video Cable Connections* for more information on the cable connections.

$\overline{\mathrm{XCLKIN}}$: This signal is used to clock data into the input port. This clock signal has it's own return line, $\overline{\mathrm{XCLKIN\_RET}}$.

$\overline{\mathrm{TRIGIN}}$: This input signal is polled by the CPU and can be used to signal an event or trigger some action on the part of the system. The signal is a TTL signal and is active low.

$\overline{\mathrm{TRIGOUT}}$: This output signal can be used to trigger an external device to take some action. It is a TTL level signal and is active low.

SDA_SEND/_REC: This is the data for the I^{2}C bus. The SDA_REC connection should be used at the external device for connecting to the SDA_SEND signal. See *SGI Digital Video Cable Connections* for more information.

SCL_SEND/_REC: This is the clock for the I^{2}C bus. The SCL_REC connection should be used at the external device for connecting to the SCL_SEND signal. See *SGI Digital Video Cable Connections* for more information.

+12V_SEND/_REC: This is a +12 Volt supply used for the IndyCam. Output capacity is limited to 100 mA. This signal (and the other two supply signals) support the power requirements of the IndyCam only. This signal is not for use by any other external device.

+5V_SEND/_REC: This is a + 5 Volt supply used for the IndyCam. Output capacity is limited to 100 mA. This signal (and the other two supply signals) support the power requirements of the IndyCam only. This signal is not for use by any other external device.

-12V_SEND/_REC: This is a - 12 Volt supply used for the IndyCam. Output capacity is limited to 100 mA. This signal (and the other two supply signals) support the power requirements of the IndyCam only. This signal is not for use by any other external device.

SGI Digital Video - Electrical

The electrical characteristics of the SGI Digital Video signals are shown in Table 2. One key difference between the signals available with the 60 pin connector and those available on the internal 34 pin connector is that the signals on the 60 pin connector have been buffered and have EMI filtering. This is the usual practice for any signal going into or out of the machine. The signals available on the 34 pin connector are not buffered and do not have any EMI filtering.

Table 2 SGI Digital Video Signal Electrical Characteristics

Signal(s)	Interface Characteristics	
	Levels	Timing
XDATIO.[0-9]	TTL	See SMPTE RP 125-1984
$\overline{\text{XCLKIO}}$		
DIR		Static
XDATIN.[0-9]		See SMPTE RP 125-1984
$\overline{\text{XCLKIN}}$		
$\overline{\text{TRIGIN}}$		Asynchronous
$\overline{\text{TRIGOUT}}$		
SDA	See the I^2C Interface Specification	
SCL		

Timing

The XDATAIO, XCLKIO, XDATAIN and XCLKIN signals conform to the timing requirements as stated in the SMPTE Recommended Practice 125-1984. The SDA and SCL signals conform to the timing requirements as set out in the I^2C Interface specification (see the Phillips Semiconductors *Desktop Video Data Handbook* for this specification).

The $\overline{\text{TRIGIN}}$ and $\overline{\text{TRIGOUT}}$ signals are asynchronous with respect to the other signals on this interface.

The DIR signal is not meant to be a dynamic signal. It is meant purely as an indication of the direction of signal flow. This signal defaults to an input status.

Terminations

The IndyCam port found on Indy and the SGI Digital Video port found on Indigo and Indigo^2 differ slightly in their termination schemes. The IndyCam port is a high impedance input suitable for a series termination of 33 Ω at the source. The SGI Digital Video port lines are terminated with a series R-C network from the line to ground. The values of the R and C are 120 Ω and 0.001 µF. If a device will only drive the IndyCam input port and not be expected to receive any data, the signals can be source-terminated by using a series resistor with a value of 33 Ω. This style of termination is designed specifically for IndyCam and is not intended for long (> 4 feet) cables. However, if the device is expected to both send and receive data, then the lines should use the series R-C termination scheme as mentioned above.

Pin #	Signal Name	I/O
1	XDATAIO.0	I/O
2	XDATAIO.0_RET	I/O
3	XDATAIO.1	I/O
4	XDATAIO.1_RET	I/O
5	XDATAIO.2	I/O
6	XDATAIO.2_RET	I/O
7	SDA_SEND	O
8	DIR_SEND	O
9	SCL_SEND	O
10	$\overline{\text{TRIGIN\_RET}}$	I
11	$\overline{\text{TRIGIN}}$	I
12	$\overline{\text{XCLKIN\_RET}}$	I
13	$\overline{\text{XCLKIN}}$	I
14	*SPAREBIN_RET*	I
15	*SPAREBIN*	I
16	XDATAIO.3	I/O
17	XDATAIO.3_RET	I/O
18	XDATAIO.4	I/O
19	XDATAIO.4_RET	I/O
20	XDATAIO.5	I/O
21	XDATAIO.5_RET	I/O
22	+12V_SEND	O
23	+5V_SEND	O
24	-12V_SEND	O
25	*SPAREAIN_RET*	I
26	*SPAREAIN*	I
27	XDATAIN.7_RET	I
28	XDATAIN.7	I
29	XDATAIN.6_RET	I
30	XDATAIN.6	I
31	XDATAIN.3	I
32	XDATAIN.3_RET	I
33	XDATAIN.4	I
34	XDATAIN.4_RET	I
35	XDATAIN.5	I
36	XDATAIN.5_RET	I
37	+12V_REC	I
38	+5V_REC	I
39	-12V_REC	I
40	*SPAREAIO_RET*	I/O
41	*SPAREAIO*	I/O
42	XDATAIO.7_RET	I/O
43	XDATAIO.7	I/O
44	XDATAIO.6_RET	I/O
45	XDATAIO.6	I/O
46	XDATAIN.0	I
47	XDATAIN.0_RET	I
48	XDATAIN.1	I
49	XDATAIN.1_RET	I
50	XDATAIN.2	I
51	XDATAIN.2_RET	I
52	SDA_REC	I
53	DIR_REC	I
54	SCL_REC	I
55	$\overline{\text{TRIGOUT\_RET}}$	O
56	$\overline{\text{TRIGOUT}}$	O
57	$\overline{\text{XCLKIO\_RET}}$	I/O
58	$\overline{\text{XCLKIO}}$	I/O
59	*SPAREBIO_RET*	I/O
60	*SPAREBIO*	I/O

Table 3 SGI Digital Video Connector Pin Assignments (External)

Pin #	Signal Name	I/O
1	Ground	-
2	XDATAIN.0	I
3	XDATAIN.1	I
4	XDATAIN.2	I
5	XDATAIN.3	I
6	Ground	-
7	XDATAIN.4	I
8	XDATAIN.5	I
9	XDATAIN.6	I
10	XDATAIN.7	I
11	Ground	-
12	XCLKIN	I
13	Vcc (+5 Volts)	O
14	XDATAIO.0	I/O
15	XDATAIO.1	I/O
16	XDATAIO.2	I/O
17	XDATAIO.3	I/O

Pin #	Signal Name	I/O
18	Ground	-
19	XDATAIO.4	I/O
20	XDATAIO.5	I/O
21	XDATAIO.6	I/O
22	XDATAIO.7	I/O
23	Ground	-
24	XCLKIO	I/O
25	Vcc (+5 Volts)	O
26	DIR_SEND	O
27	+12 Volts	O
28	SCL	O
29	Vcc (+5 Volts)	O
30	SDA	O
31	Ground	-
32	XTRIGIN_N	I
33	-12 Volts	O
34	XTRIGOUT_N	O

Table 4 SGI Digital Video Connector Pin Assignments (External)

SGI Digital Video Connector Pin Assignment

External Connection

Table 3 defines the pinout used for the SGI Digital Video connector. This connector is a 60 pin high density connector. It has four rows of 15 contacts each. Figure 2 shows this connector and its numbering scheme. Only those signals that are shown shaded are available at the IndyCam port. While the ninth and tenth data bits are currently not used, their pins are assigned. These signal names are shown in italics. The connector is a female Molex LFH type (Molex P/N 70928-2002) or equivalent.

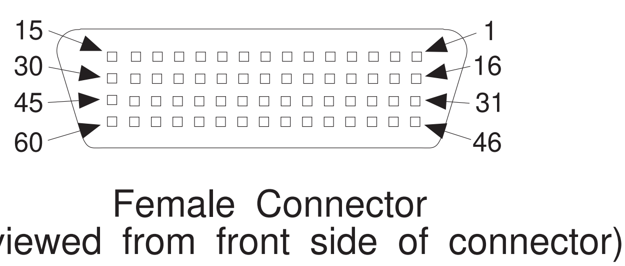

Figure 2 SGI Digital Video Connector Numbering

Internal Connection (to Indy Video)

Table 4 defines the pinout used for connecting to the Indy Video card. This connector is a 34 pin high density connector. It has two rows of 17 pins and is designed to interface to a flat cable connector. Figure 3 shows this connector and its pin numbering scheme. The part numbers of the mating connectors and flat cable are shown in Table 5 below.

Part	Manufacturer	Manufacturer's Part Number
PC Board Connector	AMP	1-104068-3
Flat Cable Connector	AMP	4-57013-9
Flat Cable	AMP	111196-8

Table 5 Internal Connection Parts

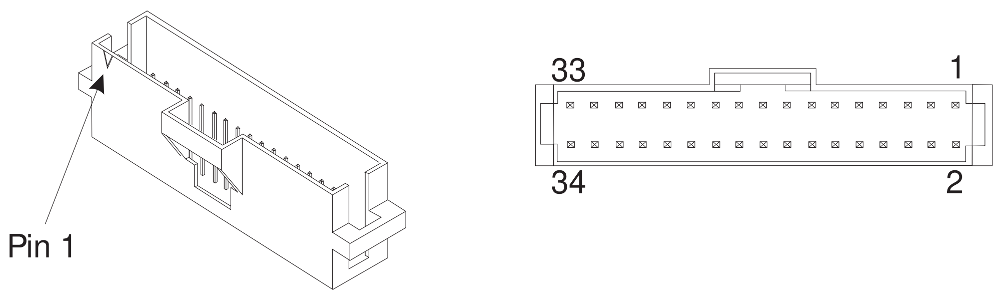

Figure 3 Indy Video Connector

Digital Video Sampling

CCIR Recommendation 601 regarding Digital Video states that pixel sampling will be done at 13.5 MHz. Not all the Silicon Graphics systems or options support this capability. For example, the IndyCam port on the Indy workstation supports only square pixel sampling at either 12.2727 MHz for NTSC, or 14.750 MHz for PAL. Other products, such as the Galileo product for Indigo^2, support both square pixel sampling and fully compliant 601 sampling at 13.50 MHz. In the case of products that support both sampling methods, the sampling method is determined by a software call. The table below shows the sampling method supported by each Silicon Graphics product with an SGI Digital Video port.

Table 6 Video Sampling Support

	CCIR 601 Sampling	Square Pixel
IndyCam Input		X
Indy Video		X
Galileo for Indigo	X	X
Galileo for Indigo^2	X	X

Digital Video Format Overview

From a format point of view, the SGI Digital Video format is identical to CCIR 601. The data coming out or going into the SGI Digital Video port is a stream of multiplexed luminance and chrominance values plus timing information. This video is of the 4:2:2 format. Video data for any active video line follows the form:

U0Y0V0 Y1 U2Y2V2 Y3 U4Y4V4 Y5 U6Y6V6 Y7 ......UnYnVn

where U0Y0V0 are co-sited spatially.

CCIR Recommendation 601 specifies that each active line of video contains 1440 samples - 720 luminance samples and 360 samples of each color-difference signal. As mentioned above, the sample rate for this method is 13.5 MHz. The number of samples per line is the same for both NTSC and PAL type systems. The difference between the two is the number of samples that are outside the active line (i.e. in the blanking area).

In systems that sample at a rate other than the 13.5 MHz required by CCIR 601, the number of total samples and the number of samples in the active and blanking periods is different. The table below shows these values.

Table 7 Sampling Rates and Samples

Sampling Method	Sample Frequency	Samples (per line)			Lines	
		Total	Active line	Blanking	Total	Active
CCIR 601 - NTSC	13.5 MHz	1716	1440	276	525	487
CCIR 601 - PAL	13.5 MHz	1728	1440	288	625	576
Square Pixel - NTSC	12.27 MHz	1560	1280	280	525	487
Square Pixel - PAL	14.75 MHz	1888	1536	352	625	576

Valid values for the luminance component are 16_{10} (black) through 235_{10} (peak white). During the blanking period the luminance values transmitted are black (16_{10}). Luminance values received during the blanking period are ignored.

Valid values for the chrominance components are 16_{10} through 240_{10}. During the blanking period the chrominance values transmitted are 128_{10}. Chrominance values received during the blanking period are ignored.

The beginning and end of active video information is indicated by a three byte preamble and a byte containing field, horizontal and vertical timing information. The three-byte preamble is defined as FF 00 00 (in hex). The fourth byte contains timing information. This byte can be decoded as follows:

Table 8 Timing Byte Definition

Bit	Name	Meaning
7	-	Always set to 1
6	F	Field type - 0 = odd, 1 = even
5	V	V=1 during vertical blanking, changes when H=1 (EAV)
4	H	H=1 at end of active video (EAV), h=0 at beginning of video
3	P3	Hamming code error protection
2	P2	Hamming code error protection
1	P1	Hamming code error protection
0	P0	parity

The following table shows the values for the Hamming Code bits and parity bit for values of F, V, and H.

Table 9 Hamming Code and Parity Bits

Signal (Bit #)			Signal (Bit #)			
F (6)	V (5)	H (4)	P3 (3)	P2 (2)	P1 (1)	P0 (0)
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

This scheme protects the F, V and H bits and can correct a one bit error or detect a two bit error.

SGI Digital Video Cable Connections

Since the frequency of the multiplexed luminance and chrominance samples is 20 to 30 MHz and the density of pins on the connector is high, care needs to be taken in creating cables for connecting the SGI Digital Video port with other devices. Through our experiments, we have found that best results are obtained when using cables of 8 feet or less, with multiple 75Ω coax cables (minimum 34 AWG) bundled together surrounded by a braided shield. Twisted pair and flat ribbon cable do not work properly. For this reason, we recommend that the cable type specified in Table 8 be used. No currently available cable exists with the right combination of coaxes, braided shield and cover so custom cables are required. The cable specified in the table below is the individual coax that has been used for each signal in the prototypes we have had made. The connectors and backshells used for the cable and the connector for PCB mounting are also defined in this table.

Table 10: Digital Video Cable Components

Manufacturer	Description	Part Number
Tensolite	Coax Cable, 75Ω	32453/50275X-1(LD)
Molex	Connector, Male, Straight, 60 pin	70929-1001
Molex	Backshell	82007-0131
Molex	Connector, Female, Right Angle, 60 pin	70928-2002

Also important to the quality of the cable is the quality of the cable shields and their connection to the backshells. The shields should be connected to the backshell at both ends of the cable such that the connector housing of the SGI Digital Video port on the platform and the connector housing at the external device are connected by a low impedance path. This will result in lower EMI emissions and less probability that the signals in the cable will be effected by external equipment.

The SGI Digital Video port pinout has been defined so that cables for connecting the port with external devices can be made where there is no difference between the pin configuration at each end. This could be considered a “Null Modem” style cable. In other words, the cable ends can be swapped with no effect on function. An example of this kind of cable is shown in Figure 3. The wiring list for the cable shown in Figure 3 is shown in Table 9.

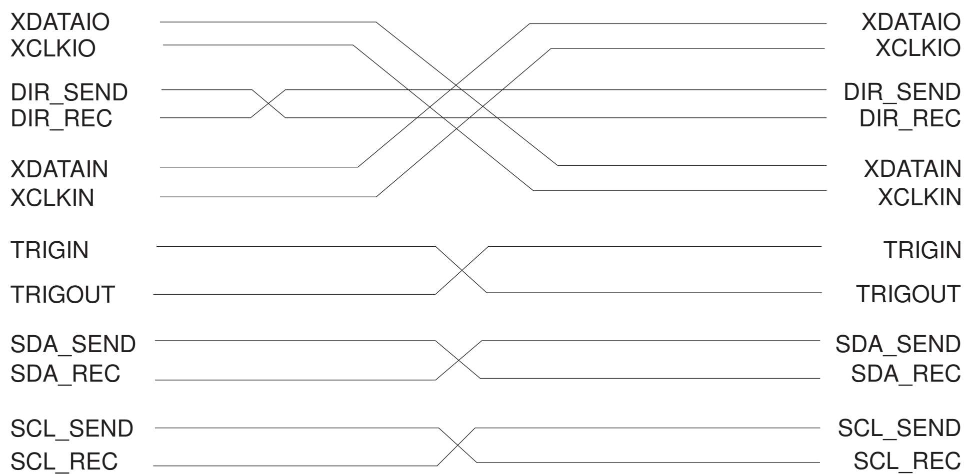

Figure 4 SGI Digital Video Cable

From		To	
Pin	Signal	Pin	Signal
1	XDATAIO.0	46	XDATAIN.0
2	XDATAIO.0_RET	47	XDATAIN.0_RET
3	XDATAIO.1	48	XDATAIN.1
4	XDATAIO.1_RET	49	XDATAIN.1_RET
5	XDATAIO.2	50	XDATAIN.2
6	XDATAIO.2_RET	51	XDATAIN.2_RET
7	SDA_SEND	52	SDA_REC
8	DIR_SEND	53	DIR_REC
9	SCL_SEND	54	SCL_REC
10	$\overline{\text{TRIGIN\_RET}}$	55	$\overline{\text{TRIGOUT\_RET}}$
11	$\overline{\text{TRIGIN}}$	56	$\overline{\text{TRIGOUT}}$
12	$\overline{\text{XCLKIN\_RET}}$	57	$\overline{\text{XCLKIO\_RET}}$
13	$\overline{\text{XCLKIN}}$	58	$\overline{\text{XCLKIO}}$
14	SPAREBIN_RET	59	SPAREBIO_RET
15	SPAREBIN	60	SPAREBIO
16	XDATAIO.3	31	XDATAIN.3
17	XDATAIO.3_RET	32	XDATAIN.3_RET
18	XDATAIO.4	33	XDATAIN.4
19	XDATAIO.4_RET	34	XDATAIN.4_RET
20	XDATAIO.5	35	XDATAIN.5
21	XDATAIO.5_RET	36	XDATAIN.5_RET
22	+12V_SEND	-	NC
23	+5V_SEND	-	NC
24	-12V_SEND	-	NC
25	SPAREAIN_RET	40	SPAREAIO_RET
26	SPAREAIN	41	SPAREAIO
27	XDATAIN.7_RET	42	XDATAIO.7_RET
28	XDATAIN.7	43	XDATAIO.7
29	XDATAIN.6_RET	44	XDATAIO.6_RET
30	XDATAIN.6	45	XDATAIO.6

From		To	
Pin	Signal	Pin	Signal
31	XDATAIN.3	16	XDATAIO.3
32	XDATAIN.3_RET	17	XDATAIO.3_RET
33	XDATAIN.4	18	XDATAIO.4
34	XDATAIN.4_RET	19	XDATAIO.4_RET
35	XDATAIN.5	20	XDATAIO.5
36	XDATAIN.5_RET	21	XDATAIO.5_RET
37	+12V_REC	-	NC
38	+5V_REC	-	NC
39	-12V_REC	-	NC
40	SPAREAIO_RET	25	SPAREAIN_RET
41	SPAREAIO	26	SPAREAIN
42	XDATAIO.7_RET	27	XDATAIN.7_RET
43	XDATAIO.7	28	XDATAIN.7
44	XDATAIO.6_RET	29	XDATAIN.6_RET
45	XDATAIO.6	30	XDATAIN.6
46	XDATAIN.0	1	XDATAIO.0
47	XDATAIN.0_RET	2	XDATAIO.0_RET
48	XDATAIN.1	3	XDATAIO.1
49	XDATAIN.1_RET	4	XDATAIO.1_RET
50	XDATAIN.2	5	XDATAIO.2
51	XDATAIN.2_RET	6	XDATAIO.2_RET
52	SDA_REC	7	SDA_SEND
53	DIR_REC	8	DIR_SEND
54	SCL_REC	9	SCL_SEND
55	$\overline{\text{TRIGOUT\_RET}}$	10	$\overline{\text{TRIGIN\_RET}}$
56	$\overline{\text{TRIGOUT}}$	11	$\overline{\text{TRIGIN}}$
57	$\overline{\text{XCLKIO\_RET}}$	12	$\overline{\text{XCLKIN\_RET}}$
58	$\overline{\text{XCLKIO}}$	13	$\overline{\text{XCLKIN}}$
59	SPAREBIO_RET	14	SPAREBIN_RET
60	SPAREBIO	15	SPAREBIN

Table 9: SGI Digital Video Cable Wiring List

I^2C Interface

I^2C is a very simple serial control protocol, developed by Phillips, that has found application in the SGI digital video standard. It is composed of two wires, a data line and a clock line.

A number of devices can share the bus typically with one master and a number of slaves. The protocol is described in detail in Phillips Semiconductors *Desktop Video Data Handbook*, but here are the basics of a simple interaction:

- When inactive, both the clock and data lines are pulled high by pull-up resistors in the system.
- An interaction is initiated by the master by transmitting a one byte word representing a slave station address. The LSB of this station address indicates if this device is to be written to or read from (0 for write, 1 for read)
- A start condition, at the beginning of a transaction, is indicated by the data line being pulled low before the clock goes low.
- Conversely, a stop condition is indicated by the data line being released high by the master after the clock is already high.
- A slave device acknowledges its own address by pulling the data bus low. At this point the master transmits a station sub-address, also a byte long, indicating which register in the device is to be accessed. Once again the slave pulls the bus low in acknowledgment.
- Finally the last 1 byte long word is the data that is being either received or transmitted.

It is imperative for there to be no duplicate station addresses for this scheme to work. Table10 is a listing of I^2C devices and their station addresses to preclude this possibility. Addresses used in SGI products are noted in the table. An SGI workstation may internally have a SAA7191 decoder, an SAA7199 encoder or a SAA7192 colorspace converter. Which parts are present depend on the product. These addresses should NOT be used. The IndyCam has a station address of 0x56. This address should also be avoided.

Table 10: Assigned I^2C Bus Addresses

Manufacturer	Part Number	Description	I^2C Address(es)*
Signetics	PCD3311/12	Tone generator DTMF/modem/musical	0x40 & 0x4A
	PCF8200	Voice synthesizer (male or female)	0x20
	PCF8566	96-segment LCD driver 1:1 - 1:4 Mux	0x7C & 0x7D
	PCF8568	LCD row driver for dot matrix displays	0x78 & 0x7A
	PCF8569	Column driver for dot matrix displays	0x78 & 0x7A
	PCF8570/71	256 x 8, 128 x 8 static RAM	0xA0 - 0xAE
	PCF8570C	256 x 8 static RAM	0xB0 - 0xBE
	PCF8573	Clock/calendar	0xD0 - 0xD6
Phillips	PCF8574	I^2C bus to 8-bit bus converter	0x40† - 0x4E
	PCF8574A	I^2C bus to 8-bit bus converter	0x70 - 0x7E
Signetics	PCF8576	160-segment LCD driver 1:1 - 1:4 Mux	0x70 & 0x72
	PCF8577	64-segment LCD driver 1:1 - 1:2 Mux	0x74
	PCF8577A	64-segment LCD driver 1:1 - 1:2 Mux	0x76
	PCF8578	Row/column LCD dot-matrix driver	0x78 & 0x7A
	PCF8579	Row/column LCD dot-matrix driver	0x78 & 0x7A
	PCF8581	128-byte EEPROM	0xA0 - 0xAE
	PCF8582	256 x 8 EEPROM	0xA0 - 0xAE
	PCF8583	256 x 8 RAM with clock/calendar	0xA0 & 0xA2
	PCF8591	4-channel, 8-bit A/D plus 8-bit D/A	0x90 - 0x9E
	PCF8594	512-byte EEPROM	0xA0 - 0xAE
	SAA1064	4-digit LED driver	0x70 - 0x76
	SAA1136	PCM-audio indent-word interface	0x3C
	SAA1300	5-bit high current driver	0x40 - 0x46
	SAA5243/45	Enhanced teletext circuit	0x22
Phillips	SAA5252	Closed caption decoder	0x28 & 0x29
	SAA7151B	Digital multi-standard color decoder with SCART inter-face	0x8A & 0x8E†
	SAA7152	Digital combination filter	0xB2
	SAA7194(7196)	Digital video decoder and scaler circuit (DESC)	0x40 & 0x42
	SAA7191B	S-VHS digital multi-standard decoder “square pixel”	0x8A† & 0x8E
	SAA7192A	Digital color space converter	0xE0† & 0xE2
	SAA7199	Digital encoder	0xB0†
Signetics	SAA9020	Field memory controller	0x28 - 0x2E
Phillips	SAA9051	DIgital multi-standard TV decoder	0x8A
Signetics	SAA9068	(PIPCO) Picture-in-picture controller	0x24 & 0x26
	SAB3035/36/37	(CITAC) CPU interface for tuning and control	0xC0 - 0xC6
	SAF1135	Data line decoder	0x20 - 0x26

Table 10: Assigned I^{2}C Bus Addresses

Manufacturer	Part Number	Description	I^{2}C Address(es)*
Phillips	TDA4670	Picture signal improvement circuit	0x88
	TDA4680/4686	Video processor	0x88
Signetics	TDA8421		
Phillips	TDA8440	Switch for CTV receivers	0x90 - 0x9E
	TDA8442	Interface for color decoders	0x88
	TDA8443	YUV/RGB interface circuit	0xD0 - 0xDE
	TDA8444	Octuple 6-bit DAC	0x40 - 0x4E (0x48†)
Signetics	TDA8461	PAL/NTSC color decoder	0x80 & 0x8A
Phillips	TDA9141	PAL/NTSC/SECAM decoder/sync processor	0x8A & 0x8E
Signetics	TEA6100	FM/IF and tuning interface	0xC2
	TEA6300/6310T	Sound fader control circuit	0x80
	TSA5511/12/14	PLL frequency synthesizer for TV	0xC0 - 0xC6
	TSA6057	Radio tuning PLL frequency synthesizer	0xC4 - 0xC6
	UMF1009	Frequency synthesizer	0xC0 - oxC6
SGI	-	IndyCam	0x56†

* Addresses specified are in the write mode.

† This is address used in Silicon Graphics video products

Bibliography

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Available from: National Technical Information Service
5285 Port Royal Road
Springfield, Virginia 22161
(703) 487-4600

Also found in: Desktop Video Data Handbook (pages 2-29 through 2-38) [see below]

North American Phillips Corporation, I^{2}C-bus Specification [Contained in: Desktop Video Data Handbook (pages 2-185 through 2-204)], 1993, North American Phillips Corporation

Society of Motion Picture and Television Engineers, SMPTE 125M - Television - Component Video Signal 4:2:2 - Bit Parallel Digital Interface

Available from: Society of Motion Picture and Television Engineers
595 W. Hartsdale Avenue
White Plains, New York 10607
(914) 761-1100