Sirius Video Technical Report

Section 1 Product Overview

Sirius Video™ is a video option for SGI workstations equipped with RealityEngine™, RealityEngine^{2}™ or VTX graphics. It fully integrates broadcast-quality video with Silicon Graphics supercomputer graphics capabilities. Sirius Video may also be installed in CHALLENGE™ servers and POWERSeries™ server configurations, making its broadcast-quality video a network resource.

1.1 Product Features

Sirius Video has these features:

- Full implementation of CCIR 601/D1
- Video stream in the Sirius Video system is 4:4:4:4 RGBa/YUVa, 10 bits per component
- Full-size video windows in NTSC (640 x 486), PAL (768 x 576), and CCIR 720x486 and 720x576 formats
- Alpha blending:
  - Blending of any two inputs in real time at rates as high as 30 frames/second
  - Blending may be based on graphics-buffer alpha planes, external alpha values or output of on-board Alpha/Key Generator
- Programmable matrix coefficients for RGB/YUV conversion
- Data transfers over VME bus in 32- and 64-bit transfer modes
- Video-to-graphics conversion:
  - Video pixels are processed by software calls to the SGI Graphics Library and other compatible libraries, allowing, for example, the use of video for texturing
  - Windows, zooms and pans generated by graphics applications
- Multiple high-resolution formats scan-converted to 525 and 625 video formats
- Keys generated from chroma/luma of the video signal or from pixels in graphics windows
- X-Y pixel-wipes and fades generated in real time from external alpha, graphics effects, or VME data transfers
- Two 4-field-deep buffers for synchronizing video signals, storage of video frames, or transfer of still images to the workstation
- Data router serves as crosspoint switch

- Inputs:
  - Two 10-bit digital dual-link video (4:4:4:4, 4:2:2:4 or 4:2:2)
  - 10-bit analog RGBa/YUVa
  - 10-bit digital RGBa from the graphics subsystem (GFX)
  - 8-bit composite in NTSC, PAL or S-VHS
  - VME 8- and 10-bits/component, 32- and 64-bit transfer modes
- Outputs:
  - One 10-bit digital dual-link video (4:4:4:4, 4:2:2:4 or 4:2:2)
  - 10-bit analog RGBa/YUVa
  - 10-bit digital RGBa to GFX
  - 8-bit composite in NTSC, PAL or S-VHS
  - VME 8-and 10-bits/component, 32- and 64-bit transfer modes
- Video output genlocks to video input or to external sync (house reference)
- Multiple Sirius Video boards can be operated in serial or parallel
- Can be installed on servers
- Built-in V-LAN™ transmitter
- Built-in General Purpose Interface (GPI)
- Optional serial digital (SD1 option) provides serial CCIR601 input and output—parallel CCIR601 is standard

1.2 Physical Characteristics

Sirius Video is an expansion board. It occupies one VME slot in the workstation or server chassis. Input and output connectors are in a breakout box.

Section 2 How to Use Sirius Video

A Sirius Video-equipped workstation or server integrates real-time 4:4:4:4 digital video processing with high-end, 2D and 3D computer-generated graphics effects and image processing. It can output the result to host memory or to any standard digital or analog playback or storage medium.

2.1 Inputs and Outputs

Sirius Video supports real-time input and output of video at frame rates to 30 frames/second in the full range of video and SGI graphics formats. A breakout box houses the input/output connectors because of space limitations on some chassis.

Input to either of the two frame buffers may be the following:

- 10-bit digital video (4:4:4:4, 4:2:2:4 or 4:2:2)
- 10-bit analog RGBa/YUVa
- 10-bit digital RGBa

- 8-bit composite
- VME 8- or 10-bits/component
- Feedback of the Video Out generated by the Alpha Processor.

Output from the frame buffers may be directed to the following:

- Graphics subsystem
- Video Out (digital component, analog component or analog composite)
- VME
- Frame buffer input

The frame buffers may be read out independently or blended. Video may be directed to more than one output at a time and looped, which makes possible a broad range of processing and monitoring arrangements.

2.2 Live Video

With Sirius Video, an application can send live video to raster or texture memory in the graphics subsystem, or it can send the video to host memory over the VME bus. Regardless of input format, the video stream within Sirius Video is 4:4:4:4 RGBa/YUVa, 10 bits per component.

2.3 Color Space Conversion

Sirius Video performs YUV/RGB color space conversions with a 3 x 3 matrix multiplier. The system can also maintain the color space of the input source throughout the video stream, rendering the digital processing of the video signal transparent. 4:2:2/4:4:4 conversions are filtered by 55-tap, fixed-coefficient, linear-phase half-band (low pass) digital filters.

2.4 Alpha Blending

Input to alpha buffer A may be selected from the following:

- Graphics-buffer alpha planes
- Any input alpha source
- Alpha/Key Generator output derived from any input

Input to alpha buffer B may be selected from the following:

- Input to frame buffer B
- Alpha/Key Generator output derived from input to frame buffer B

An external, 10-bit alpha key may be used for blending; the Alpha Processor generates an output or destination alpha from any pair of frame buffer alpha inputs.

2.5 Scan Conversions

High-resolution graphics and its alpha may be captured and converted to several sizes of 525 and 625 video. The captured video may also be passed through the system without scan conversion.

2.6 Keys

Chroma and luma keys are fully supported. Source input is processed in the 3 x 3 matrix multiplier. Keys may then be manipulated by editable lookup tables. Component outputs from lookup tables are used to produce an alpha/key in Alpha/Key Generator. Edges on chroma alpha/keys can be softened.

2.7 Graphics Effects

An application uses calls to IRIS Graphics Library™, ImageVision™ Library, or any compatible library of custom routines to generate graphics effects with the video.

The interface to the graphics subsystem operates in field or frame mode. Dedicated lookup tables enable an application to select the bit-depth of the interface: pixel mode: 10 bits, texture mode: 4, 5, or 8 bits.

2.8 DMA Transfers

In its default VME Slave mode, the VME interface initializes and configures the VME hardware. It can be programmed to select VME Master mode, perform DMA transfers to or from host memory over the VME bus, and return to VME Slave mode. Transfers may be in D32 or D64 mode (32-bit or 64-bit). For multiple-pixel transfers, Sirius Video supports pixel packing and unpacking. Only full video fields can be transferred to or from Sirius. All video transfers are VME master mode.

2.9 Multiple Boards

Multiple Sirius Video boards may be installed in a chassis and operated in series or parallel. This provides a means of creating multi-layered video effects and lays the foundation for video server capabilities.

2.10 Servers

Sirius Video may be installed on network servers with or without graphics subsystems. When it is installed on servers without graphics, the server-mounted Sirius Video can input and output video as a network resource. This provides all users with broadcast-quality video input and output, regardless of the computing power of their individual workstations.

Section 3 Hardware Features

3.1 System Architecture

Figure 1 is a top-level block diagram of the Sirius Video expansion board.

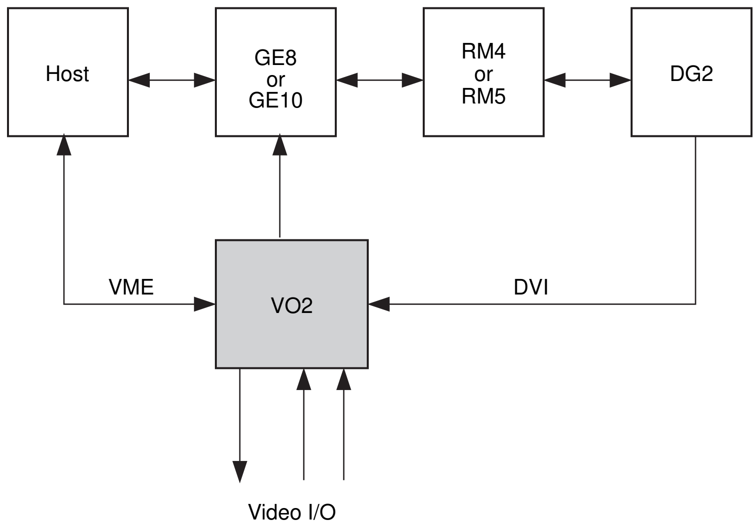

Figure 1: Sirius Video Block Diagram

Figure 2 is a functional overview of the Sirius Video option.

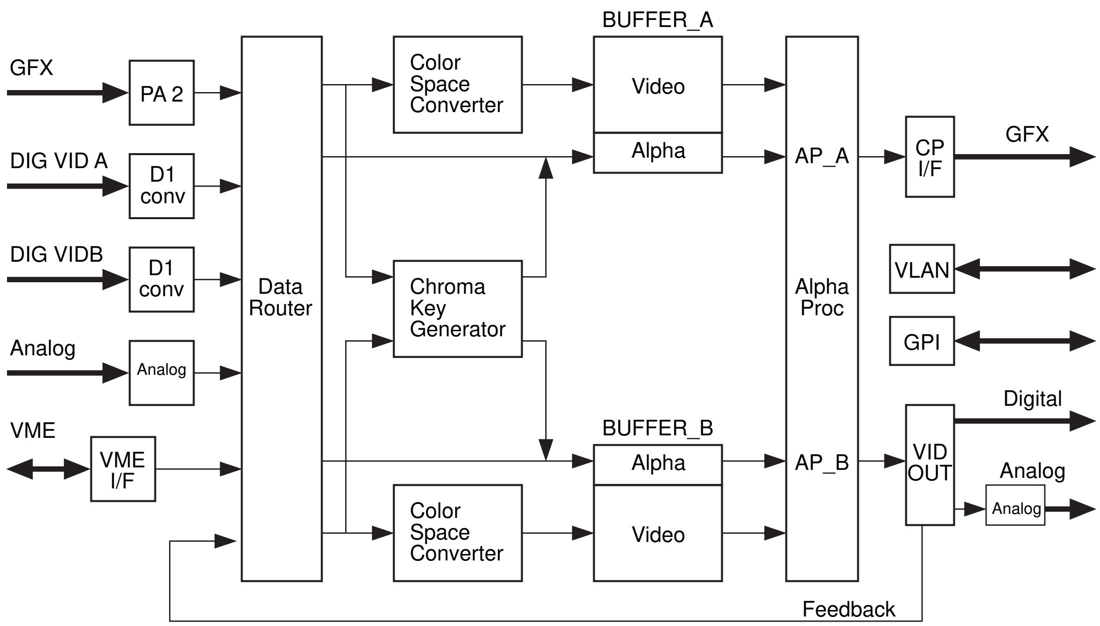

Figure 2: Functional Overview of Sirius Video Expansion Board

3.2 Quadrants

The Sirius Video expansion board can be divided into four parts, or quadrants; frame buffers serve as the quadrant boundaries. The frame and clock rates of each quadrant are fully independent, allowing the quadrants to have different inputs and outputs in different timings. Figure 3 shows the quadrants.

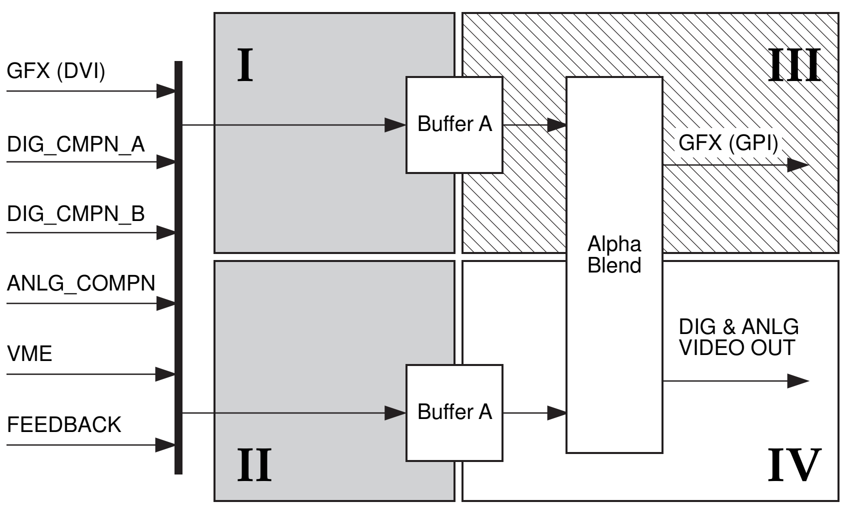

Figure 3: Four Quadrants of Sirius Video Expansion Board

3.3 VME Interface

The VME interface has these features:

- Board devices accessed by programmed I/O (PIO) cycles, except for frame buffers
- A32, D32 and D64 DMA read/write operations in VME Master mode
- With few exceptions, any board device can be accessed for DMA transfers.
- Support for 4 interrupt levels with programmable status and ID registers

3.4 Digital Video Input Ports

Sirius Video has two, 8/10-bit digital video ports for equipment that complies with CCIR 601. Each port supports an optional serial interface at 270 MHz or a parallel interface at 27 MHz. The ports run in 4:2:2 Single Link mode, 4:4:4:4, or 4:2:2:4 Dual Link mode.

Each port consists of two unidirectional interconnections, Link A and Link B:

- In 4:4:4:4 mode, Link A carries Y plus the U and V from even-numbered sample points; link B carries alpha plus the U and V from odd-numbered sample points.
- In 4:2:2:4 mode, Link A carries Y plus the U and V from even-numbered sample points; link B carries alpha only.

3.5 Data Router

Crosspoint switching is performed by the data router subsystem. It selects inputs to the frame buffers and routes data to and from the VME bus.

There are four routers in the subsystem, one for each component (YUVa/RGBa). Any input source and its alpha may be sent to either frame buffer.

3.6 Interpolation/Decimation Filters

Digital filters convert video between 4:2:2 and 4:4:4 formats. The filters are 55-tap, fixed-coefficient, linear-phase half-band (low pass) filters. They can halve or double the sample rate. When a 4:2:2 signal is fed to a color space converter, filters on each chroma difference channel double the sample rate of U and V. A line FIFO on the Y and alpha channels act as a programmable delay element to compensate for the delays produced by the filtering.

3.7 Input Color Space Converter

Each of the two inputs to the frame buffers has a TRW TMC2272 Digital Color Space Converter, which is a 3 x 3 matrix multiplier with programmable coefficients. The matrix provides 12-data, 10-bit coefficients and 23-bit precision internally. FPGAs control over- and underflow, color range offsets, and 2’s complement numbers.

3.8 Frame Buffers

Sirius Video has two identical frame buffers. The buffers are symmetrical, except that the alpha buffer of frame store A can be accessed independently of its corresponding video buffer, whereas this is not true of the alpha buffer of frame store B. Writes to video and/or alpha buffers may be masked.

Each buffer stores 4 fields of R/R-Y, G/Y, B/B-Y and alpha pixels 10-bits wide. Storage is comprised of 256 K x 8 field memories, organized as a 256 K-deep FIFO with two data ports, each port having its own dedicated control and clock signals.

Each buffer has a buffer controller. The controllers are FPGAs; they contain the logic that generates the signals controlling reads and writers to the buffers.

The buffers are configured as a ring and accessed sequentially. A buffer cannot be written to and read from in the same operation, and a buffer's contents cannot be displayed while it is being written to. Pixels being read out are counted in order to format the output correctly, since the buffers are simple FIFOs, not randomly addressable.

3.9 Scan Converter

Scan conversion is performed by a proprietary ASIC chip.

3.10 Alpha Processor and Alpha/Key Generator

The Alpha Processor produces alpha blends from the inputs to the two alpha buffers. The Alpha/Key Generator extracts an alpha from any input channel; it can direct its output to the alpha frame buffers.

3.11 Vlists

Vlists are local memories on the Sirius Video board. They load parameters into on-board control registers during vertical blanking; these parameters might otherwise be loaded during active video by the host. The parameters include color and alpha lookup tables, coefficients, mode registers, and coordinates for video windows.

There are four Vlists, one for each quadrant of the Sirius Video board (see Section 3.2). Loads from the Vlists are dedicated to vertical blankings; the Vlists are bypassed if their blankings are not available. The Vlist controller subsystem consists of a controller and an arbiter. The latter decides which board quadrant to update with data, provided data is present and vertical blanking is available.

3.12 Video-to Graphics Interface

The video-to-graphics interface moves data between Sirius Video and the Geometry Engine (GE) board of the graphics subsystem. It consists of a controller, a matrix multiplier, a data formatter, a frame buffer and data drivers.

The video data sent to the graphics subsystem may be fields or frames. Video fields can be combined within the graphics subsystem to form frames. Pixel data is sent as fields with 48 bits per pixel. Texture data is sent as frames in RGB (5-6-5) or RGBA8 (8:8:8:8) texture format.

Section 4 Software Features

Software for Sirius Video follows Silicon Graphics successful strategy of providing common functionalities in a library of device-dependent and device-independent routines addressed through an API. Libraries insure that upgrades are compatible with current releases, that applications developed for one product can be ported easily to other products, and that functions provided by one library interface reliably and consistently with the functions of other libraries.

The software consists of the standard Video Library components plus enhancements specific to Sirius Video. Please see the *Video Library Programming Information* guide for additional information.

Section 5 Specifications

Table 1 lists current Sirius Video specifications. The data is subject to change.

Board Function	**Specification**	**Value**	**Comment**
Video formats	Digital component	4:4:4:4, 4:4:4:2, 4:2:2 in 525 and 625 timings	CCIR 601 (8/10 bits); SMPTE Dual Link (8/10 bits)
	Analog component	RGBa, YUVa, PrYPba in 525 and 625 timings	Betacam®, MII, SMPTE; 10-bit ADC/DAC; 2x oversampling output
	Analog composite	525 and 625 timings	NTSC, PAL, S-VHS
Analog input channels	Input impedance	50 KOhm; 5 pF capacitance	
	Return loss	>40 dB to 5.5 MHz	
	Frequency response	0.25 dB to 1 MHz; 0.5 dB to 5.5 MHz	
	Group delay	20 nsec to 5.5 MHz	
Analog output channels	Frequency response	0.25 dB to 1 MHz; 0.5 dB to 5.5 MHz; with sin x/x compensation	
	Group delay	20 nsec to 5.5 MHz	
	S/N ratio	>65 dB, weighted 5.0 MHz	

Connectors	Video input	2 pairs of serial/parallel digital	CCIR 601, SMPTE Dual Link, optional serial I/O
		1 analog component	RGBa, YUVa, PrYPba
		1 analog composite	NTSC, PAL, S-VHS
	Video output	2 serial/parallel digital	CCIR 601, optional serial I/O
		1 analog component	RGBa, YUVa, PrYPba
		1 analog composite	NTSC, PAL, S-VHS
Controls		2 GPI input lines 2 GPI output lines V-LAN interface Genlock/Sync input Loopthru's for all analog inputs	
Frame buffers (2)		256K x 10 bits x 4 fields x 4 colors (RGBa or YUVa)	
VME bus	Transfer rate	~28 Mb/second in D32 mode ~55 Mb/second in D64 mode	D64 mode available only on Onyx and CHALLENGE systems
Video-to-graphics interface	Bandwidth	40 MHz	8 and 10 bits per component, user-selected
Filtering	4:2:2/4:4:4 conversions	55-tap FIR interpolating/ decimating filters	
System requirements	Minimum configurations	1 VME slot	
		RealityEngine, RealityEngine^2 or VTX graphics	Full functionality with integrated graphics support
		Crimson, POWERSeries or CHALLENGE systems (servers, XS, XS24, Elan, Extreme and VGX/T graphics systems)	Reduced functionality without integrated graphics

Table 1: Sirius Video Expansion Board Specifications