SGS-THOMSON
MICROELECTRONICS

SEA OF GATES - STRUCTURED ARRAYS

ISB 35000 SERIES

0.5 micron, triple level metal HCMOS Technology. Typical delay 0.21ns for 2-input NAND gate

GENERAL FEATURES

- 0.5 micron triple layer metal HCMOS process featuring retrograde well technology, low resistance salicided active areas, polysilicide gates and thin metal oxide
- 3.3 V optimized transistor with 5 V I/O interface capability
- Metallised generators to support SPRAM and DPRAM, plus an extensive embedded function library
- Fully independent power and ground configurations for inputs, core and outputs
- Programmable I/O ring capability up to 1000 pads
- Combines Standard Cell Features with Sea of Gates time to market

Process Technology	Complexity	Delay (ns)	Gate Power (μw/Gate/MHz)	Single Output Drive (mA)	I/O Interface	Module Generators
0.5 μm, triple level metal	9 generics (initial) 58K to 500K usable gates	0.21 typ. for 2-input NAND gate ND2P	.76	up to 24	LVCMOS LVTTL GTL PECL IEEE LVDS	See Table Next Page

PRODUCT RANGE

Internal Device Name	Total Sites[1]	Estimated[2] Gates	Total Usable[3] Gates	Maximum[4] Device Pads	Maximum[5] I/O
ISB35083	124,416	82,944	58,060	188	172
ISB35130	194,400	129,600	90,720	232	216
ISB35166	249,696	166,464	116,524	260	244
ISB35208	311,904	207,936	145,555	288	272
ISB35279	418,176	278,784	195,148	332	316
ISB35389	584,064	389,376	253,094	388	372
ISB35484	726,624	484,416	314,870	432	416
ISB35666	998,784	665,856	399,513	504	488
ISB35832	1,247,616	831,744	499,046	560	544

Notes:
1. Internal sites is based on the number of placement sites available to the route and place software.
2. A factor of 1.5 is used to derive the gate complexity from the total available sites. This number is in Nand2 equivalents.
3. Factors of 70%, 65%, and 60% have been used to calculate the routing efficiency. This number may vary depending on the design.
4. 16 corner pads are dedicated to internal and external power supplies. I/O pads may be configured for additional power.
5. Maximum I/O = Total device pads minus power pads.

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MODULE GENERATOR LIBRARY

Cell		Description
SPRAM	Metallised	8K bits max 2048 word max 64 bit max Zero static current Tristate output
	Embedded	256K bits max 16K word max 64 bit max Zero static current Tristate outputs
DPRAM	Metallised	4K bits max 1024 word max 64 bit max Zero static current Separate read/write ports Tristate outputs
	Embedded	128K bits max 8K word max 64 bit max Zero static current Tristate outputs
ROM	Embedded	2M bits max 32K word max 64 bit max Diffusion programmable Tristate outputs

STANDARD PACKAGE RANGE

Type	Package	Pins
ISB35083	PQFP TQFP	44 to 160 64 to 100, 144, 176
ISB35130	BGA PQFP TQFP	256 44 to 160 64 to 100, 144, 176
ISB35166	BGA PQFP TQFP	256 64 to 160 100, 144, 176
ISB35208	BGA PQFP TQFP	256 64 to 208 100, 144, 176
ISB35279	BGA PQFP TQFP	256 64 to 208 100, 144, 176
ISB35839	BGA PQFP TQFP	256 128 to 208 144, 176
ISB35484	BGA PQFP	256, 352 128 to 208
ISB35666	BGA PQFP	256, 352 128 to 208