future focus

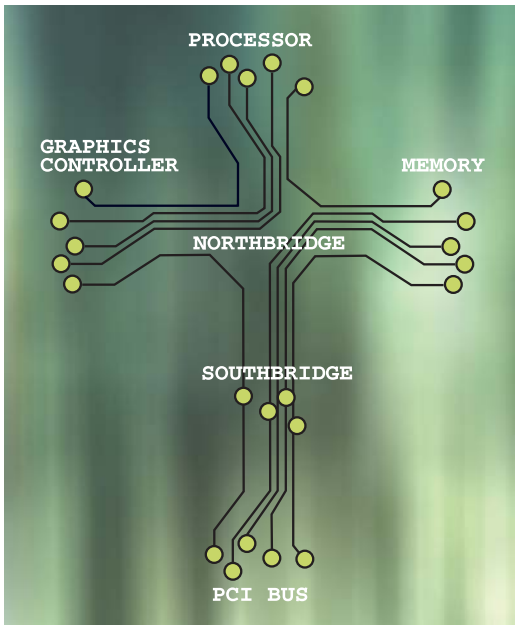
Bigger file sizes and operations mean that PCs need to be able to shuffle information between components faster than ever.

The latest innovation in internal data movement is AMD's HyperTransport, and Will Head asks whether it could be the answer

As PCs get bigger, better and faster, there's one area that has largely been overlooked in their evolution: the internal interconnects that govern the speed at which information gets shunted around inside the beige box. USB 2.0 may bring fast external peripherals to the desktop, but it could also unearth a huge bottleneck in the PC's internal architecture.

Take it to the bridges

If you break a motherboard down into its basic components you'll find the processor, memory, graphics controller, north bridge, south bridge and PCI bus (these are the slots on the motherboard for expansion cards, providing a communications link to the rest of the system). All these components need to talk to one another. The north bridge is the central component, connecting together the processor, memory, graphics controller and the south bridge, with the PCI bus communicating through the south bridge. Other motherboard components, like USB and network ports, also connect through the south bridge.



Interconnects used to offer performance similar to the standard PCI bus, providing approximately 1Gbps (gigabit per second) of bandwidth. As faster processor, graphics and memory technologies have evolved, interconnect bandwidths have increased accordingly.

The north bridge's links to the processor and memory now run on a 133MHz DDR bus (266MHz effective) providing close to 17Gbps of bandwidth. The AGP (accelerated graphics port), which connects the graphics controller to the north bridge, has also increased in bandwidth. The forthcoming AGP 8x standard will offer almost 17Gbps of bandwidth, like the other interconnects.

However, the north bridge/south bridge link got left behind in this process of evolution, and is still based on the original PCI standard and limited bandwidth. The low bandwidth demands of USB 1.1 and 10/100 ethernet networking technology has meant that until recently this has not been an issue. But with USB 2.0, offering 480Mbps (megabits per second) of bandwidth, the north bridge/south bridge link will become a bottleneck. What you really need is a standard that can provide plenty of bandwidth, has been designed for the purpose and is readily available, which is exactly what AMD thinks it has with HyperTransport.

HyperTransport supports a maximum bandwidth of 51.2Gbps in both directions, so is more than up to the job removing the north bridge/south bridge bottleneck

Talking fast

HyperTransport began life in 1997, when AMD looked into designing a standard for high-bandwidth chip-to-chip communication. In July 2001 the HyperTransport Consortium was founded by AMD, API Networks, Apple, Cisco, nVidia, PMC-Sierra, Sun and Transmeta to promote the standard.

HyperTransport's design goals include increased internal bandwidth, minimal software support, straightforward physical and electrical design, reduced power requirements and improved scalability (the ability to build small or large systems using the same technology).

HyperTransport supports a maximum bandwidth of 51.2Gbps in both directions, so is more than up to the job removing the north bridge/south bridge bottleneck. It has already made an appearance in the desktop market on motherboards that use nVidia's nForce chipset. It forms the link between the IGP (integrated graphics processor) and the MCP (media communications processor) – in effect linking the north and south bridges. The HyperTransport link on the nForce chipset provides over 6Gbps of bandwidth, six times greater than the traditional north bridge/south bridge link.

The Xbox also uses HyperTransport to ensure there's enough bandwidth to shift the large amounts of graphics data around.

For AMD, HyperTransport plays a significant part in its forthcoming Hammer processors. Hammer integrates the memory controller on to the processor, so memory connects directly to the chip. HyperTransport provides the link between the processor and the AGP controller which in turn connects to the south bridge, also via HyperTransport.

Xbox aside, HyperTransport has only been implemented on AMD platforms. USB 2.0 will expose the lack of bandwidth available, but we'll have to wait and see if HyperTransport becomes the *de facto* standard for high-bandwidth interconnects on non-AMD PCs. Intel is bound to come up with its own technology, so we should see some competition soon enough. ■

ILLUSTRATION: NATALIE WINTER