## 5.13 SWIM floppy disk interface

The SWIM interface is a combination MFM/GCR controller that connects directly to the CPU data bus. It is designed to replace the Integrated Woz Machine (IWM) and is pin and function compatible with the IWM. The SWIM chip is a combination of the traditional IWM chip, an ISM chip, and a combination logic chip.

The SWIM (Super Woz Integrated Machine) supports all IWM extensions including a status register, a mode register, and the following modes of operation:

- asynchronous mode
- fast mode
- optional 1-second one-shot

See the section in Chapter 3, “FDHD, the high-density floppy disk drive,” for a description of the application of the SWIM floppy disk interface.

The SWIM also extends the IWM by providing an ISM mode supporting a high-speed rate twice that of the IWM, and programmable input clock frequencies. Other features of the ISM mode are

- Supports standard MFM format
- Supports Apple GCR format
- Write precompensation
- Read postcompensation
- Asymmetry and speed error compensation
- Programmable parameters for using both variable and fixed speed drives
- Two-byte data FIFO
- Motor time out
- Asynchronous mode with pollable handshake registers

The ISM makes it possible to read and write both MFM and Apple GCR formats on the same disk drive, and also makes it possible to write MFM format on a variable speed, 3.5-inch drive in such a way that it can be read back on a fixed speed 3.5-inch drive.

The ISM provides the ability to do write precompensation to correct for peak shift effects that occur in magnetically stored media.

The ISM also provides a very sophisticated, and rarely used, form of read postcompensation which corrects for peak shift effects on disks with insufficient precompensation.

The ISM uses a programmable parameter scheme that makes it possible to read and write 3.5-inch variable and fixed speed drives, as well as standard 5.25-inch drives.

The ISM contains a two-byte read and write FIFO stack to provide more software flexibility.

A Motor Time Out is included which will keep the drive enabled for 0.5 s to 1 s to provide time for software to begin another read or write operation without bringing the drive back up to speed.

The ISM makes it possible to program the phase lines as either inputs or outputs, which make it possible to interface with a wide variety of drives.

The SWIM interface consists of a single CMOS SWIM chip, an internal ribbon connector, and an external DB-19 connector. The pinout for the external connector is given in Table 5-7.

**Table 5-7** SWIM Connector Pinouts

| Pin Number | External DB-19 |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | GND |
| 4 | GND |
| 5 | n.c. |
| 6 | +5V |
| 7 | +12 |
| 8 | +12 |
| 9 | n.c. |
| 10 | n.c. |
| 11 | PH0 |
| 12 | PH1 |
| 13 | PH2 |
| 14 | PH3 |
| 15 | /WREQ |
| 16 | HDSEL |
| 17 | /ENBL2 |
| 18 | RD |
| 19 | WR |

The SWIM is a CMOS device and is controlled through a set of read and write registers that are byte addressable only and which are to be accessed through the Device Manager and the driver as described in Chapter 3, "*Firmware*," under the heading "FDHD, the High Density Floppy Disk Drive".

The floppy disk drive can read and write on a 3.5-inch disk in any of the following modes: 1 MB Apple GCR (Group Code Recording) on a 1 MB disk, 1 MB MFM (Modified Frequency Modulation) on a 1 MB disk, and 2 MB MFM on a 2 MB disk.

The drive consists of two read/write heads, head positioning mechanism, disk motor, interface logic circuitry, read/write circuitry, and motor control circuitry. It includes auto inject/eject mechanisms and uses a 3.5-inch floppy disk for data storage.

## 5.14 SCC Interface

The Serial Communications Controller (SCC) is an 8 MHz CMOS Z8530 which has two independent ports for serial communication. Each port can be independently programmed for asynchronous, synchronous, or AppleTalk protocols.

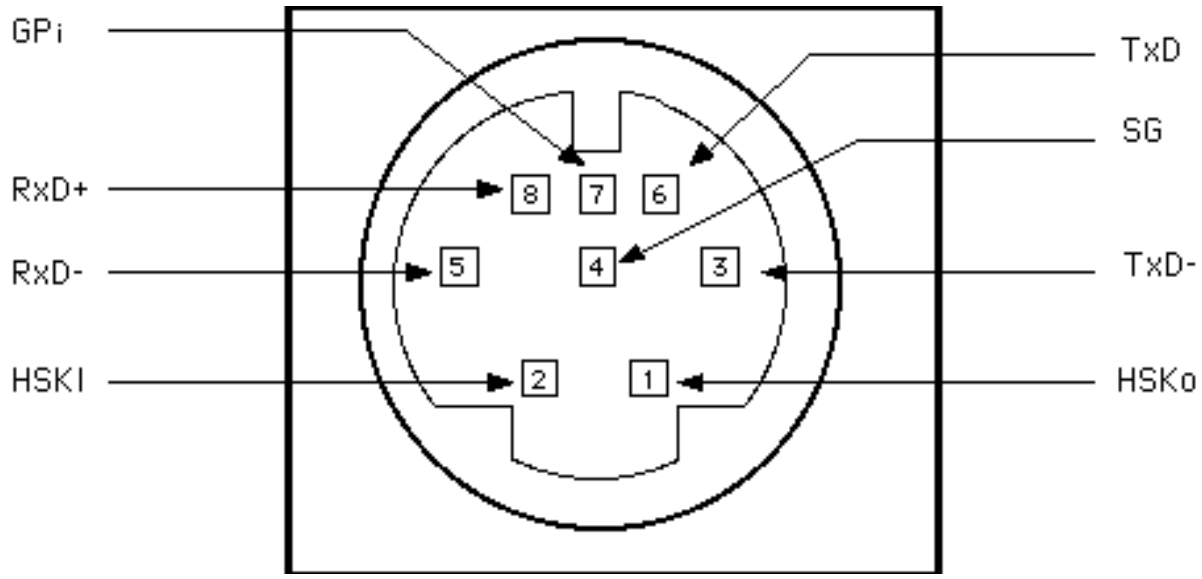
Power is applied to these ports under control of the power manager and this will occur only when you make the correct Toolbox calls. See Chapter 2, "Software Developer Guidelines," and Chapter 6, "The Power Manager."

The serial interface is connected to the output ports through two eight-pin miniature DIN connectors. Each signal line contains a 47-ohm series termination resistor. The pinout for the external connector is given in Table 5-8.

**Table 5-8** SCC Connector Pinout

| Pin Number | Port A | Port B | Description |
|---|---|---|---|
| 1 | | | HSKo HSKo Handshake output; Connected to SCC RTS; Tri-stated when DTR is inactive; Voh = 3.6V; Vol = -3.6V; Rl = 450Ω |
| 2 | | | HSKi HSKi Handshake input; Connected to SCC;CTS and TRxC; Vih = 0.2V; Vil = -0.2V; Ri = 12KΩ |
| 3 | | | TxD- TxD- Transmit data (inverted); Connected to SCC TxD; Tri-stated when DTR is inactive; Voh = 3.6V; Vol = -3.6V;Rl = 450Ω |
| 4 | | | SG SG Signal ground. Connected to logic and chassis ground. |
| 5 | | | RxD- RxD- Receive data (inverted); Connected to SCC RxD; Vih = 0.2V; Vil = -0.2V; Ri = 12KΩ |
| 6 | | | TxD+ TxD+ Transmit data; Connected to SCC TxD; Tri-stated when DTR is inactive; Voh = 3.6V; Vol = -3.6V; Rl = 450Ω |
| 7 | | | GPi GPi General purpose input; Connected to SCC DCD; Vih = 0.2V; Vil = -0.2V; Ri = 12KΩ |
| 8 | | | RxD+ RxD+ Receive data; Connected to SCC RxD. Vih = 0.2V; Vil = -0.2V; Ri = 12KΩ |

**Figure 5-8** SCC Mini-8 Connector




In the SCC, register addressing is direct for the *data* registers only. In all other cases (with the exception of WR0 and RR0), programming the Write registers requires two write operations and reading the Read registers requires both a write and a read operation. The first write is to WR0 (the Command Register) and contains three bits that point to the selected register. The second write (also to the Command Register) is the actual control word for the selected register; if the second operation is a read, the selected read register is accessed. All the registers in the SCC, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again. All address references to the SCC use offsets from the constant sccRBase ($FD 0000) for reads, and sccWBase for writes, as the base address and are byte-only addressable. These base addresses are also available in the global variables SCCRd and SCCWr. The offsets to the command and data registers are given in Table 5-9.

**Table 5-9** SCC Address Offsets

| Device | Base (R) | Base (W) | Register | Offset |
|---|---|---|---|---|
| SCC | $FD 0000 | $FD 8000 | Port A Command | $0002 |
| | | | Port A Data | $0006 |
| | | | Port B Command | $0000 |
| | | | Port B Data | $0004 |

The SCC has a timing restriction in the time between accesses to the chip. Accesses to the chip must be at least 1.8 µsec from the end of the first access to the beginning of the second. The hardware implementation will prevent the next access until the appropriate wait has occurred, making this constraint transparent to the programmer.

## 5.15 Apple Desktop Bus (ADB)

The communication of data to the host 68HC000 from the keyboard, keypad, trackball and any other input device is via the Apple Desktop Bus (ADB), which consists of one serial, bi-directional data line, a 5 Vdc supply line, and ground, which is common for power and signal return. The ADB transceiver functions are implemented in the power manager processor while the keyswitch encoding is done by an ADB keyboard processor.

The standard configuration of the Macintosh Portable contains a miniature, low-power, ADB trackball. Input devices designated as *low-power* typically operate on about one tenth the current of standard types. The trackball module is designed to be installed—by the factory, dealer, or end user—into the position normally occupied by a numeric keypad in some other keyboards.

▲ **WARNING:** Any input devices connected, either internally or externally, to the Macintosh Portable ADB should be low-power versions in order to maximize operating time per battery charge. This means that normal keyboards and mouse devices from other members of the Macintosh family are usable with the Macintosh Portable, but at some sacrifice in reduced battery life between recharges. ▲

The operator input area of the Macintosh Portable has provision for, and comes equipped with, an alphanumeric keyboard module (keyboard) and a trackball module (see Figure 1-1). The trackball module may be placed by the user, either to the left or right of the keyboard. The trackball may also be replaced by an optional numeric keypad module (see Chapter 8, “Options”).

## The keyboard processor

The keyboard processor is a Mitsubishi M50740 8-bit microcomputer chip. The M50740’s distinctive features are

- 3072 bytes of ROM
- 96 bytes of RAM
- 15 mW power dissipation
- 8-bit timer
- 32 programmable I/O ports

The keyboard processor is used to interpret the keyboard and numeric keypad matrix switch closures. The best way to visualize the internal actions of this processor is to recognize that it is the same as performed by the processors found in Apple's other keyboards. In the Macintosh Portable, however, the processor physically resides on the main logic board instead of the keyboard PCB.

The keyboard processor communicates with the power manager via the ADB in exactly the same fashion as it would if it were a separate, stand-alone keyboard.

## Low-Power keyboard

The alphanumeric keyboard module is an array of switches only, without any active electronics. Each module has a steel plate into which have been inserted the keyswitches. The switches are interconnected by a PC board.

The alphanumeric keyboard has 63 keyswitches. The keyswitches are quiet-tactile, full-travel, and low-profile. The keycaps are a tapered style, and are platinum color.

The keyboard module is designed to be installable into the Macintosh Portable from the outside, by the customer. The module may be placed on the left or right side of the housing.

The alphanumeric keyboard module has two connectors, wired identically in parallel. The trackball/numeric keypad module has one connector. The connectors on the keyboard are wired with the pinout in Table 5-10.

**Table 5-10** Keyboard Connectors Pinout

| Signal Name | Pin Number | | | Pin Number | Signal Name |
|---|---|---|---|---|---|
| GND3 | 1 | • | • | 2 | X0 (KEYMATRIX) |
| X1 | 3 | • | • | 4 | X2 |
| X3 | 5 | • | • | 6 | X4 |
| X5 | 7 | • | • | 8 | X6 |
| X7 | 9 | • | • | 10 | X8 |
| X9 | 11 | • | • | 12 | X10 |
| Y0 | 13 | • | • | 14 | Y1 |
| Y2 | 15 | • | • | 16 | Y3 |
| Y4 | 17 | • | • | 18 | Y5 |
| Y6 | 19 | • | • | 20 | Y7 |
| CAPS LOCK | 21 | • | • | 22 | SHIFT |
| CONTROL | 23 | • | • | 24 | OPTION |
| COMMAND | 25 | • | • | 26 | GND1 |
| GND2 | 27 | • | • | 28 | (SPARE) |
| ADB | 29 | • | • | 30 | BUTTON |
| See Note 8. | 31 | • | • | 32 | See Note 8. |
| (SPARE) | 33 | • | • | 34 | GND3 |

Notes:

1. This connector interfaces to the keyboard, the numeric keypad, the trackball, or any compatible ADB device.
2. GND1 is keyboard common for contact closures.
3. GND2 is ADB systems signal/power return ground.
4. GND3 is ESD/EMC/Chassis ground.
5. Disposition of grounds is handled on main logic board.
6. Two cables/connectors are required on main logic board, one at either side of computer housing.
7. Cable connectors from CPU board are to mate with 34-pin center-polarized headers. (Molex 5342-NGS2 series, No. 39-26-7349, or equivalent).
8. Pins 31 and 32 are connected together on the ISO (European) keyboards; this connection is used to identify such keyboards.

**Low-power trackball**

The trackball is electrically compatible with the ADB, although it uses few of the pins in a large, shared connector instead of the dedicated mini-circular type. Table 5-11 shows the pinout for the trackball connector.

In the trackball's intended application, the host controls the flow of power to the trackball, and it may be removed or restored at any time. Although not a strict ADB spec requirement, this unit is designed to be operational in the default mode, within 80 ms of the application of power.

The trackball's default handler ID is 0001 and its address is 0011, the same as a mouse.

Movement of the top of the ball's surface to the right is in the Positive X direction, and movement Down is in the Positive Y direction (see Figure 5-9).

There is one button for the trackball, which is the equivalent of the button on a mouse The trackball and the button are equally available to left- or right-handed users.

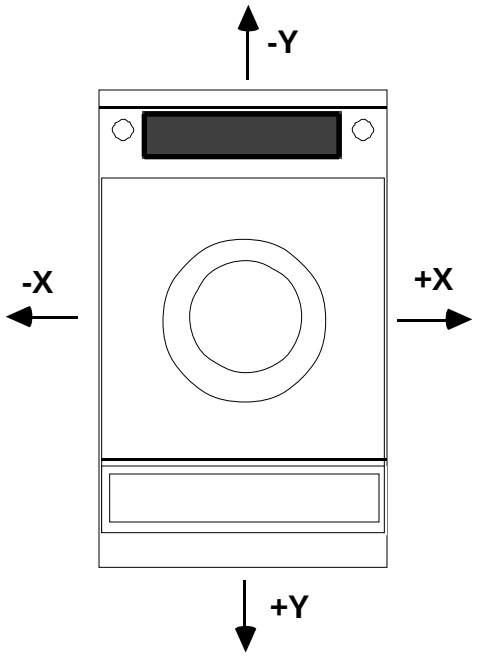
The 34-pin trackball connector, into which a cable from the 68HC000 CPU is plugged, is a dual-row, center-polarized header.

■ **Table 5-11** Trackball Connector Pinout

| Pin Number | Signal Name | Function |
|---|---|---|
| Pin 27 | GND2 | Signal power ground return |
| Pin 28 | +5V | Power supply from host |
| Pin 29 | ADB DATA | Bi-directional serial data |
| Pins 1 and 34 | GND3 | Shield ground |

◆ All other connector pins should NOT be connected.

**Figure 5-9** Trackball Direction Conventions




## 5.16 Sound interface

The sound interface is designed to be upward compatible with Macintosh sound using the Apple Sound Chip (ASC); it offers stereo sound and other enhancements not available in the classic Macintosh and Macintosh SE computers and available for the first time in the Macintosh II. This chip has two output channels and four major functional modes:

1. Four Voice Synthesis (mono)
2. Two Voice Synthesis (stereo)
3. Single Voice (stereo)
4. Single Voice (mono)

The hardware of the Apple Sound Chip subsystem consists of these components:

- the Apple Sound Chip (ASC)
- two analog sound-processing chips (the Sony sound chips)
- an internal high-impedance speaker
- a stereo phono jack

The speaker is a permanent magnet moving-coil type. The Macintosh Portable stereo-phone jack is located on the rear of the machine.

The features of this subsystem are available through the Macintosh Sound Manager.

---

## 5.17 Macintosh Portable expansion bus interface

The Macintosh Portable expansion interface follows closely that of the Macintosh SE. The 68HC000 signals are brought out on a processor direct slot (PDS), which is a 96-pin Euro DIN connector, allowing for expansion capabilities not available through other features of the machine. The pinout for the expansion connector is given in Table 5-12. Table 5-13 gives the signal descriptions.

**Table 5-12** PDS Expansion Connector Pinout

| Pin Number | Row A | Row B | Row C |
|---|---|---|---|
| 1 | GND | GND | GND |
| 2 | +5V | +5V | +5V |
| 3 | +5V | +5V | +5V |
| 4 | +5V | +5V | +5V |
| 5 | /DELAY.CS | SYS.PWR/ | VPA/ |
| 6 | /VMA | /BR | /BGACK |
| 7 | /BG | /DTACK | R/W |
| 8 | /LDS | /UDS | /AS |
| 9 | GND (Pmgr Switched) | +5/0 V | A1 |
| 10 | A2 | A3 | A4 |
| 11 | A5 | A6 | A7 |
| 12 | A8 | A9 | A10 |
| 13 | A11 | A12 | A13 |
| 14 | A14 | A15 | A16 |
| 15 | A17 | A18 | Reserved |
| 16 | Reserved | Reserved | Reserved |
| 17 | Reserved | Reserved | Reserved |
| 18 | Reserved | Reserved | Reserved |
| 19 | Reserved | +12 V | D0 |
| 20 | D1 | D2 | D3 |
| 21 | D4 | D5 | D6 |
| 22 | D7 | D8 | D9 |
| 23 | D10 | D11 | D12 |
| 24 | D13 | D14 | D15 |
| 25 | +5/3.7 V | +5V | GND |
| 26 | A19 | A20 | A21 |
| 27 | A22 | A23 | E |
| 28 | FC0 | FC1 | FC2 |
| 29 | /IPL0 | /IPL1 | /IPL2 |
| 30 | /BERR | /EXT.DTACK | /SYS.RST |
| 31 | GND | 16M | GND |
| 32 | GND | GND | GND |

**Table 5-13** PDS Expansion Connector Signal Descriptions

| Signal Designator | Signal Description |
|---|---|
| GND | Logic ground |
| D0–D15 | 68HC000 unbuffered data bus 0–15 |
| A1–A23 | 68HC000 unbuffered address bus 1–23 |
| 16M | 16 MHz clock |
| /EXT.DTACK | External DTACK. This signal is an input to the CPU logic glue and allows for external generation of /DTACK. |
| E | 68HC000 ECLK |
| /BERR | 68HC000 Bus Error |
| IPL2–IPL0 | 68HC000 Interrupt Priority Level 2–0 |
| /SYS.RST | 68HC000 Reset |
| /AS | 68HC000 Address Strobe |
| /UDS | 68HC000 Upper Address Strobe |
| /LDS | 68HC000 Lower Address Strobe |
| R/W | 68HC000 Read/Write |
| /DTACK | 68HC000 Data Acknowledge |
| /BG | 68HC000 Bus Grant |
| /BGACK | 68HC000 Bus Grant Acknowledge |
| /BR | 68HC000 Bus Request |
| /VMA | 68HC000 Valid Memory Address |
| /VPA | 68HC000 Valid Peripheral Address |
| FC2–0 | 68HC000 Function Code 2:0 |

The current available to an expansion card inserted in the processor direct slot (PDS) is given in Table 5-14. This current allocation is part of a worst-case current budget that is estimated to reduce the system operating time per battery charge by fifty percent.

**Table 5-14** Current Available To The Processor Direct Slot

| Power Supply | Operating State | Sleep State |
|---|---|---|
| + 5 V, Always-on | 50 ma maximum | 1 ma maximum |
| + 5 V, Switched | * | 0 ma maximum |
| + 12 V | 25 ma maximum | 0 ma maximum |

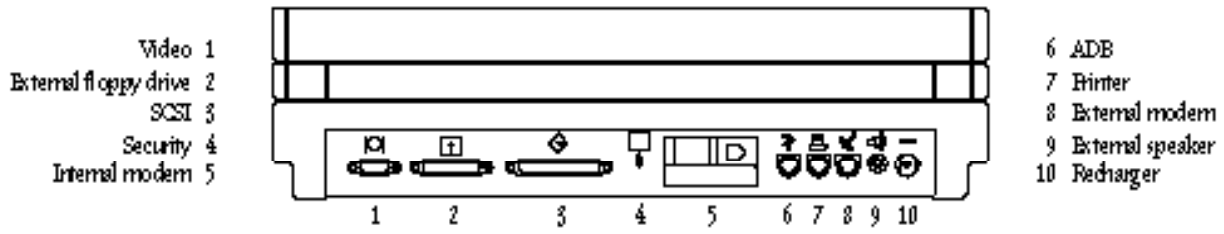
* The 50 ma maximum applies to the sum of the loads on the switched and unswitched (by the power manager) +5 V supplies.

## 5.18 The Macintosh Portable I/O port connectors

This section describes the connectors on the rear of the Macintosh Portable. Figure 5-10 shows these connectors. Descriptive names for these connectors, from left to right in the figure, are

- Video
- External disk drive
- External SCSI device
- RJ-11 Telephone receptacle
- Apple Desktop Bus (ADB)
- Serial port (Modem)
- Serial port (Printer)
- Stereo sound
- Battery charger, DC power input

**Figure 5-10** I/O port connectors




The connectors are described in the following sections. For each I/O connector, there is a drawing showing the pin or socket location and numbering. Each drawing is followed by a tabular description of signal names and functions.

## Video connector

The Macintosh Portable has a DB-15 connector at the rear that provides the video output signals to an external video adapter. The adapter produces video signals with Macintosh II, NTSC, or PAL formats.

The physical connection is a "D" subminiature receptacle connector. The pinout of this connector is shown in Figure 5-11. The signal names and descriptions are given in Table 5-15.

**Figure 5-11** External video connector

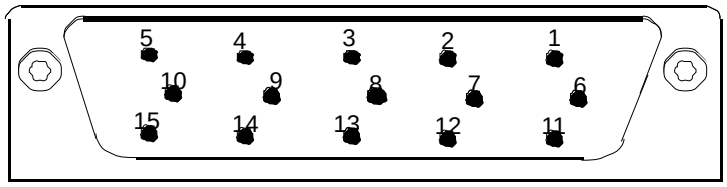



**Table 5-15** Video connector signal assignments

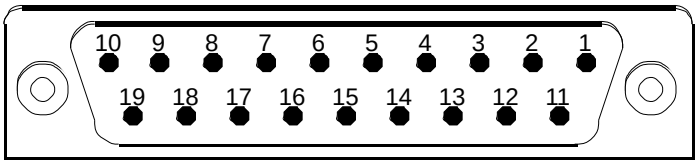
| Pin number | Signal name | Signal description |
|---|---|---|
| 1 | D0 | Data bit 0 |
| 2 | D1 | Data bit 1 |
| 3 | +5V | |
| 4 | D2 | Data bit 2 |
| 5 | D3 | Data bit 3 |
| 6 | D4 | Data bit 4 |
| 7 | GND | Signal Ground |
| 8 | Vbb | Battery Voltage |
| 9 | GND | Signal Ground |
| 10 | D5 | Data bit 5 |
| 11 | D6 | Data bit 6 |
| 12 | D7 | Data bit 7 |
| 13 | +5V | |
| 14 | New_Frame | FLM from Video Display Interface chip, Begin frame scan over |
| 15 | New_Byte | CL2 from Video Display Interface chip, Byte clock |

## External disk drive connector

This port can be used to support the external 3.5-inch disks used by all Macintosh computers, as well as the Apple Hard Disk 20.

The pinout of the external disk drive connector is given in Figure 5-12. The connector is a receptacle, DB-19 type.

**Figure 5-12** External Disk Drive Connector



The signal names and descriptions for the external disk connector are given in Table 5-16

**Table 5-16** External disk drive connector signal assignments

| Pin number | Signal name | Signal Description |
|---|---|---|
| 1 | GND | Logic ground |
| 2 | GND | |
| 3 | GND | |
| 4 | GND | |
| 5 | no connection | |
| 6 | +5V | |
| 7 | +12 | |
| 8 | +12 | |
| 9 | no connection | |
| 10 | no connection | |
| 11 | PH0 | Phase 0 |
| 12 | PH1 | Phase 1 |
| 13 | PH2 | Phase 2 |
| 14 | PH3 | Phase 3 |
| 15 | /WREQ | |
| 16 | HDSEL | Head select |
| 17 | /ENBL2 | Enable |
| 18 | RD | Read |
| 19 | WR | Write |

## External SCSI connector

Like the Macintosh SE,the the Macintosh Portable has a built-in SCSI port for high-speed parallel communications. The SCSI interface can communicate with up to seven SCSI devices, such as hard disks, streaming tapes, and high-speed line printers. The external SCSI port is a DB-25 connector as shown in Figure 5-13.

**Figure 5-13** External SCSI connector

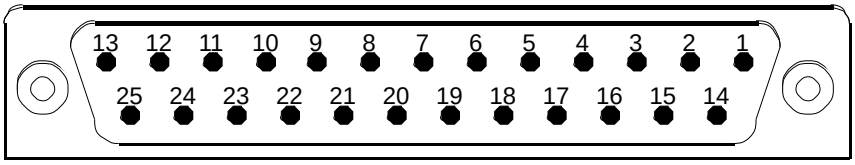



Table 5-17 shows the signal assignments for the SCSI DB 25-pin external connector. These signals are described in detail in the *NCR 5380 SCSI Interface Chip Design Manual* and the IEEE SCSI specification—Section D, ANSIX3T9.2 (version 17B).

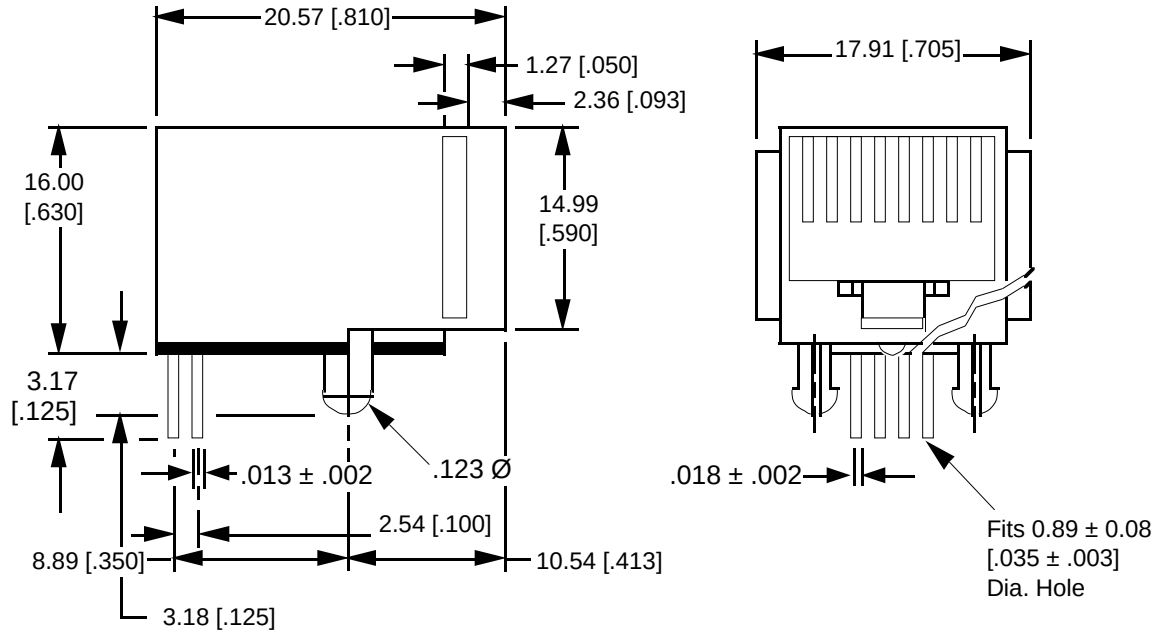
**Table 5-17** External SCSI Connector Signal Assignments

| Pin number | Signal name | Signal description |
|---|---|---|
| 1 | /REQ | Request for a REQ/ACK data transfer handshake |
| 2 | /MSG | Indicates the Message phase |
| 3 | /I/O | Controls the direction of data movement |
| 4 | /RST | SCSI bus reset |
| 5 | /ACK | Acknowledge for a REQ/ACK data transfer handshake |
| 6 | /BSY | SCSI data bus is busy |
| 7 | GND | Ground |
| 8 | /DB0 | Bit 0 of SCSI data bus |
| 9 | GND | Ground |
| 10 | /DB3 | Bit 3 of SCSI data bus |
| 11 | /DB5 | Bit 5 of SCSI data bus |
| 12 | /DB6 | Bit 6 of SCSI data bus |
| 13 | /DB7 | Bit 7 of SCSI data bus |
| 14 | GND | Ground |
| 15 | /C/D | Indicates whether control or data is on the SCSI bus |
| 16 | GND | Ground |
| 17 | /ATN | Indicates an attention condition |
| 18 | GND | Ground |
| 19 | /SEL | Select a target or an initiator |
| 20 | /DBP | Parity bit for SCSI data bus |
| 21 | /DB1 | Bit 1 of SCSI data bus |
| 22 | /DB2 | Bit 2 of SCSI data bus |
| 23 | /DB4 | Bit 4 of SCSI data bus |
| 24 | GND | Ground |
| 25 | NC | No connection |

## RJ-11 telephone receptacle

The RJ-11 receptacle, which is mounted on (and a part of) the optional modem card, is accessable through the rear of the Macintosh Portable. Figure 5-14 is a drawing of this connector.

**Figure 5-14** RJ-11 Telephone Receptacle




Dimensions are in units of mm [inch].

## Apple Desktop Bus (ADB) connector

The ADB is a serial communications bus designed to accommodate low-speed input devices. The ADB port is a 4-pin mini DIN connector as shown in Figure 5-15.

▲ **WARNING:** Any input devices connected, either internally or externally, to the Macintosh Portable ADB should be low-power versions in order to maximize operating time per battery charge. This means that normal keyboards and mouse devices from other members of the Macintosh family are usable with the Macintosh Portable, but at some sacrifice in reduced battery life between recharges. ▲

**Figure 5-15** The Macintosh Portable ADB connector

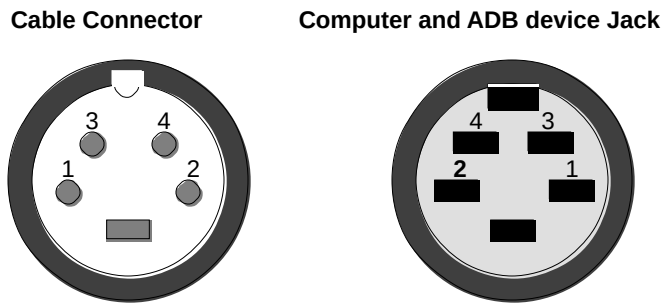



**Table 5-18** The Macintosh Portable ADB signal assignments

| Pin number | Signal name | Signal description |
|---|---|---|
| 1 | | ADB The bidirectional data bus used for input and output. It is pulled up to +5V through a 470 ohm resistor on the logic board, and is an open collector type signal. |
| 2 | n.c. | Not connected |
| 3 | +5V | +5V power |
| 4 | GND | The logic ground and power return |

## Serial ports (modem/printer)

The Macintosh Portable has two RS–422 serial I/O ports for printers, modems, and other standard serial I/O devices. Two mini-8 connectors on the computer's back panel are used for the serial ports. As shown in Figure 5-10, the modem port is labeled with a phone handset icon while the printer port is labeled with a printer icon. Figure 5-16 details the pin numbering of the mini-8 connectors.

The Macintosh Portable incorporates an internal modem connector. A compatible modem inserted into the modem slot connector is connected to the modem port. (Hardware supports the internal modem being switched to operate through either of the two ports, but firmware accomodates operation only through the modem port.)

An *external* modem may be connected to either the modem or the printer port when an internal modem is *not* used; the user of the Macintosh Portable makes a selection through the Control Panel. See Chapter 8, "Options," for details on the Apple modem and the interface to any card you might design to use in the modem slot connector.

The two serial ports are identical except that the modem port has a higher interrupt priority, making it more suitable for high-speed communication. See *Inside Macintosh*, Volume III or *Macintosh Family Hardware Reference* for additional details.

**Figure 5-16** Serial ports

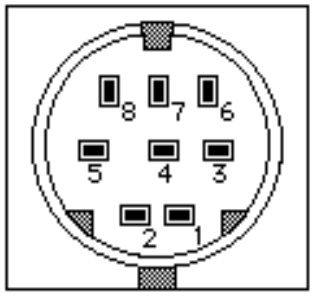



Table 5-19 shows the signal assignments for the serial ports.

**Table 5-19** Serial Port Signal Assignments

| Pin number | Signal name | Signal description |
|---|---|---|
| 1 | HSKo | Output handshake |
| 2 | HSKi | Input handshake or external clock |
| 3 | TxD– | Transmit data – |
| 4 | SG | Signal ground |
| 5 | RxD– | Receive data – |
| 6 | TxD+ | Transmit data + |
| 7 | GPi | General purpose input |
| 8 | RxD+ | Receive data + |

## Stereo phone jack

The stereo phone output is capable of driving headphones of 8 to 600 ohms and is short-circuit protected.

The connector is a miniature phone jack (receptacle) connector.

**Table 5-20** Stereo phone jack pinout

| Pin Number | Function |
|---|---|
| 1 | Ground |
| 2 | Left channel |
| 3 | Right channel |

### DC power input for the battery recharger

The power jack is the interface between the Macintosh Portable and the power adapter which recharges the battery. Table 5-21 provides the pinout.

**Table 5-21** Power Jack Pinout

| Pin Number | Function |
|---|---|
| 1 | + Battery voltage |
| 2 | – Battery return |
| 3 | No connection |

## 5.19 Battery recharger

The recharger is an enclosed, wall-mounted module provided with an AC input plug; a DC output cable terminates in a connector that mates with the battery recharger connector, whose location is shown in Figure 1-2.

**Table 5-22** Electrical Requirements

| Parameter | Minimum | Nominal | Maximum | Units |
|---|---|---|---|---|
| AC Input Voltage Range | 85 | 120/240 | 270 | VACrms |
| AC Input Frequency Range | 48 | 50/60 | 62 | Hz |
| DC Output Voltage Range | 7.0 | 7.5 | 7.6 | Volts |
| DC Output Current Range | 0.005 | 1.5 | 2.0 | Amperes |

...