5.6 Permanent RAM array

The RAM interface in the Macintosh Portable is designed to support between 1 MB and
5 MB of CMOS static RAM. The RAM is in two areas:

1) 1 MB permanent main memory soldered to the main logic board
2) Up to 4 MB of internally expandable RAM, on an optional memory expansion card

Permanent main memory is 1 MB total, and is arranged as a 512K x 16 bit array. This RAM array is located in the system memory map between addresses $00 0000 and $0F FFFF, and is overlayed by the system ROM after a system reset and before the first ROM access.

There is one 68HC000 processor wait state when accessing memory locations in permanent RAM. There is no device contention for permanent memory bandwidth other than the 68HC000, and because this memory array is built from static RAM there is no reason to refresh it, as would be the case for dynamic RAM.

Permanent main memory is battery backed-up when the Macintosh Portable is in the sleep state. This means that the contents of this memory array are retained when the computer is not in use, as long as the battery remains charged.

5.7 Permanent ROM array

The Macintosh Portable ROM is largely based on the Macintosh SE ROM, and includes bug fixes from the Macintosh SE ROM. It also includes a new ADB implementation, a new real-time clock implementation, code to support communication with the power manager, and code to support the various power-saving techniques that the Macintosh Portable incorporates.

The ROM interface on the Macintosh Portable is designed to support a minimum of 256 KB and an additional maximum of 4 MB of CMOS ROM. The ROM configuration is in two areas:

- 256 KB built-in, or permanent, ROM soldered to the printed circuit board
- Up to 4 MB of expansion ROM, using an internal connector. Expansion ROM address space is for you–the developer. See Macintosh Technical Note #255 for further details. (Also, see the "Internal ROM Expansion" section, later in this chapter).

Permanent ROM is 256 KB total, and is arranged as a 128K x 16 bit array. The array is physically made of two 128K x 8-bit devices.

This ROM array is word addressable and is located in the system memory map between addresses $90 0000 and $93 FFFF. Immediately after system reset, however, its starting address is located at both $90 0000 and $00 0000, to allow the 68HC000 to access a standard default set of exception vectors and trap addresses, as well as a starting address to begin executing code. This process is known as *RAM overlay* and is performed because it can be assumed that the contents of RAM are not in any known or deterministic state. The first access to $90 0000 (or any actual ROM addresses), however, will return RAM to $00 0000 and ROM will be located only at $90 0000.

There are two 68HC000 processor wait states when accessing memory locations in permanent ROM.

5.8 Memory Expansion

The growth of application program size makes it desirable to offer the RAM expansion cards described in this section, as well as others.

The Apple ROM expansion card has two functions which lead to its being called an upgrade and expansion card

- one side of the card contains a ROM to replace the one soldered to the main logic board, in case a code upgrade is necessary
- the other side of the card contains provisions for you, the developer, inserting ROM chips to utilize the address space shown as available in Figure 3-1

The RAM and ROM expansion connectors provide you with convenient access to the necessary signal lines in order to expand system memory.

Internal RAM Expansion

Internal RAM expansion is available through a single 50-pin connector (also called a slot). See Figure 5-5. All of the appropriate signals (address bus, data bus, and control) are brought up to the memory expansion board where they are decoded into chip selects, write signals, etc., by the RAM Expansion Buffer custom IC and routed to address and data buffers. Table 5-3 provides signal names and descriptions. Buffering the address and data bus is important to reduce capacitive loading.

The memory expansion board contains either 1 MB or 4 MB of static RAM, which allows for internal memory expansion to either a 2 MB machine or a 4 MB machine. Each expansion board is self-configured: no modifications (switches, jumpers, or other) to the main logic board are necessary to change the RAM configuration.

The 1 MB expansion card is arranged as a 512K x 16 bit array. The access time and cycle time for these devices is 100 ns.

The 4`MB expansion card is arranged as a 1.5 M x 16 bit array. The access time and cycle time for these devices is 100 ns.

This RAM array is located in the system memory map between addresses $10 0000 and $1F FFFF (for the 1 MB expansion card) and between $10 0000 and $3F FFFF (for the 3 MB expansion card). When installed, this memory array is always available and is unaffected by the state of the overlay bit (unlike permanent main memory).

There is one 68HC000 processor wait state when accessing memory locations in internal expansion RAM. Such an access requires a bus cycle time of nominally 320 ns. Like permanent main memory, there is no device contention for bandwidth other than the 68HC000, and because this memory array is built from static RAM there is no reason to refresh it, as would be the case for dynamic RAM.

Also like permanent main memory, internal expansion memory is battery backed-up when the Macintosh Portable is in the sleep state. This means that the contents of this memory array are retained when the computer is not in use, as long as the battery remains charged.

Figure 5-5 Internal RAM expansion connector

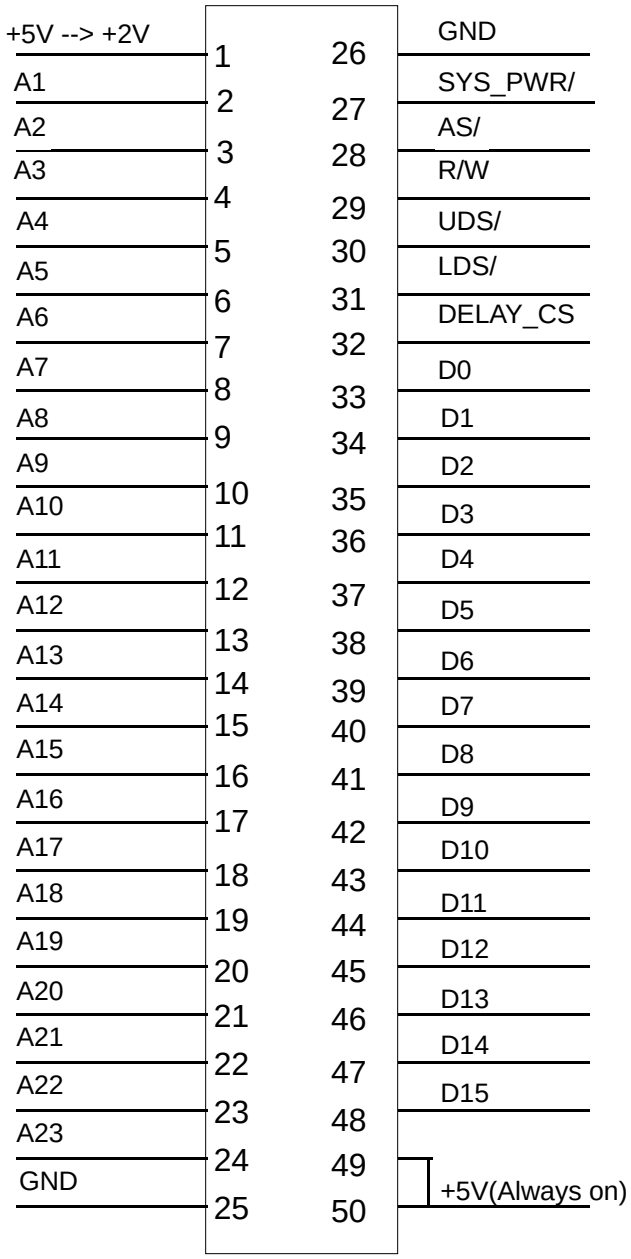


Table 5-3 Internal RAM Expansion Connector Signals

Pin Number	Name	Description
1	+5V	Vcc
2–24	A1–23	Unbuffered 68HC000 address signals A1–23
25–26	GND	Logic ground
27		/SYS_PWR This signal controls whether the CPU is in the active or sleep state.
28	/AS	68HC000 address strobe signal
29	R/W	Permanent ROM CS/ signal
30	/UDS	16 MHz system clock
31	/LDS	External DTACK/ signal that is an input to the Coarse Address Decode chip
32		DELAY_CS This signal is generated by the Coarse Address Decode chip and is used to put the RAM array into the idle mode
33–48	D0–15	68HC000 unbuffered data signals D0:15
49–50	+5V	Vcc

Internal ROM Expansion

Up to 4 MB of expansion ROM address space is available. The expansion ROM array is expandable to any size or capacity that fits into the expansion address space. The implementation of expansion ROM is very similar to that of internal expansion RAM (i.e., circuitry for decoding, control, and buffering must be part of the expansion board) except that the number of wait states is controlled by the expansion board (instead of the Coarse Address Decode and GLU chip, as is the case for RAM) via an external DTACK signal that is an output of the ROM expansion card.

ROM expansion is available through a single 50-pin connector (slot). See Figure 5-6. All of the appropriate signals (address bus, data bus, and control) are brought up to the memory expansion slot where they are decoded into chip selects, and also routed to address and data buffers. Table 5-4 provides signal names and descriptions. Buffering the address and data bus is important to reduce capacitive loading.

Replacing or upgrading the permanent ROM soldered to the main logic board is possible by using this same mechanism. By installing a board into the ROM expansion slot, and using the same /ROM CS signal that controls permanent ROM, a virtual replacement for the on-board ROM can be implemented.

Figure 5-6 Internal ROM Expansion Connector

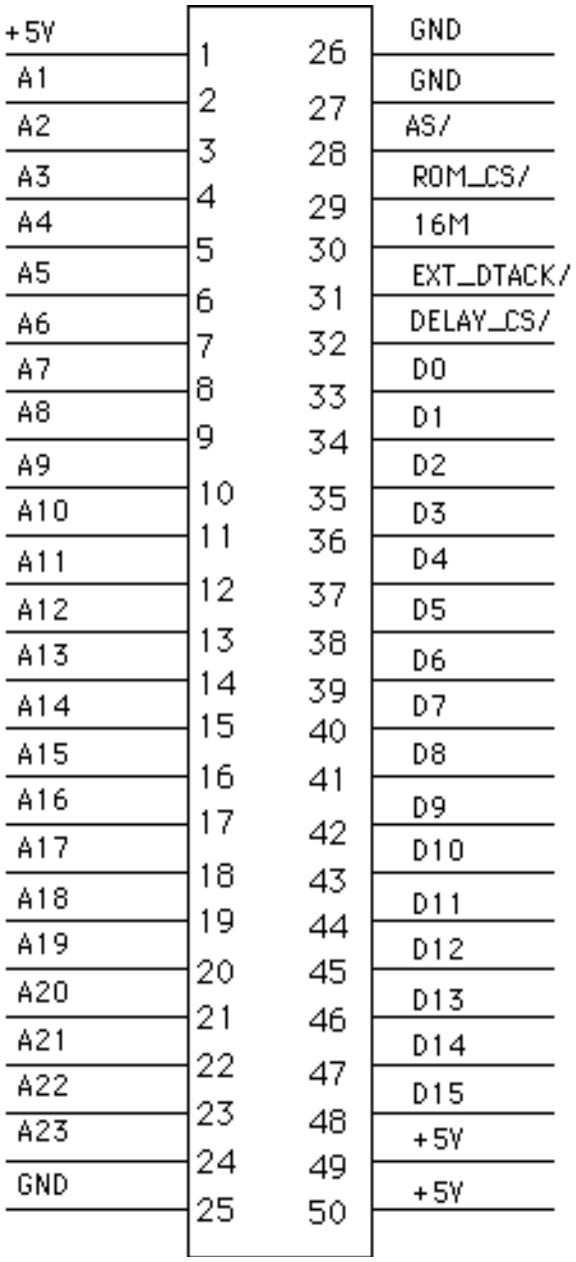


Table 5-4 Internal ROM Expansion Connector Signals

Pin Number	Signal Name	Signal Description
1	+5V	Vcc
2–24	A1–23	Unbuffered 68HC000 address signals A1–23
25–27	GND	Logic Ground
28	/AS	68HC000 address strobe signal
29	/ROM.CS	Permanent ROM chip select signal
30	16M	16 MHz system clock
31	/EXT.DTACK	External /DTACK signal that is an input to Coarse Address Decode chip
32	DELAY.CS	This signal is generated by Coarse Address Decode chip and is used to put the RAM array into the idle mode
33–48	D0–15	68HC000 unbuffered data signals D0–15
49–50	+5V	Vcc

ROM expansion jumper on the main logic board

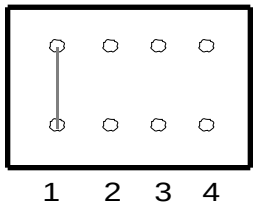
Figure 5-7 shows a detailed view of the jumper block on the Macintosh Portable main logic board. Jumpers are required in positions 1 or 2, and in position 3 when ROM on an expansion card is to replace the ROM soldered on the main logic board. Jumper 4 is used when an alternative power manager processor chip is mounted on a card inserted into the ROM expansion slot.

Figure 5-7 Internal ROM Expansion Jumper (see also Figure 1-2)

Jumper(s) Inserted
In Position Number

1) 2 wait-state ROM access
or
2) 1 wait-state ROM access

3) system ROM on expansion card
4) on-board power manager processor access



5.9 Coarse Address Decode and GLU

The Coarse Address Decode and GLU chip is a custom gate array designed as a generalized logic chip for the Macintosh Portable. It does coarse address decodes to system RAM and ROM as well as the SCC, SCSI, VIA, SWIM, and Video Display Interface peripheral chips. It controls the transmission direction of the RAM data buffers and generates upper and lower RAM write strobes. It also provides several support functions such as the CPU clock generator, sleep state circuit, and DTACK generator.

5.10 Fine Address Decode and GLU

The Fine Address Decode and GLU chip is a custom CMOS gate array chip that accepts partially decoded addresses from the Coarse Address Decode and GLU chip and further decodes them to generate the chip selects for RAM. It also provides power manager timing signals, floppy disk drive enable signals, and serial port output signals.

5.11 VIA interface

The VIA is a 65C22A or 65C23 (depending on the manufacturer) CMOS Versatile Interface Adapter containing multiple registers. Which of these registers drives the 68000 data lines (a CPU read) or is driven by them (a CPU write) is determined by the four RS (Register Select) pins which are connected to four CPU address lines. Register A connects to the 8-bit I/O bus of the power manager processor, and it is through this port that the communication between the power manager and the central processor takes place. Another function of the VIA is synchronous and asynchronous

generation of interrupts (for display vertical blanking every page scan, one-second intervals from the real-time clock, SCSI pseudo-DMA, and power manager initiated interrupts of the CPU). Control functions affect floppy disk head selection and serial communications controller write signaling.

5.12 SCSI Interface

The Small Computer System Interface (SCSI) consists of the NCR 53C80 chip between the CPU and an external DB-25 connector. Multiple SCSI devices may be connected to the SCSI bus through this connector; the 53C80 accomplishes the bus arbitration to allocate access to the 68HC000 central processor. An internal SCSI connector is used for connection to the optional internal hard disk drive.

The pinout for the external connector is shown in Table 5-5, and the pinout for the internal connector in Table 5-6.

▲ **WARNING:** Any internal hard drive connected to the Macintosh Portable SCSI bus should be a low-power version in order to maximize operating time per battery charge. ▲

The NCR 53C80 is a CMOS device designed to support the SCSI as defined by the American National Standards Institute (ANSI) X3T9.2 Committee. This device supports arbitration of the SCSI bus, including reselection. The chip is controlled through a set of read and write registers that are byte addressable only, and which are accessed through the SCSI Manager

The SCSI bus consists of eight data lines, a parity line, and nine control signal lines; the remaining connector pins are for power (supplied by the terminating device) or ground. A pseudo-DMA mode allows read and write transfers at the faster bus-limited speed, without processor control of every byte transfer. This interface is unchanged from that in the Macintosh SE, except that the Macintosh Portable does *not* supply the termination power.

The NCR 53C80 is connected directly to both the internal and external connectors and is capable of sinking 48 mA through each of the pins connected to the bus. The data and control lines on the SCSI bus are active low signals driven by open-drain outputs.

Termination power is *not* supplied by the Macintosh Portable, therefore it cannot be expected that the bus will remain in a known state if all external SCSI devices are powered off. The normal termination configuration connection is a 220Ω resistor to +5V and a 330Ω resistor to ground on each of the active signals. The internal SCSI connector is an exception to this scheme, however. Internal termination is supplied by the drive itself and is configured as a single-ended 1.3KΩ pull-up resistor to +5V.

■ **Table 5-5** SCSI External Connector Pinout

Connector Pin Number	SCSI Bus Name	53C80 Pin Name
1	/REQ	/REQ
2	/MSG	/MSG
3	I/O	/I/O
4	/RST	/RST
5	/ACK	/ACK
6	/BUSY	/BSY
7	GND	
8	/DATA0	/DB0
9	GND	
10	/DATA3	/DB3
11	/DATA5	/DB5
12	/DATA6	/DB6
13	/DATA7	/DB7
14	GND	
15	C/D	/C/D
16	GND	
17	/ATN	/ATN
18	GND	
19	/SEL	/SEL
20	/PARITY	/DBP
21	/DATA1	/DB1
22	/DATA2	/DB2
23	/DATA4	/DB4
24	GND	
25	NO CONNECTION	

Table 5-6 SCSI Internal Connector Pinout

Connector Pin Number	SCSI Bus Name
1	/REQ
2	GND
3	/MSG
4	/C/D
5	/I/O
6	GND
7	/ACK
8	/ATN
9	/BSY
10	/RST
11	GND
12	/SEL
13	/DBP
14	/DB0
15	/DB1
16	GND
17	/DB2
18	/DB3
19	/DB4
20	/DB5
21	/DB6
22	/DB7
23	+5V
24	+5V
25	+12V
26	+12V
27	GND
28	GND
29-30	MOTOR GND
31-32	+12 V (MOTOR)
33-34	+5 V (MOTOR)