Chapter 1 Macintosh Classic II Hardware

The Macintosh Classic II computer is a low-cost, compact Macintosh computer that provides approximately 2.5 times the performance of a Macintosh Classic. It appeals to a wide range of markets, including educators, homes, and businesses. This developer note describes the major features of the Macintosh Classic II computer and emphasizes
the differences between it and other members of the Macintosh computer family.

Major features

The Macintosh Classic II computer includes the following features:

- Microprocessor: MC68030 running at 15.6672 MHz.
- Read-only memory (ROM): 512 KB socketed to main logic board. ROM can be expanded to 1 or 2 MB on the main logic board. Additional ROM can also be installed on an FPU/ROM card.
- Random-access memory (RAM): 2 MB soldered to main logic board; 2 SIMM (Single In-line Memory Module) sockets for expansion to 10 MB.
- Floppy disk: One internal 20-pin floppy disk connector. One internal 1.4 MB Apple SuperDrive with SWIM (Super Woz Integrated Machine) interface is standard. A second 1.4 MB SuperDrive can be installed externally as an option.
- Hard disk: One internal SCSI (Small Computer System Interface) hard disk is standard. A SCSI hard disk can also be installed externally as an option.
- Input/output (I/O): One ADB (Apple Desktop Bus) port, two mini-DIN 8 serial ports, one SCSI port, one audio output jack (for headphone or external speaker), one
  audio input jack (for microphone or line input), and one external DB-19 floppy
  disk connector.
- Video display: Built-in 9-inch monitor provides 512 x 342 x 1 monochrome display (same as in Macintosh Classic).
- Sound: Monaural sound output system similar to Apple Sound Chip and identical to Macintosh LC. The sound circuitry has also been enhanced to provide a sound input capability. Sound from a microphone or line input is sampled at a rate of 22 kHz or 11 kHz, digitized, and stored along with other data to be used for a variety of purposes such as presentations or the creation of “living” documents. The microphone is included with the Macintosh Classic II computer as standard equipment.
- Optional FPU/ROM card: A 50-pin connector on the main logic board accommodates a card with an MC68882 FPU (floating-point unit) coprocessor or (optional) additional ROM. The Macintosh Classic II computer does not include a PDS (processor-direct slot) connector.
- Keyboard: A detached ADB keyboard with numeric keypad and ADB mouse (same as in the Macintosh Classic).

Design differences

Although the physical appearance of the Macintosh Classic II computer is very similar to that of the Macintosh Classic, the electrical design of the Macintosh Classic II is based as much as possible on the Macintosh LC architecture. Figure 1-1 is an overall block diagram of the Macintosh Classic II. Notice that the number of components has been significantly reduced through the use of custom integrated circuits. The following are the major changes in the Macintosh Classic II design:

- The Macintosh Classic II uses an MC68030 processor rather than the MC68020 used by the Macintosh LC.
- A new custom VLSI (very large-scale integration) chip, the EAGLE gate array, is the heart of the hardware design. It integrates the timing, memory mapping, video generation, clock generation, sound control, and glue functions that were provided by individual chips in the earlier Macintosh computers.
- The Macintosh Classic II uses the same ADB microcontroller as the Macintosh LC and the Macintosh IIsi. This single-chip Motorola 68HC05 microcontroller integrates the functions of ADB interface, real-time clock, power-on reset, parameter RAM storage, and keyboard-controlled reset and NMI (nonmaskable interrupt). On the Macintosh Classic II, the NMI and reset functions can also be hardware controlled by the programmer's switch and the reset switch. The ADB microcontroller also controls the DFAC (digital filter audio chip), a custom IC that performs the analog processing functions of the sound system.
- A custom chip (Combo), identical to the Combo chip in the Macintosh LC, combines the functions of the SCC (Serial Communications Controller) and the SCSI in a single device that is completely compatible with the SCC (85C30) and SCSI (53C80) chips that were used in earlier Macintosh computers.

■ **Figure 1-1** Block diagram of the Macintosh Classic II computer

- Two SIMM sockets allow RAM expansion in increments of 2 MB, 4 MB, and 8 MB. This feature, which is similar to RAM expansion on the Macintosh LC, provides more RAM expansion than in the Macintosh Classic.
- A sound input capability, similar to that in the Macintosh LC, has been added to the sound system. Like that in the Macintosh LC, the Macintosh Classic II sound system does not support wavetable mode.
- Software is required to reset the SCC (hardware reset is not provided).
- The brightness CDev uses a modified brightness driver in ROM to control screen brightness in the same manner that brightness is controlled in the Macintosh Classic.

Compatibility issues

This section describes issues that may affect system compatibility.

ADB implementation

The Macintosh Classic II uses a custom chip to integrate the ADB and a number of other functions, including the real-time clock, parameter RAM, power-on reset, keyboard reset, and NMI. This implementation is described later in the section "Apple Desktop Bus (ADB) Microcontroller." If you have developed applications that address the ADB hardware directly, they will probably not function under this new scheme. Also, you will have to revise debuggers to support the keyboard-based NMI.

SCSI and SCC implementation

A Combo chip combines the functions of SCSI and SCC. This chip, which is also used in the Macintosh LC, is described later in the section "SCSI and SCC Interfaces." Although the Combo chip is software-compatible with the previous implementation of these functions, if your applications attempt to access the hardware directly, they will probably be inoperable.

Sound input/output hardware

Details on the Macintosh Classic II computer's sound system implementation are provided later in the section "Sound Interface." The Macintosh Classic II implements a subset of the Apple Sound Chip (ASC), but, unlike previous ASC-equipped Macintosh computers, it supplies only monaural sound output. If your application uses the Sound Manager calls and does not try to access the sound hardware directly, your application will work as documented; however, if your application tries to direct sound to the unused (right) stereo channel, it will not produce any sound. Also, the Macintosh Classic II does not support the wavetable sound output mode used on previous Macintosh computers. If your application addresses the wavetable hardware directly, the application will not work on the Macintosh Classic II. To ensure that your application operates properly, Apple strongly advises that you use the Sound Manager routines. Applications using the older Sound Driver software will not be compatible with the Macintosh Classic II.

No on-board mathematics coprocessor (FPU)

Although the Macintosh Classic II does not include an FPU as a standard feature, the EAGLE gate array provides the necessary decoding for an optional FPU. You can design an FPU/ROM card for the FPU/ROM connector because the FPU select signal is supplied to the FPU/ROM connector. FPU/ROM card design guidelines are provided later in the section "FPU/ROM Connector."

Application software should not assume that the Macintosh Classic II has an FPU simply because it uses an MC68030 microprocessor. To ensure that your application is compatible with Macintosh Classic II and future Macintosh computers that do not have FPUs, use the Gestalt Manager (the successor to SysEnvirons). This will allow you to determine the exact configuration of the machine on which you are running.

Your application should first check for the presence of an FPU if the application is provided in two versions, one that uses SANE (Standard Apple Numerics Environment) software and another that requires the FPU hardware to perform its numeric calculations, or if it makes a conditional branch to execute floating-point instructions directly.

Hardware overview

This section provides a functional description of the Macintosh Classic II computer's
hardware systems.

△ **Important** Memory sizes, addresses, and other data are specific to each type of Macintosh computer and are provided for informational purposes only. To ensure that your application software maintains compatibility across the Macintosh line and to allow for future changes to the Macintosh Classic II hardware, you are strongly
advised to use Macintosh Toolbox and Operating System routines wherever provided. In particular, never use absolute addresses
to access hardware, because these addresses are different on
different models. △

Main processor

The Macintosh Classic II uses an MC68030 microprocessor running at a system clock speed of 15.6672 MHz. Processing speed varies significantly depending on whether you are accessing ROM or RAM.

EAGLE gate array

The EAGLE gate array is a new custom chip that implements many functions that were provided by individual chips in earlier Macintosh computers. These functions include timing, video generation, memory mapping, sound, clock generation, and miscellaneous GLU (general logic unit) functions. For example, the Macintosh IIci included an RBV (RAM-based video) chip, an MDU (memory decode unit) chip, a VIA (Versatile Interface Adapter) chip, and an ASC. Functions similar to these are now integrated into the EAGLE gate array.

Address decode and memory mapping

One of the EAGLE gate array's most important functions is providing address decode
and memory mapping functions for the Macintosh Classic II computer. The EAGLE implements two memory address mapping modes, a 24-bit mode and a 32-bit mode (see Table 1-1). As in other Macintosh computers, a function code control bit determines which map is to be used in the Macintosh Classic II.

△ **Important** The addresses shown in this section apply only to the Macintosh Classic II computer, and only for the version of the ROM current at the time of publication of this developer note. It is highly recommended that you use the Macintosh Toolbox calls, system traps, and global variables listed in *Inside Macintosh* to access the hardware. △

Notice that in the 24-bit mode, the highest address byte (8 bits) is not used, and all addresses appear as 32-bit logical addresses. The same address can be used in either 24-bit or 32-bit modes. This addressing scheme is similar to the one used in the Macintosh LC.

A bus error results if you try to access address $FF FFFF in the 24-bit mode or to address $FFFF FFFF in the 32-bit mode.

■ **Table 1-1** Memory map summary

Function	24-bit mode	32-bit mode
RAM		
2 MB	$00 0000–$1F FFFF	$0000 0000–$001F FFFF
4 MB	$00 0000–$3F FFFF	$0000 0000–$003F FFFF
6 MB	$00 0000–$5F FFFF	$0000 0000–$005F FFFF
10 MB	$00 0000–$9F FFFF	$0000 0000–$009F FFFF
Video main page	$9F 9A80–$9F F000	$009F 9A80–$009F F000
ROM	$A0 0000–$AF FFFF	$40A0 0000–$40AF FFFF
Expansion FPU/ROM	$B0 0000–$DF FFFF	$40B0 0000–$40DF FFFF
I/O space	$F0 0000–$FF FFFF	$50F0 0000–$50FF FFFF

◆ *Note:* Table 1-1 shows the default condition of 1 MB of on-board ROM and 3 MB of expansion FPU/ROM address space. When the ROM SELECT signal is low (jumper installed), ROM addresses are located in 32-bit address space from $40A0 0000 to $40BF FFFF, and expansion FPU/ROM slot addresses are located in 32-bit address space from $40C0 0000 to $40DF FFFF. See Table 1-2 for details.

VIAs

The EAGLE includes a full-function VIA1, a pseudo-VIA2 that consists of registers similar to those that were implemented in the RBV of the Macintosh IIci, and several registers similar to the registers in the Apple Sound Chip. The Macintosh Classic II computer uses these functions to connect the MC68030 processor to the necessary control functions.

ROM

The Macintosh Classic II computer's main ROM is implemented as four 32-pin, 128K x 8-bit ICs (integrated circuits) providing a standard configuration of 512 KB of read-only memory. By using a configuration of four 256K x 8-bit ICs, you can fill the 1 MB of address space that is reserved for main ROM at locations $40A0 0000 through $40AF FFFF. The default condition for the system ROM is 1 MB on the main logic board and 3 MB on an FPU/ROM card. By installing the ROM SELECT jumper on connector J9, you can change the allowable configuration to 2 MB on the main logic board and 2 MB on an FPU/ROM card. The addresses allocated for main ROM and expansion card ROM in both the default and jumpered conditions are shown in Table 1-2. For more information on the design of an FPU/ROM card, see the section "FPU/ROM Connector" later in this chapter.

■ **Table 1-2** ROM address allocations

Condition	Main ROM	FPU/ROM-card
Default	$40A0 0000–$40AF FFFF	$40B0 0000–$40DF FFFF
With jumper	$40A0 0000–$40BF FFFF	$40C0 0000–$40DF FFFF

Power-on overlay function

The Macintosh Classic II, like all other Macintosh computers, implements an overlay function at power up or reset that maps ROM address space (in this case, $40A0 0000 through $40DF FFFF) to RAM space starting at location $0000 0000. Following the first access to the normal ROM address range, the ROM image at $0000 0000 is cleared and replaced by RAM.

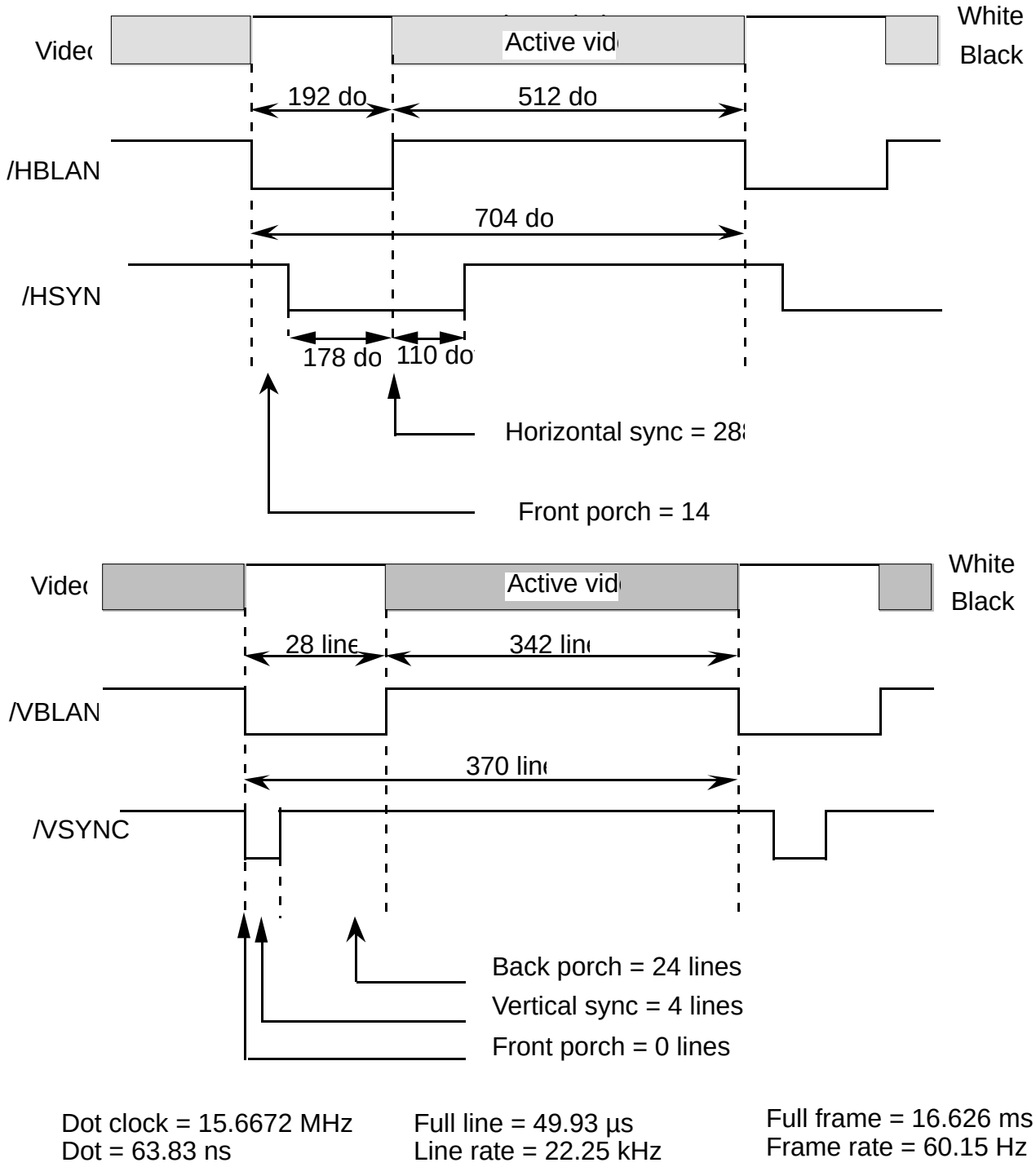
RAM

Although the first 10 MB of address space is reserved for RAM, the Macintosh Classic II is shipped with only 2 MB of RAM soldered to the main logic board. Two SIMM sockets allow you to expand the RAM by 2 MB, 4 MB, or 8 MB. Both of the SIMM sockets must be loaded with the same size SIMM modules (for example, 1 MB, 2 MB, or 4 MB). The EAGLE chip generates the DSACK (data transfer and size acknowledge) signal for all accesses to RAM. Three bits in the EAGLE chip's expansion register are set by the software at power on to indicate the actual size of the RAM.

Video

The Macintosh Classic II is designed to support a 512 x 342 x 1-bit built-in monochrome display. It does not include support for any type of external monitor. All video timing is generated by the EAGLE gate array. Memory is shared by the MC68030 processor and the video controller located in the EAGLE chip. Figure 1-2 shows the timing for the 512 x 384 video display. The figure illustrates the blanking, synchronizing, and active video regions of the video scan waveforms in terms of dot or pixel times. A dot is the time required to draw a single pixel.

■ **Figure 1-2** 512 x 342 video timing



Dot clock = 15.6672 MHz
Dot = 63.83 ns

Full line = 49.93 µs
Line rate = 22.25 kHz

Full frame = 16.626 ms
Frame rate = 60.15 Hz

Sound interface

The Macintosh Classic II sound system includes a built-in speaker; an external stereo headphone jack, which plays in mono but to both ears, and a microphone input jack for the sound input feature. A microphone is included with the system.

The sound system in the Macintosh Classic II is similar to the Macintosh Plus and Macintosh SE sound systems in that main memory is used for the sound buffer. Because the Macintosh Classic II computer's video modes have different line times than those of the Macintosh Plus, the Macintosh Classic II sound system has its own timing chain, which samples at the same 44-microsecond rate used in the older Macintosh machines and also generates the 60.15-Hz interrupt that is produced by all Macintosh computers.

The EAGLE chip includes a subset of the Apple Sound Chip for accessing the sound buffer in main memory. A FIFO (first in, first out) memory controlled by the EAGLE is used for sound playback and recording, but the memory used for the FIFO sound buffer is part of the system main memory.

Sound input feature

In addition to sound output, the Macintosh Classic II provides a sound input feature that allows sounds to be recorded digitally. Also, by using a playthrough feature, you can mix an external audio source with computer-generated sound and play it back through a speaker or headphones.

- *Note: Inside Macintosh,* Volume VI, explains the application-programmer interface for the Sound Input Manager and describes the high-level and low-level calls that you can implement in your application programs to allow users to take advantage of the Macintosh Classic II computer's sound input feature.

The DFAC is a custom IC that does the analog processing functions for the sound system. The DFAC contains a switched filter capacitor, an A/D converter, and switching and amplifier circuits. A shift register in the 65HC05 microcontroller provides to the DFAC 8 bits that control the routing of the analog sound signals through the system.

The setting of the 8 DFAC control bits determines the mode of sound operation. The three most commonly used modes are sound playback with playthrough, sound playback, and sound record.

Sound playback with playthrough: This mode provides sound output and is used most often. Because the Macintosh Classic II has sound input capability, you can also use this mode to add digitized sound input to normal Macintosh sound. For example, you can
play a line-level input through the built-in speaker concurrently with computer-generated sounds.

Sound playback: This mode permits only sound output. It is identical to the sound output implementation used in most other Macintosh computers. Sound playback is used primarily as a backup to sound playback with playthrough in case that mode does not give good sound quality.

Sound record: This mode takes advantage of the sound input feature and is the method normally used to record sound.

SCC and SCSI interfaces

A custom chip called Combo combines the functions of the SCC and the SCSI controller in a single device. This device is completely software compatible with the SCC (85C30) and SCSI (53C80) chips it replaces.

SCC

The SCC portion of the combination SCC/SCSI device includes two independent ports for serial communication. Each port can be independently programmed for asynchronous, synchronous, or AppleTalk protocols.

Two 8-pin miniature DIN connectors connect the SCC to the external world. The connectors are the same as those currently used on other Macintosh II–family computers. Table 1-3 shows the pinout for the serial ports. Notice that pin 7 is used as a general-purpose input, the same purpose it has in the Macintosh SE and the Macintosh II. However, in the Macintosh Classic and Macintosh LC, this pin is not connected,
resulting in limited support for synchronous modems.

Table 1-3 Serial port pinout

Pin number	Signal description
1	Handshake output
2	Handshake input
3	Transmit data –
4	Ground
5	Receive data –
6	Transmit data +
7	General-purpose input (GPI)
8	Receive data +

SCSI

The SCSI portion is completely compatible with the SCSI controller chip used on current members of the Macintosh II family. It is designed to support the SCSI interface as defined by the American National Standards Institute (ANSI) X3T9.2 committee. In addition to the SCSI portion of the combined SCC/SCSI device, the interface consists of an internal 50-pin ribbon connector and an external DB-25 connector (see Table 1-4).

The new combination chip provides certain advantages to the SCSI interface, including

- less susceptibility to noise on the bus, which could cause faulty data transactions
- internal protection that helps to reduce failures caused by ESD (electrostatic discharge)

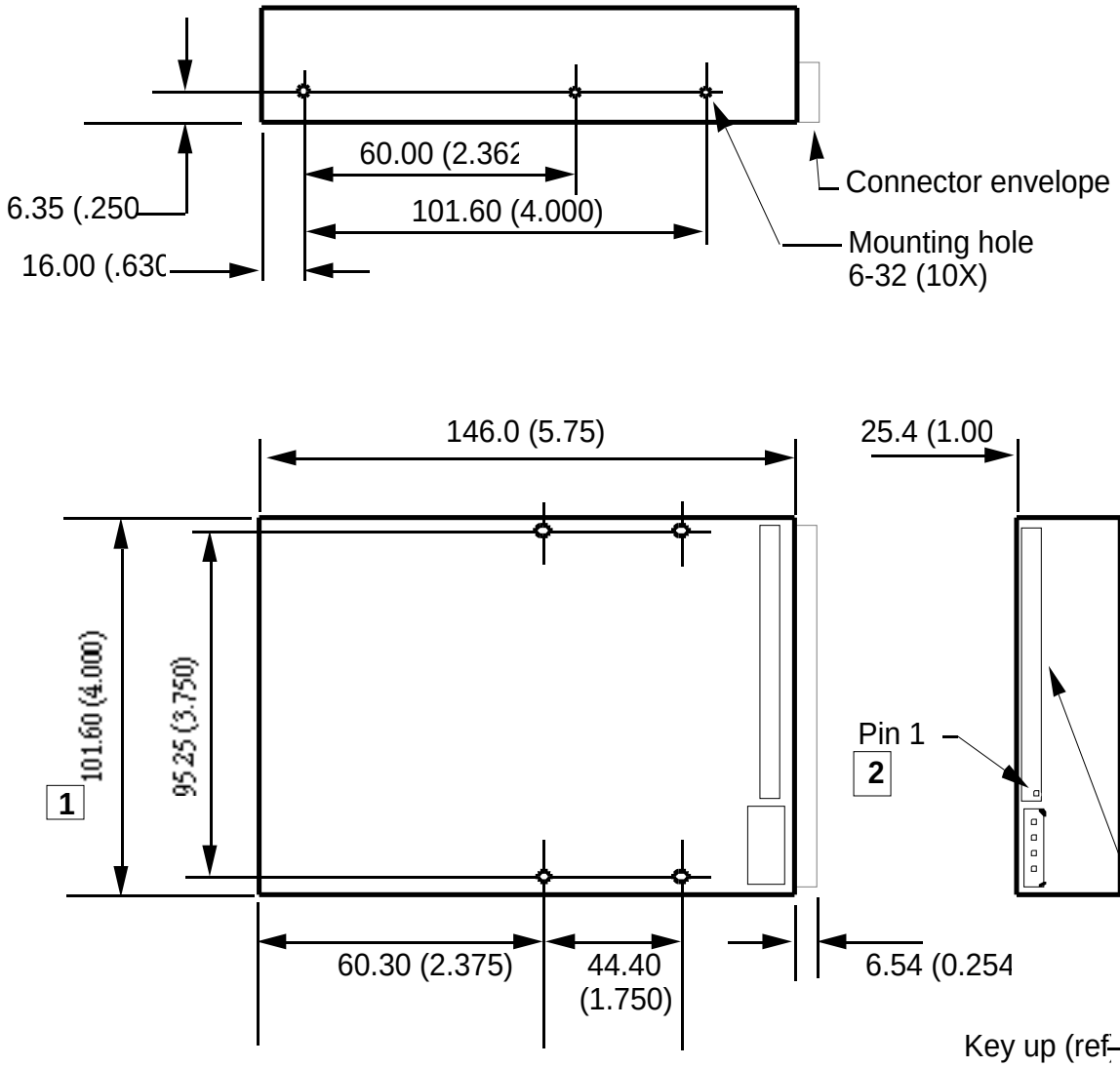
■ **Table 1-4** Pinouts for internal and external SCSI connectors

Internal (50-pin)	External (25-pin)	Signal name
48	1	/REQ
42	2	/MSG
46	15	/C/D
50	3	/I/O
40	4	/RST
32	17	/ATN
38	5	/ACK
36	6	/BSY
44	19	/SEL
18	20	/DBP
2	8	/DB0
4	21	/DB1
6	22	/DB2
8	10	/DB3
10	23	/DB4
12	11	/DB5
14	12	/DB6
16	13	/DB7
26	25	TPWR
All odd pins (25 total)	7, 9, 14, 16, 18, and 24	GND

Hard disk drive dimensions and mounting requirements

Figure 1-3 shows the drive and connector envelope and mounting hole requirements for the hard disk drive. The drive and its mating connectors are constrained to the envelope shown.

■ **Figure 1-3** Envelope requirement for 3.5-inch hard disk drive



Notes:

1. Dimension to be measured at centerline of side mount hol
2. 50-pin SCSI and 4-pin power connector placement may be reversed.
3. Tolerances: X = +/–
   XX = +/– .:

Floppy disk interface

A single SWIM chip controls one internal 3.5-inch SuperDrive as well as an optional external floppy disk drive. A 20-pin connector provides the signal interface between the
SWIM chip and the internal drive. A DB-19 connector on the back of the Macintosh Classic II case provides the interface with an external drive. Table 1-5 shows the pinout
for the internal floppy disk connector. Table 1-6 shows the pinout for the external floppy disk connector.

■ **Table 1-5** Pinout for internal floppy disk connector

Pin number	Signal name	Signal description
1	GND	Ground
2	PH0	Phase 0: state control line
3	GND	Ground
4	PH1	Phase 1: state control line
5	GND	Ground
6	PH2	Phase 2: state control line
7	GND	Ground
8	PH3	Phase 3: register write strobe
9	n.c.	Not connected
10	/WRREQ	Write data request
11	+5V	+5 V
12	SEL	Head select
13	+12V	+12 V
14	/ENBL	Drive enable
15	+12V	+12 V
16	RD	Read data
17	+12V	+12 V
18	WR	Write data
19	+12V	+12 V
20	+5V	+5 V

■ **Table 1-6** Pinout for external floppy disk connector

Pin number	Signal name	Signal description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	–12V	–12 V
6	+5V	+5 V
7	+12V	+12 V
8	+12V	+12 V
9	n.c.	Not connected
10	PU	Pull up
11	PH0	Phase 0: state control line
12	PH1	Phase 1: state control line
13	PH2	Phase 2: state control line
14	PH3	Phase 3: register-write strobe
15	/WRREQ	Write data request
16	SEL	Head select
17	/ENBL2	External drive enable
18	RD	Read data
19	WR	Write data

Apple Desktop Bus (ADB) microcontroller

The Macintosh Classic II computer uses the same custom microprocessor that is used in the Macintosh LC and the Macintosh IIsi to integrate the functions of the ADB controller, RTC (real-time clock), PRAM (parameter RAM), power-on reset, and keyboard reset and NMI. In previous Macintosh models, these functions were provided by separate devices on the main logic board.

◆ *Note:* The Macintosh Classic II computer case also includes switches (commonly called programmer's switches) that permit hardware control of the reset and NMI functions.

Apple Desktop Bus interface

The ADB is a single-master, multiple-slave, serial communication bus that uses an asynchronous protocol and connects keyboards, graphics tablets, mouse devices,
and other devices to the Macintosh Classic II. The custom ADB microcontroller drives
the bus and reads status from the selected external device. A 4-pin miniature DIN connector connects the ADB controller to the outside world. Table 1-7 shows the
ADB connector pinout.

■ **Table 1-7** ADB connector pinout

Pin number	Name	Description
1	ADB	Bidirectional data bus used for input and output; open-collector signal pulled up to +5 V through 470 Ω resistor on main logic board.
2	PSW	Power-on signal that generates reset and interrupt key combinations.
3	+5V	+5 V from computer. 1-amp fuse at output satisfies safety requirements.
4	GND	Ground from computer.

Real-time clock and parameter RAM

The custom ADB microcontroller provides the functions of the RTC and the PRAM. The microcontroller includes a 32-bit counter that operates similarly to the existing RTC chip used in other members of the Macintosh II family. A backup battery allows the ADB microcontroller to continue counting and preserves the PRAM data even when the Macintosh Classic II is powered off.

Low-level access to the RTC or PRAM is different from that in previous Macintosh computers. It is accomplished through modified ADB-style commands. Applications that use existing traps to read and write to the RTC and the PRAM will continue to work on the Macintosh Classic II without any problems. However, any software that attempts to address the hardware directly will not work unless the software is modified.

Power-on reset

When the ADB microcontroller turns the power supply on, it also asserts the reset signal. The reset signal, which goes to the processor and other I/O devices, allows the processor to stabilize before executing any cycles.

Keyboard reset and NMI

Although there are hardware switches for controlling the reset and NMI functions, these functions may also be controlled from the keyboard by the custom ADB microprocessor. You can assert the NMI signal by pressing the Command key and the power button at the same time. NMI is a diagnostic signal that enables the debugging software to halt execution of an application and change to a debugger for low-level software and hardware testing. You can assert a hard reset, identical to a power-on reset, by pressing the Command key, Control key, and power button at the same time. The NMI and reset key sequences were chosen for compatibility with currently existing Macintosh utility software.

FPU/ROM connector

The main logic board on the Macintosh Classic II computer includes a 50-pin connector referred to as the FPU/ROM connector. This feature allows third-party developers to design a card that can provide a 68882 FPU coprocessor or additional ROM. All necessary signals including address, data, FPU select, on-card ROM enable, read/write, data strobe acknowledge, reset, and the system clock are provided to the FPU/ROM connector. Another signal, ROM select, is used in conjunction with a jumper on J9 to control the ROM configuration. Two ROM configurations are possible:

- If the jumper is not connected (default condition) and the ROM select signal is high, you can have 3 MB of additional ROM on the FPU/ROM card but only 1 MB of main ROM socketed to the main logic board.
- If you connect the jumper and the ROM select signal is low, you can have only 2 MB of additional ROM on the FPU/ROM card and 2 MB of main ROM socketed to the main logic board.

△ **Important** Apple strongly discourages the development of a third-party FPU/ROM card for any type of internal expansion other than a 68882 FPU coprocessor or additional ROM. This includes any internal hardware modifications such as clipping on to the main processor. Following are several reasons why you should not use the FPU/ROM card for other types of internal development:

- The power budget for the Macintosh Classic II computer does not allow any margin for additional internal devices.
- The Macintosh Classic II computer's cooling fan has insufficient capacity to dissipate the excess heat that may result.
- Electromagnetic interference (EMI) testing did not take into account the possibility of additional internal devices or the fact that antennae are created whenever additional external cabling is added.
- Any additional load on the Macintosh Classic II computer's data lines could result in noise leading to data errors and unreliable software.
- The address space assigned to the FPU/ROM connector was originally envisioned to support additional ROM therefore, it will support only read access.

The development of an FPU/ROM card for any type of internal expansion other than an FPU or a ROM will not be supported by Apple Developer Technical Support (DTS) and may void Apple's customer warranty. △

Electrical description of the FPU/ROM connector

The FPU/ROM connector is a 50-pin straight socket connector. Figure 1-4 is a pinout of the FPU/ROM connector. Table 1-8 gives the pin number, signal name, description, and load capacity of each signal supplied to the FPU/ROM connector.

■ **Figure 1-4** Pinout of FPU/ROM connector

■ **Table 1-8** Signals on the FPU/ROM connector

Pin number	Signal name	Direction	Description	Load capacity
1	+5V	VDD	+5 V	800 mA
2	A11	I/O	Address bit 11	100 µA/8 mA
3	A1	I/O	Address bit 1	100 µA/8 mA
4	A12	I/O	Address bit 12	100 µA/8 mA
5	A2	I/O	Address bit 2	100 µA/8 mA
6	A13	I/O	Address bit 13	100 µA/8 mA
7	A3	I/O	Address bit 3	100 µA/8 mA
8	A14	I/O	Address bit 14	100 µA/8 mA
9	A4	I/O	Address bit 4	100 µA/8 mA
10	A15	I/O	Address bit 15	100 µA/8 mA
11	A5	I/O	Address bit 5	100 µA/8 mA
12	A16	I/O	Address bit 16	100 µA/8 mA
13	A6	I/O	Address bit 6	100 µA/8 mA
14	A17	I/O	Address bit 17	100 µA/8 mA
15	A7	I/O	Address bit 7	100 µA/8 mA
16	A18	I/O	Address bit 18	100 µA/8 mA
17	A8	I/O	Address bit 8	100 µA/8 mA
18	A19	I/O	Address bit 19	100 µA/8 mA
19	A9	I/O	Address bit 9	100 µA/8 mA
20	A20	I/O	Address bit 20	100 µA/8 mA
21	A10	I/O	Address bit 10	100 µA/8 mA
22	A21	I/O	Address bit 21	100 µA/8 mA
23	+5V	VDD	+5 V	800 mA
24	GND	VSS	Ground	800 mA
25	/EXPROM	O	Expansion ROM enable	100 µA/100 µA
26	D31	I/O	Data bit 31	500 µA/1 mA
27	/RW	I/O	Read/write	100 µA/8 mA
28	D30	I/O	Data bit 30	500 µA/1 mA
29	D16	I/O	Data bit 16	500 µA/1 mA
30	D29	I/O	Data bit 29	500 µA/1 mA

(continued)

■ **Table 1-8** Signals on the FPU/ROM connector (continued)

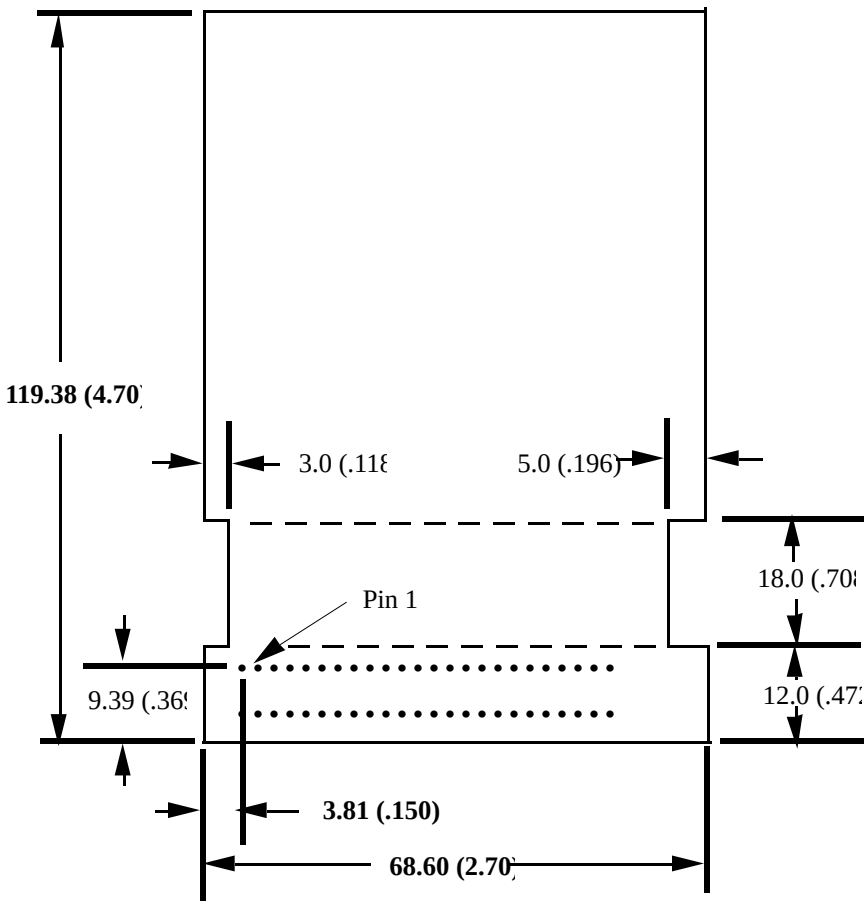
Pin number	Signal name	Direction	Description	Load capacity
31	D17	I/O	Data bit 17	500 µA/1 mA
32	D28	I/O	Data bit 28	500 µA/1 mA
33	D18	I/O	Data bit 18	500 µA/1 mA
34	D27	I/O	Data bit 27	500 µA/1 mA
35	D19	I/O	Data bit 19	500 µA/1 mA
36	D26	I/O	Data bit 26	500 µA/1 mA
37	D20	I/O	Data bit 20	500 µA/1 mA
38	D25	I/O	Data bit 25	500 µA/1 mA
39	D21	I/O	Data bit 21	500 µA/1 mA
40	D24	I/O	Data bit 24	500 µA/1 mA
41	D22	I/O	Data bit 22	500 µA/1 mA
42	D23	I/O	Data bit 23	500 µA/1 mA
43	/FPU.SEL	O	FPU chip select	100 µA/100 µA
44	/DSACK1	I/O	Data strobe acknowledge	100 µA/8 mA
45	GND	VSS	Ground	800 mA
46	C16M	I	16-MHz clock	100 µA/100 µA
47	GND	VSS	Ground	800 mA
48	/DS	I/O	Data strobe	100 µA/8 mA
49	/AS	I/O	Address strobe	100 µA/8 mA
50	/RESET	I/O	System reset	100 µA/8 mA

Physical design guidelines for the FPU/ROM card

This section provides the physical information you will need to design an FPU/ROM card for the Macintosh Classic II computer. Figure 1-5 gives the maximum length and width of the FPU/ROM card and shows the location of the 50-pin connector.

▲ **Warning** Figure 1-5 is a preliminary drawing. It was correct at the time of publication but is subject to change in the future. ▲

■ **Figure 1-5** Design guide for an FPU/ROM card



Dimensions are in millimeters
with inches in parentheses

FPU/ROM connector power budget

The following shows the DC voltage supplied to the FPU/ROM connector and the maximum allowable current load for that voltage.

Voltage	Maximum current load
+5 V	800 mA

Power restrictions in the Macintosh Classic II limit the amount of power that can be dissipated by the FPU/ROM card to a maximum of 4 watts.

▲ **Warning** An FPU/ROM card that dissipates more than 4 watts may overheat and damage the Macintosh Classic II computer's circuitry or cause it to become inoperable. ▲