Annex B. Backplane Physical Layer Configuration Guide

B.1 Timing Formulas (informative)

[tbd. This will contain the formulas used to derive the Serial Bus timing for the backplane physical layer. These will be useful for future enhancements to the standard and are needed to derive the timing for non-standard topologies of the Serial Bus to support much longer or shorter busses.]

B.2 .Backplane Arbitration Timing

Arbitration uses an asynchronous process. To eliminate the possibility for metastability, the incoming arbitration sequence is synchronized to an internal clock before it is sampled. This introduces a "sync delay" which is equal to the one-way bus propagation delay plus one base rate bit sample time (20.345 ns).

The "sample delay" is an integral number of base rate bit times which is greater than the sum of the sync delay and the round trip bus propagation delay. The bus requires one round trip delay to settle because of glitches for BTL and reflections for TTL.

The "hold delay" is an integral number of base rate bit times which is greater than the sync delay. This ensures that all participants in the arbitration process have had a chance to sample the bus.

The arbitration bit period is equal to the sum of the sample delay (5 base rate bit times) and the hold delay (3 base rate bit times).

Figure B-1 – Arbitration symbol timing derivation

B.3 Backplane Gap Timing

An inter-packet gap is a period of time during which the bus (both SBUS_STRB and SBUS_DATA) is unasserted. The bus signals are sampled to determine the length of the gaps (at the base rate of 49.152 MHz). There are three types of gaps.

The bus becomes idle once two bit periods have occurred during which neither SBUS_DATA or SBUS_STRB have made a transition. Because an incoming transmission may be at 49.152 MBd or 24.576 MBd, an idle bus is detected after 4 base rate bit times (at 20.345 ns) have occurred without a transition. These 4 base rate bit times, plus an extra bit time, makes for a gap "sample time" of 5 base rate bit times.

Gap timing and detection is an asynchronous process. To eliminate the possibility for metastability, the bus signals are synchronized to an internal clock before they are sampled. This introduces a "sync delay" which is equal to the round trip bus propagation delay plus one base rate bit sample time (20.345 ns). Because the round trip propagation delay is assumed to be 2 base rate bit times or less, the total sync delay is 3 base rate bit times.

An acknowledge gap occurs immediately after the end of asynchronous data transfers or between isochronous packet transfers. The bus has been in an unasserted state for at least 8 base rate code bit times (≈ 162.8 ns). This time consists of a sample delay (5 base rate bit times) and a sync delay (3 base rate bit times).

A subaction gap appears before asynchronous packets within a fairness interval. The bus has been in an unasserted state for at least 14 base rate code byte times (≈ 284.8 ns). This time includes two extra sync delays (6 base rate bit times) which distinguish it from an acknowledge gap. This additional time allows a responder to detect an acknowledge gap and assert the bus before another node can detect a subaction gap.

An arbitration reset gap appears before an asynchronous packet when the fairness interval starts. The bus has been in an unasserted state for at least 20 base rate code bit times (≈ 406.9 ns). This time includes two extra sync delays (6 base rate bit times) which distinguish it from a subaction gap. This additional time allows an arbitrating node to detect a subaction gap and assert the bus before another node can detect an arbitration reset gap.

Figure B-2 – Gap TIming