

## **Annex A. Cable Physical Layer Configuration Guide**

### **A.1 Timing Formulas (informative)**

[tbd. This will contain the formulas used to derive the Serial Bus timing for the cable physical layer. These will be useful for future enhancements to the standard and are needed to derive the timing for non-standard topologies of the Serial Bus to support much longer or shorter busses.]

### **A.2 Cable Arbitration Timing**

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### **Figure A-1 – Cable environment arbitration timing**

### **A.3 Cable Environment Jitter Budget**

The following tables give the jitter budget for the three cable PMD data rates. These can be used to compute the jitter margin for each data rate using the formula:

$(\text{Bit cell time} - (\text{Data jitter} + \text{Strobe jitter} + \text{Skew})) = \text{Margin}$

**Table A-1 – C100-PMD jitter budget (ns)**

	<b><u>Data jitter</u></b>	<b><u>Strobe jitter</u></b>	<b><u>Skew</u></b>
<u>Transmitter skew</u>			<u>0.4</u>
<u>Transmitter jitter</u>	<u>0.80</u>	<u>0.80</u>	
<u>Cable reflections</u>	<u>0.13</u>	<u>0.13</u>	
<u>Cable intersymbol</u>	<u>0.1</u>	<u>0.1</u>	
<u>Cable delay mismatch</u>			<u>0.4</u>
<u>Channel margin</u>	<u>0.05</u>	<u>0.05</u>	
<u>Jitter at receive pins</u>	<u>1.08</u>	<u>1.08</u>	<u>0.8</u>
<u>Receiver offset</u>	<u>0.5</u>	<u>0.5</u>	<u>0.2</u>
<u>Receiver intersymbol &amp; power supply rejection</u>	<u>0.5</u>	<u>0.5</u>	
<u>Flip flop setup &amp; hold</u>	<u>1.0</u>	<u>1.0</u>	
<u>Total</u>	<u>3.08</u>	<u>3.08</u>	<u>1.0</u>

The margin for the C100-PMD rate is:

$= (10.17 - (3.08 + 3.08 + 1.0)) = 3.01 \text{ ns.}$

**Table A-2 – C200-PMD jitter budget (ns)**

	<b>Data jitter</b>	<b>Strobe jitter</b>	<b>Skew</b>
<u>Transmitter skew</u>			<u>0.25</u>
<u>Transmitter jitter</u>	<u>0.5</u>	<u>0.5</u>	
<u>Cable reflections</u>	<u>0.1</u>	<u>0.1</u>	
<u>Cable intersymbol</u>	<u>0.1</u>	<u>0.1</u>	
<u>Cable delay mismatch</u>			<u>0.4</u>
<u>Channel margin</u>	<u>0.05</u>	<u>0.05</u>	
<u>Jitter at receive pins</u>	<u>0.75</u>	<u>0.75</u>	<u>0.65</u>
<u>Receiver offset</u>	<u>0.25</u>	<u>0.25</u>	<u>0.1</u>
<u>Receiver intersymbol &amp; power supply rejection</u>	<u>0.25</u>	<u>0.25</u>	
<u>Flip flop setup &amp; hold</u>	<u>0.5</u>	<u>0.5</u>	
<u>Total</u>	<u>1.75</u>	<u>1.75</u>	<u>0.75</u>

The margin for the C200-PMD rate is:

$$= (5.08 - (1.75 + 1.75 + 0.75)) = 0.83 \text{ ns.}$$

**Table A-3 – 400 Mbit/sec jitter budget (ns)**

	<b>Data jitter</b>	<b>Strobe jitter</b>	<b>Skew</b>
<u>Transmitter skew</u>			<u>0.2</u>
<u>Transmitter jitter</u>	<u>0.25</u>	<u>0.25</u>	
<u>Cable reflections</u>	<u>0.11</u>	<u>0.11</u>	
<u>Cable intersymbol</u>	<u>0.12</u>	<u>0.12</u>	
<u>Cable delay mismatch</u>			<u>0.4</u>
<u>Channel margin</u>	<u>0</u>	<u>0</u>	
<u>Jitter at receive pins</u>	<u>0.48</u>	<u>0.48</u>	<u>0.6</u>
<u>Receiver offset</u>	<u>0.14</u>	<u>0.14</u>	<u>0.05</u>
<u>Receiver intersymbol &amp; power supply rejection</u>	<u>0.1</u>	<u>0.1</u>	
<u>Flip flop setup &amp; hold</u>	<u>0.2</u>	<u>0.2</u>	
<u>Total</u>	<u>0.92</u>	<u>0.92</u>	<u>0.65</u>

The margin for the C400-PMD rate is:

$$= (2.54 - (0.92 + 0.92 + 0.65)) = 0.05 \text{ ns.}$$