Chapter 1 Macintosh LC Hardware

This chapter describes the major features of the Macintosh® LC computer and emphasizes the differences between it and other members of the Macintosh computer family.

Introduction

The Macintosh LC computer is a high-volume, low-cost Macintosh computer that provides raw performance approximating that of the Macintosh II computer and uses internal video to drive an external color or monochrome monitor. The Macintosh LC computer incorporates a sleek, lightweight design that makes it extremely easy to transport.

The Macintosh LC is Apple Computer's most affordable color Macintosh computer. It is an ideal computer for business productivity, terminal replacement, creativity, animation, entertainment, and teaching and learning.

Major features

The Macintosh LC computer includes the following features:

- Microprocessor: 68020 running at 15.6672 MHz.
- Read-only memory (ROM): 512 KB socketed to main logic board. Optional expansion to 4 MB.
- Random-access memory (RAM): 2 MB soldered to main logic board; 2 SIMM (Single In-line Memory Module) sockets for expansion to 4 MB or 10 MB.
- Floppy disk: two internal 20-pin floppy disk connectors. One 1.4 MB SuperDrive™ with Super Woz Integrated Machine (SWIM) interface is standard. A second 1.4 MB SuperDrive can be installed as an option.
- Hard disk: in addition to a SuperDrive, one optional internal Small Computer System Interface (SCSI) hard disk can be installed. An external SCSI hard disk is also supported as an option.
- I/O: one Apple Desktop Bus™ (ADB) port, two mini-DIN 8 serial ports, one SCSI port, one audio-output jack (for headphone or external speaker), one audio-input jack (for microphone or line input), and one DB-15 video connector.
- Video: on-board video support for 512 x 384 monochrome or 8-bit color display on a 12-inch RGB monitor, and for a 640 x 480 monochrome or 4-bit color display on a Macintosh II 13-inch RGB monitor using the RS-343 interface.

◆ *Note:* Apple offers a card that allows users to run their Apple IIe software on the Macintosh LC computer. With this card installed in the expansion slot, the 12-inch color monitor will support a 560 x 384 x 4-bit color display mode for Apple® IIe software.

A color look-up table (CLUT) allows the selection of 256 colors from a palette of 16 million colors.

Video data is stored in 256 KB of video RAM (VRAM) installed in a special SIMM. When the 256 KB VRAM is replaced by an optional 512 KB of VRAM , 640 x 480 x 8-bit and 512 x 384 x 16-bit display modes are supported.

An internal video connector facilitates the development of a video overlay card for the expansion slot.

- Sound: monaural sound output system similar to that of the Apple Sound Chip (ASC). The sound circuitry has also been enhanced to provide a sound input capability. Sound from a microphone or line input is sampled at a 22 kHz or 11 kHz rate, digitized, and stored along with other data to be used for a variety of purposes such as presentations or the creation of "living" documents. The microphone and RCA adapter plug are included with the Macintosh LC computer as standard equipment.
- Expansion: a Euro-DIN 96-pin connector on the main logic board provides direct access to the 68020 processor by an optional expansion card. Maximum power budget is 4 watts (800 mA at +5 volts).
- Keyboard: a new detached ADB keyboard with numeric keypad and ADB mouse. (See Appendix A for keyboard layout.)
- Networking: LocalTalk® is standard; future support of network booting over LocalTalk, EtherTalk®, and TokenTalk®. Apple will also offer an Ethernet card.

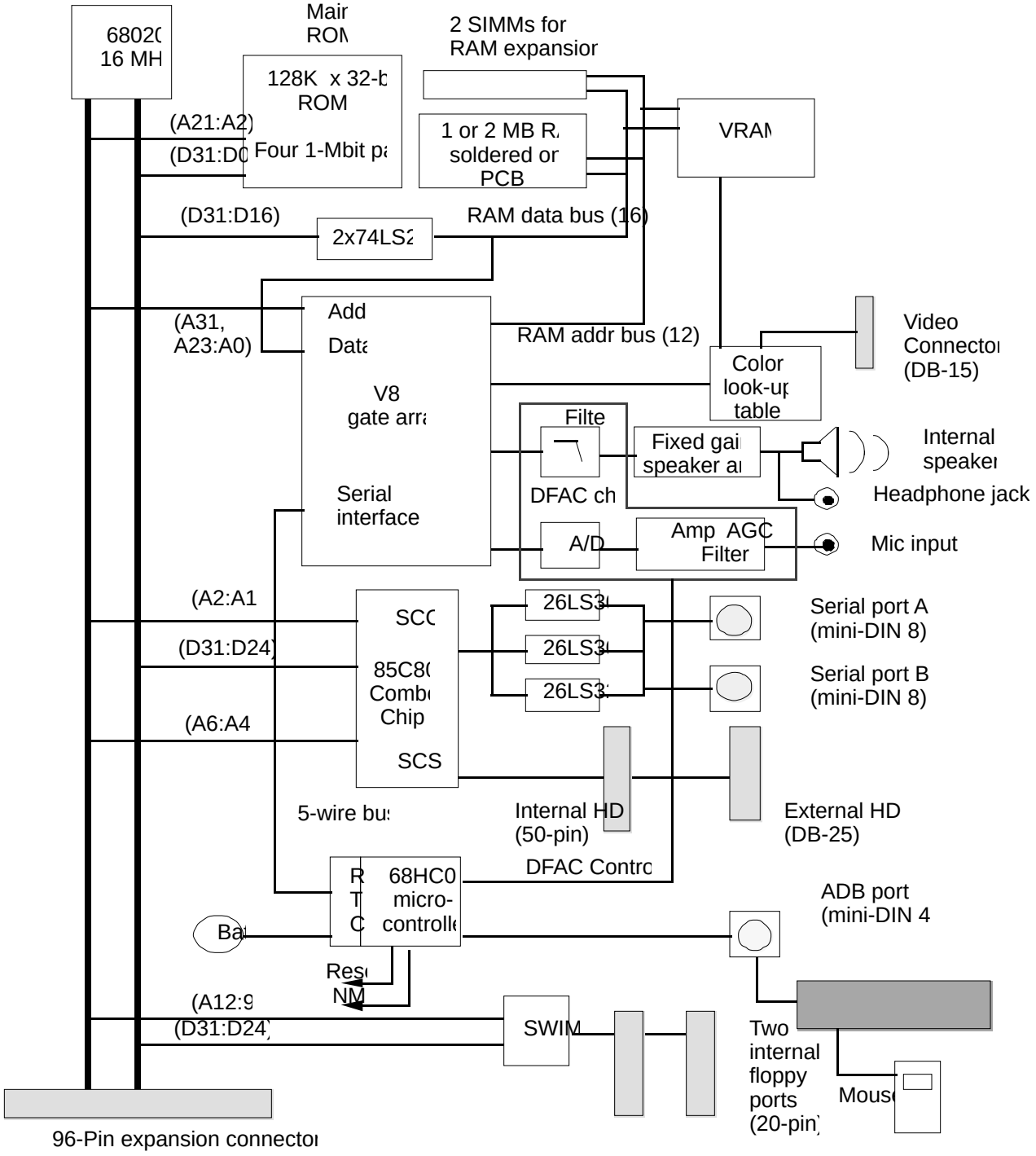
Design differences

The design of the Macintosh LC computer is based as much as possible on the Macintosh IIci architecture. However, as shown in the block diagram in Figure 1-1, the number of components has been significantly reduced through the use of custom integrated circuits. The following are the major changes in the Macintosh LC design:

- The Macintosh LC uses a 68020 processor rather than a 68030.
- A new custom VLSI (very large scale integration) chip, the V8 gate array, is the heart of the hardware design. It integrates the timing, address decode, video generation, clock generation, sound control, and GLU (general logic unit) functions that were provided by individual chips in earlier Macintosh computers.

- A single-chip Motorola 68HC05 microcontroller integrates the functions of ADB interface, real-time clock, power-on reset, parameter RAM storage, and keyboard-controlled reset and NMI (nonmaskable interrupt). On earlier Macintosh computers, the reset and NMI functions were hardware controlled by the programmer's switch and the Reset switch. The ADB microcontroller also controls the DFAC (digital filter audio chip), a custom IC (integrated circuit) that performs the analog processing functions of the sound system.
- A custom chip (Combo) combines the functions of the SCC (Serial Communications Controller) and the SCSI in a single device that is completely compatible with the SCC (85C30) and SCSI (53C80) chips that were used in earlier Macintosh computers.
- The Macintosh LC computer has only one processor-direct expansion slot (no NuBus™ slots).
- The Macintosh LC computer has an internal video connector that facilitates the development of a video overlay card for the expansion slot. It provides the path for the monitor drive signals, thus eliminating the need for a loopthrough cable.
- RAM is expandable in increments of 2 MB and 8 MB. Size bits are in a different location than in Macintosh II–family computers.
- A sound input capability has been added to the sound system.
- The sound system does not support wavetable mode.
- The video base address is different from that of the Macintosh IIci computer.
- With a maximum of 512 KB VRAM installed in a SIMM socket, the Macintosh LC can support the 512 x 384 monitor at up to 16 bits per pixel and the 640 x 480 monitor at 8 bits per pixel.
- The size of the CLUT (color look-up table) as well as the method of access are different from those used in the Macintosh IIci computer.
- Software is required to reset the SCC (hardware reset is not provided).

Figure 1-1 Block diagram of the Macintosh LC computer



Compatibility issues

New ADB implementation

The Macintosh LC computer uses a custom chip to integrate ADB and a number of other functions, including real-time clock, parameter RAM, power-on reset, keyboard reset, and NMI. This implementation is described later in the section "ADB Microcontroller." If you have developed applications that address the ADB hardware directly, they will most likely not function under this new scheme. Also, you will have to revise debuggers to support the keyboard-based NMI.

New SCSI and SCC implementation

The new Combo chip which combines the functions of SCSI and SCC is described later in the section "SCSI and SCC Interfaces." Although this new chip is software compatible with the previous implementation of these functions, your applications will probably be inoperable if they attempt to access the hardware directly.

New sound input/output hardware

Details on the Macintosh LC computer's sound system implementation are provided later in the section "Sound Interface." The Macintosh LC computer implements a subset of the ASC but unlike previous ASC-equipped Macintosh computers, the macintosh LC supplies only monaural sound output. If your application uses the Sound Manager calls and does not try to access the ASC hardware directly, the application should work as documented; however, if your application tries to direct sound to the unused (right) stereo channel, it will not produce any sound. Also, the Macintosh LC computer does not support the wavetable sound output mode used on previous Macintosh computers. Your application will not work on Macintosh LC computer if it addresses the wavetable hardware directly. To ensure that your application operates properly, Apple strongly advises that you use the Sound Manager routines. Applications using the older Sound Driver software will not be compatible with the Macintosh LC computer.

No on-board mathematics coprocessor

Although the Macintosh LC computer does not include an FPU (floating-point unit) as a standard feature, the V8 gate array provides the necessary decoding for an optional FPU. Expansion card designers may want to include an optional FPU on an expansion card because the /FPU select signal is supplied to the 68020 Direct Slot expansion connector. Expansion card design guidelines are provided later in the section “68020 Direct Slot Expansion.”

Application software should not assume that the Macintosh LC computer has an FPU simply because it uses a 68020 microprocessor. To ensure that your application is compatible with the Macintosh LC and future Macintosh computers that do not have FPUs, use the Gestalt Manager (the successor to SysEnvirons). This practice will allow you to determine the exact configuration of the machine you are running on.

If your application is provided in two versions, one that uses SANE® (Standard Apple Numerical Environment) software and another that requires the FPU hardware to perform its numeric calculations, or if your application makes a conditional branch to execute floating-point instructions directly, it should first check for the presence of an FPU . The following pseudo code shows the correct way to check for an FPU.

```
IF I require an FPU THEN
      Call Gestalt Manager
      IF FPU is present THEN
            FPU_Present=True
END IF
```

New color resolution and pixel density

The new 512 x 384 x 8-bit color monitor is the first non–640 x 480 Apple monitor to be used with a Macintosh computer. To make sure that your application works well regardless of the monitor used, follow Apple’s published compatibility guidelines and size your windows automatically according to the appropriate QuickDraw™ variables. Also, be aware that the new color monitor has a 64-DPI (dots per inch) display instead of the 72-DPI display of the Macintosh II RGB monitor.

Color compatibility

You should design your programs so that they take full advantage of all of Color QuickDraw's features and can also work with multiple display devices. The Macintosh LC computer is currently designed to drive an 8-bit color display. However, you should not limit your new color applications to working on only the current version of the Macintosh LC computer but should design your software so that it is capable of working with other display devices that could eventually be supported by the Macintosh LC and future Macintosh computers. Apple has defined high-level calls and documented data structures for determining characteristics of display devices. These calls are documented in the "Graphics Devices" section of *Inside Macintosh, Volume V.* Taking advantage of these calls and data structures will increase the functionality, flexibility, and longevity of your programs. The Macintosh LC computer's 32-bit color QuickDraw is further documented in the 32-bit QuickDraw Release Notes and in Developer Technical Support's Technical Note #275.

Your application should use the Gestalt Manager (included in system software version 6.0.4 and later) to determine the resolution and size of the attached monitor. You can make sure your application will be compatible with future CPUs by designing it to check explicitly for each required feature.

Hardware overview

This section provides a functional description of the Macintosh LC computer's hardware systems.

△ **Important** Memory sizes, addresses, and other data are specific to each type of Macintosh computer and are provided for informational purposes only. To ensure that your application software maintains compatibility across the Macintosh line, and to allow for future Macintosh LC hardware changes, you are strongly advised to use Macintosh Toolbox and Operating System routines wherever provided. In particular, never use absolute addresses to access hardware, because these addresses are different on different models. ▵

Main processor

The Macintosh LC computer uses an 68020 microprocessor running at a system clock rate of 15.6672 MHz. Processing speed varies significantly depending on whether you are getting access to ROM or to RAM. Access to the 16-bit RAM data bus requires one wait state; access to the 32-bit ROM data bus require two wait states.

V8 gate array

The V8 gate array is a new custom chip that implements many functions that were provided by individual chips in computers such as the Macintosh IIci computer. These functions include timing, video generation, memory mapping, sound, clock generation, and miscellaneous GLU functions. For example, the Macintosh IIci computer included an RBV (RAM-Based Video) chip, a MDU (Memory Decode Unit) chip, a VIA (Versatile Interface Adaptor) chip, and an ASC. Functions similar to these are now integrated in the V8.

Address decode and memory mapping

One of the V8 gate array's most important functions is to provide address decode and memory-mapping functions for the Macintosh LC computer. The V8 implements two memory address-mapping modes, a 24-bit mode and a 32-bit mode. (See Table 1-1). As in other Macintosh computers, a control bit determines which map is to be used.

△ **Important** The addresses shown in this section apply only to the Macintosh LC computer and only for the version of the ROM current at the time this developer note is published. It is highly recommended that you use the Macintosh Toolbox calls, system traps, and global variables listed in *Inside Macintosh* to access the hardware. ▵

Notice that in the 24-bit mode, the highest address byte (8 bits) is not used, and all addressable devices appear in the 16 MB address space. ROM appears in the range

$00A0 0000 through $00DF FFFF, and the expansion slot appears from $00E0 0000 through $00EF FFFF.

In the 32-bit mode, however, ROM appears from $40A0 0000 through $40DF FFFF, and the expansion slot appears from $FE00 0000 through $FFFF FFFF.

Table 1-1 Memory map summary

Function	24-bit mode	32-bit mode
RAM	$00 0000–$9F FFFF	$0000 0000–$009F FFFF
ROM	$A0 0000–$DF FFFF	$40A0 0000–$40DF FFFF
Expansion space	$E0 0000–$EF FFFF	$FE00 0000–$FEFF FFFF
I/O space	$F0 0000–$FF FFFF	$50F0 0000–$50FF FFFF
VRAM	$F4 0000–$FB FFFF	$50F4 0000–$50FB FFFF

◆ *Note:* The Macintosh LC computer is shipped with 256 KB of VRAM installed in a SIMM socket. With this configuration, main memory is not used for storing video data. Without VRAM installed, it is possible to use main memory for video storage but only to support the 640 x 480 monochrome video mode. The possible VRAM configurations are described later in the section “VRAM.”

To maintain compatibility with current addressing conventions, application software should address the expansion slot as if it were NuBus physical slot 6 (logical slot $E) by using either the 16 MB standard slot space from $FE00 0000 through $FEFF FFFF or the
256 MB super slot space from $E000 0000 through $EFFF FFFF.

A bus error results if you try to access address $FF FFFF in the 24-bit mode or address $FFFF FFFF in the 32-bit mode.

VIAs

The V8 includes a full-function VIA1, a pseudo-VIA2 that consists of registers similar to those implemented in the RBV of the Macintosh IIci computer, and several registers similar to those in the Apple Sound Chip. The Macintosh LC computer uses these functions to connect the 68020 processor to the necessary control functions. Most of the VIA implementation differences between Macintosh LC and Macintosh IIci computers are caused by the following:

- a new implementation of the real-time clock in the Macintosh LC computer
- the lack of parity checking in Macintosh LC computer
- a single processor-direct slot (no NuBus slots) in the Macintosh LC computer.

ROM

The Macintosh LC computer's main ROM is implemented as four 32-pin, 128K x 8-bit ICs providing a standard configuration of 512 KB of read-only memory; however, 4 MB of space is reserved for future ROM expansion.

Power-on overlay function

The Macintosh LC computer, like all other Macintosh computers, implements an overlay function at power-up or reset that maps ROM address space (in this case, $40A0 0000 through $40DF FFFF) to RAM space starting at location $0000 0000. Following the first access to the normal ROM address range, the ROM image at $0000 0000 is cleared and replaced by RAM.

RAM

Although the first 10 MB of address space is reserved for RAM, the Macintosh LC computer is shipped with only 2 MB of RAM soldered to the main logic board. Two SIMM sockets allow you to expand the RAM by 2 MB, 4 MB, or 8 MB. The V8 chip generates the DSACK (data transfer and size acknowledge) signal for all accesses to RAM. Three bits in the V8 chip's expansion register are set by the software at power on to indicate the actual size of the RAM.

Video

The Macintosh LC computer is designed to support 512 x 384 monochrome or 8-bit color displays, 640 x 480 x 4-bit monochrome or Macintosh II RGB color displays, and
560 x 384 x 4-bit color displays (Apple IIe emulation mode). All video timing is generated by the V8 gate array. The VRAM functions as the video frame buffer. The amount of access time required by the video is a function of the video mode being supported.

The 512 x 384 and 560 x 384 color modes all use the 256 x 24-bit CLUT which is provided by a separate custom chip. The monochrome mode also uses the CLUT but drives the red, green, and blue inputs with the same signal.

The 560 x 384 mode requires a 17.234 MHz clock input on pin B-31 of the expansion connector. This clock provides timing for 560 pixels that is equivalent to the timing for 512 pixels in the 512 x 384 mode with the 15.6672 MHz clock.

VRAM

The Macintosh LC computer normally uses VRAM to store video data. Three possible configurations can be used in the 68-pin SIMM socket that is reserved for VRAM:

- No VRAM: Although not recommended, it is possible to install a SIMM containing two 74LS373 transparent latches. With this configuration, the Macintosh LC computer uses the main memory for storing video data and can support only the 640 x 480 x 1-bit monochrome video mode.
- 256KB VRAM: This SIMM contains two 128K x 8-bit VRAMs. It supports the 512 x 384 monitor at up to 8 bits per pixel and the 640 x 480 monitors at up to 4 bits per pixel.
- 512 KB VRAM: This SIMM contains four 256K x 4-bit VRAMs. It supports the 512 x 384 monitor at up to 16 bits per pixel and the 640 x 480 monitors at up to 8 bits per pixel.

◆ *Note:* If none of the above configurations is used (that is, if the SIMM socket is left empty), the Macintosh LC computer will be unable to generate video.

Monitors supported

Monitors supported include a new 12-inch color monitor that supports the 512 x 384 x 8-bit color mode (or the 560 x 384 x 4-bit color mode when the Apple IIe emulation card is installed in the expansion slot), the existing Macintosh II 640 x 480 x 4-bit RGB monitor, and a 640 x 480 x 4-bit monochrome monitor. The monitor is connected to the Macintosh LC computer through a DB-15 external video connector on the back of the Macintosh LC case. The monitor identifies itself to the Macintosh LC computer by sending a pre-wired 3-bit identification code via this connector. If no monitor is connected, the timing for the 512 x 384 video mode is automatically selected. Table 1-2 shows the pinout for the video connector.

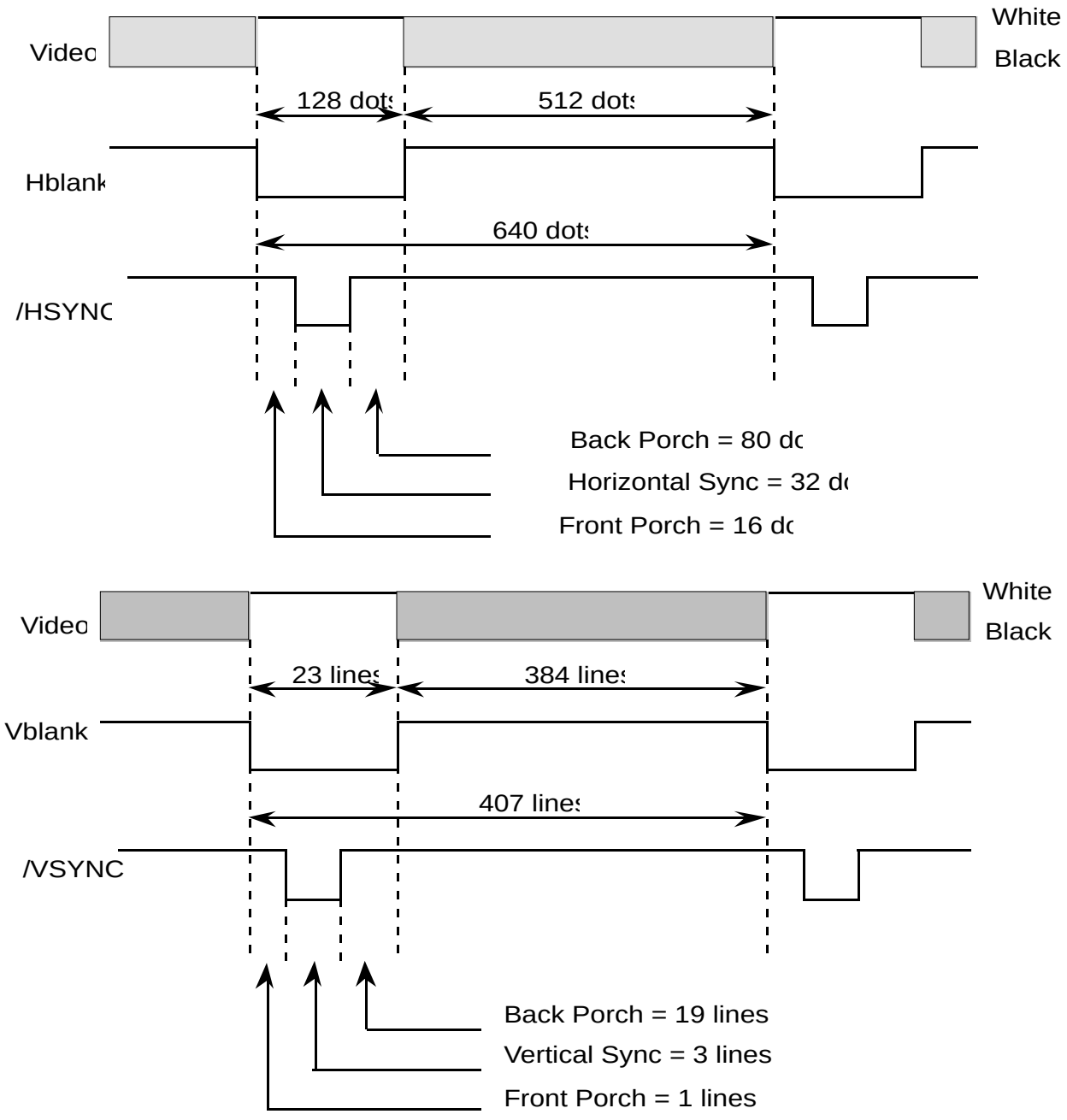
Table 1-2 Pinout for external video connector

Pin	Signal name	Description
1	R.GND.	Red video ground
2	R.V.	Red video
3	/CSYNC	Composite horizontal and video sync
4	ID1	Monitor ID bit 1
5	G.V.	Green video
6	G.GND.	Green video ground
7	ID2	Monitor ID bit 2
8	—	(Not used)
9	B.V.	Blue video
10	ID3	Monitor ID bit 3
11	GND	CSYNC ground
12	/VSYNC	Vertical sync
13	B.GND.	Blue video ground
14	—	(Not used)
15	—	(Not used)
Shell	S.GND.	Shield ground

Video timing

Figures 1-2 through 1-4 show timing information for the supported video modes. These figures define the blanking, synchronizing, and active video regions of the video scan waveforms in terms of dot or pixel times. A dot is the time required to draw a single pixel.

Figure 1-2 512 x 384 video timing

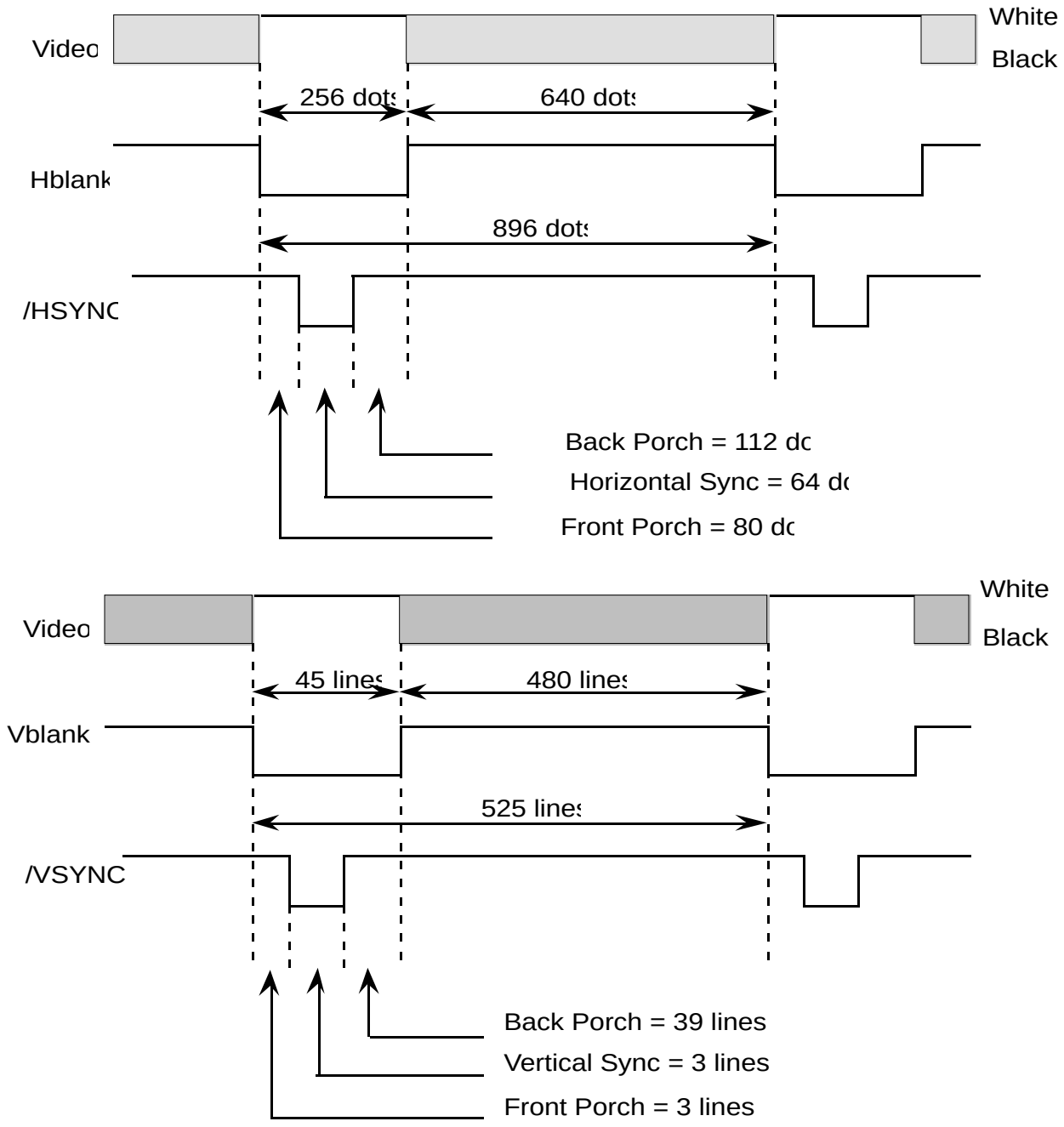


Dot Clock = 15.6672 MHz
Dot = 63.83 ns

Full line = 40.85 µs
Line rate = 24.48 kHz

Full frame = 16.626 ms
Frame rate = 60.15 Hz

Figure 1-3 640 x 480 video timing

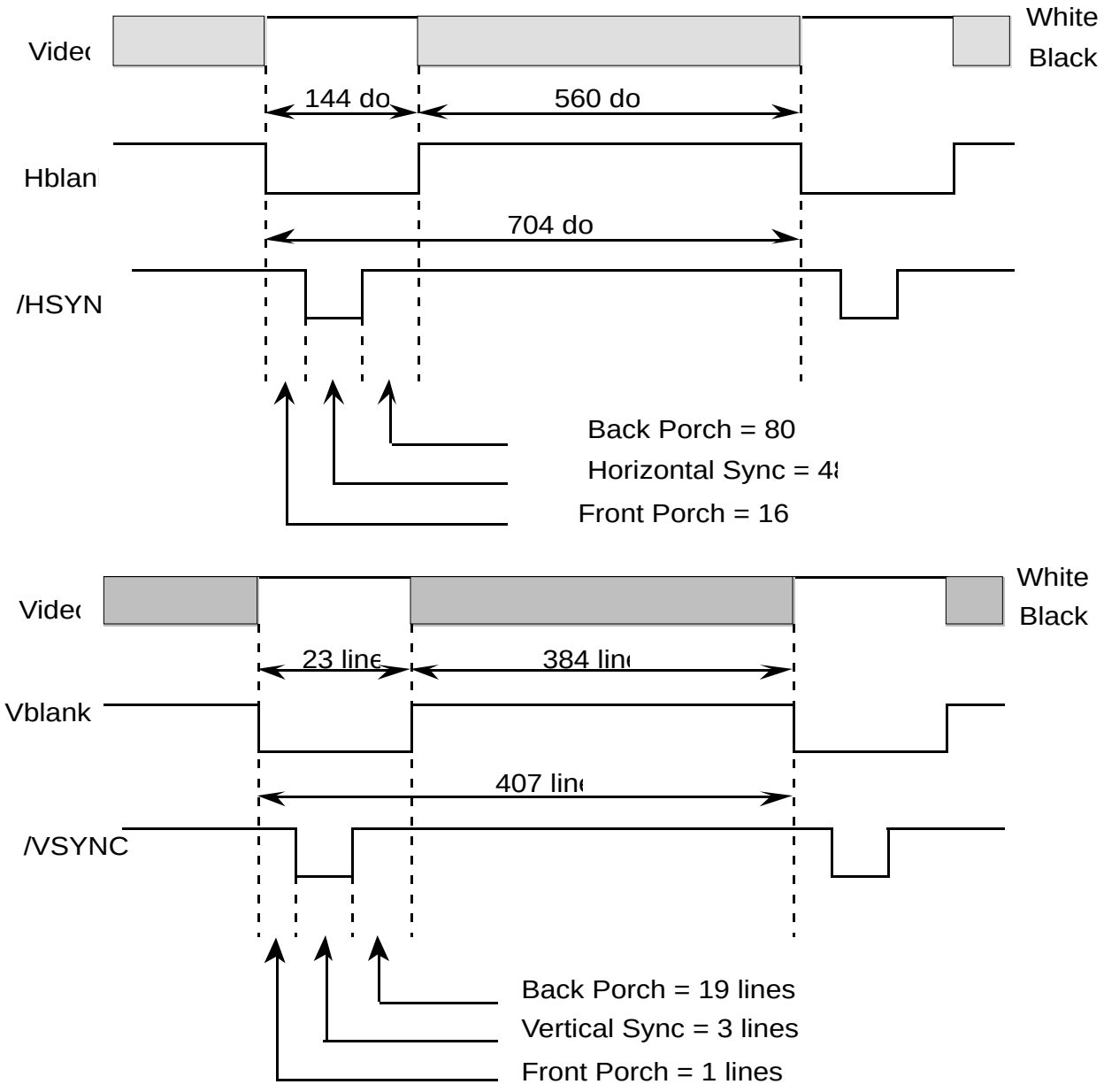


Dot Clock = 31.3344 MHz
Dot = 31.91 ns

Full line = 28.59 µs
Line rate = 34.975 kHz

Full frame = 15.01 ms
Frame rate = 66.62 Hz

Figure 1-4 560 x 384 video timing



Dot Clock = 17.234 MHz
Dot = 58.02 ns

Full line = 48.85 µs
Line rate = 24.48 kHz

Full frame = 16.63 ms
Frame rate = 60.15 Hz

Sound interface

The Macintosh LC sound system includes a built-in speaker, an external stereo headphone jack that plays in monaural but to both ears, and a microphone input jack for the sound input feature. A microphone is included with the system.

The sound system is similar to the Macintosh Plus and Macintosh SE sound systems in that main memory is used for the sound buffer. Because the Macintosh LC computer's video modes have different line times than those of the Macintosh Plus computer, the sound system has its own timing chain, which samples at the same 44-microsecond rate used in the older Macintosh machines and also generates the 60.15 Hz interrupt produced by all Macintosh computers.

The V8 chip includes a subset of the Apple Sound Chip for accessing the sound buffer in main memory. A FIFO (first in, first out) memory controlled by the V8 is used for sound playback and recording, but the memory used for the FIFO sound buffer is part of the system main memory.

Sound input feature

In addition to sound output, the Macintosh LC computer has a sound input feature that allows sound to be recorded digitally. Also, by using a playthrough feature, you can mix an external audio source with computer-generated sound and play it back through a speaker or headphones.

- *Note:* Chapter 3, "Sound Input," explains the application-programmer interface for the Sound Input Manager and describes the high-level and low-level calls that you can implement in your application programs to allow users to take advantage of the Macintosh LC computer's sound input feature.

The DFAC is a custom IC that does the analog processing functions for the sound system. The DFAC contains a switched filter capacitor, an analog to digital converter, and switching and amplifier circuits. A shift register in the 65HC05 microcontroller provides the DFAC with 8 bits that control the routing of the analog sound signals through the system.

The setting of the 8 DFAC control bits determines the mode of sound operation. The three most commonly used modes are sound playback with playthrough, sound playback, and sound record.

Sound playback with playthrough: This mode provides sound output and is used most often. Because the Macintosh LC computer has sound input capability, you can also use this mode to add digitized sound input to normal Macintosh sound. For example, you can play a line-level input through the built-in speaker concurrent with computer-generated sounds.

Sound playback: This mode permits only sound output. It is identical to the sound output implementation used in most other Macintosh computers. Sound playback is used primarily as a backup to sound playback with playthrough in case that mode does not give good sound quality.

Sound record: This mode takes advantage of the sound input feature and is the method normally used to record sound.

SCC and SCSI interfaces

A new custom chip called the Combo combines the functions of the SCC and the SCSI controller in a single device. This device is completely software compatible with the SCC (85C30) and SCSI (53C80) chips it replaces.

The SCC portion of the combination SCC/SCSI device includes two independent ports for serial communication. Each port can be independently programmed for asynchronous, synchronous, or AppleTalk® protocols.

Two 8-pin miniature DIN connectors connect the SCC to the external world. The connectors are the same as those currently used on other Macintosh II–family computers. Table 1-3 shows the pinout for the serial ports.

Table 1-3 Serial port pinouts

Pin number	Signal description
1	Handshake output
2	Handshake input
3	Transmit data –
4	Ground
5	Receive data –
6	Transmit data +
7	No connection
8	Receive data +

The SCSI portion is completely compatible with the SCSI controller chip used on current members of the Macintosh II family. It is designed to support the SCSI interface as defined by the American National Standards Institute (ANSI) X3T9.2 committee. In addition to the SCSI portion of the combined SCC/SCSI device, the interface consists of an internal 50-pin ribbon connector and an external DB-25 connector.

The new combination chip provides certain advantages to the SCSI interface, including

- less susceptibility to noise on the bus which could cause faulty data transactions
- internal protection that helps to reduce failures caused by ESD (electrostatic discharge)

Table 1-4 shows the pinouts for internal and external SCSI connectors.

Table 1-4 Pinouts for internal and external SCSI connectors

Internal (50-pin)	External (25-pin)	Signal name
48	1	/REQ
42	2	/MSG
46	15	/C/D
50	3	/I/O
40	4	/RST
32	17	/ATN
38	5	/ACK
36	6	/BSY
44	19	/SEL
18	20	/DBP
2	8	/DB0
4	21	/DB1
6	22	/DB2
8	10	/DB3
10	23	/DB4
12	11	/DB5
14	12	/DB6
16	13	/DB7
26	25	TPWR
All odd pins (25 total)	7, 9, 14, 16, 18, and 24	GND

Floppy disk interface

A single SWIM chip controls two internal 3.5-inch SuperDrives, one standard and the other installed as an option. A 20-pin connector provides the signal interface between the SWIM chip and the drive(s). Table 1-5 shows the pinout for the floppy disk connector.

Table 1-5 Pinout for floppy disk internal connector

Pin number	Signal name	Signal description
1	GND	Ground
2	PH0	Phase 0: state-control line
3	GND	Ground
4	PH1	Phase 1: state-control line
5	GND	Ground
6	PH2	Phase 2 :state-control line
7	GND	Ground
8	PH3	Phase 3: register write strobe
9	n.c.	Not connected
10	/WRREQ	Write data request
11	+5V	+5 volts
12	SEL	Head select
13	+12V	+12 volts
14	/ENBL	Drive enable
15	+12V	+12 volts
16	RD	Read data
17	+12V	+12 volts
18	WR	Write data
19	+12V	+12 volts
20	+5V	+5 volts

ADB microcontroller

The Macintosh LC computer uses a new custom microprocessor that integrates the functions of ADB controller, RTC (real-time clock), PRAM (parameter RAM), power-on reset, keyboard reset, and NMI (nonmaskable interrupt). In previous Macintosh models, these functions were provided by separate devices on the main logic board.

ADB interface

The ADB is a single-master, multiple-slave, serial communications bus that uses an asynchronous protocol and connects keyboards, graphics tablets, mouse devices, and other devices to the Macintosh LC computer. The custom ADB microcontroller drives the bus and reads status from the selected external device. A 4-pin miniature-DIN connector connects the ADB controller to the outside world. Table 1-6 lists the ADB connector pinout.

Table 1-6 ADB connector pinout

Pin number	Name	Description
1	ADB	Bidirectional data bus used for input and output. It is an open-collector signal pulled up to +5 volts through a 470 ohm resistor on the main logic board.
2	PSW	Power-on signal that generates Reset and Interrupt key combinations.
3	+5V	+5 volts from the computer. A 1-ampere fuse at the output satisfies safety requirements.
4	GND	Ground from the computer.

Real-time clock and parameter RAM

The custom ADB microcontroller provides the functions of the RTC and the PRAM. The microcontroller includes a 32-bit counter that operates similarly to the existing RTC chip used in other members of the Macintosh II family. A backup battery allows the ADB microcontroller to continue counting and preserves the PRAM data even when the Macintosh LC computer is powered off.

Low-level access to the RTC or PRAM is different from that in previous Macintosh computers. It is accomplished through modified ADB-style commands. Applications that use existing traps to read and write to the RTC and the PRAM will continue to work on the Macintosh LC computer without any problems. However, any software that attempts to address the hardware directly will not work unless that software is modified.

Power-on reset

When the ADB microcontroller turns the power supply on, it also asserts the Reset signal. The Reset signal, which goes to the processor and other I/O devices, allows the processor to stabilize before executing any cycles.

Keyboard reset and NMI

There are no external reset or NMI switches (commonly referred to as programmer's switches) on the Macintosh LC computer. These functions are now controlled from the keyboard by the custom ADB microprocessor. You can assert the NMI signal by pressing the Command key and the Power button at the same time. NMI is a diagnostic signal that enables the debugging software to halt execution of an application and change to a debugger for low-level software and hardware testing. You can assert a hard reset, identical to a power on reset, by pressing the Command key, Control key, and Power button at the same time.

- *Note:* You must hold down the above sequence of keys for at least 1 second to allow the microcontroller time to respond to the NMI or hard reset signal.

The NMI and reset key sequences were chosen for compatibility with currently existing Macintosh utility software.

Network booting

The Macintosh LC computer is designed to provide future support for network booting (for example, starting up from a file server rather than an internal disk drive). The network booting feature is active only if the PRAM value is set correctly. This feature will allow you to use the control panel to set a flag in the ADB microcontroller that causes the system to boot over a communication network such as Ethernet or LocalTalk.

68020 Direct Slot expansion

A 96-pin connector on the main logic board permits an expansion card to communicate directly with the 68020 processor. This feature provides an opportunity for hardware developers to increase the functionality of the Macintosh LC computer by designing expansion cards such as coprocessors, video cards, networking cards, and so on. The features that you implement in your design are limited only by the size of the card (approximately 3 inches by 5 inches) and the available power (maximum 4 watts at +5 volts).

Electrical description of the expansion connector

A Euro-DIN 96-pin socket connector provides processor-direct slot (PDS) expansion for the Macintosh LC computer. This connector is physically (but not electrically) identical to the PDS connector used on the Macintosh SE. The expansion connector provides access to the MC68020 processor's full 32-bit data bus and 29 address lines, as well as to a selection of control signals. Table 1-7 shows the pinout for the expansion connector.

Table 1-7 Macintosh LC 68020 Direct Slot connector pinout

Pin	Row A	Row B	Row C
1	SND	GND (analog only)	/FPU
2	/SLOTIRQ	R/W	/DS
3	/AS	+5V	/BERR
4	/DSACK1	+5V	/DSACK0
5	/HALT	SIZ1	SIZ0
6	FC2	GND	FC1
7	FC0	C16M	/RESET
8	RMC	GND	/BG
9	D31	D30	D29
10	D28	D27	D26
11	D25	D24	D23
12	D22	D21	D20
13	D19	D18	D17

14	D16	D15	D14
15	D13	D12	D11

(continued)

■ **Table 1-7** Macintosh LC 68020 Direct Slot connector pinout (continued)

Pin	Row A	Row B	Row C
16	D10	D9	D8
17	/BGACK	/BR	A0
18	A1	A31	A27
19	A26	A25	A24
20	A23	A22	A21
21	A20	/IPL2	/IPL1
22	/IPL0	D3	D4
23	D2	D5	D6
24	D1	D0	D7
25	A4	A2	A3
26	A6	A12	A5
27	A11	A13	A7
28	A9	A8	A10
29	A16	A15	A14
30	A18	A17	A19
31	FAN	AIICLOCK	FC3
32	+12V	GND	–5V

△ **Important** Under no circumstances should you use the analog GND pin (Row B, pin 1) for a digital ground on an expansion card. Doing so will cause digital noise to be coupled into the audio system resulting in degraded sound quality. △

Since most of the expansion connector signals connect to MOS (metal oxide semiconductor) devices, the DC load on the processor bus signals is minimal. Only one LS (low-power Shottky) load is connected to the high 16 data lines (D31 to D16). All of the signals can drive at least one TTL (transistor-transistor logic) load (1.6 mA sink current and 400 µA source current).

Most of the expansion connector signals are processor direct which means that they are tied directly to signals with identical names on the 68020 processor bus. Some of the signals do not tie directly to the processor but are used to satisfy other functional requirements of the Macintosh LC computer. Table 1-8 describes the functions of the processor-direct expansion connector signals. Table 1-9 describes the functions of non-processor-direct signals.

Table 1-8 Processor-direct expansion connector signal descriptions

Signal name	Description
A0–A29, A30, A31	Address lines.
D0–D31	Data lines.
/AS	Address strobe. Tristate output signal indicating that valid address is on processor bus.
/BERR	Bus error. Bidirectional signal indicating that invalid bus operation is being attempted.
/BG	Bus grant. Output signal indicating that external device can become bus master following completion of current processor bus cycle.
/BR	Bus request. Input signal indicating that external device wishes to become bus master.
/BGACK	Bus grant acknowledge. Input signal indicating that external device has become bus master.
/DS	Data strobe. During read operation, /DS indicates that external device should place data on data bus; during write operation, /DS indicates that 68020 processor has placed valid data on the data bus.
/DSACK–/DSACK1	Data transfer acknowledge signals that indicate completion of data transfer operation.
FC0–FC2	3-bit function code used to identify address space of current bus cycle.
/HALT	Signal indicating that 68020 processor should suspend all bus activity.
/IPL0–IPL2	Interrupt priority-level lines.
/RESET	Bidirectional signal that initiates system reset.
/RMC	Tristate output signal that identifies current bus cycle as part of indivisible read-modify-write operation.
R/W	Read/write. Tristate output signal that defines bus transfer as read or write operation.
SIZ0–SIZ1	Tristate output signals that work in conjunction with processor's dynamic bus sizing capabilities to indicate number of bytes remaining to be transferred during current bus cycle.

Table 1-9 Non-processor-direct expansion connector signals

Signal name	Description
AIICLOCK	Pin that requires a 17.234 MHz clock input to generate timing for 560 x 384 video mode.
C16M	15.6672 MHz clock that runs CPU.
FAN	Voltage, normally about 2 volts, required to operate Macintosh LC fan. If your expansion card requires more cooling, you can ground this pin to speed up fan.
/FC3	Function code bit that selects memory address map. Low selects 24-bit map; high selects 32-bit map.
/FPU	Select signal for optional floating-point unit.
SND	Input to speaker amplifier that permits you to drive speaker from expansion card without involving CPU.
/SLOTIRQ	Signal that expansion card uses to generate interrupt request. When active low, this signal generates level-2 interrupt if slot interrupt enable bit in V8 chip is set. (Similar to the /NMRQ line in Macintosh II–family computers.

Load/drive limits of the PDS expansion connector signals

Table 1-10 provides the load presented or drive available to each pin of an expansion card and indicates whether the signals are inputs or outputs.

In the column labeled *Input/output* in Table 1-10*,* input refers to a signal from the expansion card to the processor and corresponds directly to the load shown in the column labeled *Load or drive limits.* Output refers to a signal from the processor to the expansion card and corresponds directly to the drive shown in that column. An example may be helpful in interpreting the *Load or drive limits* column. The /RESET line is shown as presenting a load of 100 µA/8 mA, 200 pF. This is the maximum expected load that an expansion card must drive when sending a /RESET signal to the main logic board. The DC load is given in the format *signal high/signal low*. This means that the expansion card must drive a load of up to 100 uA when it drives /RESET high (logic 1) and a load of up to 8 mA when it drives /RESET low (logic 0). The AC load is given as 200 pF, the maximum capacitance to ground presented by the main logic board to AC signals from an expansion card.

Additionally, /RESET presents a drive of 50 uA/50 µA, 30 pF. This is the maximum amount of drive from the main logic board that is available to integrated circuits on the expansion card. The /RESET line can drive an expansion card DC load of up to 50 µA in both the high state and the low state. The AC drive is given as 30 pF, the maximum capacitance to ground that an expansion card may present to AC signals from the /RESET line.

Table 1-10 PDS expansion connector signals, loading or driving limits

Signal name	Input/output	Load or drive limits
A0–A31	In/Out	Load: 100 µA/8 mA, 100 pF Drive: 50 µA/400 µA, 30 pF
D0–D15	In/Out	Load: 500 µA/1 mA, 80 pF Drive: 40 µA/.2 mA, 30 pF
D16–D23	In/Out	Load: 500 µA/1 mA, 100 pF Drive: 40 µA/.2 mA, 30 pF
D24–D31	In/Out	Load: 500 µA/1 mA, 130 pF Drive: 40 µA/.2 mA, 30 pF
/RESET	In/Out	Load: 100 µA/8 mA, 200 pF Drive: 50 µA/50 µA, 30 pF
/BERR	In/Out	Load: 100 µA/8 mA, 75 pF 4.7 kΩ pullup Drive: 100 µA/1 mA, 30 pF
/HALT	In/Out	Load: 100 µA/8 mA, 75 pF 4.7 kΩ pullup Drive: 100 µA/5 mA, 50 pF
FC0–FC2	In/Out	Load: 100 µA/8 mA, 75 pF Drive: 100 µA/1 mA, 30 pF
/BR	Input	Load: 100 µA/8 mA, 75 pF 4.7 kΩ pullup
/BG	Output	Drive: 40 µA/400 µA, 30 pF
/BGACK	Input	Load: 100 µA/8 mA, 75 pF 4.7 kΩ pullup
SIZ0–SIZ1	In/Out	Load: 100 µA/100 µA, 75 pF Drive: 100 µA/1mA, 30 pF
/AS	In/Out	Load: 100 µA/8 mA, 75 pF Drive: 40 µA/2 mA, 30 pF 4.7 kΩ pullup
/DSACK0–/DSACK1	In/Out	Load: 100 µA/8 mA, 75 pF 4.7 kΩ pullup Drive: 100 µA/1 mA, 30 pF
R/W	In/Out	Load: 100 µA/8 mA, 100 pF Drive: 40 µA/1 mA, 30 pF
/DS	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.4 mA, 30 pF

(continued)

■ **Table 1-10** PDS expansion connector signals, loading or driving limits

Signal name	Input/output	Load or drive limits
/RMC	Output	Drive: 100 µA/2 mA, 30 pF
/IPL0–/IPL2	Output	Drive: 40 µA/400 µA, 30 pF 4.7 kΩ pullup
/SLOTIRQ	Input	Load: 100 µA/8 mA, 20 pF 4.7 kΩ pullup
/FC3	Output	Drive: 1 mA/1 mA, 20 pF
AIICLOCK	Input	Load: 100 µA/8mA, 20 pF 4.7 kΩ pullup
C16M	Output	Drive: 100 µA/100 µA, 20 pF
/FPU	Output	Drive: 100 µA/100 µA, 30 pF
SND	Input	Use transistor with analog grounded emitter and series resistor (4.7 kΩ nominal) 4.7 kΩ pullup
FAN	Input	Digitally grounding this pin increases speed of the fan and improves thermal conditions
GND (analog only)	In/Out	This is the audio subsystem ground; it is not to be used for digital ground

Expansion connector power budget

The DC voltages supplied to the Macintosh LC computer's expansion connector and the maximum allowable current load for each voltage are the following.

Voltage	Current load
+5V	800 mA
–5V	20 mA
+12V	200 mA

Power restrictions in the Macintosh LC computer limit the amount of power that can be dissipated by an expansion card to a maximum of 4 watts. The entire 4 watts can be from the +5-volt supply, or from a combination of the three supply voltages, but the total cannot exceed 4 watts.

▲ **Warning** Cards dissipating more than 4 watts may overheat and damage the Macintosh LC computer's circuitry or cause it to become inoperable ▲

Electrical design guidelines for the Macintosh LC 68020 Direct Slot expansion card

This section provides the electrical information you need to design an expansion card for the Macintosh LC computer.

Addressing guidelines

Although the Macintosh LC computer does not have the NuBus expansion interface, you should design your expansion card to occupy an address location corresponding to the
32-bit address space that would be occupied by a NuBus card in slot space $E. This method of emulating NuBus address space is called *pseudo-slot* design. The only additional constraints to your design are a need for a declaration ROM and adherence to some address-decoding rules.

The expansion card address is a function of the memory map selected. The card appears in address space $E0 0000 through $EF FFFF in the 24-bit map and in address space $FE00 0000 through $FFFF FFFF in the 32-bit map. However, to allow the existing Macintosh II Slot Manager to control your card as though it were a NuBus card in slot $E, software must address the card as if it were in either the 16 MB standard slot space ($FE00 0000 through $FEFF FFFF) or the 16 MB super slot space ($E000 0000 through $EFFF FFFF). This means that you will not have to develop a new software driver because the driver for the NuBus expansion interface will also work with your processor-direct expansion card.

To ensure compatibility with future hardware and software, you should decode all the address bits to minimize the chance of address conflicts. To ensure that the Slot Manager recognizes your card, make sure that the declaration ROM resides at the upper address limit of the 16 MB address space.

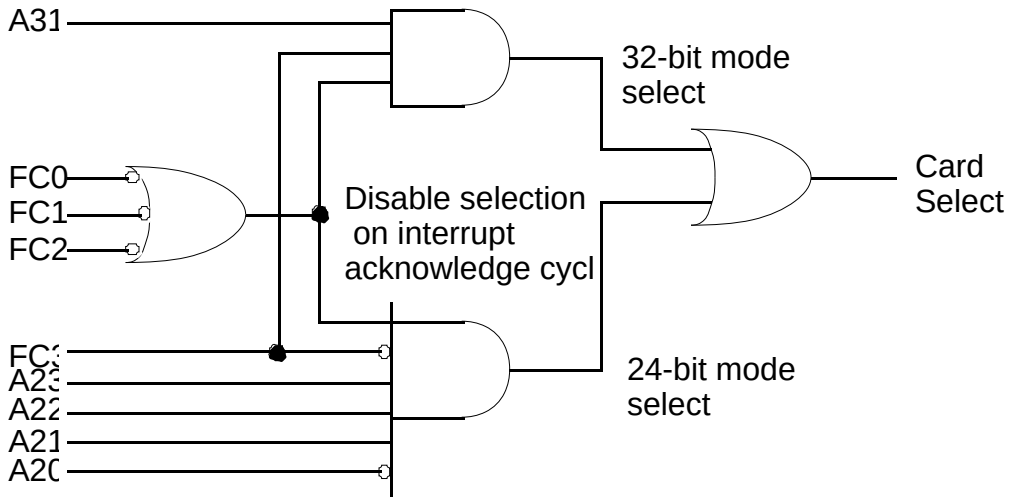
Electrical design considerations

When designing an expansion card for the Macintosh LC computer, you should make sure that your card's timing matches the timing requirements of the MC68020 microprocessor. For information on the processor's timing requirements, see the *MC68020 User's Manual.*

To protect the timing signal margins of the Macintosh LC computer's main logic board, your design should never extend the processor signals beyond their specified current load limits.

Your expansion card must generate its own Card Select signal. Figure 1-5 shows a typical example of the required logic. Notice that a function code of 111 (CPU space) disables the Card Select signal. This action is important because it prevents the card from being selected during interrupt acknowledge cycles.

.■ **Figure 1-5** Expansion card selection logic



A bus timer in the Macintosh LC computer generates a bus error (/BERR) signal if the expansion card fails to transmit a data transfer acknowledge (/DSACK) signal within 45 µs to 90 µs of the active low assertion of the address strobe (/AS) signal. The /BERR signal is generated after counting two clock cycles while /AS is low. Your expansion card design must generate a /DSACK or other termination signal within this period. This action will permit the Slot Manager to determine whether an expansion card is in the slot. Since, in the 32-bit mode of operation, address bit A31 = 1 selects the expansion card, it is not necessary for the Slot Manager to search all NuBus slots for cards as it does in other Macintosh systems; only slot space $E should be scanned

Accessing I/O and memory devices from the expansion card

The expansion card's task of accessing resources on the main logic board is somewhat more complex than the 68020 processor's task of accessing the electronics on an expansion card. When the expansion card needs access to the Macintosh LC computer's resources, it activates the bus request (/BR) signal to request the bus from the 68020 processor. The processor grants the bus (/BG) and tristates itself off the bus at the end of that bus cycle. The processor also generates the bus grant acknowledge (/BGACK) signal to indicate that an external device has become bus master. At this point, the expansion card coprocessor has complete access to all of the Macintosh LC electronics.

The timing of an access is controlled by the V8 gate array for all devices on the main logic board. Once the coprocessor is bus master, it asserts a valid address and an address strobe (/AS) signal. The gate array detects the address, generates the necessary chip selects, and activates the data transfer acknowledge (/DSACK) signals to inform the coprocessor of cycle completion.

Physical design guidelines for the Macintosh LC 68020 Direct Slot expansion card

This section provides the physical information you need to design an expansion card for the Macintosh LC computer. The information includes mechanical drawings showing dimensions and component mounting restrictions.

▲ **Warning** The drawings in this section are reduced copies of mechanical design guides used within Apple Computer, Inc. They are correct at the time of publication but are subject to change in the future. ▲

Figure 1-6 gives the maximum length and width of the expansion card and shows the location of the 96-pin connector. Figure 1-7 provides component location and height restrictions for the expansion card.

▲ **Warning** The component locations and height restrictions shown in Figure 1-7 are critical to your expansion card design. Failure to adhere to these specifications could cause card failure and possible damage to the main logic board. ▲

Figure 1-8 is a design guide for the shield plate that is required with the expansion card to maintain EMI/RFI (electromagnetic interference/ radio-frequency interference) integrity. Figure 1-9 shows the steps for positioning the expansion card on the main logic board.

■ **Figure 1-6** Expansion card design guide

■ **Figure 1-7** Expansion card component location and height restrictions

■ **Figure 1-8** Design guide for expansion card shield plate

Figure 1-9 Positioning the expansion card on the main logic board

Specifications for 96-pin connectors

Figure 1-10 is a detailed drawing of the Euro-DIN 96-pin expansion connector (socket) that mounts on the Macintosh LC computer's main logic board. Figure 1-11 gives the prominent details of the 96-pin expansion connector (plug) used on an expansion card.

You can order Euro-DIN 96-pin connectors meeting Apple specifications from

Amp Incorporated
Harrisburg, PA 17105

Because of high volume requirements, Apple purchases specially modified versions of the Euro-DIN 96-pin connector from this vendor. You may purchase a standard configuration mating connector for your expansion card from this or other vendors.

Figure 1-10 96-pin expansion connector on main logic board

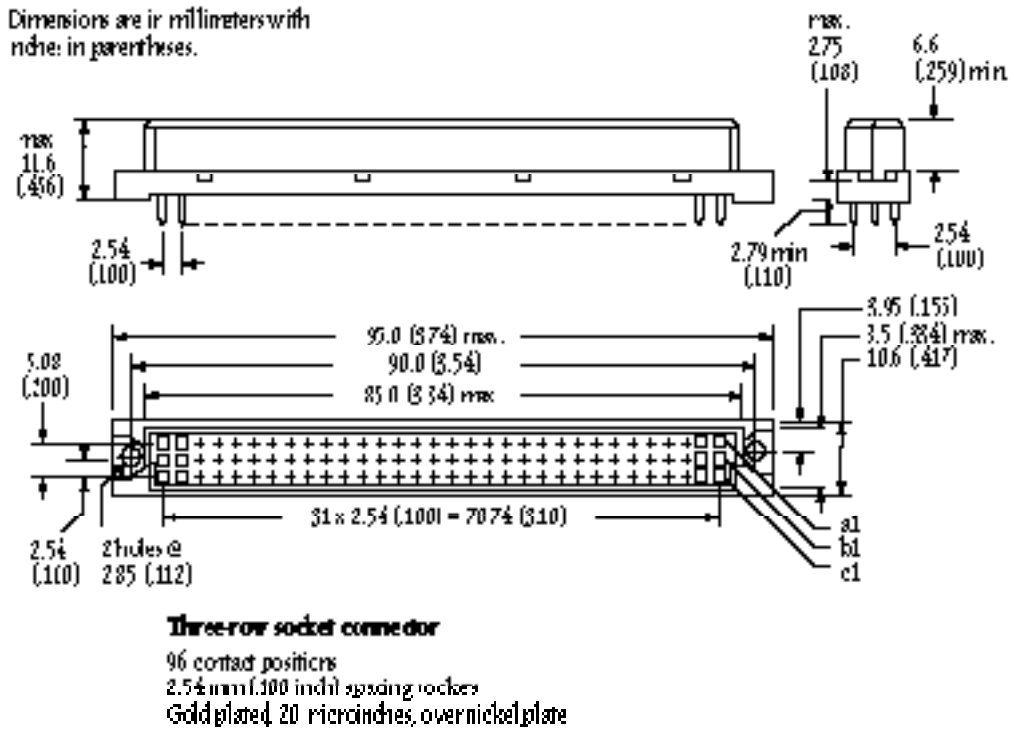
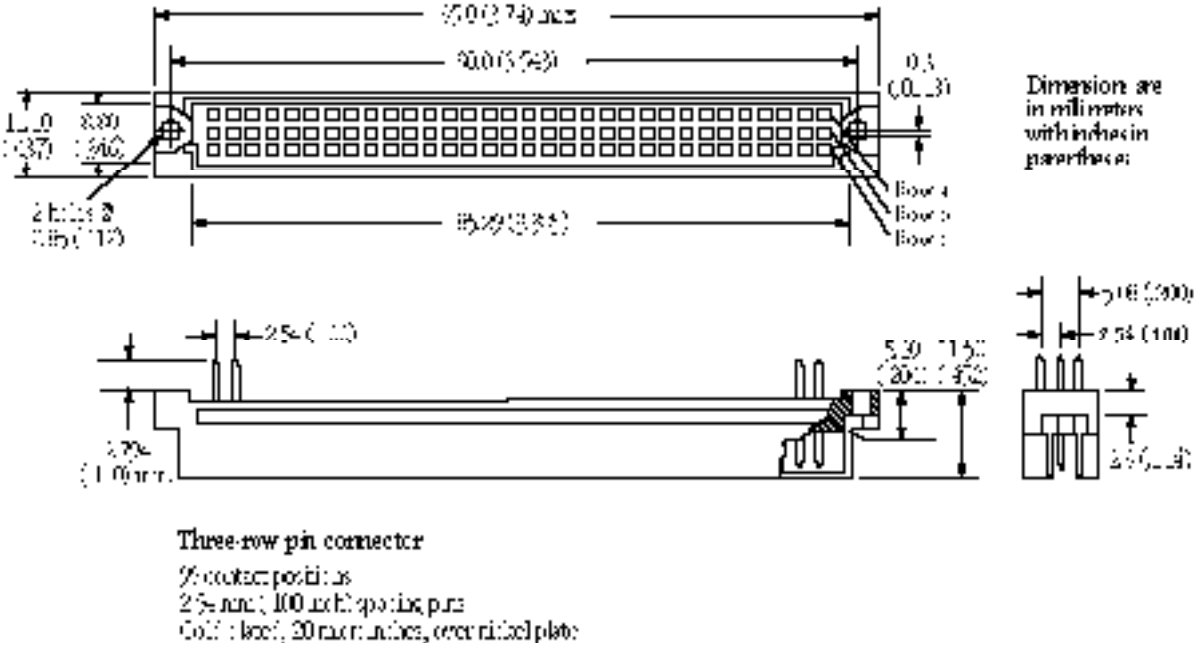


Figure 1-11 96-pin plug connector for a Macintosh LC expansion card



External access opening

An opening in the rear of the Macintosh LC case allows an expansion card to communicate with external devices. This opening accommodates a DB-15 connector, which you can include as an integral part of your expansion card design. The connector attaches to the expansion card in the area shown in Figure 1-6.

Card installation

The expansion card mounts parallel to the main logic board, component side facing component side (see Figure 1-9). It is important that you adhere to height restrictions and do not place hot components in those areas called out in Figure 1-7. You maintain the EMI/RFI integrity of the system by installing the shield plate (Figure 1-8) between the card and the external access opening on the rear of the Macintosh LC case.

Internal video connection

The Macintosh LC computer includes a 12-pin surface-mount internal video connector. This feature allows you to design a video overlay card for the 512 x 384 monitor. The card plugs into the 96-pin expansion connector and uses the video connector to send the drive signals to the monitor without requiring an external loopthrough cable. The video overlay card attaches to the video connector via a small flex cable, which the card manufacturer must provide. Table 1-11 shows the pinout for the internal video connector.

Table 1-11 Internal video connector pinout

Pin number	Signal	Definition
1	GND	Ground
2	GREEN	Green video
3	GND	Ground
4	RED	Red video
5	GND	Ground
6	BLUE	Blue video
7	GND	Ground
8	/CBLANK	Composite blanking
9	GND	Ground
10	OVERLAY	Overlay signal
11	GND	Ground
12	/CSYNC	Composite horizontal and video sync signal

The three video signals shown in Table 1-11 are the same as the RS-343 signals that appear on the external DB-15 video connector. /CBLANK and /CSYNC are TTL signals that drive the CLUT (color look-up table).

The internal video connector does not provide a pixel clock signal for a video overlay card. Your card can, however, use the CPU clock (C16M) from the Macintosh LC computer's processor-direct slot to generate its pixel clock and can synchronize itself with the internal video controller using the /CSYNC and /CBLANK signals. C16M is the same frequency and phase as the pixel clock required by the 512 x 384 monitor.

The OVERLAY signal selects which video controller is driving the monitor. Normally this is the DAC (digital-to-analog controller) on the Macintosh LC computer's main logic board, but the DAC on a video overlay card can also act as master. The master DAC drives the video outputs when the OVERLAY signal is high; the slave DAC drives them when the OVERLAY signal is low.

Transmission line effects are minimized by the fact that the video DAC outputs are current outputs and are terminated with 75-ohm resistors located on the Macintosh LC computer's main logic board. There is a 2- pixel clock delay period between the time when the OVERLAY signal is asserted and the time when the master DAC outputs go off. Even when the master DAC is off, it puts out blanking and setup current, so if there is no slave DAC, video outputs are driven to the completely dark level.

If you are planning to design a video overlay card, your card's flex cable must have a 12-pin SMT (surface mount) type, vertical board-mounting connector (without mounting boss) to mate with the internal video connector on the Macintosh LC. One source for this connector is

Amp Incorporated
Harrisburg, PA. 17105.

Their part number for the connector is 4-174904-2.