Chapter 4 The Video Interface

The Macintosh IIsi computer, like the Macintosh IIci computer, incorporates video on the main logic board. The on-board video supports many of the Apple Macintosh video monitors. The electrical and physical specifications for the Macintosh IIsi computer's on-board video are provided in this chapter.

On-board video

In addition to the existing NuBus video options, a new video solution has been built into the Macintosh IIsi computer, supporting the Macintosh II 12-inch B&W, 12-inch and 13-inch RGB monitors and the 15-inch B&W portrait monitor. The 12-inch and 13-inch monitors are supported at up to 8 bits per pixel (256 colors or shades of gray) and the 15-inch portrait monitor is supported at up to 4 bits per pixel (16 grays).

The video signals are generated by the Apple custom RAM-Based Video (RBV) chip and are driven through a combination color lookup table (CLUT) and video digital to analog converter (VDAC) chip. Each monitor identifies itself by grounding certain pins on the RBV causing it to automatically select the appropriate pixel clock and sync timing parameters. See “Video Cables” later in this chapter for cable wiring details.

When an unknown monitor (or no monitor) is plugged in, on-board video is halted. As shown in Table 4-1, the monitor.ID bits can specify eight possible combinations, each of which may indicate a particular monitor.

Table 4-1 Monitor ID values

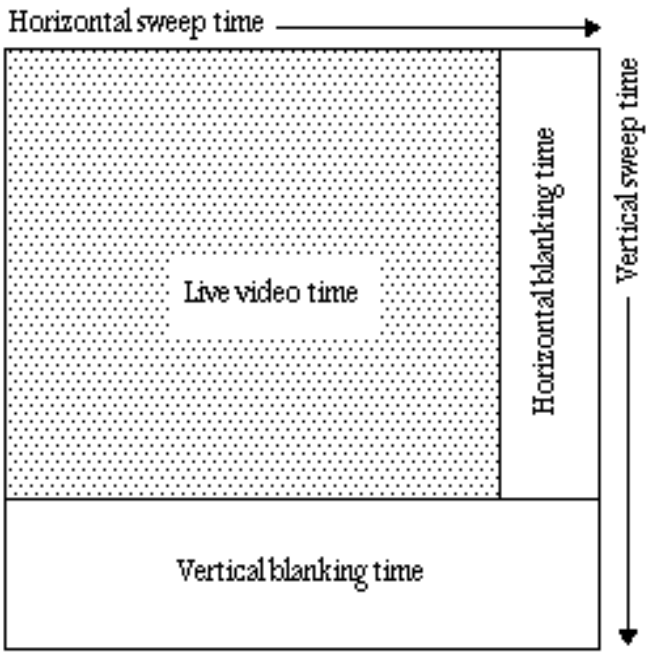
MON ID3	MON ID2	MON ID1	Monitor selected
0	0	0	Unsupported monitor (video halted)
0	0	1	15" B & W Portrait monitor
0	1	0	12" RGB monitor
0	1	1	Unsupported monitor (video halted)
1	0	0	Unsupported monitor (video halted)
1	0	1	Reserved for use by Apple
1	1	0	Macintosh II 12" B & W, 13" RGB
1	1	1	No external monitor (video halted)

The RBV and Bank A of DRAM share a separate RAM data bus that can be connected to or disconnected from the CPU data bus by the bus buffers (see “Use of RAM by the Video” in Chapter 3). Data stored in Bank A of system DRAM is used by the RBV to feed a constant stream of video data to the display monitor during the live video portion of each horizontal screen line. The RBV asks the MDU for data as it is needed; the MDU responds by disconnecting the RAM data bus from the CPU data bus and performing an eight-longword DMA (direct-memory access) burst read from RAM while clocking the read data into the RBV FIFO (first in, first out) buffer.

If a video burst is in progress, a CPU access to RAM Bank A is delayed, effectively slowing down the CPU. This effect is more pronounced for the larger monitors and for more bits per pixel. Note that only accesses to RAM Bank A are affected by video. The optional Bank B of DRAM connects directly to the CPU data bus, and the CPU has full access to this bank at all times, as it does to ROM and the I/O devices.

Figure 4-1 shows the time spent displaying video (labeled “Live video time”) and the time spent during blanking when no video memory accesses are occurring (labeled “Horizontal blanking time” and “Vertical blanking time”).

Figure 4-1 Video timing

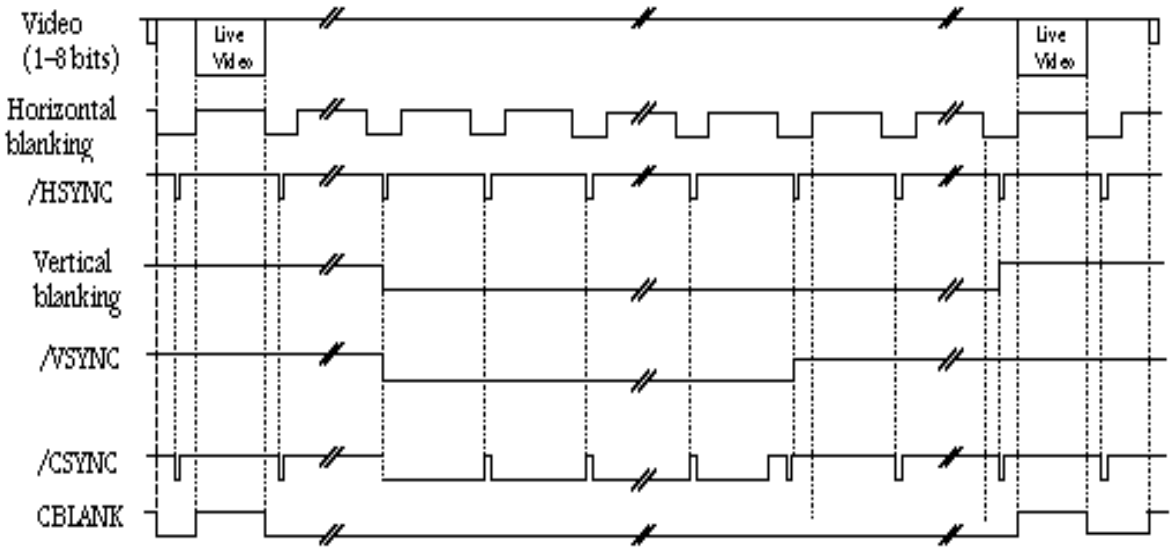


The RBV knows nothing about screen mapping or video addresses. Likewise, the MDU knows nothing about video. Each simply follows a protocol for passing data. The RBV drives certain signals based on the monitor indicated by the monitor ID bits (see Table 4-2). The monitor asserts its monitor ID (MON.ID1–3) by grounding lines for 0's and leaving no connects for 1's. The video signal sync timing for monitors supported by the Macintosh IIsi computer is shown in Figure 4-2. Figures 4-3 through 4-5 show the horizontal and vertical signal timing for these monitors.

■ **Table 4-2** RBV signal descriptions

MON ID 321	Monitor selected	Signals driven	Signals stopped	Cols/ Rows	Dot Clock/ Dot	Line/ Rate	Frame/ Rate
0 0 1	15" Portrait	VID.OUT(0-7) /CBLANK /HSYNC /VSYNC	/CSYNC = 1	640 870	17.457 ns 57.2832 MHz	14.52 µs 68.850 KHz	13.33 ms 75 Hz
0 1 0	12" RGB	VID.OUT(0-7) /CBLANK /CSYNC	/HSYNC = 1 /VSYNC = 1	512 384	63.83 ns 15.6672 MHz	40.85 µs 24.48 KHz	16.63 ms 60.15 Hz
1 1 0	12" B/W 13" RGB	VID.OUT(0-7) /CBLANK /CSYNC	/HSYNC = 1 /VSYNC = 1	640 480	33.07 ns 30.2400 MHz	28.57 µs 35.0 KHz	15.00 ms 66.67 Hz
0 0 0 1 0 0 0 1 1 1 1 1	Video halted	None	VID.OUT(0-7) = 1's /CBLANK = 0 /CSYNC = 1 /HSYNC = 1 /VSYNC = 1				

Figure 4-2 Video signal sync timing



NOTES:

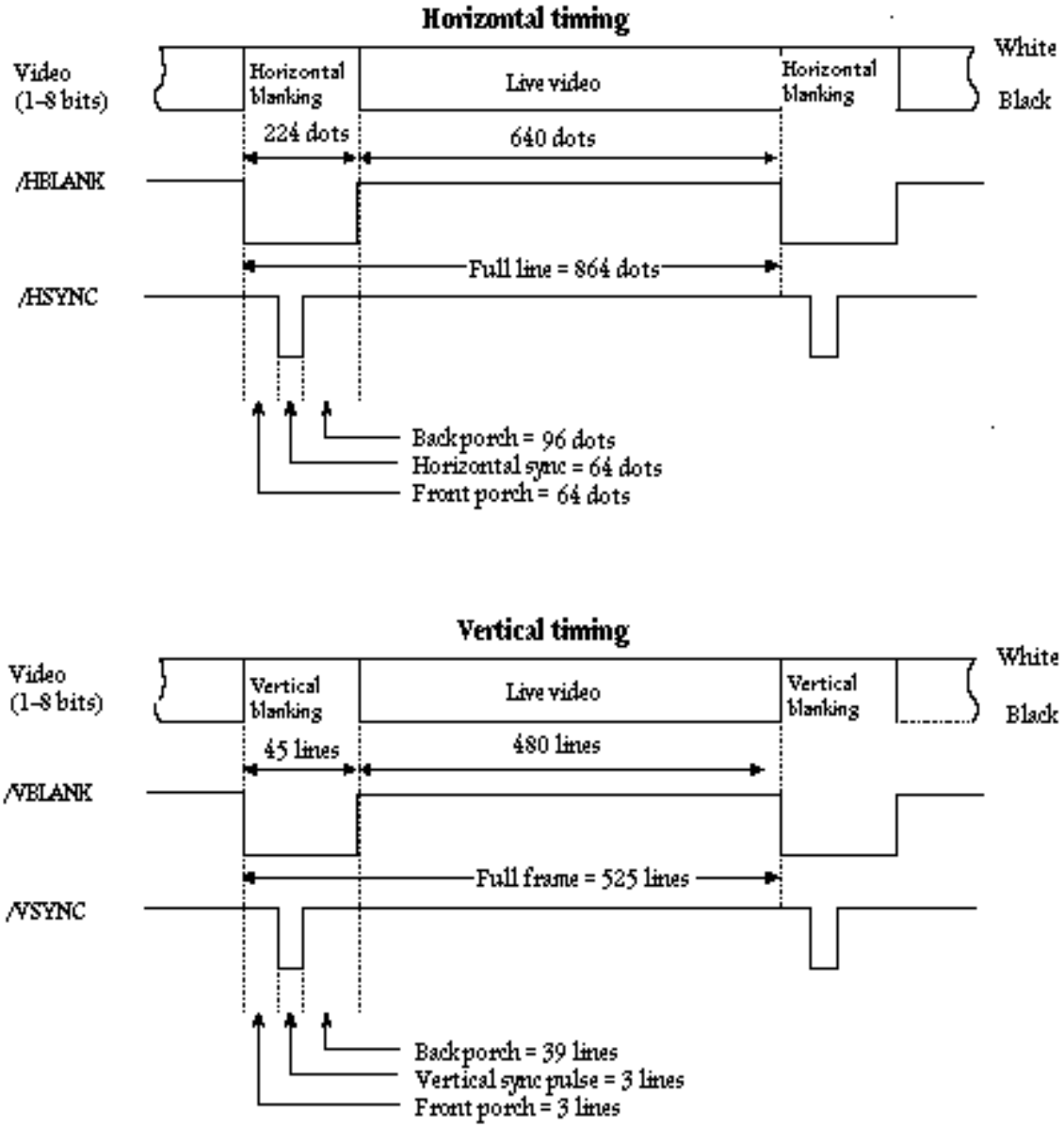
1. All signals change on the rising edge of the dot clock.

2. Signals with names in mixed case are used inside the RBV and are not available on output pins.

3. The width of the pulse on /CSYNC during /VSYNC low is the same width as the /HSYNC pulse (and therefore the width of the pulse on /CSYNC during /VSYNC high).

4. For the 12-inch RGB, 13-inch RGB, and 12-inch B&W monitors, and 15-inch B&W Portrait monitor, both edges of /VSYNC coincide with /HSYNC falling.

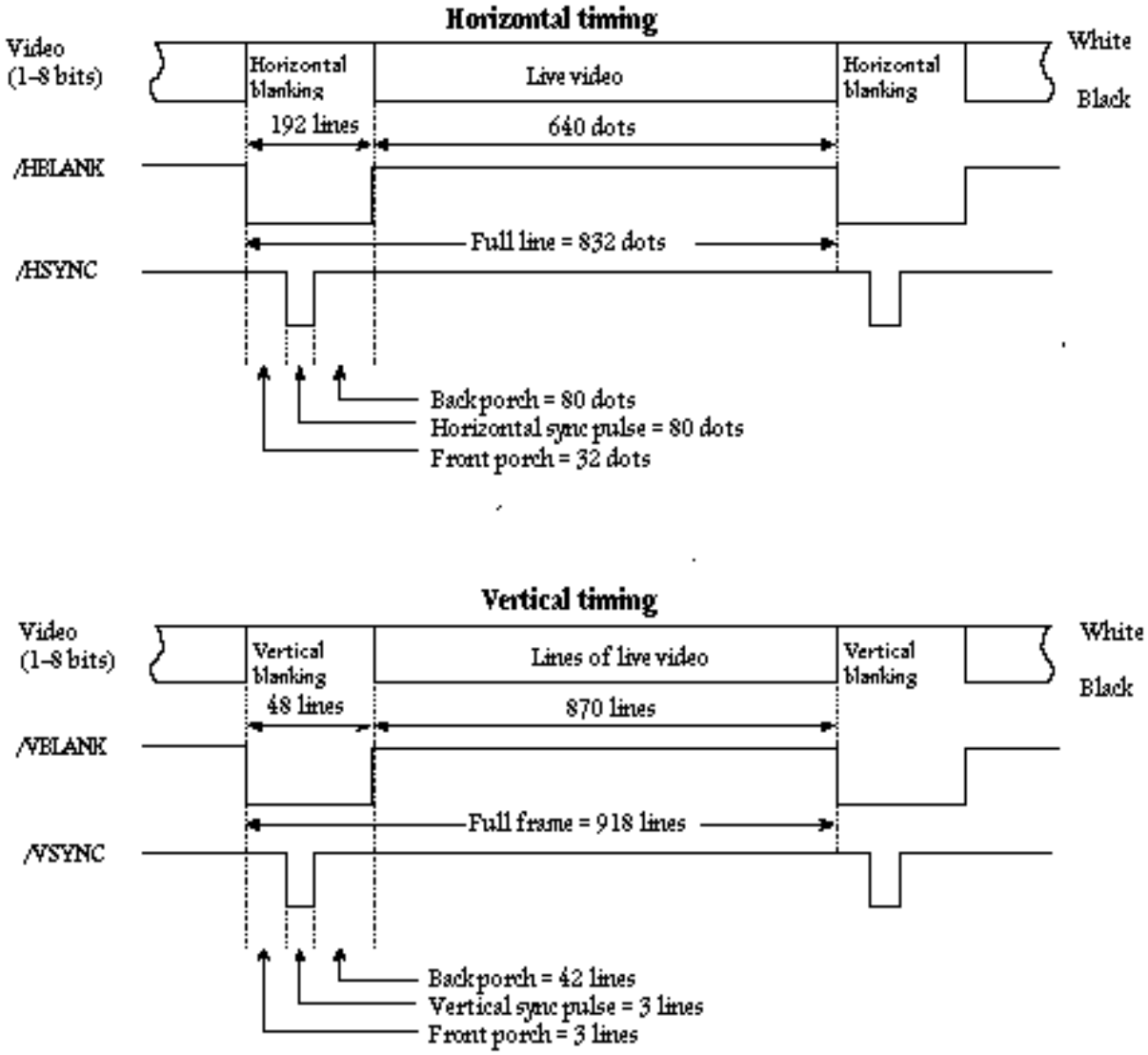
Figure 4-3 Video signal timing for the Apple 13-inch RGB and 12-inch B & W monitors



Dot clock = 30.2400 MHz ±.1%	Full line = 28.57 µs	Full frame = 15.00 ms
Dot = 33.07 ns	Line rate = 35.0 kHz	Frame rate = 66.67 Hz

All timings are derived from the dot clock and have ths same tolerance.

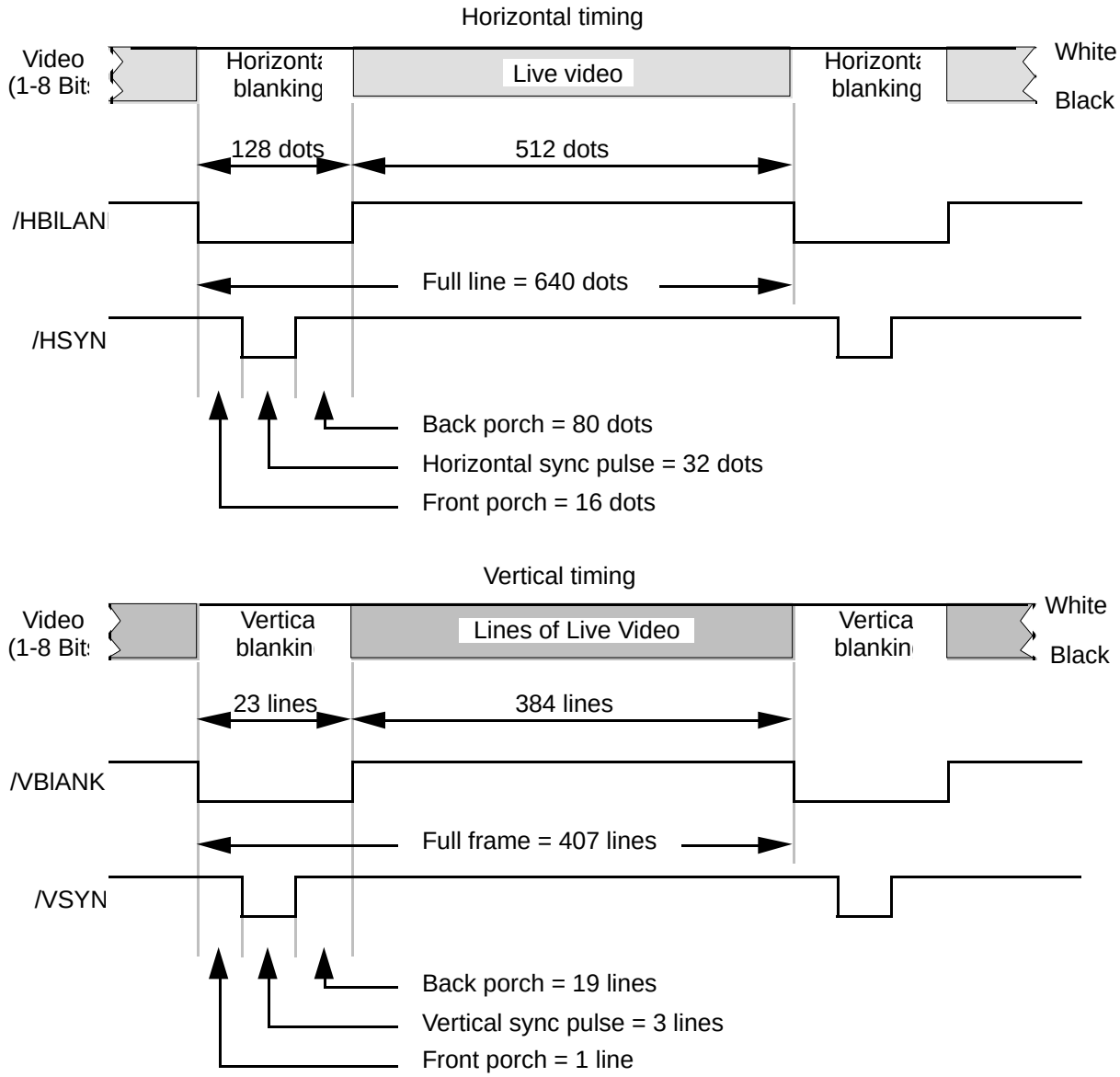
Figure 4-4 Video signal timing for the Apple 15-inch B & W portrait monitor.



Dot clock = 57.2832 MHz ± 1%	Full line = 14.52 µs	Full frame = 13.33 ms
Dot = 17.457 ns	Line rate = 68.850 kHz	Frame rate = 75 Hz

All timings are derived from the dot clock and have the same tolerance.

Figure 4-5 Video signal timing for the Apple 12-inch RGB monitor.



Dot clock = 15.6672 MHz ± .1%
Dot = 63.83 nS

Full line = 40.85 µs
Line rate = 24.48 KHz

Full frame = 16.626 ms
Frame rate = 60.15 Hz

All timings are derived from the dot clock and have the same tolerance.

Video cables

The video connector on the back of the Macintosh IIsi computer is a DB-15, as shown in Figure 4-6. The connector on the monitor will be either a DB-15 (for the 12-inch B&W, 12-inch RGB, and 13-inch RGB monitors) as shown in Figure 4-7, or a D-25 (for the 15-inch Portrait monitor), as shown in Figure 4-8. The DB-15 monitor connector pin numbers are the same as the Macintosh IIsi computer pin numbers, pin for pin.

Figure 4-6 DB-15 video connector on the Macintosh IIsi computer

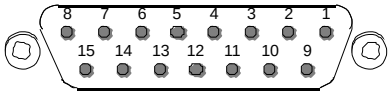


Figure 4-7 DB-15 video connector on the monitor

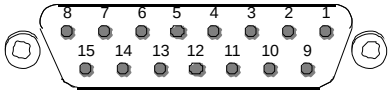
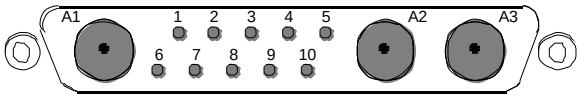


Figure 4-8 D-25 video connector on the monitor

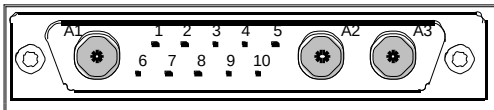


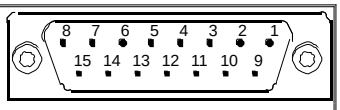
The video connector pinouts for each monitor supported by the Macintosh IIsi computer are listed in Table 4-3. Table 4-4 gives the pin-to-pin connections for the cable used to connect the Portrait monitor to the Macintosh IIsi computer.

Table 4-3 Macintosh IIsi video connector and monitor cable pinouts

Pin	Signal	Description	12" B&W, 13" RGB	12" RGB	15" B&W
1	RED.GND	Red Video Ground	RED.GND	RED.GND	n.c.
2	RED.VID	Red Video	RED.VID	RED.VID	n.c.
3	/CSYNC	Composite Sync	/CSYNC	/CSYNC	n.c.
4	MON.ID1	Monitor ID, Bit 1	ID1.GND	ID1.GND	n.c.
5	GRN.VID	Green Video	GRN.VID	GRN.VID	n.c.
6	GRN.GND	Green Video Ground	GRN.GND	GRN.GND	n.c.
7	MON.ID2	Monitor ID, Bit 2	n.c.	n.c.	ID2.GND
8	n.c.	no connection	n.c.	n.c.	n.c.
9	BLU.VID	Blue Video	BLU.VID	BLU.VID	BLU.VID
10	MON.ID3	Monitor ID, Bit 3	n.c.	ID3.GND	ID3.GND
11	C&VSYNC.GND	CSYNC & VSYNC Ground	CSYNC.GND	CSYNC.GND	VSYNC.GND
12	/VSYNC	Vertical Sync	n.c.	n.c.	/VSYNC
13	BLU.GND	Blue Video Ground	BLU.GND	BLU.GND	BLU.GND
14	HSYNC.GND	HSYNC Ground	n.c.	n.c.	HSYNC.GND
15	/HSYNC	Horizontal Sync	n.c.	n.c.	/HSYNC
Shell	CHASSIS.GND	Chassis Ground	CHASSIS.GND	CHASSIS.GND	CHASSIS.GND

Table 4-4 Apple 15-inch portrait monitor cable connections





Portrait monitor D-25 pin no.	Signal name	Macintosh IIsi DB-15 pin no.
1	HSYNC.GND	14
2	/VSYNC	12
3	MON.ID3	10
4	(no wire)	8
5	/CSYNC	3
6	/HSYNC	15
7	VSYNC.GND	11
8	MON.ID2	7
9	MON.ID1	
10	CSYNC.GND	11
A1 (center)	BLU.VID9	
A1 (outer)	BLU.GND13	
A2 (center)	GRN.VID5	
A2 (outer)	GRN.GND6	
A3 (center)	RED.VID2	
A3 (outer)	RED.GND1	
Shell	CHASSIS.GND	Shell

NOTES:

1. The lines labeled /CSYNC and CSYNC.GND are not needed for the 15-inch portrait or larger monitors because those monitors use separate /VSYNC and /HSYNC signals. /CSYNC and CSYNC.GND are needed in the cable only for connecting a portrait monitor's NuBus video card's D-25 connector to a DB-15 connector.

2. Notice that CSYNC.GND and VSYNC.GND share the same pin on the DB-15 connector.

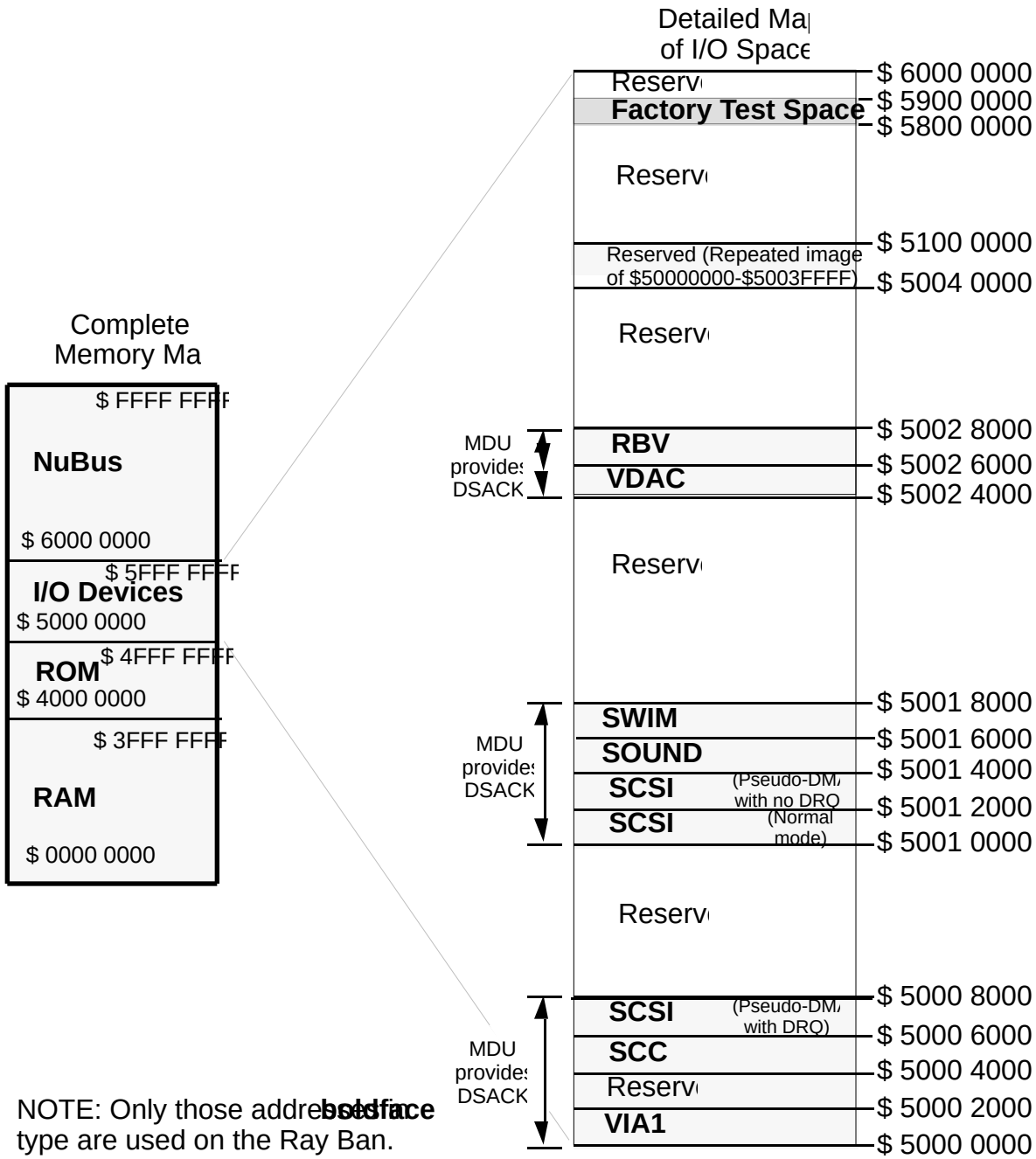
3. The green video and the red video coax cables are not needed for the 15-inch black & white portrait monitor.

Chapter 5 Input/Output Interfaces

This chapter describes the input/output interface configurations used on the Macintosh IIsi computer. These include two serial ports, one external floppy disk drive port, one SCSI port, one ADB port, one sound output port, and one sound input port. In addition, the CPU communicates with the VIA1 chip and the VIA2 registers in the RBV and with the optional numerics coprocessor, if included in the system. The address map of the I/O space is shown in Figure 5-1.

This chapter describes primarily those interfaces that are unique to the Macintosh IIsi computer or are implemented through the use of new hardware. Those I/O interfaces that are the same as those in current Macintosh II–family computers are mentioned only briefly.

Figure 5-1 Macintosh IIsi computer input/output address space



NOTE: Only those addresses in **boldface** type are used on the Ray Ban.

SCC and SCSI interfaces

A new custom chip, Combo, combines the functions of the SCC (Serial Communications Controller) and the SCSI (Small Computer System Interface) controller in a single device. This device is completely software compatible with the SCC (85C30) and SCSI (53C80) chips it replaces.

SCC interface

The SCC portion of the combination SCC/SCSI device includes two ports for serial communication. Each port can be independently programmed for asynchronous, synchronous, or AppleTalk protocols.

Two 8-pin miniature DIN connectors connect the SCC to the external world. The connectors are the same as those currently used on other Macintosh II–family computers.

Table 5-1 shows the pinouts for the serial ports.

Table 5-1 Serial port pinouts

Pin number	Signal description
1	Handshake output
2	Handshake input
3	Transmit data –
4	Ground
5	Receive data –
6	Transmit data +
7	No connection
8	Receive data +

SCSI interface

The SCSI portion of combination SCC/SCSI device is completely compatible with the SCSI controller chip used on current members of the Macintosh II family. It is designed to support the SCSI interface as defined by the American Standards Institute (ANSI) X3T9.2 committee. In addition to the SCSI portion of the combined SCC/SCSI device, the interface consists of an internal 50-pin ribbon connector and an external DB-25 connector.

The new combination chip provides certain advantages to the SCSI interface including

- less susceptibility to noise on the bus, which could cause faulty data transactions
- internal protection that helps to reduce failures caused by ESD (electrostatic discharge)

Table 5-2 shows the pinouts for the SCSI connectors.

Table 5-2 Pinouts for internal and external SCSI connectors

Internal (50-pin)	External (25-pin)	Signal name
48	1	/REQ
42	2	/MSG
46	15	/C/D
50	3	/I/O
40	4	/RST
32	17	/ATN
38	5	/ACK
36	6	/BSY
44	19	/SEL
18	20	/DBP
2	8	/DB0
4	21	/DB1
6	22	/DB2
8	10	/DB3
10	23	/DB4
12	11	/DB5
14	12	/DB6
16	13	/DB7
	25	TPWR
All odd pins (25 total)	7, 9, 14, 16, 18, and 24	GND

Floppy disk interface

A single Super Woz Integrated Machine (SWIM) chip controls both the internal 3.5-inch floppy disk drive and the optional external 3.5-inch floppy disk drive. The signal interface between the SWIM chip and the drives is identical to that used in other Macintosh II–family computers. Table 5-3 shows the pinout for the internal floppy disk connector. Table 5-4 shows the pinouts for the external DB-19 floppy disk connector.

Table 5-3 Pinout for internal floppy disk connector

Pin number	Signal name	Signal description
1	GND	Ground
2	PH0	Phase 0: state-control line
3	GND	Ground
4	PH1	Phase 1: state-control line
5	GND	Ground
6	PH2	Phase 2: state-control line
7	GND	Ground
8	PH3	Phase 3: register-write strobe
9	n.c.	Not connected
10	/WRREQ	Write data request
11	+5V	+5 volts
12	SEL	Head select
13	+12V	+12 volts
14	/ENBL	Drive enable
15	+12V	+12 volts
16	RD	Read data
17	+12V	+12 volts
18	WR	Write data
19	+12V	+12 volts
20	n.c.	Not connected

Table 5-4 Pinout for external DB-19 floppy disk connector

Pin number	Signal name	Signal description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	n.c.	Not connected
6	+5V	+5 volts
7	+12V	+12 volts
8	+12V	+12 volts
9	n.c.	Not connected
10	+5v	+5 volts
11	PH0	Phase 0: state-control line
12	PH1	Phase 1: state-control line
13	PH2	Phase 2: state-control line
14	PH3	Phase 3: register-write strobe
15	/WRREQ	Write data request
16	SEL	Head select
17	/ENBL2	External drive enable
18	RD	Read data
19	WR	Write data

Versatile Interface Adapter (VIA) interface

The Macintosh IIsi computer's hardware includes a VIA1 and a virtual VIA2 to maintain compatibility with existing Macintosh software. Several bits in VIA1 have been redefined to allow the ROM to distinguish between different computers. Although VIA2 is not a physical device on the main logic board, its functions are provided by the RBV circuitry. These VIA2 functions include decoding of the expansion slot interrupts, two SCSI interrupts, and the sound subsystem interrupt; blocking NuBus accesses to RAM; and decoding NuBus transaction errors.

Sound interface

The sound interface on the Macintosh IIsi computer has been enhanced to include not only stereo sound output but also monaural sound input. A microphone and RCA adaptor plug are shipped with the Macintosh IIsi computer to facilitate the use of the sound input feature.

Sound output

The sound output circuitry provides sound and four-voice synthesis compatible with the Macintosh II family. It consists of the Apple Sound Chip (ASC) and two Sony sound chips to filter the pulse-width-modulated signal and drive the on-board speaker or external stereo microphone jack, as was done on the Macintosh II, Macintosh IIx, Macintosh IIcx, and Macintosh IIci computers.

Sound input

The sound input circuitry consists of an input jack, an audio filter/preamplifier, a FIFO buffer memory to store the digitized data, and control logic to allow software to control the circuitry.

The main advantage of the Macintosh IIsi computer's built-in sound input over external sound input solutions is that the Macintosh IIsi sound circuit is interrupt driven and is buffered by a large FIFO buffer memory; therefore, less of the computer's bandwidth is required for sound input.

ADB microcontroller

The Macintosh IIsi computer uses a new custom microprocessor that integrates the functions of the ADB controller, RTC (real-time clock), PRAM (parameter RAM), soft power control, power-on reset, keyboard reset, and NMI (nonmaskable interrupt). In previous Macintosh models, these functions were provided by separate devices on the main logic board. Some new functions supported by the ADB microcontroller include programmable wakeup and file server mode.

ADB interface

The ADB is a single-master, multiple-slave serial communication bus, with asynchronous protocol, that connects keyboards, graphics tablets, mouse devices, and so on, to the Macintosh IIsi computer. The custom ADB microcontroller drives the bus and reads status from the selected external device. A 4-pin miniature-DIN connector connects the ADB controller to the outside world. Table 5-5 lists the connector pinout.

Table 5-5 ADB connector pinout

Pin number	Name	Description
1	Data	This bidirectional data bus is used for input and output. It is pulled up to +5 V through a 470-ohm resistor and is an open collector type signal.
2	Power on	This pin is momentarily grounded to pin 4 to turn on the power supply to the Macintosh IIsi computer. This line is filtered by an inductor in series and a .01-microfarad capacitor to ground. A 100-kilohm resistor to the power supply's +5-V trickle current is also connected to this signal. The +5-V trickle remains even when the computer is turned off, as long as it is plugged in. (Power should never be drawn through this pin.)
3	Power	This is +5 volts from the computer. A 1-ampere fuse at the output satisfies safety requirements.
4	Return	This is the ground from the computer.

Real-time clock and parameter RAM

The custom ADB microcontroller provides the functions of the RTC and the PRAM. The microcontroller includes a 32-bit counter that operates similarly to the RTC chip used in other members of the Macintosh II family. A trickle power supply or battery allows the ADB microcontroller to continue counting and preserves the PRAM data even when the Macintosh IIsi computer is turned off or unplugged.

Access to the RTC or PRAM is different from previous Macintosh computers. It is accomplished through modified ADB style commands. Software that uses the existing driver routines to gain access to the RTC and the PRAM will continue to work on the Macintosh IIsi computer without any problems. However, any software that attempted to address the hardware directly will not work.

Power control

The custom ADB microcontroller also integrates soft power control and power-on reset functions similar to those provided by the Macintosh IIcx and Macintosh IIci computers.

Soft power control

I/O ports and software on the ADB microcontroller poll inputs from the keyboard power switch or the rear-panel power switch and control the power supply through the power fail warning (PFW) signal to the power supply and the expansion interface.

Even when power is off, the power supply maintains a +5-V trickle output that allows the microcontroller to poll the keyboard and rear-panel power switches. If either switch is pressed, the PFW signal goes high, causing power to be turned on within 2 seconds.

You can use a screwdriver or coin to lock the rear-panel power switch in the on position, so that if the Macintosh IIsi computer loses AC power, it will automatically turn itself back on. This feature is important because it allows machines used as files servers to automatically recover after power failures. Pressing the rear-panel power switch when the computer is on generates a hard off that turns the Macintosh IIsi computer off after 2 milliseconds without notifying software. An automatic power on can also be programmed by the software.

The power off function is controlled by software. Using the menu command “Shutdown” causes software to send a special command that enables the ADB microcontroller to pull PFW low, causing a power supply shutdown. This gives the Macintosh IIsi computer sufficient time to complete pending activity before AC power is removed.

Power-on reset

When the ADB microcontroller turns the power supply on, it also asserts the Reset and Test signals. The Test signal, which has a shorter time constant than Reset, is used to reset the MDU. It allows the gate array to initialize the RAM controller and the I/O decode circuits before the processor attempts to execute any cycles. The Reset signal, which goes to the 68030 and other I/O devices, has a longer time constant than Test and allows the processor to stabilize before executing any cycles.

Keyboard reset and NMI

There are no external reset or NMI switches (commonly referred to as programmers switches) on the Macintosh IIsi computer. These functions are now controlled from the keyboard by the custom ADB microprocessor .

NMI is a diagnostic signal that enables the debugging software to halt execution of an application and change to a debugger for low-level software and hardware testing. You can assert the NMI signal by pressing the Command key and the power button at the same time. The NMI feature is turned off initially. It must be turned on (using a new cdev) before it can be asserted. The assumption is that most users are not programmers.

You can assert a hard reset, identical to a power-on reset, by pressing the Command key, Control key, and power button at the same time. The NMI and Reset key sequences were chosen for compatibility with currently existing Macintosh utility software.

- *Note:* You must hold down the above sequences of keys for at least 1 second to allow the microcontroller enough time to respond to the NMI or hard-reset signal.

Network booting

The Macintosh IIsi computer is designed to provide future support for network booting (for example, starting up from a file server rather than an internal disk drive). You can use the Control Panel to set a flag in the ADB microcontroller that causes the system to start up over a communications network such as Ethernet or LocalTalk®. This feature is particularly useful in classroom situations where everyone has to start up from the same system image.

Programmable wakeup

The ADB microprocessor includes a function that allows setting of a wakeup time, causing the Macintosh IIsi computer to automatically power up at a specified time and perform an operation. These wakeup flags are contained in the code of the ADB microcontroller and are controlled by software.

Chapter 6 Expansion Interface

The Macintosh IIsi computer offers a choice of two different methods of expansion. Using the 120-pin expansion connector on the main logic board and an adaptor card, you can configure the Macintosh IIsi computer for a 68030 Direct Slot or as a NuBus slot. Each configuration requires its own unique adaptor card. Both adaptor cards include 68882 floating-point units for numeric coprocessing. If customers want numeric coprocessing but don't care about expansion, they still have to use an adaptor card. Both adapter cards are user installable. This chapter describes the Macintosh IIsi computer's expansion interfaces and compares them to the expansion interfaces used on other Macintosh computers.

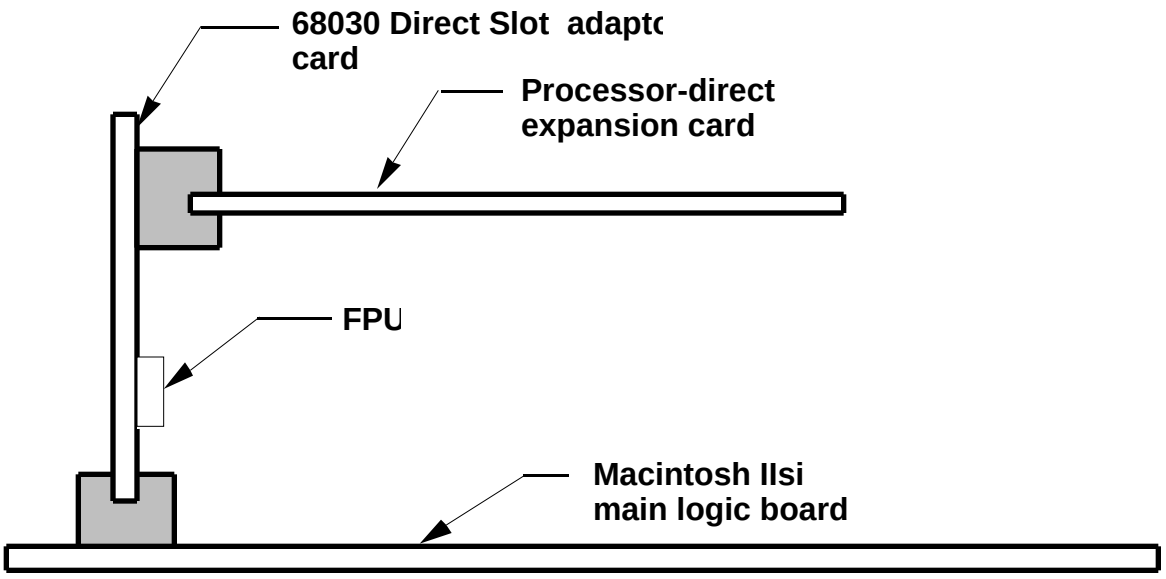
Processor-direct expansion interface

A 68030 Direct Slot adaptor kit, available from an authorized Apple dealer, allows a customer to install an existing Macintosh SE/30 processor-direct slot expansion card in the Macintosh IIsi computer and have it work exactly as it does in the Macintosh SE/30 computer, provided that the expansion card is able to operate at the Macintosh IIsi clock speed of 20 MHz. If it cannot, the expansion card developer must revise the card to be clock speed independent before it can be used in a Macintosh IIsi computer. Also, any new or revised cards should be designed to use 32-bit rather than 24-bit addressing.

Physical implementation of the 68030 Direct Slot adaptor kit

The 68030 Direct Slot adaptor card includes two 120-pin connectors. One is a plug connector that mates with the Euro-DIN 120-pin socket connector located on the left side (looking from the front) of the computer's main logic board. The adaptor card mounts vertically in this connector. The other connector on the adaptor card is a 120-pin socket connector (the same as the main logic board connector) into which the expansion card is installed. The expansion card is mounted horizontally over the main logic board. The adaptor kit includes a snap-in bracket that mounts to the power supply frame to support the expansion card and secure it to the machine. Figure 6-1 is a sketch showing a processor-direct slot expansion card and its adaptor card installed on the main logic board of a Macintosh IIsi computer.

Figure 6-1 Installing a PDS card and adaptor on the Macintosh IIsi main logic board



External connections for the PDS expansion card

The design of the Macintosh IIsi computer allows the use of existing hardware to connect an expansion card to the external world. This hardware is supplied with the expansion card and includes a small connector card, two screws, and a ribbon cable. You install the connector card (which is the same size as that specified for a Macintosh SE or a Macintosh SE/30 computer) to the opening in the rear of the Macintosh IIsi computer. You then plug the ribbon cable into a connector on the expansion card and route it underneath the expansion card to the connector card installed on the rear of the Macintosh IIsi computer. Current Macintosh SE/30 cards will work if their ribbon cables are at least 220 millimeters (8.6 inches) long between connectors.

◆ *Note:* The specifications for the connector card and ribbon cable have been changed to ensure compatibility with future Macintosh computers such as the Macintosh IIsi. Detailed information on the ribbon cable and connector card specifications are provided in Chapter 15 of *Designing Cards and Drivers for the Macintosh Family,* second edition. A drawing from that book showing pertinent design criteria for the connector card is provided in Figure 6-2.

■ **Figure 6-2** Connector card design guide

Figure 6-3 shows how a connector card is mounted on a Macintosh SE chassis. Although this drawing is not representative of a Macintosh IIsi computer, it emphasizes that you must include appropriate mounting holes on your connector card as well as two screws for attaching the card to the chassis. The required screw size is shown on the drawing.

■ **Figure 6-3** Connector card mounting requirements

Design considerations

Some important factors should be considered when using existing processor-direct slot expansion cards or designing new cards for the Macintosh IIsi computer.

- The fact that the ribbon cable from the expansion card to the connector card must travel the entire length of the main logic board this could have EMI implications for third-party cards. Therefore, at very least, cards should be tested to make sure that they still comply with FCC guidelines. In some cases, cables may need to be shielded or include ferrite sleeves in order not to violate the FCC specifications. At worst, the layout or design of an expansion card may need to be modified.
- Apple strongly recommends against designing cards to fit directly into the 120-pin connector on the main logic board (without an adaptor card) because the vertical position of the expansion card may cause EMI or thermal problems.
- Any processor-direct slot expansion cards designed to fit in a Macintosh SE/30 computer can be used in the Macintosh IIsi computer. Figures 6-4 through 6-6 are design guides for these expansion cards. These figures are taken from Chapter 15 of *Designing Cards and Drivers for the Macintosh Family,* second edition. For more detailed information refer to that document.

Figure 6-4 Smallest allowable PDS expansion card

■ **Figure 6-5** Largest allowable PDS expansion card

Figure 6-6 Maximum allowable component heights for PDS expansion card

Electrical implementation of a PDS expansion card

The expansion card connector on the Macintosh IIsi 68030 Direct Slot adaptor is electrically and functionally identical to the 68030 Direct Slot expansion connector on the Macintosh SE/30 computer. Figure 6-7 is a pinout of the connector, and Table 6-1 describes the signals.

A 68030 Direct Slot expansion card can occupy 32-bit addresses from $F900 0000 to $FBFF FFFF. This is equivalent to geographic NuBus locations $9, $A, and $B. (See Table 2-1.) If you are designing a new processor-direct expansion card, you should use the pseudo-slot design method to emulate this NuBus address space. Pseudo-slot design is described in Chapter 14 of *Designing Cards and Drivers for the Macintosh Family,* second edition. The advantage of designing a PDS card to occupy one of the unused NuBus addresses is that existing ROM firmware with the ability to manage NuBus slots is present in the Macintosh IIsi system ROM. If you design your card along the lines of a NuBus card (with a declaration ROM and interrupt capability), the Slot Manager in ROM controls your card as if it were a NuBus card, but the electrical interface is connected directly to the 68030 processor.

Chapter 14 of *Designing Cards and Drivers for the Macintosh Family,* second edition also includes information on interrupt handling, design considerations, and power budget that applies to Macintosh IIsi processor-direct slot expansion cards.

Figure 6-7 Macintosh IIsi 68030 Direct Slot expansion connector pinout

Table 6-1 Macintosh IIsi 68030 Direct Slot expansion connector signals

Connector	name	Signal description	Signal	Row	Pin
A	1	Reserved	For use by Apple		
A	2	Reserved	For use by Apple		
A	3	/BUSLOCK	NuBus buslock		
A	4	/IRQ3	Interrupt input 3		
A	5	/IPL2	Interrupt priority 2		
A	6	/CIOUT	Cache inhibit out		
A	7	/STERM	Synchronous termination		
A	8	/DSACK1	Data acknowledge 1		
A	9	SIZ1	Transfer size bit 1		
A	10	/BGACK	Bus grant acknowledge		
A	11	FC2	Function code 2		
A	12	/RESET	System reset		
A	13	D0	Data bit 0		
A	14	D2	Data bit 2		
A	15	D5	Data bit 5		
A	16	D8	Data bit 8		
A	17	D10	Data bit 10		
A	18	D13	Data bit 13		
A	19	D16	Data bit 16		
A	20	D18	Data bit 18		
A	21	D21	Data bit 21		
A	22	D24	Data bit 24		
A	23	D26	Data bit 26		
A	24	D29	Data bit 29		
A	25	A31	Address bit 31		
A	26	A29	Address bit 29		
A	27	A26	Address bit 26		
A	28	A23	Address bit 23		
A	29	A21	Address bit 21		
A	30	A18	Address bit 18		
A	31	A15	Address bit 15		
A	32	A13	Address bit 13		
A	33	A10	Address bit 10		
A	34	A7	Address bit 7		
A	35	A5	Address bit 5		
A	36	A2	Address bit 2		
A	37	+5V	5 volts		
A	38	CPUCLK	20 MHz CPU clock		

(continued)

Table 6-1 Macintosh IIsi 68030 Direct Slot expansion connector signals (continued)

Connector	Signal name	Signal description	Signal	Row	Pin
A	39	GND	Ground		
A	40	–12V	–12 volts		
B	1	Reserved	For use by Apple		
B	2	GND	Ground		
B	3	/TM1A	NuBus transfer mode bit 1		
B	4	/IRQ2	Interrupt input 2		
B	5	/IPL1	Interrupt priority 1		
B	6	/DS	Data strobe		
B	7	/CBACK	Cache burst acknowledge		
B	8	/DSACK0	Data acknowledge 0		
B	9	SIZ0	Transfer size bit 0		
B	10	/BG	Bus grant		
B	11	FC1	Function code 1		
B	12	/BERR	Bus error		
B	13	+5V	5 volts		
B	14	D3	Data bit 3		
B	15	D6	Data bit 6		
B	16	GND	Ground		
B	17	D11	Data bit 11		
B	18	D14	Data bit 14		
B	19	+5V	5 volts		
B	20	D19	Data bit 19		
B	21	D22	Data bit 22		
B	22	GND	Ground		
B	23	D27	Data bit 27		
B	24	D30	Data bit 30		
B	25	+5V	5 volts		
B	26	A28	Address bit 28		
B	27	A25	Address bit 25		
B	28	GND	Ground		
B	29	A20	Address bit 20		
B	30	A17	Address bit 17		
B	31	+5V	5 volts		
B	32	A12	Address bit 12		
B	33	A9	Address bit 9		
B	34	GND	Ground		
B	35	A4	Address bit 4		

(continued)

Table 6-1 Macintosh IIsi 68030 Direct Slot expansion connector signals (continued)

Connector	name	Signal description	Signal	Row	Pin
B	36	A1	Address bit 1		
B	37	+5V	5 volts		
B	38	ECLK	E clock		
B	39	GND	Ground		
B	40	–5V	–5 volt		
C	1	/PFW	Power fail warning signal		
C	2	/NUBUS	NuBus space access		
C	3	/TM0A	NuBus transfer mode bit 0		
C	4	/IRQ1	Interrupt input 1		
C	5	/IPL0	Interrupt priority 0		
C	6	/RMC	Read modify cycle		
C	7	/CBREQ	Cache burst request		
C	8	/R/W	Read/write		
C	9	/AS	Address strobe		
C	10	/BR	Bus request		
C	11	FC0	Function code 0		
C	12	/HALT	Halt		
C	13	D1	Data bit 1		
C	14	D4	Data bit 4		
C	15	D7	Data bit 7		
C	16	D9	Data bit 9		
C	17	D12	Data bit 12		
C	18	D15	Data bit 15		
C	19	D17	Data bit 17		
C	20	D20	Data bit 20		
C	21	D23	Data bit 23		
C	22	D25	Data bit 25		
C	23	D28	Data bit 28		
C	24	D31	Data bit 31		
C	25	A30	Address bit 30		
C	26	A27	Address bit 27		
C	27	A24	Address bit 24		
C	28	A22	Address bit 22		
C	29	A19	Address bit 19		
C	30	A16	Address bit 16		
C	31	A14	Address bit 14		
C	32	A11	Address bit 11		

(continued)

Table 6-1 Macintosh IIsi 68030 Direct Slot expansion connector signals (continued)

Connector	name	Signal description	Signal	Row	Pin
C	33	A8	Address bit 8		
C	34	A6	Address bit 6		
C	35	A3	Address bit 3		
C	36	A0	Address bit 0		
C	37	+5V	5 volts		
C	38	C16M	15.6672 MHz gen clock		
C	39	GND	Ground		
C	40	+12V	+12 volts		

Table 6-2 provides the load presented or drive available to each pin of an expansion card and indicates whether the signals are inputs or outputs.

In the column labeled *Input/output* in Table 6-2*,* input refers to a signal from the expansion card to the processor and corresponds directly to the load shown in the column labeled *Load or driv*e *limits.* Output refers to a signal from the processor to the expansion card and corresponds directly to the drive shown in that column. An example may be helpful in interpreting the *Load or drive limits* column. The /RESET line is shown as presenting a load of 300 µA/8 mA, 50 pF. This is the maximum expected load that an expansion card must drive when sending a /RESET signal to the main logic board. The DC load is given in the format *signal high/signal low*. This means that the expansion card must drive a load of up to 300 uA when it drives /RESET high (logic 1) and a load of up to 8 mA when it drives /RESET low (logic 0). The AC load is given as 50 pF, the maximum capacitance to ground presented by the main logic board to AC signals from an expansion card. The notation “Open collector; 1 kΩ pullup” in the table means that the /RESET line is normally in the open collector state; it is only driven low, and a 1 kilohm pullup resistor on the main logic board returns the line to a logic 1.

Additionally, /RESET presents a drive of 40 uA/.4 mA, 30 pF. This is the maximum amount of drive from the main logic board that is available to integrated circuits on the expansion card. The /RESET line can drive an expansion card DC load of up to 40 µA in the high state or up to .4 mA in the low state. The AC drive is given as 30 pF, the maximum capacitance to ground that an expansion card may present to AC signals from the /RESET line.

Some of the expansion connector signals are specified to drive one 74LS input (a standard 74LS input load is 20 µA high, .2 mA low); other signals can drive two 74LS inputs. These strict limitations are imposed to protect the noise and timing margins of the main logic board. All signals needed by an expansion card should be buffered at the expansion connector. The use of newer logic families with very low input loading allows you more margin and flexibility in your expansion card designs.

Where “Load:” is in parentheses, the pin carries a signal that is usually an output driven by the MC68030 but that is tri-stated by the MC68030 after granting the bus to a DMA requester. When tri-stated by the MC68030, this signal may be driven by an expansion card.

Table 6-2 Macintosh IIsi 68030 Direct Slot signals, loading or driving limits

Signal name	Input/output	Load or drive limits
A0–A31	In/Out	Load: 300 µA/5 mA, 100 pF Drive: 40 µA/.4 mA, 30 pF
D0–D23	In/Out	Load: 300 µA/5 mA, 100 pF Drive: 40 µA/.4 mA, 30 pF
D24–D31	In/Out	Load: 300 µA/5 mA, 100 pF Drive: 20 µA/.2 mA, 30 pF
/RESET	In/Out	Load: 300 µA/8 mA, 50 pF Drive: 40 µA/.4 mA, 30 pF Open collector, 1 kΩ pullup
/BERR	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.4 mA, 30 pF Open collector, 1 kΩ pullup
/HALT	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.4 mA, 30 pF Open collector, 1 kΩ pullup
FC0–FC2	Output	Drive: 20 µA/.2 mA, 30 pF (Input) (Load: 100 µA/8 mA, 50 pF) Open collector, 1 kΩ pullup
/BR	Input	Load: 100 µA/8 mA, 50 pF 1 kΩ pullup
/BG	Output	Drive: 40 µA/.4 mA, 30 pF
/BGACK	Input	Load: 100 µA/8 mA, 50 pF 1 kΩ pullup
SIZ0–SIZ1	Output	Drive: 40 µA/.4 mA, 30 pF (Input) (Load: 100 µA/100 µA, 50 pF)
/AS	Output	Drive: 40 µA/.2 mA, 30 pF (Input) (Load: 100 µA/8 mA, 50 pF) Open collector, 1 kΩ pullup
/DSACK0–/DSACK1	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.2 mA, 30 pF Open collector, 1 kΩ pullup

(continued)

Table 6-2 Macintosh IIsi 68030 Direct Slot signals, loading or driving limits (continued)

Signal name	Input/output	Load or drive limits
R/W	Output	Drive: 40 µA/.4 mA, 30 pF (Input) (Load: 400 µA/8 mA, 50 pF) Open collector, 1 kΩ pullup
/STERM	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.4mA, 30 pF Open collector, 1 kΩ pullup
/CBACK	Input	Load: 100 µA/100 µA, 50 pF
/CBREQ	Output	Drive: 40 µA/.4 mA, 30 pF
/CIOUT	Output	Drive: 40 µA/.4 mA, 30 pF
/DS	Output	Drive: 40 µA/.4 mA, 30 pF (Input) Load: 100 µA/8 mA, 50 pF Open collector, 1 kΩ pullup
/RMC	Output	Drive: 40 µA/.4 mA, 30 pF
/IPL0–/IPL2	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.4 mA, 30 pF
/IRQ0–/IRQ3	Input	Load: 400 µA/4 mA, 50 pF
/TM0A	Input	Load: 400 µA/2 mA, 50 pF
/TM1A	Input	Load: 400 µA/2 mA, 50 pF
/BUSLOCK	Input	Load: 400 µA/2 mA, 50 pF
/NUBUS	Output	Drive: 40 µA/.4 mA, 30 pF
PFW	Output	Drive: 40 µA/.4 mA, 30 pF
CPUCLK	Output	Drive: 40 µA/.4 mA, 30 pF
C16M	Output	Drive: 40 µA/.4 mA, 30 pF
ECLK	Output	Drive: 40 µA/.4 mA, 30 pF

RAM access from a PDS expansion card

The memory cycle for a Macintosh IIsi processor-direct expansion card operating as bus master is substantially different from that of the Macintosh SE/30 computer. It has been changed to support burst transfers using the /STERM signal generated by the MDU rather than the /DSACK signal generated by the general logic unit chip. If bus master cards look only for /DSACK, they will not work. Figures 6-8 through 6-9 show the timing for both random and burst writes to RAM and reads from RAM.

Figure 6-8 RAM burst write timing

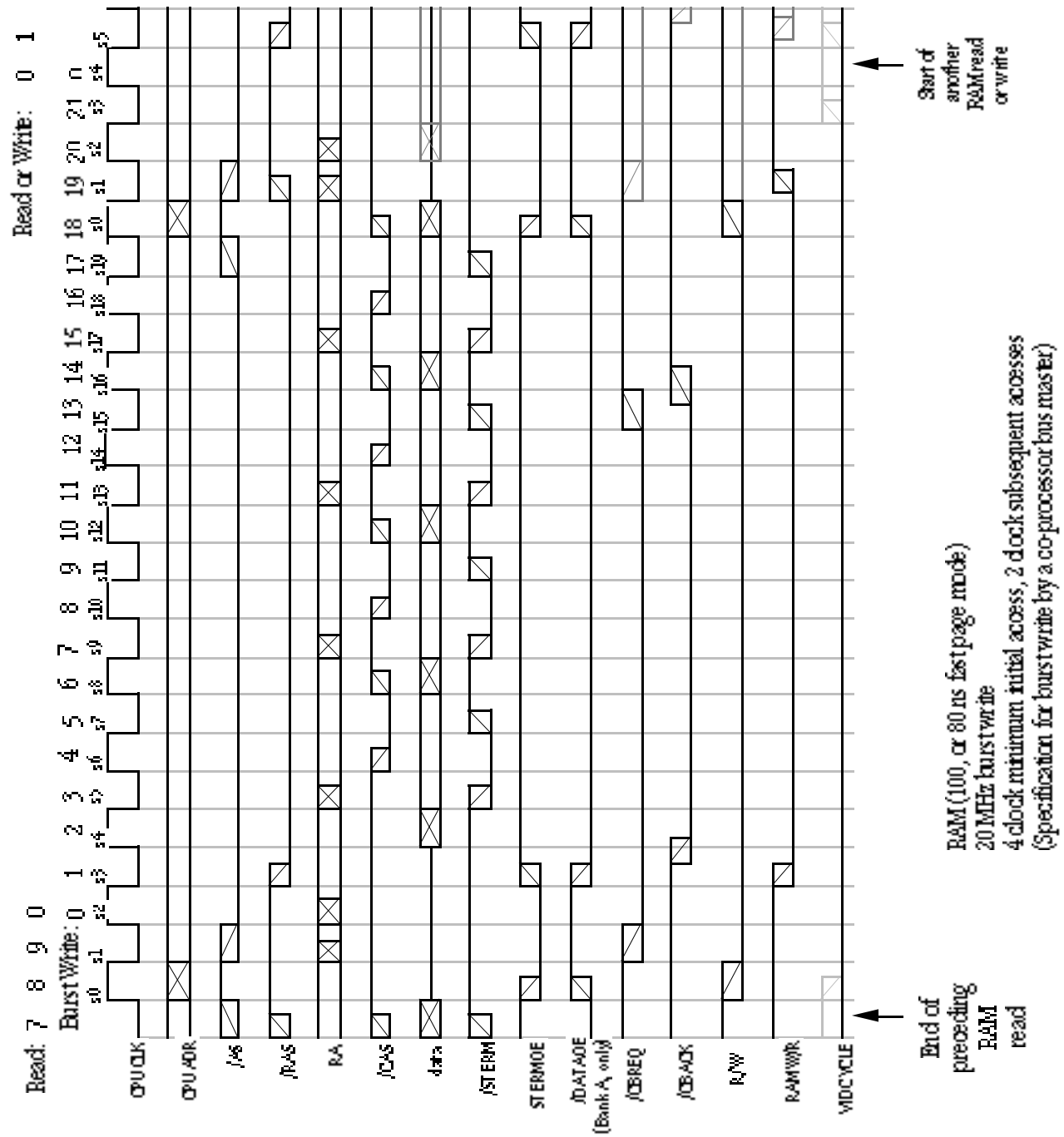


Figure 6-9 RAM random write timing

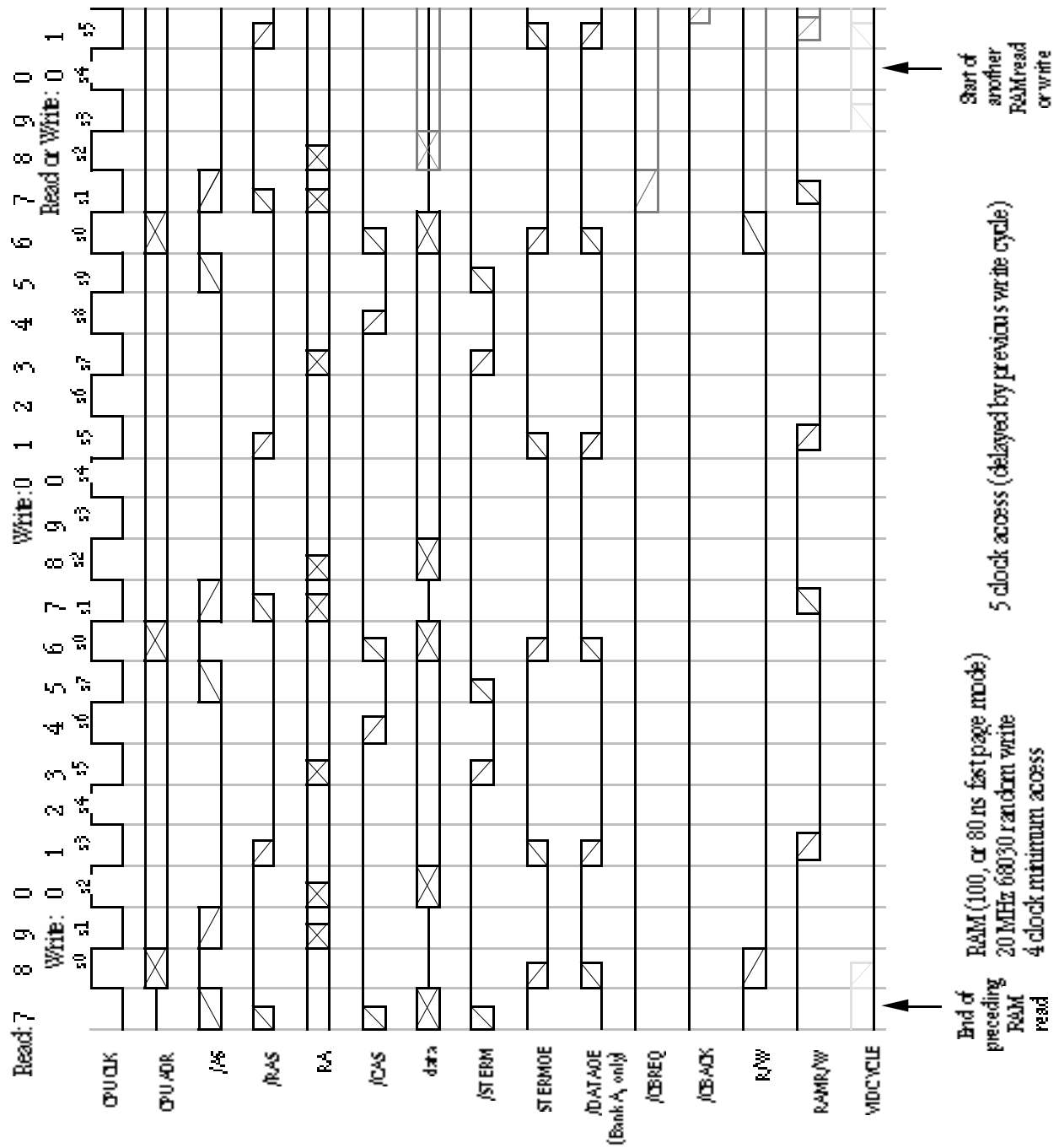


Figure 6-10 RAM burst read timing

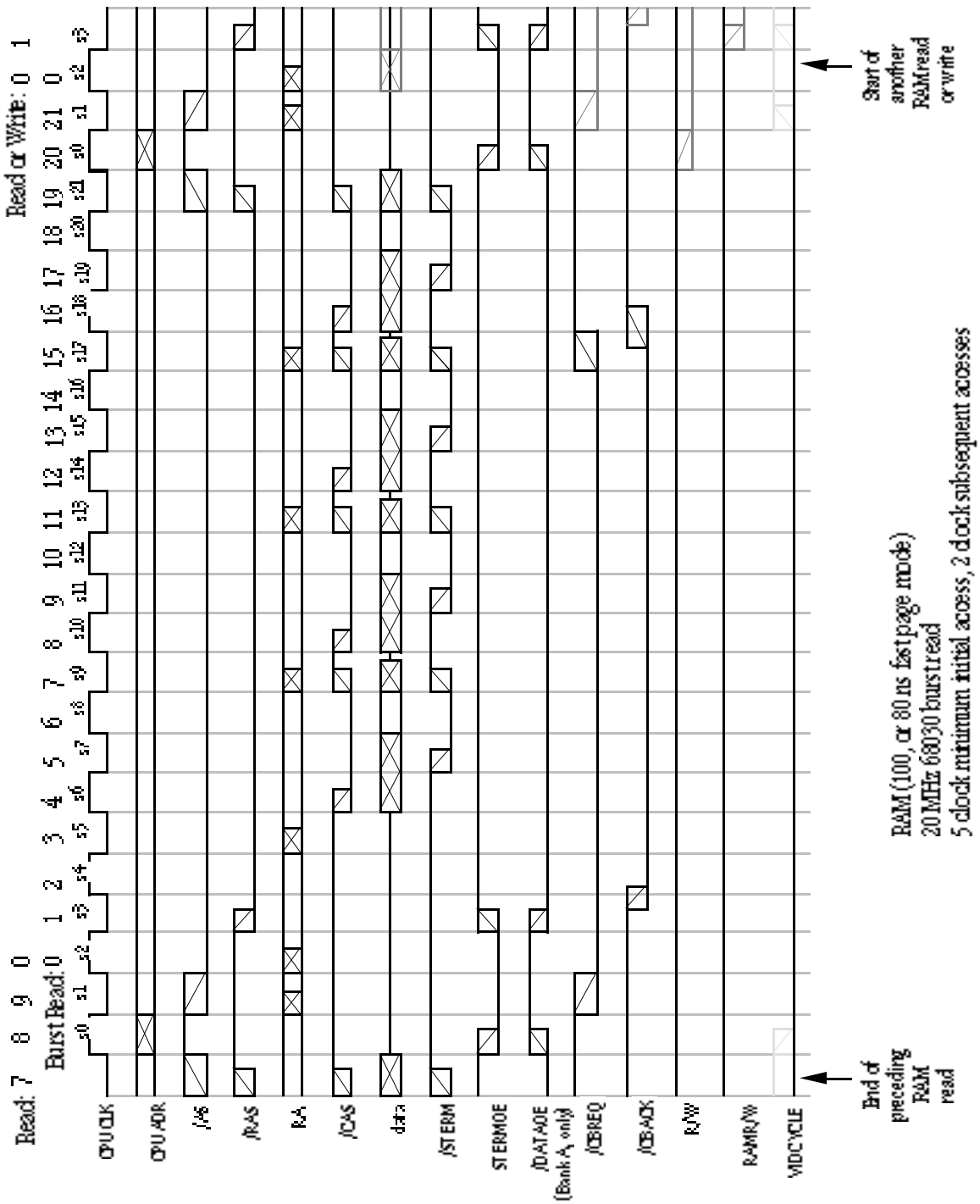
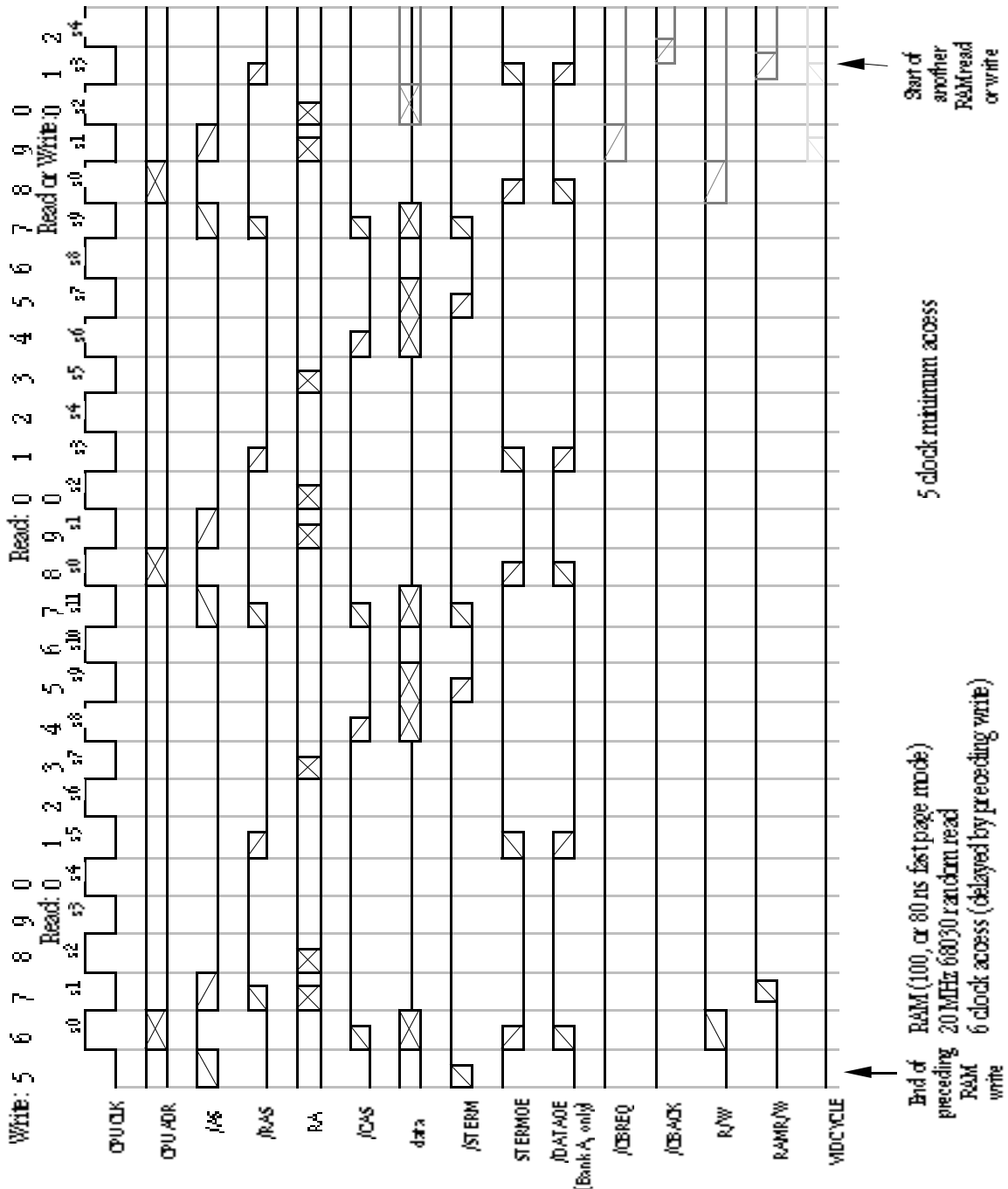


Figure 6-11 RAM random read timing



NuBus expansion interface

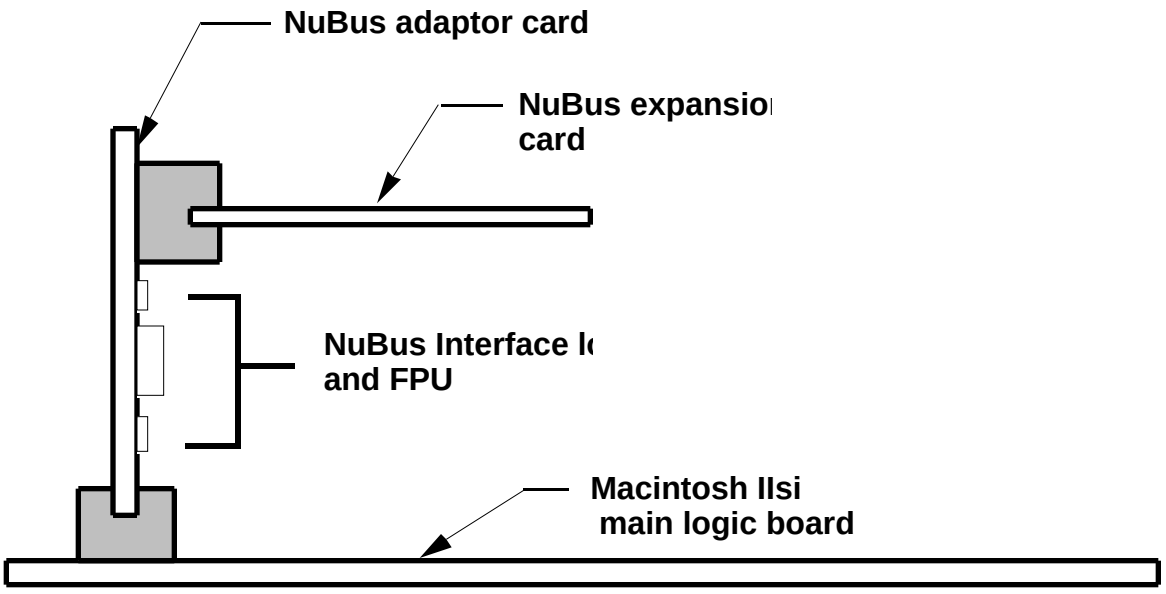
A NuBus adaptor kit, available from an authorized Apple dealer, allows a customer to install a NuBus card in the Macintosh IIsi computer and have it function exactly as if it were in any other Macintosh II–family computer. The major difference between the Macintosh IIsi computer and other Macintosh II–family computers is that the Macintosh IIsi computer has only one NuBus slot which is mapped to geographic address $9. (See Table 2-1.) On the Macintosh IIci computer, for example, there are three NuBus slots, mapped to geographic addresses $C through $E. The different address mappings are transparent to the cards.

Physical implementation of the NuBus adaptor kit

The NuBus adaptor card includes two different connectors. One is a 120-pin plug connector that mates with the Euro-DIN 120-pin socket connector on the left side (looking from the front) of the main logic board. The adaptor card mounts vertically in this connector. The other is a 96-pin socket connector (the same as the NuBus connectors on the main logic boards of other Macintosh II–family computers). The NuBus card plugs into this connector and is positioned horizontally over the main logic board. The adaptor card also includes a bracket that adapts the NuBus card's connector to the opening in the back of the Macintosh IIsi computer. This bracket provides both EMI protection and support for the card. Two screws are included in the adaptor card kit to secure the bracket to the opening in the chassis. The top cover of the Macintosh IIsi computer includes grooves that hold the NuBus card in place when the cover is closed. There is just enough gap between the top cover and bottom half of the case for a .062-inch thick card, which is Apple's specification for a NuBus card. Any size NuBus card specified by Apple can be accommodated in the Macintosh IIsi computer.

Figure 6-12 is a sketch showing a NuBus card and its adaptor card installed on the main logic board of a Macintosh IIsi computer. Notice that, unlike the 68030 Direct Slot adaptor card, the NuBus card has other electrical components in addition to the FPU, including the custom NuChip 30 and associated transceiver chips that comprise the NuBus interface logic. Although functionally identical to that of the Macintosh IIsi, the NuBus interface logic in other Macintosh II–family computers is on the main logic board.

Figure 6-12 Installing a NuBus card and adaptor on the Macintosh IIsi main logic board



Electrical implementation of a NuBus expansion card

The NuBus cards used in the Macintosh IIsi computer are electrically and functionally identical to those used in all other computers in the Macintosh II family. Table 6-3 is a pinout of the 96-pin NuBus connector, and Table 6-4 describes the signals.

Additional information on the NuBus interface can be found in Part I of *Designing Cards and Drivers for the Macintosh Family,* second edition.

Table 6-3 NuBus connector pin assignments

Pin	Row A	Row B	Row C	Pin	Row A	Row B	Row C
1	–12V	–12V	/RESET	17	/AD23	GND	/AD22
2	‡	GND	‡	18	/AD25	GND	/AD24
3	/SPV	GND	+5V	19	/AD27	GND	/AD26
4	/SP	+5V	+5V	20	/AD29	GND	/AD28
5	/TM1	+5V	/TM0	21	/AD31	GND	/AD30
6	/AD1	+5V	/AD0	22	GND	GND	GND
7	/AD3	+5V	/AD2	23	GND	GND	/PFW
8	/AD5	†	/AD4	24	/ARB1	†	/ARB0
9	/AD7	†	/AD6	25	/ARB3	†	/ARB2
10	/AD9	†	/AD8	26	/ID1	†	/ID0
11	/AD11	†	/AD10	27	/ID3	†	/ID2
12	/AD13	GND	/AD12	28	/ACK	+5V	/START
13	/AD15	GND	/AD14	29	+5	+5V	+5V
14	/AD17	GND	/AD16	30	/RQST	GND	+5V
15	/AD19	GND	/AD18	31	/NMRQ	GND	GND
16	/AD21	GND	/AD20	32	+12V	+12V	/CLK

† These pins are connected but not supplied with the –5.2 V described in the Texas Instruments NuBus specification.

‡ These pins are reserved in the standard IEEE 1196; in the Macintosh II family, they are grounded.

Table 6-4 NuBus signal descriptions

Classification	Signal	Signal description	Number of pins
Utility	/RESET	Reset	1
	/CLK	Clock	1
	/PFW	Power fail warning	1
	/NMRQ	Nonmaster request	1
Control	/START	Start	1
	/ACK	Acknowledge	1
	/TM0	Transfer mode 0	1
	/TM1	Transfer mode 1	1
Address/data	/AD31–/AD0	Address/data	32
Arbitration	/ARB3–/ARB0	Arbitration	4
	/RQST	Request	1
Parity	/SP	System parity	1
	/SPV	System parity valid	1
Slot ID	/ID3–/ID0	Slot identification	4
		Total signals	**51**
Power/ground	+5V		11
	+12V		2
	–12V		2
	–5V (not supplied) †		8
	GND	Ground	20
	Reserved	Reserved	2
		Total pin count	**96**

† These pins are wired together but not supplied with power from the computer.