Chapter 1 Introduction

The Macintosh® IIsi computer is a new midrange Macintosh computer based on the modular design concept. It offers significantly improved performance (approximately six times faster speed than that of the Macintosh Plus computer), new features, and increased flexibility. This chapter describes the features of the Macintosh IIsi computer.

Features

The Macintosh IIsi computer shares many, but not all of the features of the more powerful Macintosh IIci computer. Like that of the Macintosh IIci, the architecture of the Macintosh IIsi is based on the Memory Decode Unit (MDU) and RAM-Based Video (RBV) chips.

Key features are the computer's 20 MHz clock speed, on-board video, sound input capability, flexible expansion (NuBus™ or processor-direct slot), custom microcontroller that controls the Apple Desktop Bus™ (ADB), real-time clock, soft power control, power-on reset functions, and custom chip that combines SCSI (Small Computer Systems Interface) and SCC (Serial Communications Controller) functions.

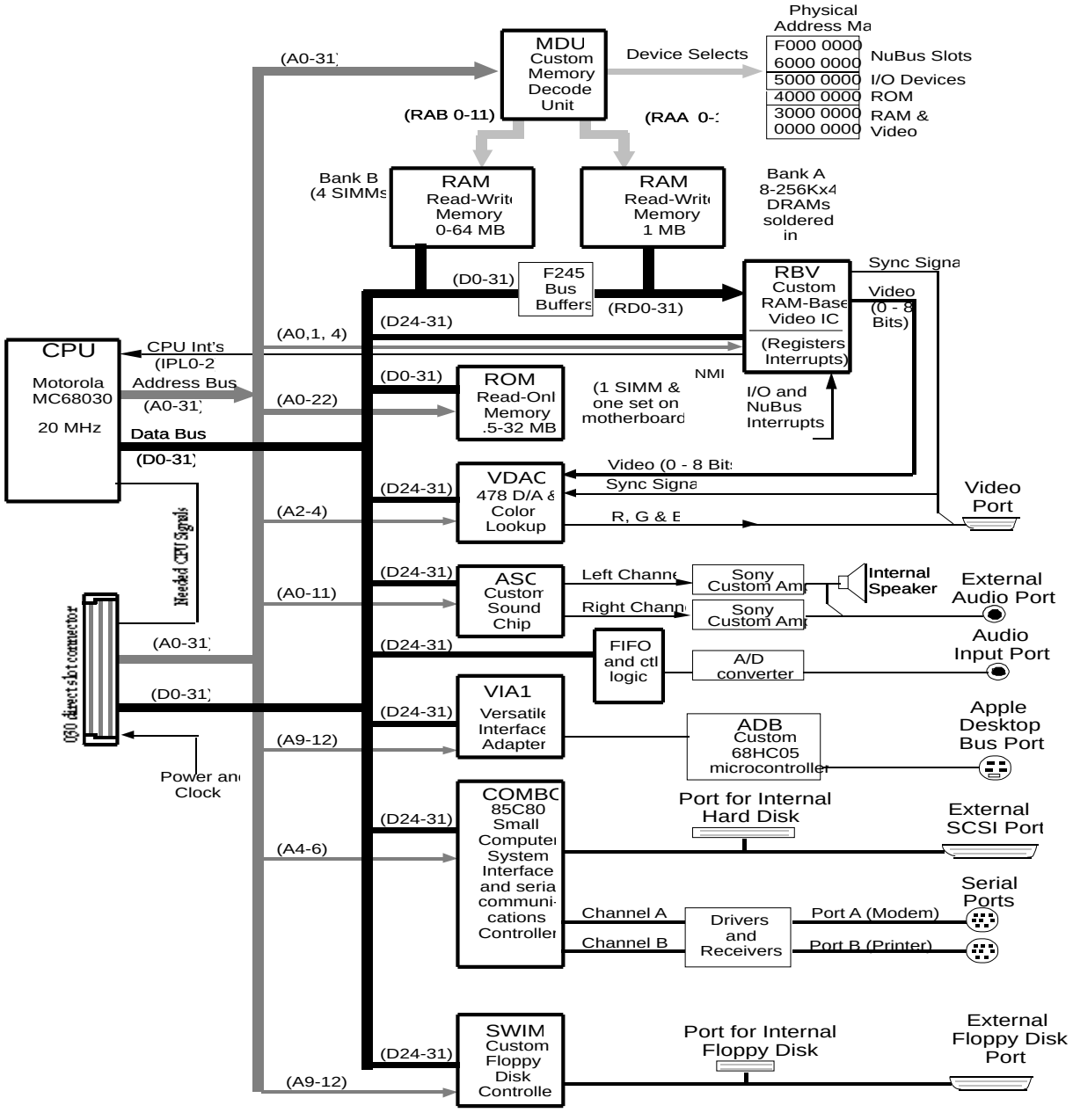
The major features of the Macintosh IIsi computer's design are the following:

- MDU/RBV architecture: new chip set providing memory decoding and low-cost video by utilizing existing on-board dynamic random-access memory (DRAM) for the frame buffer.
- Burst reads: MDU supports 68030 burst reads from random-access memory (RAM.)
- On-board video: on-board video support for 12-inch B & W, 12-inch RGB, and 13-inch RGB monitors and 15-inch B & W portrait monitor.
- RAM expansion: address space for from 1 MB to 65 MB of RAM on the main logic board. The basic system includes 1 MB of RAM soldered to the main logic board and 1 MB in four expansion Single Inline Memory Module (SIMM) sockets. Four-Mbit DRAM is currently supported (16-Mbit DRAM will be supported if the refresh frequency remains compatible).
- ROM expansion: basic system consists of 512 KB of ROM soldered on the main logic board. A ROM SIMM allows future ROM revision or expansion in the field.
- Flexible slot expansion: one 120-pin expansion connector. Optional user-installable adaptors allow installation of either one 68030 Direct Slot expansion card or one NuBus card. Each adaptor includes a floating-point unit (FPU) numerics coprocessor.
- Hard drive support: one internal hard drive (3.5 inch, one-third height, 40 or 80 MB) with 50-pin SCSI interface. Additional storage capacity available by connecting up to 6 additional external hard drives to the SCSI port on back of the computer.
- Floppy drive support: one internal 1.4 MB, 3.5-inch SuperDrive™. Support for one external 800 KB floppy drive or one 1.4 MB, 3.5-inch SuperDrive. (See "Compatibility" later in this chapter.)

- 68030 processor: true 32-bit processor running at 20 MHz. The 68030 has internal 256-byte data and instruction caches as well as on-chip memory management. Burst reads to the on-chip cache are supported. The 68030 is compatible with existing Macintosh timings and software.
- Memory management: true 32-bit address translation with hardware page replacement.
- Built-in serial ports: two Macintosh 8-pin serial ports supporting RS-232, RS-422 and AppleTalk®.
- ADB: one ADB port supporting the standard input devices (keyboard and mouse) and allowing additional input devices (for example, a graphics tablet) to be added at any time. A maximum of three chained devices is supported.
- ADB microcontroller: a custom version of the Motorola 68HC05 microcontroller that integrates the functions of ADB, soft power control, real-time clock, parameter RAM, and power on reset. The ADB keyboard interface also provides keyboard-controlled reset and nonmaskable interrupt (NMI) functions. (On other Macintosh models, these functions are hardware controlled by the programmers switch and the Reset switch.)
- Numerics processor: 20 MHz 68882 FPU that allows high-speed, high-accuracy floating-point computation to IEEE standards. The FPU is not part of the basic machine. It is included on both the NuBus and 68030 Direct Slot expansion card adaptors. These adaptors are available from authorized Apple dealers and can be installed by users.
- Sound: Apple Sound Chip provides Macintosh-compatible sound output and four-voice synthesis in hardware. The sound circuitry has also been enhanced to provide sound input capability. Sound from a microphone or line input is digitized (8-bit monaural) and stored along with other data to be used for a variety of purposes such as presentations or the creation of “living” documents. Microphone and RCA adaptor plug are included with the Macintosh IIsi computer as standard equipment.
- Video: on-board video support for Apple 12-inch B&W, 12-inch RGB, and 13-inch RGB monitors and the 15-inch B&W Portrait monitor. Processor-direct slot (PDS) and NuBus video card options are also available.

Figure 1-1 is a detailed block diagram showing the relationships of all the major components of the Macintosh IIsi computer.

Figure 1-1 Block diagram of the Macintosh IIsi computer



Compatibility

The Macintosh IIsi computer is based on an existing chip set but incorporates some new features, resulting in some possible hardware and software compatibility issues. The rest of this chapter describes those features and their related comnpatibility issues.

Floppy disks

The external floppy drive port on the Macintosh IIsi does not support the 400 KB floppy disk drive. It supports 400 KB disks used in the 800 KB drive.

Hard disks

The Macintosh IIsi computer's internal one third-height, 40 or 80 MB hard drive connects to the 50-pin industry standard SCSI connector on the Macintosh IIsi main logic board. Support for an HD20 hard drive is provided through an 'INIT' resource that you can install in the System Folder

Memory

Physical memory in the Macintosh IIsi is not contiguous, as it is on the Macintosh II, IIx, and IIcx computers. In the Macintosh IIsi, the 68030 on-chip memory management unit (MMU) is used to join the discontiguous blocks of physical memory to present contiguous logical memory to application software. RAM must be 100 nanoseconds access time (or faster), fast page mode. For additional RAM specifications, see "RAM Interface" in Chapter 3.

New ADB implementation

The Macintosh IIsi computer uses a custom chip to integrate the ADB and a number of other functions, including real-time clock, parameter RAM, power-on reset, keyboard reset, and NMI. This implementation is described in Chapter 5 in the section "ADB Microcontroller." If you have developed applications that address the ADB hardware directly, they will probably not function under this new scheme. Also, you will have to revise debuggers to support the keyboard-based NMI.

New SCSI and SCC implementation

The new Combo chip which combines the functions of SCSI, and SCC is described in Chapter 5 in the section "SCSI and SCC Interfaces." Although this new chip is software compatible with the previous implementation of these functions, your applications will possibly be inoperable if they attempt to access the hardware directly.

New sound input/output hardware

Details on the Macintosh IIsi computer's sound system implementation are provided in Chapter 5 in the section "Sound Interface." The Macintosh IIsi computer uses the Apple Sound Chip (ASC) to provide sound output and four-voice synthesis. The sound circuitry has also been enhanced to provide a sound input capability. If your application uses the Sound Manager calls and does not try to access the ASC hardware directly, it will work as documented.

No on-board mathematics coprocessor (FPU)

The Macintosh IIsi does not include an FPU as a standard feature. The FPU is available, however, on the 68030 Direct Slot and NuBus adaptor cards. Either of these optional cards may be purchased from an Apple dealer. For more information on the FPU, refer to Chapter 6, "Expansion Interface.'"

Application software should not assume that the Macintosh IIsi has an FPU simply because it uses a 68030 microprocessor. To ensure that your application is compatible with the Macintosh IIsi and future Macintosh computers that do not have FPUs, use the Gestalt Manager (the successor to SysEnvirons). Using the Gestalt manager allows you to determine the exact configuration of the machine you are running on.

If the application is provided in two versions, one that uses SANE® (Standard Apple Numerics Environment) software and another that requires the FPU hardware to perform its numeric calculations, or if it makes a conditional branch to execute floating-point instructions directly, then your application should check first for the presence of an FPU. The following pseudocode shows the correct way to check for an FPU:

```
IF I require an FPU THEN
      Call Gestalt Manager
      IF FPU is present THEN
            FPU_Present=True
END IF
```

Color compatibility

You should not limit your new color applications to working on only the current version of the Macintosh IIsi. Instead, you should design your software so that it is capable of working with other display devices that could eventually be supported by the Macintosh IIsi and future Macintosh computers. Apple has defined high-level calls and documented data structures for determining characteristics of display devices. These calls are documented in the "Graphics Devices" section of *Inside Macintosh,* Volume V. Taking advantage of these calls and data structures will increase the functionality, flexibility, and longevity of your programs. The Macintosh IIsi computer's 32-bit color QuickDraw™ is further documented in the 32-bit QuickDraw release notes, and in Developer Technical Support's Technical Note #275.

Your application should use the Gestalt Manager (included in system software version 6.0.4 and later) to determine the resolution and size of the attached monitor. You can make sure your application will be compatible with future computers by designing it to check explicitly for each required feature.

Chapter 2 Address Mapping

The Macintosh IIsi computer uses a memory-mapping scheme that is implemented by a custom integrated circuit called the Memory Decode Unit. The memory map controlled by the MDU is described in this chapter.

Address space

The address space is decoded by the Memory Decode Unit (MDU). On power-up, ROM is mapped by the MDU to physical location $0000 0000. This mapping enables the starting address retrieved by the 68030 on reset to be stored in ROM. After the first access to the true ROM address space ($4000 0000 through $4FFF FFFF), the normal memory map is imposed by the MDU. The only change from one map to the other is that in the power-up map, ROM is selected for addresses $0000 0000 through 3FFF FFFF, whereas the normal map selects RAM for that address space, as shown in Figure 2-1.

Programmable memory management

Memory mapping is performed by the MMU (memory management unit), whose function is built into the 68030 microprocessor. Having the MMU function built into the microprocessor saves one wait state over the use of an external 68851 Paged Memory Management Unit (PMMU) or Apple Hochsprung Memory Management Unit (HMMU) with the 68020 microprocessor on the Macintosh II. However, the 68030 on-chip MMU provides only a subset of the 68851 coprocessor's capabilities. The 68030 allows memory management that is required when running virtual memory systems such as A/UX®.

Software determines the memory size at power-on and compiles a table describing the current memory configuration. The MMU is then programmed based on this table to provide contiguous logical memory from the potentially noncontiguous physical segments in Banks A and B.

The memory map

The memory map is designed to allow existing Macintosh software to use a 24-bit address mode and new software to use the full 32-bit address space. The memory map is implemented as a simple direct mapping, as shown in Figure 2-2 and Table 2-1. The memory maps are set up by the 68030 microprocessor's on-chip MMU. Note that this memory mapping scheme maps the video frame buffer into the NuBus super slot space.

Figure 2-1 The physical memory maps

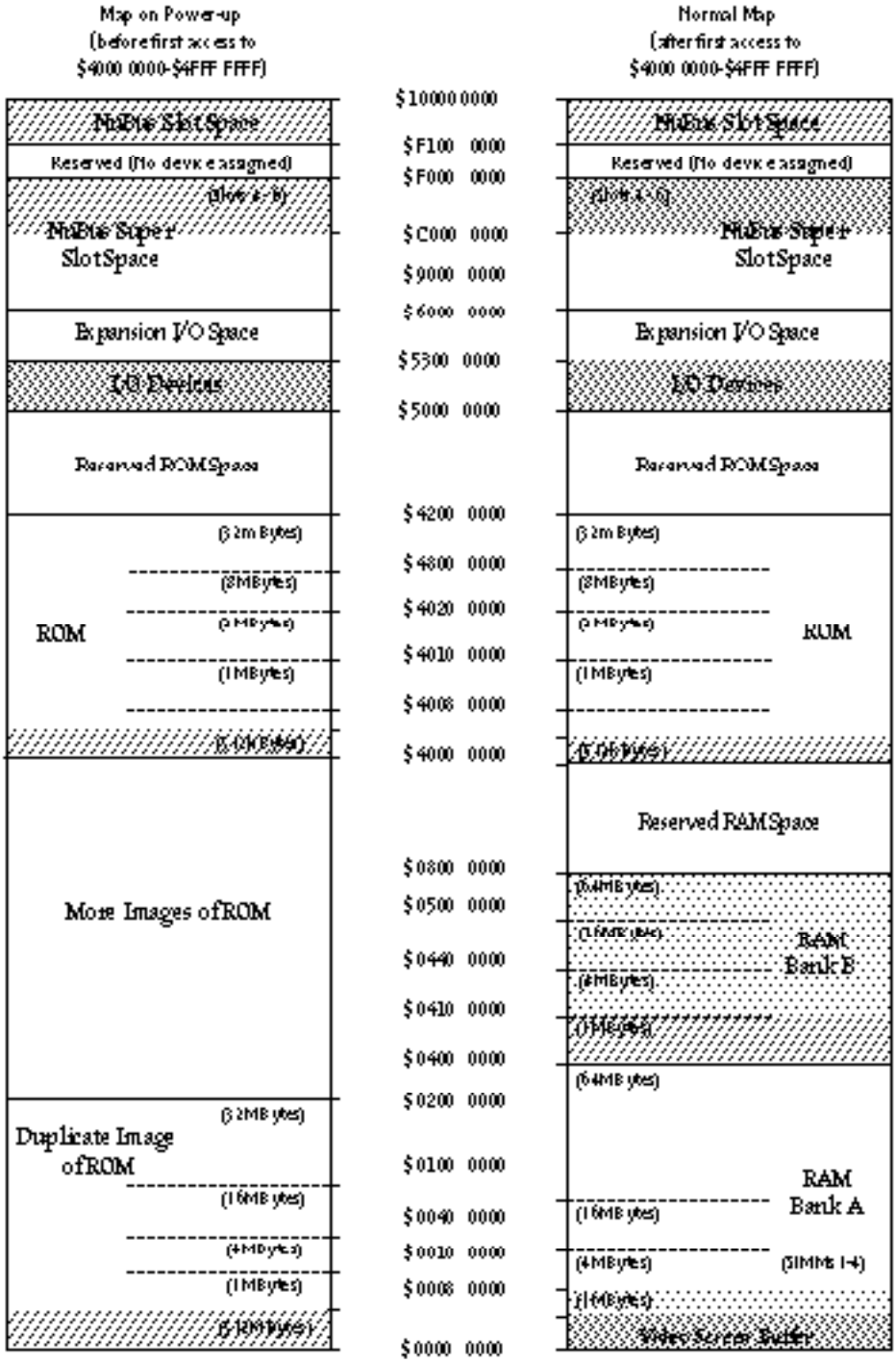
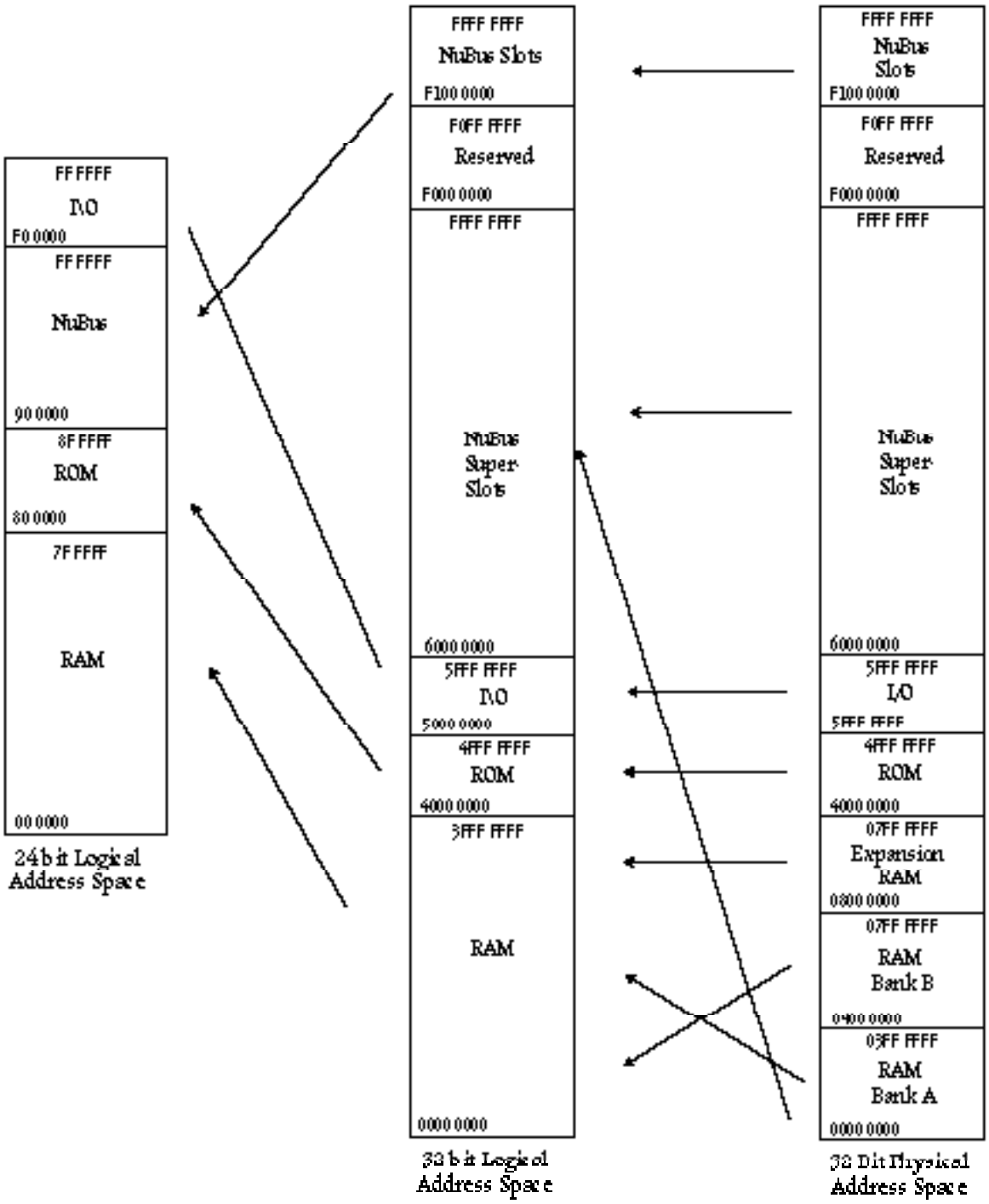


Table 2-1 24-bit–to–32-bit mapping mode

Usage		24 bit Address Range		32 bit Address Range	
		from	to	from	to
RAM		$xx00 0000	$xx7F FFFF	$0000 0000	$07FF FFFF
ROM		$xx80 0000	$xx8F FFFF	$4000 0000	$400F FFFF
NuBus/030 slot	NuBus Address $9	$xx90 0000	$xx9F FFFF	$F900 0000	$F90F FFFF
030 slot	NuBus Address $A	$xxA0 0000	$xxAF FFFF	$FA00 0000	$FA0F FFFF
030 slot	NuBus Address $B	$xxB0 0000	$xxBF FFFF	$FB00 0000	$FB0F FFFF
not used		$xxC0 0000	$xxCF FFFF	$FC00 0000	$FC0F FFFF
not used		$xxD0 0000	$xxDF FFFF	$FD00 0000	$FD0F FFFF
on-board video	NuBus Address $E	$xxE0 0000	$xxEF FFFF	$FE00 0000	$FE0F FFFF
I/O Space		$xxF0 0000	$xxFF FFFF	$5000 0000	$500F FFFF

Figure 2-2 24- and 32-bit address spaces



Chapter 3 The Memory Interface

This chapter provides the electrical and physical details of the RAM and ROM memory implementation in the Macintosh IIsi computer.

RAM interface

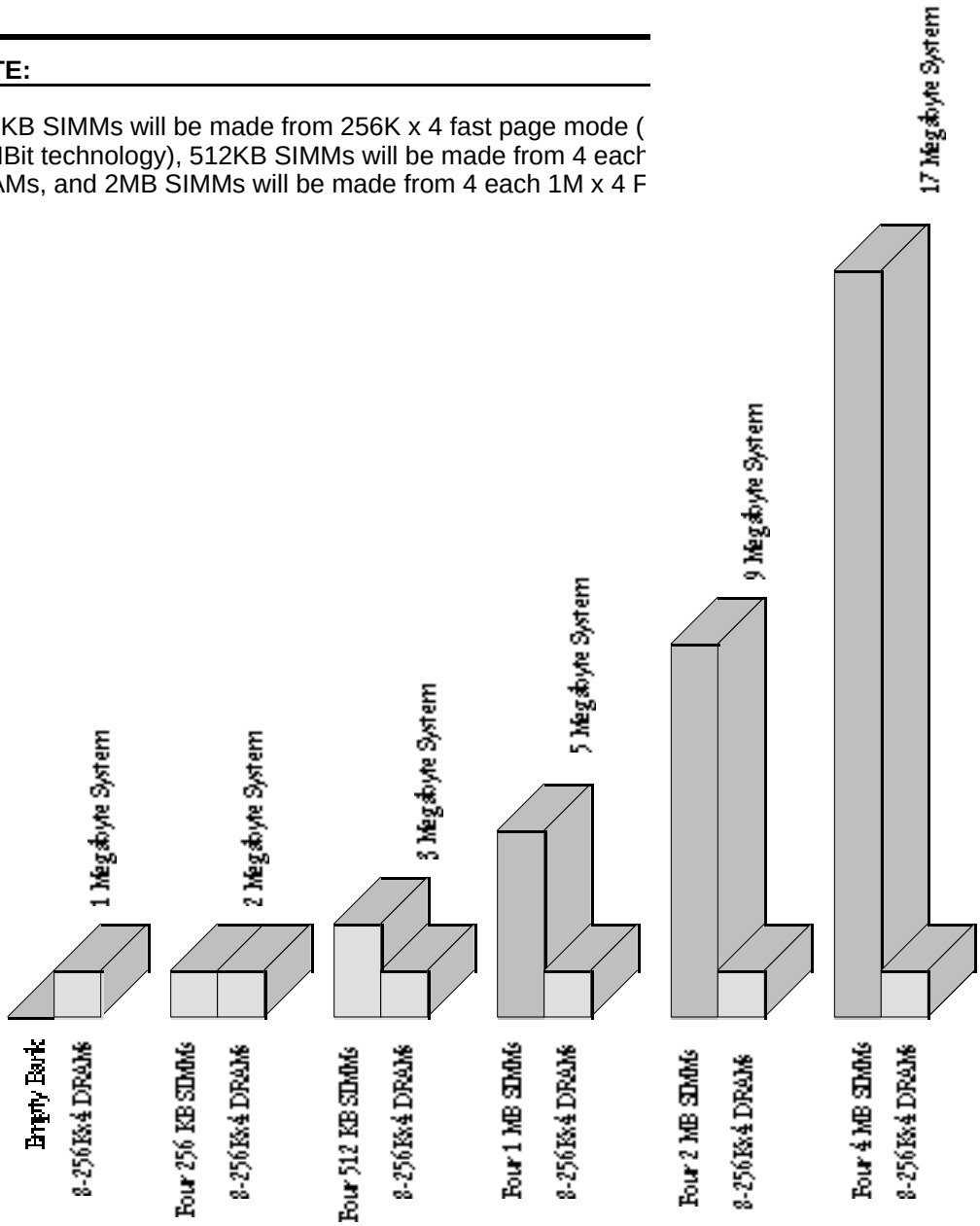
The random-access memory (RAM) interface on the main logic board is designed to support from 1 MB to 65 MB of RAM. The interface uses the /STERM synchronization memory termination signal to support burst-read mode, a mode which allows a 5-clock initial access followed immediately by three 2-clock accesses. The first 1 MB of RAM is soldered onto the main logic board and is called Bank A. The Bank A memory consists of eight 256K x 4 DRAMs with fast page mode capability. On-board video operates out of Bank A. Expansion RAM is supplied by four Single Inline Memory Module (SIMM) sockets and is called Bank B. The Bank B expansion memory can contain either four 256 KB SIMMs (made from 1-Mbit fast page mode parts), four 1 MB SIMMs, four 4 MB SIMMs, or four 16 MB SIMMs. (For increased noise immunity, only a four layer printed circuit board should be used for the expansion RAM SIMM.) The Bank A main logic board RAM cannot be changed in the field. See Figure 3-1 for currently available RAM configurations.

Each bank of RAM is decoded into one of two fixed contiguous 64 MB address spaces. Since these banks are at fixed physical locations (see Figure 2-1), the overall RAM address space will not be contiguous. Bank A occupies physical addresses $0000 0000 to $03FF FFFF and Bank B occupies physical addresses $0400 0000 to $07FF FFFF. Unless
16-Mbit DRAMs are used in a bank of memory, some part of the 64 MB address space will be unused. Such space will wrap, containing multiple images of the existing RAM in that bank's address space. For example, with 1 MB of RAM soldered on the main logic board (Bank A), addresses $0000 0000 to $000F FFFF contain the normal image, $0001 0000 to $0001 FFFF contain the second image, and so on, with a total of 63 copies of the normal 1 MB address range. This address wrapping allows the ROM to determine how much memory is present in each bank.

Figure 3-1 RAM configurations

NOTE:

256 KB SIMMs will be made from 256K x 4 fast page mode (
(1-MBit technology), 512KB SIMMs will be made from 4 each
DRAMs, and 2MB SIMMs will be made from 4 each 1M x 4 F



NOTE: 256KB SIMMs will be made from 256K x 4 fast page mode DRAM parts (1-MBit technology).

Use of RAM by the video

If the on-board video is used, the main logic board RAM (Bank A) is used as the frame buffer. The RBV's frame buffer is variable in size, depending on the currently selected bit depth and the size of the video monitor plugged into the on-board video port. The RBV requires only the amount of memory necessary to hold the contents of the screen; the RBV uses no additional memory for the frame buffer. Software (by either default or previous selection by the user) determines the maximum video bit depth to be made available at startup and sets aside that memory for video. If the user selects a bit depth smaller than this maximum, operating system software may make use of the additional space.

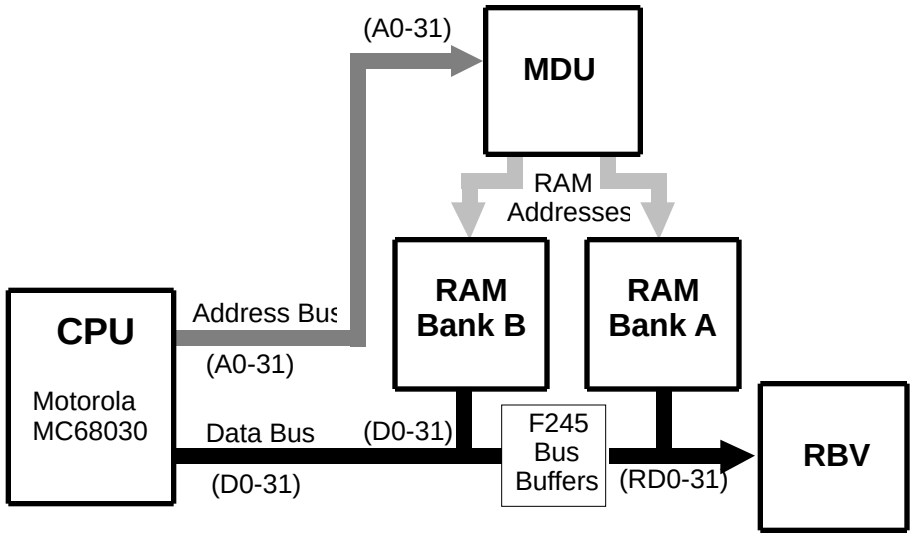
The RBV requests memory in bursts, and the MDU passes the data from memory, automatically incrementing a pointer to the current location in the frame buffer. The RBV tells the MDU to reset this pointer at the end of a screen, and the MDU sets the frame buffer pointer back to physical address $0000 0000. (All addresses used by the MDU must be physical because all logical memory mapping is performed by the 68030 microprocessor's on-board MMU.)

The operating system may map this region of memory elsewhere in order to make it look like any other video device. The video memory in the Macintosh IIsi computer is mapped to occupy NuBus super slot logical address space ($E) so it can be treated like a NuBus card. The operating system decides at startup how much of Bank A to devote to video and how much to map to the normal RAM address space.

Video accesses affect only Bank A memory access because the data bus between the RAM banks can be disconnected by a bus buffer, as shown in Figure 3-2. This fact allows the RBV to fetch data from Bank A without interrupting CPU access to Bank B or to I/O devices. The MDU accesses each bank of RAM independently, so it can decode addresses for the CPU and the RBV at the same time without interference.

For clarity, only the necessary components are illustrated in Figure 3-2.

Figure 3-2 RAM and video block diagram



DRAM requirements and refresh

The RAM interface requires 100 nanoseconds Row Address Strobe (RAS) access time DRAMs and 25 nanosecond Column Access Strobe (CAS) access time DRAMs with /CAS before /RAS refresh and fast page mode. Table 3-1 gives more detailed DRAM specifications. The expansion DRAMs must be mounted on 30-pin SIMMs with bypass capacitors. Table 3-2 shows the pinout for the SIMMs and the connections made to the processor bus. Figure 3-3 is a diagram of a RAM SIMM.

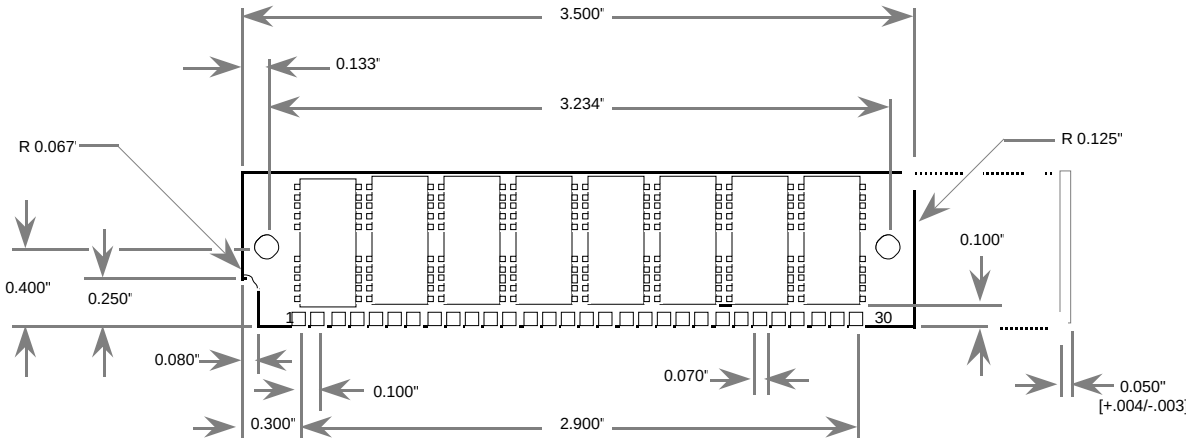
Table 3-1 DRAM access time requirements

RAS Access Time	100 ns
CAS Access Time	25 ns
Access Type	Fast Page Mode
Refresh Type	/CAS before /RAS
Refresh Period	15.6 µs

Table 3-2 8-bit DRAM SIMM pinout

Pin #	SIMM function	Processor bus function	Pin #	SIMM function	Processor bus function
1	+5V	+5V	16	DQ4	D4, D12, D20, *or* D28
2	/CAS	/CASLL, /CASLM, /CASUM, *or* /CASUU	17	RA8	$A19_{RAS}$, $A18_{CAS}$
3	DQ0	D0, D8, D16, *or* D24	18	RA9	$A21_{RAS}$, $A20_{CAS}$
4	RA0	$A6_{RAS}$, $A2_{CAS}$	19	RA10	$A23_{RAS}$, $A22_{CAS}$
5	RA1	$A7_{RAS}$, $A3_{CAS}$	20	DQ5	D5, D13, D21, *or* D29
6	DQ1	D1, D9, D17, *or* D25	21	/WE	RAMRW
7	RA2	$A8_{RAS}$, $A4_{CAS}$	22	+5V	+5V
8	RA3	$A9_{RAS}$, $A5_{CAS}$	23	DQ6	D6, D14, D22, *or* D30
9	GND	GND	24	RA11	$A24_{RAS}$, $A25_{CAS}$
10	DQ2	D2, D10, D18, *or* D26	25	DQ7	D7, D15, D23, *or* D31
11	RA4	$A11_{RAS}$, $A10_{CAS}$	26	NC	NC
12	RA5	$A13_{RAS}$, $A12_{CAS}$	27	/RAS	/RAS0 *or* /RAS1
13	DQ3	D3, D11, D19, *or* D27	28	NC	Pullup to +5V
14	RA6	$A15_{RAS}$, $A14_{CAS}$	29	NC	NC
15	RA7	$A17_{RAS}$, $A16_{CAS}$	30	+5V	+5V

Figure 3-3 RAM SIMM diagram



RAM refresh is performed by the MDU with /CAS before /RAS cycles. The refresh cycles are six CPU clocks long. Refresh is initiated at the same time in both banks of RAM every 15.6 microseconds; however, it continues independently in each bank so that if it must be held off until the completion of a CPU or video access in one bank, the other bank's refresh is not also held off. Refresh does not affect the processor at all if the processor is addressing anything except RAM.

ROM interface

The first production units of the Macintosh IIsi will use a 512 KB ROM SIMM module rather than having ROM soldered to the main logic board. Later units will also have a 512 KB ROM but it will be provided by a 4-Mbit device soldered to the main logic board. The device is 256K x 16 bits in a 44-pin quad flat pack. The board has the capacity for 1 MB of soldered RAM but only half of this capacity is used. Future ROM upgrades are accommodated with a single SIMM socket.

The Macintosh IIsi computer accesses ROM in five clock cycles. The MDU does not support burst reads in the ROM address space.

The ROM SIMM uses a 64-pin SIMM socket that is based on 0.05 inch spacings. This configuration provides a single SIMM only 0.2 inches wider than the 30-pin SIMM used for RAM. Since the ROM SIMM does not fit the RAM SIMM, inadvertent interchange is not a problem. Table 3-3 provides a pinout of the 64-pin ROM SIMM.

■ **Table 3-3** 64-pin ROM SIMM pinout

Pin number	Description	Pin number	Description
1	+5V	33	A10
2	A0	34	A11
3	A1	35	A12
4	A2	36	A13
5	A3	37	A14
6	A4	38	A15
7	A5	39	A16
8	A6	40	A17
9	A7	41	A18
10	GND	42	A19
11	GND (/CS0)	43	A20
12	/ROMOE	44	A21
13	+5V	45	A22
14	D0	46	A23
15	D1	47	D16
16	D2	48	D17
17	D3	49	D18
18	D4	50	D19
19	D5	51	D20
20	D6	52	D21
21	D7	53	D22
22	D8	54	D23
23	D9	55	D24
24	D10	56	D25
25	D11	57	D26
26	D12	58	D27
27	D13	59	D28
28	D14	60	D29
29	D15	61	D30
30	GND	62	D31
31	A8	63	+5V (/CS1)
32	A9	64	GND