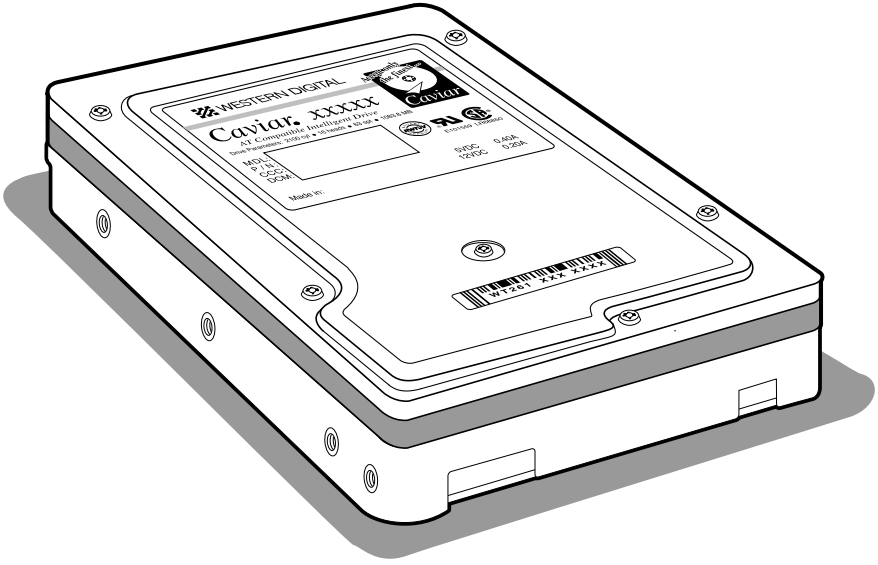
Caviar AC21600, AC32100 and AC32500 (CCC:F3) Technical Reference Manual



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1. DESCRIPTIONS AND FEATURES

1.1 General Description

The Caviar® AC21600, AC32100 and AC32500 Enhanced IDE (EIDE) hard drives are high-performance solutions designed to meet the requirements of today's most powerful systems from home and business PC's to workstations and servers. These drives are based on our successful proven design concepts. By combining enhanced electronics with new head and read-channel technology, we have produced the market-leading areal density and the highest performance Caviar drives to date.

High-speed host data transfers, advanced caching, increased rotational speeds, and low mechanical latency combine to give the AC21600, AC32100 and AC32500 the level of performance demanded by today's most advanced systems. These drives support host data transfers of 16.6 MB/s Mode 4 PIO and 16.6 MB/s Mode 2 multi-word DMA enabling VESA VL or PCI local bus EIDE integration. In addition, these drives feature Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.) which enables the drive to alert the host system of a negative reliability status condition.

The AC21600, AC32100 and AC32500 offer a rotational speed of 5200 RPM and include CacheFlow4. CacheFlow4 offers adaptive read and write caching capabilities which complements the advanced caching capabilities of today's major operating systems. An average read seek time of sub 12 ms and rotational latency of 5.8 ms combine to provide fast mechanical access.

The AC21600, AC32100 and AC32500 offer performance beyond that of the ISA bus. Optimum performance is obtained when these drives are integrated into a VESA VL or PCI local bus EIDE environment. System integration of these drives in a DOS or Windows environment requires either BIOS, device driver or operating system support for EIDE disk drives with capacities greater than 528 MB.

The AC21600, AC32100 and AC32500 drives support advanced power management capabilities that can reduce power requirements by over 85 percent. All Caviar drives are preformatted (low-level) and defects are mapped out before shipment. Additional Caviar features include logical block addressing, linear logical/physical universal address translation, automatic head parking, embedded servo control data on each track, and ECC on-the-fly correction.

Western Digital's award-winning Caviar drives are designed and manufactured to the highest standards of quality and reliability. This is demonstrated by their three year warranty, 300,000 hours Mean Time Between Failure, and guaranteed compatibility.

The Caviar AC21600, AC32100 and AC32500 drives are today's solution to the computer market's ever-increasing demand for higher performance and expanded connectivity capability and they still provide the advantages of low cost, compatibility and ease of use.

1.2 Advanced Product Features

- **CacheFlow4** – Western Digital's unique, fourth-generation caching algorithm evaluates the way data is read from and written to the drive and adapts on-the-fly to the optimum read and write caching methods. CacheFlow4 minimizes disk seeking operations and the overhead due to rotational latency delays.

  CacheFlow4 includes random and sequential write cache. Incorporating write cache with other CacheFlow4 features enables the user to cache both read data as well as write data. Multiple writes can now be held in the cache and then written collectively to the hard disk. Data is held in the cache no longer than the time required to write all cached commands to the disk.

  CacheFlow4 constantly evaluates not only the size of the read data request but the type of data request, that is, whether the data request is sequential, random, or repetitive. CacheFlow4 then dynamically partitions the Caviar's 128-Kbyte DRAM buffer into equal-sized segments and selects the appropriate caching mode for optimum system performance.
- **Advanced Host Transfer** – The AC21600, AC32100 and AC32500 support Mode 4 PIO (16.6 MB/s) and Mode 2 multi-word DMA (16.6 MB/s) as defined by the ATA-2 standards. To achieve Mode 4 PIO burst transfers, hard disk drives must be able to throttle the host via the IORDY signal. Systems typically require a high-speed VL or PCI local bus in order to support Mode 4 PIO.
- **High-Speed DMA Capability** – DMA Read and DMA Write commands are ATA-2-compatible and provide significant improvement in CPU bandwidth over conventional PIO data transfers. The system CPU is free to accomplish other tasks while the Caviar drive transfers data directly to/from system memory.
- **Power Conservation** – The AC21600, AC32100 and AC32500 support the ATA-2 power management command set. This command set allows the host to reduce the power consumption of the drive by issuing a variety of power management commands.
- **Block Mode** –ATA-2 compatible Read Multiple and Write Multiple commands are supported. Block mode increases overall data transfer rates by transferring more data between system interrupts.
- **Logical Block Addressing (LBA)** – The AC21600, AC32100 and AC32500 support both LBA and CHS-based addressing. LBA is included in advanced BIOS and operating system device drivers and ensures high-capacity disk integration.

- **Automatic Head Parking** – Head parking is automatic with Caviar drives. On power down, the heads retract to a safe, non-data landing zone and lock into position, improving data integrity and resistance to non-operational shock.
- **Advanced Defect Management** – These Caviar drives are preformatted (low-level) at the factory and come with a full complement of automatic defect management functions. Extensively tested during the manufacturing process, media defects found during intelligent burn in are mapped out with Western Digital's high performance defect management technique. No modifications are required before installation.
- **Embedded Servo Control** –The AC21600, AC32100 and AC32500 feature an embedded servo concept as the means of providing sampled position feedback information to the head position servo system. Servo bursts are located along a radial path from the disk center, ensuring that head positioning data occurs at constant intervals. This high sampling rate supports the high frequency servo bandwidth required for fast access times as well as highly accurate head positioning. The embedded servo concept provides the means of generating accurate feedback information without requiring a full data surface as would a dedicated servo control concept.
- **Dual Drive Operation** – These Caviar drives support dual drive operation by means of a daisy chain cable assembly and configuration options for master or slave drive designation. They also supports Cable Select (CSEL) for master or slave designation.
- **Universal Address Translation** – A linear disk address translator is provided by this series of Caviar drives to convert logical sector addresses to physical sector addresses which provides for easy installation and compatibility with numerous drive types.
- **Guaranteed Compatibility** – Western Digital performs extensive testing in its Functional Integrity Test Lab (FIT Lab) to ensure compatibility with all 100% AT-compatible computers and standard operating systems.
- **Reed Solomon ECC On-the-Fly** – The Caviar implements Reed Solomon error correction techniques to obtain extremely low read error rates. This error correction algorithm corrects errors on-the-fly without any performance penalties. It allows for hardware corrections of up to a 24-bit error span on-the-fly.
- **Automatic Defect Retirement** – If the Caviar drive detects a defective sector while reading or writing, it automatically relocates the sector without end-user intervention.

- **Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)** – S.M.A.R.T. enables a drive's internal status to be monitored through diagnostic commands at the host level or during off-line activities. S.M.A.R.T. devices employ data analysis algorithms that are used to predict the likelihood of some near-term degradation or fault conditions. When used with a S.M.A.R.T. application, the drive can alert the host system of a negative reliability status condition. The host system can then warn the user of the impending risk of data loss and advise the user of appropriate action.

2. SPECIFICATIONS

2.1 Performance Specifications

Average Seek - Read - Write	 Sub 12 ms typical, 15 ms maximum Sub 14 ms typical, 17 ms maximum
Track-to-Track Seek	3.0 ms typical, 6 ms maximum
Full Stroke Seek	22 ms typical, 27 ms maximum
Index Pulse Period	11.53 ms
Average Latency	5.76 ms
Rotational Speed	5200 RPM
Controller Overhead	0.3 ms average
Data Transfer Rate - Buffer to Host - Buffer to Disk	 12.5 MB/s 16.6 MB/s (Mode 4 PIO) 16.6 MB/s (Mode 2 multi-word DMA) 49 Mbits/s minimum 95 Mbits/s maximum
Interleave	1:1
Buffer Size	128-KB DRAM
Error Rate - Unrecoverable	<1 in 10^{13} bits read
Spindle Start Time - From Power-on to Drive Ready[1] - From Power-on to AT Speed[2]	 10.8s typical, 18s maximum 7s typical, 15s maximum
Spindle Stop Time	5s typical
Contact Start/Stop Cycles (CSS)	40,000 minimum

[1] *Defined as the time from power-on to the setting of Drive Ready and Seek Complete including calibration.*

[2] *Defined as the time from power-on to the setting of the AT speed bit by spindle firmware.*

2.2 Physical Specifications

Physical Specifications	Caviar AC21600	Caviar AC32100	Caviar AC32500
Recommended Setup Parameters[1]	3148 x 16 x 63 (Cyl x Hd x SPT)	4092 x 16 x 63 (Cyl x Hd x SPT)	4960 x 16 x 63 (Cyl x Hd x SPT)
Formatted Capacity[2]	1624.6 MB	2111.8 MB	2559.8 MB
Interface	40-pin EIDE	40-pin EIDE	40-pin EIDE
Actuator Type	Rotary Voice Coil	Rotary Voice Coil	Rotary Voice Coil
Number of Disks	2	3	3
Data Surfaces	4	5	6
Number of Heads	4	5	6
Bytes per Sector	512	512	512
User Sectors per Drive (max.)	3,173,184	4,124,736	4,999,680
Servo Type	Embedded	Embedded	Embedded
Recording Method	GCR 8, 9 PRML	GCR 8, 9 PRML	GCR 8, 9 PRML
ECC	Reed Solomon	Reed Solomon	Reed Solomon
Head Park[3]	Automatic	Automatic	Automatic
PRML - Partial Response Maximum Likelihood EIDE - Enhanced Integrated Drive Electronics			

[1] Do not exceed the maximum sector capacity when specifying the number of cylinders, heads and sectors per track. Exceeding the specified limits causes disk controller to return an ID NOT FOUND error to the host.

[2] Western Digital defines a megabyte (MB) as 1,000,000 bytes.

[3] Turning the system power off causes the Caviar to perform an automatic head park operation.

2.2.1 Physical Dimensions

Note: All measurements are maximum values in the following table.

	English		Metric	
	Dimension	**Tolerance**	**Dimension**	**Tolerance**
Height	1.00 inch	±0.02 inch	25.4 mm	±0.51 mm
Length	5.75 inches	±0.02 inch	146.05 mm	±0.51 mm
Width	4.00 inches	±0.02 inch	101.6 mm	±0.51 mm
Weight	1.1 pound	±0.11 pound	.500 kg	±0.050 kg

2.3 Mechanical Specifications

Figure 2-1 shows the mounting dimensions and locations of the screw holes for the Caviar drive.

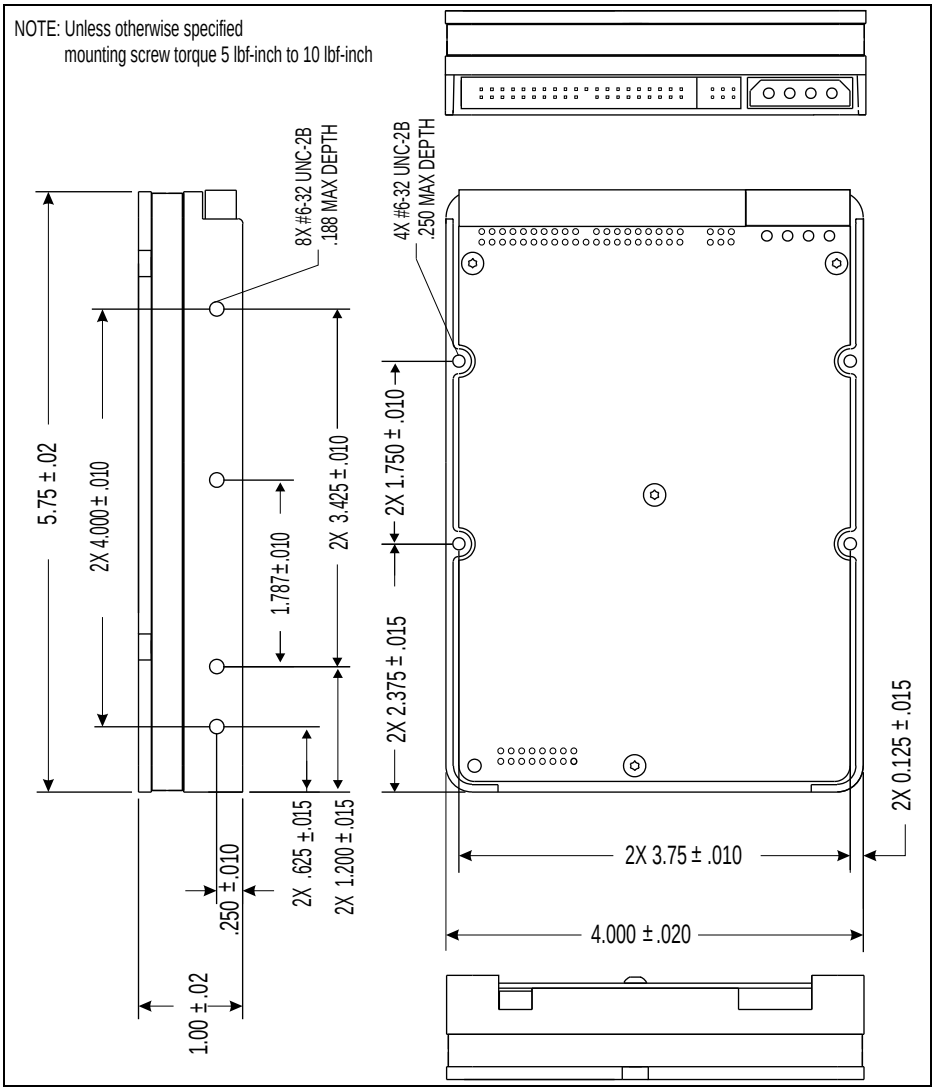

Figure 2-1. Mounting Dimensions

2.4 Electrical Specifications

2.4.1 Current Requirements and Power Dissipation

Operating Mode	RMS Current[1]		Power, Typical[1]
	12 VDC	5 VDC	
Spinup	955 mA 1.4 A Max	190 mA	12.4 W 18.7 W Max
Read/Write	258 mA	400 mA	5.1 W
Seek	475 mA	400 mA	7.7 W

POWER MANAGEMENT COMMANDS			
Operating Mode	**RMS Current[1]**		**Power, Typical[1]**
	12 VDC	**5 VDC**	
Idle (E1H)	258 mA	400 mA	5.1 W
Standby (E0H)	13 mA	87 mA	0.6 W
Sleep (E6H)	13 mA	87 mA	0.6 W

[1] *All values are typical. (25°C, 5.0V, and 12V input) except where specified as maximum.*

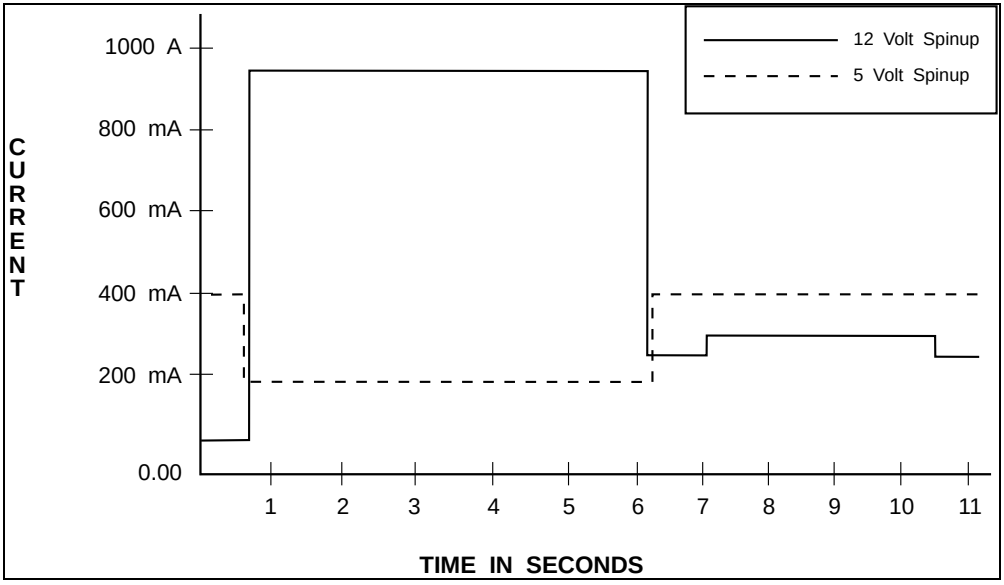

Figure 2-2. Typical +12V/+5V Current Draw During Spinup

2.4.2 Input Voltage Requirements

The input voltage requirements for the AC21600, AC32100 and AC32500 are: +5.0V ± 5% and +12.0V ±8%

2.4.3 Ripple

	+12 VDC	**+5 VDC**
Maximum Frequency	200 mV (double amplitude) 0-20 MHz	100 mV (double amplitude) 0-20 MHz

2.4.4 Power Connectors and Cables

Power Connector	4-pin AMP (P/N 84069-1 or equivalent)
Mating Connector	Body (AMP 1-480424-0 or equivalent) Pins (AMP 60619-4 or equivalent)
Power Cable Wire Gauge	18 AWG

2.4.5 DC Electrical Specifications

The DC electrical specification table is located in Section 4.8.

2.5 Environmental Specifications

2.5.1 Shock and Vibration

Shock	
Operating	10G (2 per second maximum)
Non-operating	150G (3 drops per axis maximum)
Note: Half-sine wave 3 ms duration, measured without shock isolation and without non-recoverable errors.	
Vibration	
Operating	5-20 Hz, 0.037 inches (double amplitude) 20-300 Hz, 0.75G (0 to peak)
Non-operating	5-20 Hz, 0.195 inches (double amplitude) 20-500 Hz, 4.0G (0 to peak)
Sweep Rate	One-octave/minute minimum
Drive Generated Vibration	
Operating	.10G maximum with the drive in an unconstrained condition

2.5.2 Temperature and Humidity

Temperature & Humidity	
Operating [1]	
Temperature	5°C to 55°C (41°F to 131°F)
Humidity	8-80% RH non-condensing 33°C (maximum wet bulb)
Thermal Gradient	10°C/hour (minimum)
Humidity Gradient	20%/hour (maximum)
Non-operating [2]	
Temperature	-40°C to 60°C (-40°F to 140°F)
Humidity	5-95% RH non-condensing 33°C (maximum wet bulb)
Thermal Gradient	20°C/hour (maximum)
Humidity Gradient	20%/hour (maximum)
[1] *The system environment must allow sufficient air flow.*	
[2] *To ensure test is non-condensing, set chamber RH to 85% maximum. To maintain 85% max, set dry bulb to 35.5°C which maintains 33°C wet bulb*	

2.5.3 Atmospheric Pressure

Altitude	
Operating	-1,000 feet to 10,000 feet (-300M to 3,000M)
Non-operating	-1,000 feet to 40,000 feet (-300M to 12,000M)

2.5.4 Acoustics

TYPICAL SOUND POWER LEVEL[1]		
	TYPICAL	**MAXIMUM**
Idle Mode[2]	37 dBA	41 dBA
Seek Mode[3]	47 dBA	51 dBA

[1] Measured per ECMA-74/ISO 7779.

[2] No audible pure tones.

[3] Random seek at a rate of 23 seeks per second.

2.6 Reliability Specifications

MTBF	300,000 Power On Hours
MTTR	10 minutes (typical)
Component Design Life	5 years
Warranty Period	3 years

2.7 Agency Approvals

The Caviar meets the standards of the following regulatory agencies:

- **Federal Communication Commission:** Verified to comply with FCC Rules for Radiated and Conducted Emission, Part 15, Subpart B, for Class B Equipment
- **Underwriters Laboratories**: UL-Standard 1950, Standard for Safety of Information Technology Equipment including Electrical Business Equipment (File E101559)
- **Canadian Standards Association:** CSA-Standard C22.2, No. 950-M89, Standard for Safety of Information Technology Equipment including Electrical Business Equipment (File LR68850)
- **TUV Essen Laboratories:** IEC-950 (EN60950) Standard for Safety of Information Technology Equipment including Electrical Business Equipment.
- **CE Compliance for Europe:** Verified to comply with EN550022 for RF Emissions and EN50082-1 for Generic Immunity as applicable.

3. ADVANCED PRODUCT FEATURES

Western Digital's Caviar series of EIDE drives provides a choice of data storage capacities for AT compatible systems and include a full complement of advanced product features. This section describes the following Caviar advanced product features:

- CacheFlow4
- Push Down Defect Management and Format Characteristics
- Automatic Defect Retirement
- Error Recovery Process
- Reed Solomon ECC On-the-Fly
- Universal Address Translation
- Logical Block Addressing (LBA)
- Dual Drive Option
- Power Conservation
- High-Speed DMA Capability
- Advanced Host Transfers
- Zoned Recording
- Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
- Block Mode

3.1 CacheFlow4

CacheFlow4 is Western Digital's unique, fourth-generation disk caching system. It incorporates read cache with random and sequential write cache.

3.1.1 Purpose of CacheFlow4

CacheFlow4 was designed by Western Digital to minimize disk seeking operations and the overhead due to rotational latency delays. CacheFlow4 constantly evaluates not only the size of the data request but the type of data request, that is, whether the request is sequential, random or repetitive. CacheFlow4 then dynamically partitions the Caviar's DRAM buffer into the appropriate caching mode for optimum system performance.

3.1.2 Benefits of CacheFlow4

In a typical application, most host requests are for sequential data. CacheFlow4's adaptive design enables the Caviar to eliminate unnecessary disk seeking operations by immediately implementing the sequential mode once the data has been analyzed.

3.1.3 CacheFlow4 Operation

Sequential mode is the default mode of operation for CacheFlow4. The Caviar initially partitions the DRAM buffer into individual caching segments. As seeking operations begin, CacheFlow4 monitors the data's logical sector address and sector count parameters. CacheFlow4 then uses a simple hit score algorithm to either increase or decrease the segment size for optimal performance.

3.1.4 Write Cache

CacheFlow4 was designed to improve both single and multi-sector write performance by reducing delays caused by seek time and rotational latency.

Host retries must be enabled for write cache to be active.

If the write cache is full when a new write command is received, the data currently in the write cache is written to disk before the drive tells the host that the current command is complete.

Data is held in the drive's write cache no longer than the amount of time required to overcome seek time and rotational latency for the commands currently in the cache.

If a defective sector is found during a write cache operation, that sector is automatically relocated before the write occurs.

3.1.5 Read Cache

Sequential Mode

The sequential caching mode is the standard read-ahead cache. After reading all of the host-requested data into the segment, CacheFlow4 continues to read ahead until the cache is full. After the host reads the requested data from the cache, a new cache beginning is established following the last sector buffer returned to the host. Based on the hit score algorithm, sequential mode adapts the size of segment to optimize cache performance.

The default mode of two cache segments provides optimum cache performance. A larger number of segments may limit cache effectiveness because each segment may not store enough sequential sectors. A smaller number of segments may limit effectiveness for random reads.

Repetitive Mode

The repetitive caching mode resembles a static buffer. If the same blocks are accessed twice, the repetitive mode is selected. Repetitive mode also reads ahead and can override the number of segments to build one large segment. Unlike sequential mode, however, the sector buffer containing the host-requested data remains valid after the host reads the data.

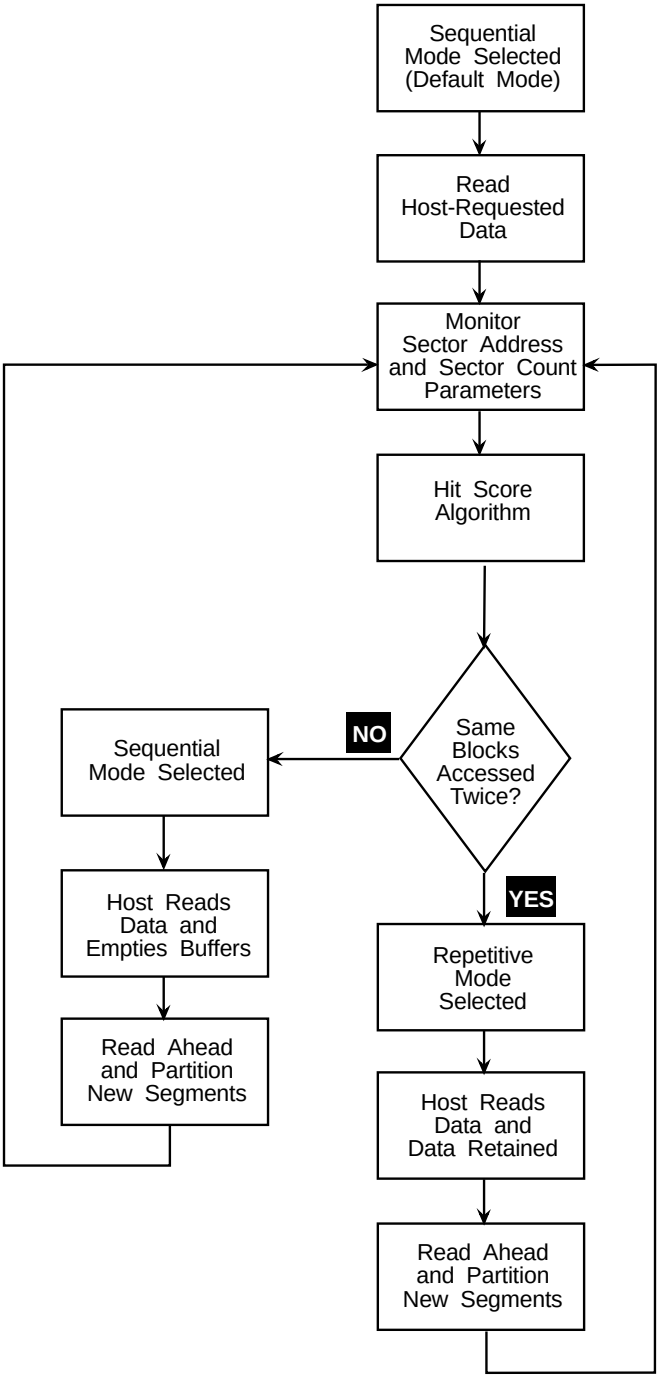

Figure 3-1. Read Cache Flow Chart

3.2 Push Down Defect Management and Format Characteristics

3.2.1 Defect Management

Every Caviar undergoes factory-level intelligent burn in, which thoroughly tests for and maps out defective sectors on the media before the drive leaves the manufacturing facility. Following the factory tests, a primary defect list is created. The list contains the cylinder, head, and sector numbers for all defects.

Defects managed at the factory are sector slipped. Grown defects that can occur in the field are mapped out by relocation to spare sectors on the inner cylinders of the drive.

3.2.2 Format Characteristics

The Caviar is shipped from the factory preformatted (low-level) with all the known defects mapped out.

In order to be compatible with existing industry standard defect management utility programs, the Caviar supports the logical format command. When the host issues the Format Track command, the Caviar performs a logical version of this command in response to the host's interleave table request for good and bad sector marking or assign/unassign the sector to/from an alternate sector.

If the host issues the Format Track Command during normal operating modes, the data fields of the specified track are filled with a data pattern of all zeros. The Format Track Command can be used to mark/unmark bad sectors, and reassign unrelocated sectors.

3.3 Automatic Defect Retirement

The automatic defect retirement feature automatically maps out defective sectors while reading or writing. If a defective sector appears, Caviar finds a spare sector.

The following items are specific to automatic defect retirement on writes (write auto-relocation):

- It is only performed when host retries are enabled. The data is always written to disk (using automatic defect retirement if required) and no error is reported.
- When host retries are disabled, Write Cache and write relocation are disabled.

The following items are specific to automatic defect retirement on reads (read auto-relocation):

- When host retries are enabled, the drive will automatically correct any recoverable errors and attempt to re-write them (no error is reported). If the re-write is unsuccessful the drive will relocate the sector and report an ECC correctable error.

- When host retries are disabled, the drive will automatically correct and attempt to re-write the data, however, no relocation will occur.

3.4 Error Recovery Process

The Caviar has four means of error recovery:

- ECC On-the-Fly
- Read/Write Retry Procedure
- Extended Read Retry Procedure
- Extended (Firmware Assisted) ECC Correction and Relocation

ECC On-the-Fly – If an ECC error occurs, the Caviar attempts to correct it on-the-fly without retries. Data can be corrected in this manner without performance penalty. The details of the correction algorithm are covered in the next section.

Read/Write Retry Procedure – This retry procedure is used by all disk controller error types. If this procedure succeeds in reading or writing the sector being tried, then recovery is complete and the controller continues with the command. Each retry operation also checks for servo errors. This procedure ends when error recovery is achieved or when all possible retries have been attempted.

Extended Read Retry Procedure – This retry procedure tries combinations of positive/negative track offsets, and data DAC manipulations to recover the data. This retry procedure is applicable only to read data recovery. The Read/Write Retry procedure is used to perform the actual retry operation.

When an extended retry operation has been successful, the controller continues with the command. The controller ensures that any changes in track offset or data DAC settings that exist are cleared before the command continues.

Extended (Firmware Assisted) ECC Correction and Relocation – If an ECC error is too large to correct using ECC on-the-fly, the Caviar can attempt to correct the error using Extended Error Correction. This allows correction of large ECC errors that ECC on-the-fly cannot correct. If the Extended Error Correction is successful, the sector is re-written or relocated. The Extended Error Correction process takes more time than ECC on-the-fly to return the corrected data. See section 3.5 for specific ECC algorithm details.

All or part of the above error recovery procedures are applied to the following errors:

- ID Not Found (IDNF)
- Data Address Mark Not Found (DAMNF)
- Error Correction Code (ECC)

The retry procedures for each type of error are described on the next page.

ID Not Found (IDNF) and Data Address Mark Not Found (DAMNF)

With host retries enabled, the Caviar attempts the following recovery procedures when IDNF or DAMNF errors occur. Error recovery ends upon successful completion of any error recovery procedure.

1. Attempt basic Read/Write Retry procedure.
2. For Reads, attempt Extended Read Retry procedure.
3. If all attempts are unsuccessful, report IDNF or DAMNF to the host.

With host retries disabled, the Caviar immediately returns an IDNF or DAMNF error to the host without performing any retry operations.

Error Correction Code (ECC)

If an ECC error occurs, the Caviar attempts to correct the data on-the-fly before any retries are attempted. This happens regardless of whether host retries are enabled or disabled. If ECC on-the-fly is successful, the corrected data is returned to the host with no performance penalties.

ECC error handling is summarized as follows:

ECC ERROR HANDLING	
1- to 17-Bit Error Span (24-bit max)	- No error reporting - Data corrected on-the-fly with no performance penalty - Sends host corrected data
18- to 65-Bit Error Span (72-bit max)	- Corrects data and attempts to re-write data - If re-write is unsuccessful, sector is relocated - If sector is relocated, CORR bit is set in the Status Register - Sends host corrected data
Greater than 65-Bit Error Span	- Reports ECC uncorrectable data - No error correction performed

3.5 Reed Solomon ECC On-The-Fly

The Caviar implements Reed Solomon error correction techniques in hardware to reduce the uncorrectable read error rate. This allows a high degree of data integrity with no impact on the drive's performance. Because on-the-fly corrected errors do not require the drive's firmware to assist with error correction, they are invisible to the host system.

To obtain the ECC check byte values, each byte within the sector is interleaved into one of three groups, where the first byte is in interleave 1, the second byte is in interleave 2, the third byte is in interleave 3, the fourth byte is in interleave 1, and so on. See Figures 3-2 and 3-3 for examples of interleaving.

Interleaving and the ECC formulas enable the drive to detect where the error occurs. A maximum of one byte can be corrected in each interleave without firmware assistance.

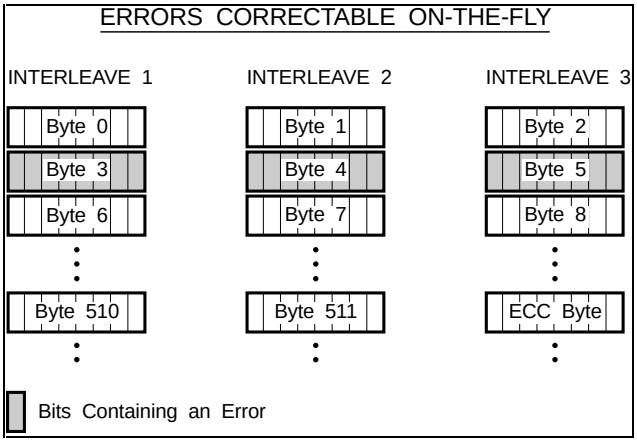

Figure 3-2. 24-Bit Correctable Error Span

An error span of 24-bits is the maximum that can be corrected on-the-fly because this is the largest error span that can be confined to one byte in each interleave.

An 18-bit error span that occupies two bytes in the same interleave cannot be corrected on-the-fly. No two bytes in an interleave can contain errors at the same time and still be corrected on-the-fly.

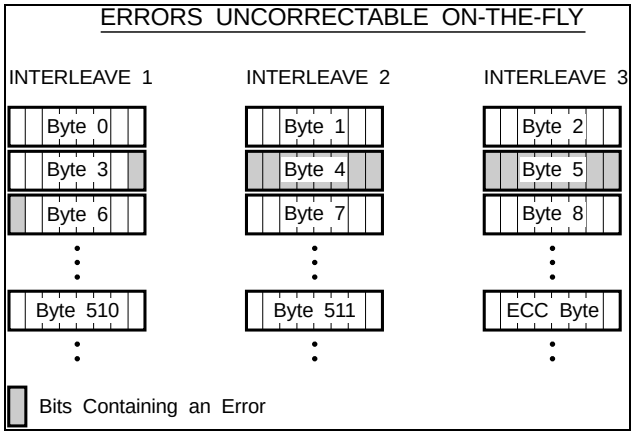

Figure 3-3. 18-Bit Uncorrectable Error Span

Note: A 17-bit error span is the maximum that is **always** correctable on-the-fly because the entire error span never occupies more than one byte in each interleave.

Firmware Assisted ECC

With firmware assisted ECC, a maximum of 3 bytes can be corrected in each interleave. In this case, a 65-bit error span is the maximum that is always correctable with firmware assistance because the entire error span will never occupy more than three bytes in each interleave.

3.6 Universal Address Translation

The Caviar implements linear address translation. The translation mode and translated drive configuration are selected by using the Set Drive Parameters command to issue head and sector/track counts to the translator. Caviar supports universal translation. Therefore, any valid combination of cylinder, head, and SPT can be assigned to the drive as long as the total number of sectors is not greater than the physical limits. The product of the cylinder, head and sectors/track counts must be equal to or less than the maximum number of sectors available to the user. The maximum number of sectors per drive are.

AC21600	–	3,173,184
AC32100	–	4,124,736
AC32500	–	4,999,680

Each sector consists of 512 bytes.

The minimum value for any translation parameter is one. The maximum value for any translation parameter is as follows:

Sectors/Track	–	255
Heads	–	16
Cylinders/Drive	–	65,535

The values in the Sector Count Register and the SDH Register determine the Sectors Per Track (SPT) and heads. Regardless of the values of the SPT and the heads, Caviar is always in the translation mode. Refer to Section 2.2 for the recommended setup parameters.

3.7 Logical Block Addressing

The Caviar drive supports Logical Block Addressing (LBA) mode. LBA allows sectors on the drive to be addressed by using cylinder, head, and sector numbers, or by using a single 28-bit logical block address. LBA mode is enabled by setting bit 6 in the SDH task file register. When entering a logical block address, the task file registers are as follows:

Task File Register	LBA Bits
Sector Number	7-0
Cylinder Low	15-8
Cylinder High	23-16
SDH (Bits 3-0)	27-24

When the LBA bit is set, logical block addressing is recognized by the following commands:

– Read Sector
– Write Sector
– Read Verify
– Read DMA
– Write DMA
– Recalibrate
– Seek
– Format Track
– Read Multiple
– Write Multiple

For all other commands, the drive ignores the LBA bit.

Sectors on the drive have a 1:1 corresponding logical block address, with LBA 0 as the first data sector on the drive. The task file following a command sent with the LBA bit set contains LBA parameters.

The AC21600, AC32100 and AC32500 support both LBA and CHS-based addressing. Support for LBA addressing is included in advanced operating system device drivers and ensures high-capacity disk integration.

3.8 Dual Drive Option

The Caviar supports ATA-2 dual drive operations by means of configuration options for master or slave drive designation. The Caviar is 100% ATA-2 compatible regarding the timing of the PDIAG- and DASP--P signals. A jumper must be placed in the drive's option area for both master and slave configurations. If a jumper is placed on the cable select (CSEL) option, the drive address selection will be determined by the CSEL signal on the drive cable. Connection to the host is implemented by means of a daisy-chain cable assembly. These configurations are described in Section 5.

The SDH Register contains the master/slave select bit for the Caviar. The DASP- signal is a time-multiplexed indicator of Drive Active or Slave Present on the Caviar's I/O interface. At reset, this signal is an output from the slave drive and an input to the master drive, showing that a slave drive is present. For all times other than reset, DASP- is asserted at the beginning of command processing and released upon completion of the command. If the master drive option has been configured, the Caviar will not respond to commands or drive status on the interface when the slave bit is selected in the SDH Register.

3.9 Power Conservation

The AC21600, AC32100 and AC32500 support the ATA-2 power management commands that lower the average power consumption of the disk drives. For example, to take advantage of the lower power consumption modes of the drive, an energy efficient host system could implement a power management scheme that issues a Standby Immediate command when a host resident disk inactivity timer has expired. The Standby Immediate command would cause the drive to spin down and enter a low-power mode. Subsequent disk access commands would cause the drive to spin up and execute the new command.

To avoid excessive wear on the drive due to the starting and stopping of the HDA, the host's disk inactivity timer should be set to no shorter than ten minutes.

3.10 Block Mode

In a standard operation, the host system gets interrupted each time a sector of data is transferred. In block mode, multiple sectors of data can be transferred with each interrupt. Data transfer overhead is reduced thereby increasing throughput and overall performance. Performance gains are most noticeable when the host requests data that is in the drive's cache buffer.

3.11 High-Speed DMA Capability

By engaging an ATA-2 compatible, Mode 2 multi-word DMA, the host CPU bandwidth is increased because the peripheral data transfer burden is off-loaded to the system's DMA channel. With the exception of DMA data transfers, which are limited to Read DMA and Write DMA commands, all other commands must be performed using PIO. DMA or PIO data transfer mode selection by the host is performed on a command-by-command basis.

3.12 Advanced Host Transfers

The AC21600, AC32100 and AC32500 support high-speed Mode 3 and 4 PIO. These are data transfer modes that utilize hardware handshaking between the host and the drive via the IORDY signal. When the drive deasserts the IORDY signal, the host extends the read/write cycle until IORDY is asserted, thereby eliminating data corruption from overrun and underrun conditions. When in Mode 3 PIO, data can be transferred in bursts to and from the host at a rate of up to 11.1 MB per second; in Mode 4 PIO, the data can be transferred at a rate of up to 16.6 MB per second.

Mode 3 and Mode 4 PIO are enabled on the drive by issuing a Set Features command. If Mode 3 or Mode 4 PIO is enabled, it can only be disabled by issuing another Set Features command, a hard reset, or by cycling power.

To support Mode 4 PIO, Flow Control must be enabled in the host system. If this mode is enabled on a system that does not support Flow Control, host FIFO errors can occur.

Mode 3 and Mode 4 PIO timings were defined to facilitate EIDE drive integration into VL and PCI local bus systems.

3.13 Zoned Recording

Zoned Recording is a mechanism for increasing the capacity of the drive by increasing the Bit-Per-Inch (BPI) density of data written on the longer outer tracks of the drive. Track capacity (number of sectors) is constant within groups of tracks or zones, and is increased when the tracks are sufficiently long to accommodate a significant number of additional sectors. This incremental increase in track capacity moving outward on the disk surface creates a series of concentric zones with different data densities.

3.14 Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)

S.M.A.R.T. enables a drive's internal status to be monitored through diagnostic commands at the host level.

The Caviar AC21600, AC32100 and AC32500 drives monitor read error rate, start/stop count, spin-up retry count, multi-zone error rate, and drive calibration retry count. All of these attributes are updated and stored on the hard drive in the reserved area of the disk. The hard drive also stores a set of attribute thresholds that correspond to the calculated attribute values. Each attribute threshold indicates the point at which its corresponding attribute value achieves a negative reliability status.

3.14.1 Supported Attributes

The Caviar AC21600, AC32100 and AC32500 drives support the following attributes.

Attribute	Attribute ID Number	Pre-Failure/Advisory Bit (Status Flags bit 0)
Read Error Rate	1	Set
Start/Stop Count	4	Clear
Spin-up Retry Count	10	Set
Drive Calibration Retry Count	11	Set
Multi-zone Error Rate	200	Set

Attributes that have the Pre-Failure/Advisory Bit Set are used for predicting future degrading or faulty conditions. Attributes that have the Failure/Advisory Bit Clear are used for informational purposes only and are not indicators of impending drive failure.

The S.M.A.R.T. data saving process is a background task. After a pre-determined idle period, the self-monitoring data is automatically saved to the disk.

3.14.2 Off-line Data Collection

The Caviar AC21600, AC32100 and AC32500 drives support off-line data collection. The Multi-zone Error Rate is an attribute computed from data gathered during off-line activities. Off-line data collection is initiated by either the Execute S.M.A.R.T. Off-line Immediate command or the enable S.M.A.R.T. Automatic Off-line command.

There are two internal firmware timers that control automatic off-line data collection. The first internal firmware timer is referred to as the Spin Timer. The Spin Timer accumulates the number of hours the drive is “spinning”. Once this timer reaches 8 hours, an off-line data collection is said to be “pending”. The second internal firmware timer is referred to as the Idle Timer. The Idle Timer accumulates the number of minutes since the drive has received a command from the host. Once the Idle Timer reaches 10 minutes, a “pending” off-line data collection process begins. However, in the case where a Standby Timer is set by the host (via the Standby with Timer, or Idle with Timer command) to be less than 10 minutes, the expiration of the Standby Timer, rather than the Idle Timer, will begin a “pending” off-line data collection process. Note that when this occurs, the drive will spin down only after the off-line data collection process completes.

Several information bytes are returned in the Read S.M.A.R.T. attribute values command that facilitate the use of the off-line data collection feature. Refer to the SFF-8035i and SFF-8055i for more detailed information.

4. HOST INTERFACE AND AT COMMAND SET

This section describes:

- J2 Pin Assignments
- Host Interface Registers
- Host Interface Commands
- Host I/O Read Timing
- Host I/O Write Timing
- Host Multi-Word DMA Read Timing
- Host Multi-Word DMA Write Timing
- DC Electrical Specifications

4.1 J2 Pin Assignments

The Caviar interfaces with the host I/O bus via the 40-pin connector (J2) illustrated in Figure 4-1. Table 4-1 identifies the pin numbers of the J2 connector and the corresponding signal names and signal functions.

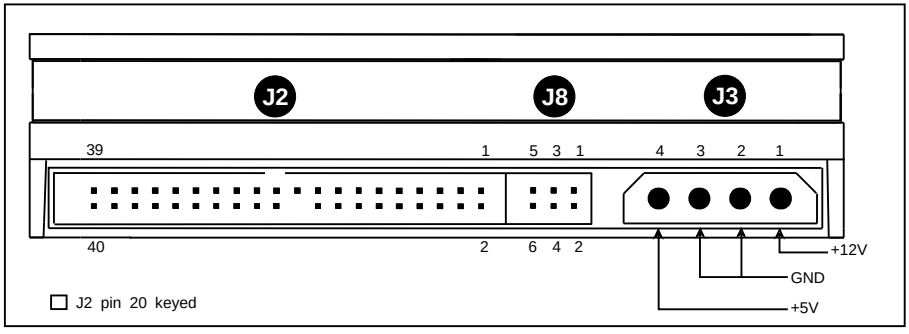

Figure 4-1. Standard Factory Connectors

PIN	MNEMONIC	I/O	DESCRIPTION
1	HRST-	I	**Host Reset** Initializes the Caviar drive when asserted.
3, 5, 7, 11 13, 15. 17 4, 6, 8, 10, 12, 14, 16, 18	HD7-0 HD8-15	I/O	**Host Data Bus Bits 7-0 and 8-15** The lower data bus is an 8-bit, tristate directional bus for transferring status, data, and control information between the host and the drive. The upper data bus is used for 16-bit data transfers only.
2, 19, 22, 24, 26, 30, 40	GND		Ground
20			Key-Not connected.
21	DMARQ	O	**DMA Request** Drive DMA signal Request to host (DMA only).
23	IOW-	I	**I/O Write** The host controller asserts IOW- when a data or control byte is written to the Caviar.
25	IOR-	I	**I/O Read** The host controller asserts IOR- when a data or status byte is read from the Caviar.
27	IORDY	O	**I/O Channel Ready** Drive ready signal to host. Used with host systems that support Flow Control Protocol to maximize burst transfer rates.
28	CSEL	I	**Cable Select** Configures the drive status as either a master or slave drive.
29	DMACK-	I	**DMA Acknowledge** Host DMACK signal to drive (DMA Mode only).
31	HINTRQ	O	**Host Interrupt Request** The Caviar asserts INTRQ to request interrupt service from the host.
32	I/OCS16-	O	**I/O Channel Select 16** Identifies data transfers to or from the host as 16 bits wide.
34	PDIAG-	I/O	**Passed Diagnostics** Output from slave drive when it has passed its diagnostics. Input to master drive.

PIN	MNEMONIC	I/O	DESCRIPTION
35, 33, 36	HA0-2	I	**Host Address Bus** A0, A1, and A2 address I/O ports 0 through 7.
37	HCS0-	I	**Host Chip Select 0** The host asserts HCS0- to address and communicate with the Caviar on the I/O channel.
38	HCS1-	I	**Host Chip Select 1** The host asserts HCS1 to address and communicate with the Caviar auxiliary registers.
39	DASP-	I/O	**Drive Active/Slave Present** This open collector output is a time-multiplexed signal indicating drive active or slave present. At reset, this signal is an output from the slave drive and an input to the master drive, showing that a slave drive is present. For all times other than reset, DASP- is asserted by the master and slave drives during command execution.

Table 4-1. J2 Pin Descriptions

4.2 Host Interface Registers

4.2.1 Register Address Map

The Task File occupies the address space shown in Table 4-2. The Task File's ten registers pass command, status, and data information between the host and the Caviar drive. All registers are 8 bits wide, except for the Data Register, which is 16 bits wide. These registers are accessed via control lines HA0-2 and HCS0- active. The Alternate Status Register is always accessible with HCS1- active.

ADDRESSES					REGISTERS	
HCS0-	**HCS1-**	**HA2**	**HA1**	**HA0**	**READ FUNCTION**	**WRITE FUNCTION**
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Features
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	SDH	SDH
0	1	1	1	1	Status	Command
1	0	1	1	0	Alternate Status	Fixed Disk Control
1	0	1	1	1	Digital Input	Not Used

Table 4-2. Task File Map

4.2.2 Data Register

The Data Register holds all the data to be transferred to or from the host on read and write commands. All data transfers are high speed and 16-bits wide, except for the ECC bytes transferred during read long or write long commands., which are 8 bits wide.

4.2.3 Error Register

The Error Register contains an error code that indicates a particular type of failure. The register contains a valid error code only if the Status Register error bit 0 is set. The only exceptions are power-up, reset, and the issuance of a diagnostic command. In these cases the Error Register contents are valid regardless of the condition of the Status Register's error bit. These two exceptions cause the following error values:

01 = No Error
02 = Not Applicable
03 = Buffer RAM Error
04 = WD61C29 Register Error
05 = Microcontroller Internal RAM Error or ROM Checksum Error
8X = Slave Drive Failed

If a slave drive is present and has failed its diagnostic, 80h is OR'ed with the master drive's status bits. To read the slave's error code, the host should select the D bit in the SDH Register. In all other cases the Error Register bits are defined as follows when asserted.

BIT POSITIONS							
7	6	5	4	3	2	1	0
BBD	ECC	0	IDNF	0	AC	TK0	DAMNF

BBD	Bad Block Detected
ECC	Error Correction Code (uncorrectable error detected)
IDNF	ID Not Found (Target sector could not be found)
AC	Aborted Command
TK0	Track 0 (Unable to find a valid track 0)
DAMNF	Data Address Mark Not Found

Error Register Bit 7 (BBD): If bit 7 is asserted, it indicates that the Caviar drive detected a Bad Block Mark in the sector ID field while attempting a read or write.

Error Register Bit 6 (ECC): If bit 6 is asserted, it indicates that the Caviar drive detected an uncorrectable data error while reading a target sector.

Error Register Bit 5: Not used.

Error Register Bit 4 (IDNF): If bit 4 is asserted, it indicates that the Caviar drive was unable to locate a valid ID field for the specified logical address.

Error Register Bit 3: Not used.

Error Register Bit 2 (AC): If bit 2 is asserted, it indicates that the Caviar drive has terminated the current command. This is due to the following:

– Illegal write current condition (write fault)
– No seek complete
– Drive not ready condition
– Invalid command code

Error Register Bit 1 (TKO): If bit 1 is asserted, it indicates that the Caviar drive was unable to locate a valid track 0 indication. This bit is only valid after a Recalibrate command.

Error Register Bit 0 (DAMNF): If bit 0 is asserted, it indicates that the Caviar drive was unable to locate a valid Data Address Mark (DAM) within a given number of byte times after the ID field.

4.2.4 Features Register

The contents of this register are used by the following commands:

– Set Features
– Execute S.M.A.R.T.

4.2.5 Sector Count Register

The Sector Count Register indicates the number of sectors to be transferred during a read, write, or verify operation. (A value of zero indicates a count of 256 sectors). During a format operation, this register contains the number of sectors per track (SPT) and must correspond with the values indicated by the Set Drive Parameters command. When read by the host, this register indicates the number of sectors, if any, that were not read or written during the previous command. The Sector Count Register contents are used by the following commands:

– Read Sector
– Write Sector
– Format Track
– Read Verify
– Set Drive Parameters
– Read Multiple
– Write Multiple
– Read DMA
– Write DMA
– Standby with Timer
– Idle with Timer
– Set Multiple
– Set Features

4.2.6 Sector Number Register

The Sector Number Register defines the target sector for the current operation when written to by the host. The contents of this register are used by the following commands:

– Read Sector
– Write Sector
– Read Verify
– Read Multiple
– Write Multiple
– Read DMA
– Write DMA
– Translate ID

When the LBA bit in the SDH register is set to 1, Logical Block Addressing is recognized by specific commands. See Section 3.7 for a detailed description of LBA mode.

4.2.7 Cylinder Low and Cylinder High Registers

The Cylinder Low and Cylinder High Registers contain the logical cylinder address for commands that require an address. The Cylinder Low Register contains the eight low-order bits of the starting cylinder number. The Cylinder High Register contains the three high-order bits of the starting cylinder number.

BIT POSITIONS							
7	6	5	4	3	2	1	0
LSB	LSB	LSB	LSB	LSB	LSB	LSB	LSB
0	0	0	0	0	MSB	MSB	MSB

The contents of the Cylinder Low and Cylinder High Registers are used by the following commands:

– Seek
– Read Sector
– Write Sector
– Format Track
– Read Verify
– Read Multiple
– Write Multiple
– Read DMA
– Write DMA
– Translate ID
– Execute S.M.A.R.T.

When the LBA bit in the SDH register is set to 1, Logical Block Addressing is recognized by specific commands. See Section 3.7 for a detailed description of LBA mode.

4.2.8 SDH Register

The SDH Register selects the drive and head number for a particular operation. The bit assignments are as follows:

BIT POSITIONS							
7	6	5	4	3	2	1	0
1	LBA	1	D	HS3	HS2	HS1	HS0
LBA	Logical Block Addressing Bit (1=LBA mode, 0=CHS mode)						
D	Drive Select Bit						
HS3-HS0	Logical Head Select Bits						

When the LBA bit is set to 1, the register usage for some commands will be different. See Section 3.7 for a complete listing of the commands supported by LBA. When the D bit is set to 1, the slave drive is selected. When the D bit is reset to 0, the master drive is selected. HS3-HS0 specify the desired logical head number. The contents of this register are used by the following commands:

– Recalibrate
– Seek
– Read Sector
– Write Sector
– Format Track
– Read Verify
– Set Drive Parameters
– Identify Drive
– Standby Immediate
– Idle Immediate
– Check Power Mode
– Translate ID
– Read Multiple
– Write Multiple
– Set Multiple
– Read Buffer
– Write Buffer
– Set Features
– Read DMA
– Write DMA
– Standby with Timer
– Idle with Timer
– Sleep
– Execute S.M.A.R.T.

4.2.9 Status Register

The Status Register contains the drive's status following a command. Reading the Status Register resets any pending interrupt. These are the bit assignments:

BIT POSITIONS							
7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	CORR	IDX	ERR

BSY	Busy, indicates state of controller
RDY	Ready, indicates state of target drive
WF	Write Fault, indicates hazardous condition and aborts the requested command
SC	Seek Complete
DRQ	Data Request
CORR	Data Was Corrected
IDX	Index, index pulse of target drive
ERR	Unrecoverable error

Status Bit 7 (BSY): This bit reflects the state of the controller. It is activated with a command request, and it is deactivated at command completion. An attempt by the host to read any task file register other than the Status Register while BSY = 1 results in the host receiving the contents of the Status Register.

Status Bit 6 (RDY): This bit reflects the state of the target drive. Any command requested while RDY = 0 is not honored. If a command request is executed and, if RDY becomes inactive, the command is aborted.

Status Bit 5 (WF): This bit indicates the occurrence of a write fault at the target drive. The presence of a write fault condition causes the current command request to abort. Subsequent command requests are not honored until the condition clears.

Status Bit 4 (SC): When set, this bit indicates the last requested seek has been completed.

Status Bit 3 (DRQ): This bit is high when data is to be transmitted between the host and target controller.

Status Bit 2 (CORR): When this bit is set, it indicates that one or more of the sectors sent to the host had a correctable error in the data field that was corrected and relocated via the ECC algorithm.

Status Bit 1 (IDX): This bit reflects the target drive's index pulse.

Status Bit 0 (ERR): When this bit is set, it indicates that an unrecoverable error has occurred. The host may ascertain the type of error by reading the Error Register.

4.2.10 Command Register

The host requests a controller/drive function by writing a function code in the Command Register. The write action sets the BSY bit in the Status Register.

4.2.11 Alternate Status Register

The Alternate Status Register provides the same information, without resetting a pending interrupt, as the Status Register at a different address.

4.2.12 Fixed Disk Control Register

The Fixed Disk Control Register allows for a programmable controller reset and provides the ability to enable or disable control of the fixed disk priority interrupt.

BIT POSITIONS							
7	6	5	4	3	2	1	0
0	0	0	0	0	RST	IDS	0

Bit 2 (RST): The software-controlled reset bit (RST) maintains the fixed disk in a reset condition as long as it is active (high). This bit must be turned on for a minimum of 5.0 microseconds, then off, to complete the reset function.

In dual drive configurations, the slave drive negates PDIAG- upon receiving the reset signal and asserts PDIAG- after completing its reset routines. The master drive, after completing its reset routines and before negating BSY, waits up to 30 seconds for the slave drive to assert PDIAG-. If PDIAG- is not asserted, the error register will contain 81h.

Bit 1 (IDS): The interrupt disable control bit (IDS) is used to disable (high) or enable (low) controller interrupts. Disabling an interrupt does not clear a pending interrupt. Disabling interrupts also tristates the INTRQ line. A pending interrupt executes once interrupts are re-enabled. Interrupts are disabled following a system master reset**.**

4.2.13 Digital Input Register

The Digital Input Register reflects the current state of the floppy change flag and the fixed disk drive's select, head select, and write gate signals. If the floppy disk option on the adapter board is not installed, bit 7 remains tristated.

BIT POSITIONS							
7	6	5	4	3	2	1	0
DCG	WTG-	HS3-	HS2-	HS1-	HS0-	DS2-	DS1-

DCG	Diskette Change Flag
WTG-	Write Gate On
HS3- to HS0-	Drive Head Selection (binary)
DS2- to DS1-	Drive Select

4.3 Host Interface Commands

Table 4-3 lists the hexadecimal codes specific to each command supported by Western Digital's Caviar drives.

COMMAND	HEX OPCODE
Recalibrate[1]	1X
Read Sector[1]	2X
Write Sector[1]	3X
Read Verify[1]	4X
Format Track[1]	50
Seek[1]	7X
Execute Diagnostic	90
Set Drive Parameters	91
Execute S.M.A.R.T.	B0
Read DMA[1]	C8 or C9
Write DMA[1]	CA or CB
Read Multiple[1]	C4
Write Multiple[1]	C5
Set Multiple	C6
Standby Immediate	E0 or 94
Idle Immediate	E1 or 95
Standby With Timer	E2 or 96
Idle With Timer	E3 or 97
Read Buffer	E4
Check Power Mode	E5 or 98
Sleep	E6 or 99
Write Buffer	E8
Identify Drive	EC
Set Features	EF
Translate ID	F5
X - Don't care	*[1] Indicates Logical Block Addressing Mode Supported*

Table 4-3. Standard Command Opcodes

To initiate a controller operation, the host first transfers the pertinent information to the task file and writes the command to the Command Register. The controller validates the contents of the task file registers and then performs the desired function. The Caviar commands are briefly defined in the following subsections.

4.3.1 Recalibrate (1Xh)

The Recalibrate command causes the Caviar to move the read/write heads from anywhere on the disk to cylinder zero. Upon receipt of the command, the drive asserts BSY and issues a seek to cylinder zero. The drive waits for assertion of SEEK COMPLETE before updating the Status Register, clearing BSY and setting INTRQ. If the read/write heads cannot reach cylinder zero, the ERR bit and TK0 bit are asserted in the Status and Error Registers, respectively.

If the LBA is set in the SDH Register, the drive seeks to LBA 0. See Section 3.7 for a detailed description of LBA mode.

The Recalibrate command does not invalidate any cache segments.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	0	0	0	1	X	X	X	X
SDH	1	LBA	1	D	X	X	X	X
Features Sector Count Sector Number Cylinder Low Cylinder High	Don't Care Don't Care Don't Care Don't Care Don't Care							
LBA = Logical Block Addressing Bit (1=LBA mode, 0=CHS mode) D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

4.3.2 Read Sector (2Xh)

For a Read Sector command, the task file registers determine the number and location of the sectors transferred to the host. The host can request a maximum of 256 sectors, but only single-sector reads are allowed in long mode. (A sector count of zero specifies 256 sectors.) If the drive is not positioned at the specified cylinder, an implied seek occurs. If the long mode bit is set, four ECC bytes are transferred along with the data. Single burst errors of up to 11 bits are corrected if retries are enabled and the long mode is not selected. An interrupt occurs before the data read from each sector is transferred to the host.

With CacheFlow4, the requested sector address and sector count parameters are monitored to perform segment partitioning and sequential/repetitive switching. If partitioning changes are not required, the currently active segment and other segments are checked for data. If there is no cache hit, the least used segment will be used to read data from disk and to store read-ahead data after the last sector.

If the LBA bit is set in the SDH Register, then Cylinder High, Cylinder Low, Sector Number, and bits 0-3 or the SDH Register are modified to support Logical Block Addressing. See Section 3.7 for a detailed description of the modified usage of these registers.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	0	0	1	0	0	0	L	R
SDH	1	LBA	1	D	HS3	HS2	HS1	HS0
Features	Don't Care							
Sector Count	1-256 Sectors to be Read							
Sector Number	Starting Sector Number							
Cylinder Low	Starting Cylinder LSB							
Cylinder High	Starting Cylinder MSB							

L = Long Mode Bit (1=enable, 0=disable)
R = Retry Bit (1=disabled, 0=enabled)
LBA = Logical Block Addressing Bit (1=LBA mode, 0=CHS mode)
D = Drive Designation Bit (0=master, 1=slave)
HS3-HS0 = Starting Head Number

4.3.3 Write Sector (3Xh)

For a Write Sector command, the host transfers a number of sectors (1-256) to the drive, starting at the logical address specified by the task file registers. An implied seek occurs if the drive is not positioned at the specified address. If the long mode bit is set, only single-sector writes are allowed, and the host transfers four ECC bytes along with the data.

An interrupt is generated as the data for each sector is required (except the first). The first data buffer contents are sent after the host has issued the command and the data request status bit is "on".

DRQ must be set before the host write buffers begin transferring to the base segment. The base segment is reserved for write operations. Other caching segments remain valid. Caching segments that contain sectors that were referenced by the disk write operation become invalid before the write is completed.

If the LBA bit is set in the SDH Register, then Cylinder High, Cylinder Low, Sector Number, and bits 0-3 of the SDH Register are modified to support Logical Block Addressing. See Section 3.7 for a detailed description of the modified usage of these registers.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	0	0	1	1	0	0	L	R
SDH	1	LBA	1	D	HS3	HS2	HS1	HS0
Features	Don't Care							
Sector Count	1-256 Sectors to be Written							
Sector Number	Starting Sector Number							
Cylinder Low	Starting Cylinder LSB							
Cylinder High	Starting Cylinder MSB							

L = Long Mode Bit (1=enabled, 0=disabled)
R = Retry Bit (1=disabled, 0=enabled)
LBA = Logical Block Addressing Bit (1=LBA mode, 0=CHS mode)
D = Drive Designation Bit (0=master, 1=slave)
HS3-HS0 = Starting Head Number

4.3.4 Read Verify (4Xh)

The Read Verify command is the same as a Read command except that the requested sectors are not transferred to the host.

With CacheFlow4, the requested sector address and sector count parameters are monitored to perform segment partitioning and sequential/repetitive switching. If partitioning changes are not required, the currently active segment is checked for data. If the physical cylinder is valid, but no data is present, a read disk operation begins. If the physical cylinder is invalid, other active cache segments are checked for data before the seeking operation begins.

If the LBA bit is set in the SDH Register, then Cylinder High, Cylinder Low, Sector Number, and bits 0-3 of the SDH Register are modified to support Logical Block Addressing. See Section 3.7 for a detailed description of the modified usage of these registers.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	0	1	0	0	0	0	0	R
SDH	1	LBA	1	D	HS3	HS2	HS1	HS0
Features	Don't Care							
Sector Count	1-256 Sectors to Verify							
Sector Number	Starting Sector Number							
Cylinder Low	Starting Cylinder LSB							
Cylinder High	Starting Cylinder MSB							

R = Retry Bit (1=disabled, 0=enabled)
LBA = Logical Block Addressing Bit (1=LBA mode, 0=CHS mode)
D = Drive Designation Bit (0=master, 1=slave)
HS3-HS0 = Starting Head Number

4.3.5 Format Track (50h)

The track specified by the task file is formatted with ID and data fields in accordance with the interleave table transferred to the sector buffer. The buffer contains the Sectors-Per-Track (SPT) entries (1 through the number of SPT) for the track's ID files. These SPT values are totally dependent upon the translation mode selected. The buffer must contain descriptors for the current translation SPT value. If these entries are not present, then no operation is executed on that sector. The data fields are initialized to zeros. The interleave table identifies any bad sectors on a given track and must contain 512 bytes of data. This table is comprised of two bytes per sector as follows:

- The first byte is set to "00h" to indicate a good sector, to "80h" to indicate a bad sector, to "20h" to request that the block be unassigned, or to "40h" to assign this sector to an alternate sector.
- The second byte designates the logical sector ID number (1-SPT).

Unused bytes may be uninitialized. The SPT value is specified in the Sector Count and SDH Register. The sectors per track value in the Sector Count Register must correspond with the values indicated by the Set Drive Parameters command. An interrupt is generated upon completion of the command.

When the Format Track command is issued with LBA mode enabled, the drive does not format a logical track but instead formats the number of blocks specified in the Sector Count Register beginning at the LBA specified.

The sector ID's in the interleave table are relative addresses to the starting LBA. For example, Sector ID 2 in the interleave table corresponds to the second sector being formatted by the Format Track Command. In all other respects the interleave table is the same as in CHS mode.

If the LBA bit is set in the SDH Register, then Cylinder High, Cylinder Low, Sector Number, and bits 0-3 of the SDH Register are modified to support Logical Block Addressing. See Section 3.7 for a detailed description of the modified usage of these registers.

REGISTER	BINARY OPCODE							
	7	6	5	4	3	2	1	0
Command	0	1	0	1	0	0	0	0
SDH	1	LBA	1	D	HS3	HS2	HS1	HS0
Features	Don't Care							
Sector Count	Number of Sectors per Track							
Sector Number	Don't Care							
Cylinder Low	Cylinder Address LSB							
Cylinder High	Cylinder Address MSB							

LBA = Logical Block Addressing Bit (1=LBA mode, 0=CHS mode)
D = Drive Designation Bit (0=master, 1=slave)
HS3-HS0 = Starting Head Number

4.3.6 Seek (7Xh)

The Seek command positions the read/write heads over the cylinder specified in the task file's cylinder number registers. When the command is received, the Caviar asserts BSY in the Status Register, starts the seek operation, and sets INTRQ. The seek is not completed before the Caviar returns the interrupt. If BSY is cleared before SEEK COMPLETE is asserted, the Caviar can receive another command. SEEK COMPLETE is asserted when the heads reach the specified cylinder.

If the LBA bit is set in the SDH Register, then Cylinder High, Cylinder Low, Sector Number, and bits 0-3 or the SDH Register are modified to support Logical Block Addressing. See Section 3.7 for a detailed description of the modified usage of these registers.

Seek does not invalidate any cache segments.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	0	1	1	1	X	X	X	X
SDH	1	LBA	1	D	X	X	X	X
Features	Don't Care							
Sector Count	Don't Care							
Sector Number	Don't Care							
Cylinder Low	Cylinder LSB							
Cylinder High	Cylinder MSB							

LBA = Logical Block Addressing Bit (1=LBA mode, 0=CHS mode)
D = Drive Designation Bit (0=master, 1=slave)
X = Don't Care

4.3.7 Execute Diagnostics (90h)

The Execute Diagnostics command causes the Caviar drive to execute its self-diagnostics and to report a result code in the Error Register as follows:

01 = No Error
02 = Not Applicable
03 = Buffer RAM Error
04 = WD61C29 Register Error
05 = Microcontroller Internal RAM error or ROM checksum error
8X = Slave Drive Failed

The following tests are performed:

- ROM checksum test
- RAM test. Tests 32 KB of the microcontroller and the DRAM. An incremental pattern is written to both internal and external RAM and then read back.
- A register test of the WD61C29 is performed.

If the Caviar drive is configured as a master drive, it monitors the PDIAG- (passed diagnostics) line. A slave drive pulls this line active low once it has successfully performed its diagnostics.

If the Execute Diagnostics command is issued with the slave drive selected, both drives execute the command just as if the command has been issued to the master drive. The master drive's task file drives the bus and it waits up to 5 seconds for the slave drive to assert PDIAG-. The Drive Designation Bit (bit 4 of the SDH Register) is always returned as zero to the host following the Execute Diagnostics command.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	0	0	0
SDH	Don't Care							
Features	Don't Care							
Sector Count	Don't Care							
Sector Number	Don't Care							
Cylinder Low	Don't Care							
Cylinder High	Don't Care							

4.3.8 Set Drive Parameters (91h)

The Set Drive Parameters command configures the Caviar for a specific number of Sectors Per Track (SPT) and heads. The values in the Sector Count Register and the SDH Register determine SPT and heads, respectively. Regardless of the values for SPT and heads, the Caviar will always be in translation mode. See Section 2.2 for the recommended set-up parameters.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	0	0	1	0	0	0	1
SDH	1	0	1	D	HS3	HS2	HS1	HS0
Features Sector Count Sector Number Cylinder Low Cylinder High	Don't Care 1-255 Sectors per Track Don't Care Don't Care Don't Care							
D = Drive Designation Bit (0=master, 1=slave) HS3-HS0 = 1-16 Heads								

4.3.9 Execute S.M.A.R.T. (B0h)

The Execute S.M.A.R.T. command provides access to attribute values, S.M.A.R.T. status, and other S.M.A.R.T. information. These commands can be used for logging and reporting purposes, and for accommodating special user needs.

Prior to writing the Execute S.M.A.R.T. command to the Command Register, the host must write key values into the Cylinder Low and Cylinder High Registers (4Fh, C2h) or the command will be aborted and an error will be reported.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	0	1	1	0	0	0	0
SDH	1	X	1	D	X	X	X	X
Cylinder Low	0	1	0	0	1	1	1	1
Cylinder High	1	1	0	0	0	0	1	0
Features Sector Number	See Table Below Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

The Execute S.M.A.R.T. command has several sub-commands that are selectable via the Features Register when the host issues the Execute S.M.A.R.T. command. To select a sub-command, the host must write the appropriate sub-command code to the Features Register before issuing the Execute S.M.A.R.T. command. The sub-commands and their respective codes are listed below. For more detailed information on executing S.M.A.R.T. commands, please see the SFF-8035i and SFF-8055i specifications.

Features Register	Sector Count	Sub-Command Description
D0h	Don't Care	Read S.M.A.R.T. Attribute Values
D2h	00 = disable F1h = enable	Enable/Disable Attribute Autosave
D4h	Don't Care	Execute S.M.A.R.T. Off-Line Immediate
D8h	Don't Care	Enable S.M.A.R.T. Operations
D9h	Don't Care	Disable S.M.A.R.T. Operations
DAh	Don't Care	Return S.M.A.R.T. Status
DBh	00 = disable F8h = enable	Enable/Disable S.M.A.R.T. Automatic Off-Line

4.3.10 Read DMA (C8h or C9h)

For a Read DMA command, the task files registers determine the number and location of the sectors transferred to the host. The host can request a maximum of 256 sectors. A sector count of zero specifies 256 sectors. If the drive is not positioned at the specified cylinder, an implied seek occurs. An interrupt occurs when all data has been transferred to the host and status is available.

For this command, the caching operation is the same as in the Read-Sector command (20h).

If the LBA bit is set in the SDH Register, then Cylinder High, Cylinder Low, Sector Number, and bits 0-3 of the SDH Register are modified to support Logical Block Addressing. See Section 3.7 for a detailed description of the modified usage of these registers.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	1	0	0	1	0	0	R
SDH	1	LBA	1	D	HS3	HS2	HS1	HS0
Features	Don't Care							
Sector Count	1-256 Sectors to be Read							
Sector Number	Starting Sector Number							
Cylinder Low	Starting Cylinder LSB							
Cylinder High	Starting Cylinder MSB							
R = Retry Bit (1=disabled, 0=enabled) LBA = Logical Block Addressing Bit (1=LBA mode, 0=CHS mode) D = Drive Designation Bit (0=master, 1=slave) HS3-HS0 = Starting Head Number								

4.3.11 Write DMA (CAh or CBh)

For a Write DMA command, the host transfers a number of sectors (1-256) to the drive, starting at the logical address specified by the task file registers. An implied seek occurs if the drive is not positioned at the specified address.

An interrupt is generated when all the data has been transferred and written to the media. The first data buffer contents are sent after the host has issued the command and the data request bit is "on".

DRQ must be received before the host write buffers begin transferring to the base segment. The base segment is reserved for write operations. Other caching segments remain valid. Caching segments that contain sectors that were referenced by the disk write operation become invalid before the write is completed.

If the LBA bit is set in the SDH Register, then Cylinder High, Cylinder Low, Sector Number, and bits 0-3 of the SDH Register are modified to support Logical Block Addressing. See Section 3.7 for a detailed description of LBA mode.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	1	0	0	1	0	1	R
SDH	1	LBA	1	D	HS3	HS2	HS1	HS0
Features	Don't Care							
Sector Count	1-256 Sectors to be Written							
Sector Number	Starting Sector Number							
Cylinder Low	Starting Cylinder LSB							
Cylinder High	Starting Cylinder MSB							

R = Retry Bit (1=disabled, 0=enabled)
LBA = Logical Block Addressing Bit (1=LBA mode, 0=CHS mode)
D = Drive Designation Bit (0=master, 1=slave)
HS3-HS0 = Starting Head Number

4.3.12 Read Multiple (C4h)

The Read Multiple command operates similarly to the Read Sectors command except for the following conditions:

- Data transfers occur in multiple sector blocks
- Long bit is invalid
- Retries are always performed

Interrupts and DRQs occur once per block of multiple sectors. The number of sectors per block is set using the Set Multiple command. When the Read Multiple command is issued, the sector count value sets the total number of sectors to be transferred (not blocks or block count). The sector count need not be a multiple of the number of sectors per block as specified by the Set Multiple command. Partial block transfers are completed when the remaining sectors are ready for transfer. The Caviar must be in multiple mode for this command to operate correctly. Otherwise, the command aborts.

If the LBA bit is set in the SDH Register, then Cylinder High, Cylinder Low, Sector Number, and bits 0-3 of the SDH Register are modified to support Logical Block Addressing. See Section 3.7 for a detailed description of the modified usage of these registers.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	1	0	0	0	1	0	0
SDH	1	LBA	1	D	HS3	HS2	HS1	HS0
Features	Don't Care							
Sector Count	1-256 Sectors to be Read							
Sector Number	Starting Sector Number							
Cylinder Low	Starting Cylinder LSB							
Cylinder High	Starting Cylinder MSB							
Retries always performed. LBA = Logical Block Addressing Bit (1=LBA mode, 0=CHS mode) D = Drive Designation Bit (0=master, 1=slave) HS3-HS0 = Starting Head Number								

4.3.13 Write Multiple (C5h)

The Write Multiple command operates similarly to the Write Sectors command except for the following conditions:

- Data transfers occur in multiple sector blocks
- Long bit is invalid
- Retries are always performed

Interrupts and DRQs occur once per block of multiple sectors. The number of sectors per block value is set using the Set Multiple command. When the Write Multiple command is issued, the sector count value sets the total number of sectors to be transferred (not blocks or block count). The sector count need not be a multiple of the number of sectors per block as specified by the Set Multiple command. Partial block transfers are completed when the remaining sectors are ready for transfer. The Caviar must be in multiple mode for this command to operate correctly. Otherwise, the command aborts.

DRQ must be asserted before the host can begin transferring to the base segment. The base segment is reserved for write operations. Other caching segments remain valid. Caching segments that contain sectors that were referenced by the disk write operation become invalid before the write is completed.

If the LBA bit is set in the SDH Register, then Cylinder High, Cylinder Low, Sector Number, and bits 0-3 of the SDH Register are modified to support Logical Block Addressing. See Section 3.7 for a detailed description of the modified usage of these registers.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	1	0	0	0	1	0	1
SDH	1	LBA	1	D	HS3	HS2	HS1	HS0
Features	Don't Care							
Sector Count	1-256 Sectors to be Written							
Sector Number	Starting Sector Number							
Cylinder Low	Starting Cylinder LSB							
Cylinder High	Starting Cylinder MSB							
Retries always performed. LBA = Logical Block Addressing Bit (1=LBA mode, 0=CHS mode) D = Drive Designation Bit (0=master, 1=slave) HS3-HS0 = Starting Head Number								

4.3.14 Set Multiple (C6h)

The Set Multiple command sets the number of sectors per block to be transferred between the host and the Caviar for the Read and Write Multiple commands. The number of sectors per block value is loaded into the Sector Count Register. The maximum number of sectors per block is 16. A value beyond the limit causes an aborted command error. A value of one is considered valid. A value of zero disables multiple mode.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	1	0	0	0	1	1	0
SDH	1	X	1	D	X	X	X	X
Features	Don't Care							
Sector Count	1-16 Sectors per Block							
Sector Number	Don't Care							
Cylinder Low	Don't Care							
Cylinder High	Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

4.3.15 Standby Immediate (E0h or 94h)

The Standby Immediate command causes the drive to set BSY, enter the Standby Power Mode, then clear BSY and generate an interrupt. The drive interface is active and is capable of accepting all the supported AT commands. However, the drive may take as long as 15 seconds to respond to a media access command because the media is not immediately accessible due to a spindown condition. The Drive Ready (DRDY) signal is not a power condition. The drive posts Ready at the interface even though the media is not accessible.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command E0h or Command 94h	1 1	1 0	1 0	0 1	0 0	0 1	0 0	0 0
SDH	1	X	1	D	X	X	X	X
Features Sector Count Sector Number Cylinder Low Cylinder High	Don't Care Don't Care Don't Care Don't Care Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

4.3.16 Idle Immediate (E1h or 95h)

The Idle Immediate command causes the drive to set BSY, enter the Idle Power Mode, clear BSY and generate an interrupt. In Idle Mode the drive will respond immediately to any media access commands.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command E1h or Command 95h	1 1	1 0	1 0	0 1	0 0	0 1	0 0	1 1
SDH	1	X	1	D	X	X	X	X
Features Sector Count Sector Number Cylinder Low Cylinder High	Don't Care Don't Care Don't Care Don't Care Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

4.3.17 Standby With Timer (E2h or 96h)

The Standby with Timer command causes the drive to set BSY, enter the Standby Power Mode, clear BSY and generate an interrupt. The drive interface is active and is capable of supporting all the supported AT commands. However, the drive may take as long as 15 seconds to respond to a media access command because the media is not immediately accessible due to a spin down condition. The Drive Ready (DRDY) signal is not a power condition. The drive posts Ready at the interface even though the media is not accessible.

The drive automatically re-enters this Power Mode upon the expiration of a prescribed time following the execution of the last command. This time interval is specified using the Sector Count Register when issuing the Standby with Timer command. If the Sector Count Register is non-zero, the automatic power-down sequence is enabled and a timer begins counting down upon completion of the last command. If the Sector Count Register is zero, the automatic power-down sequence is disabled. To optimally balance power savings against disk wear, we recommend a ten-minute spin-down period.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command E2h	1	1	1	0	0	0	1	0
or								
Command 96h	1	0	0	1	0	1	1	0
SDH	1	X	1	D	X	X	X	X
Features	Don't Care							
Sector Count	See Table Below							
Sector Number	Don't Care							
Cylinder Low	Don't Care							
Cylinder High	Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

Sector Count Register	**Timer Value**
0	disabled
1-240	count * 5 seconds
241-251	(count - 240) * 30 minutes
252	count * 5 seconds
253	10 hours
254, 255	count * 5 seconds

4.3.18 Idle With Timer (E3h or 97h)

The Idle With Timer command causes the drive to set BSY, enter the Idle Power Mode, then clear BSY and generate an interrupt. In the Idle mode the drive responds immediately to any media access commands.

The drive automatically transitions to the Standby Power Mode upon expiration of a prescribed time following the execution of the Idle With Timer (E3h or 97h) command or any other command. This time interval is specified using the sector count register in this command. If the Sector Count Register is non-zero, then the automatic power-down sequence is enabled, and a timer begins counting down upon completion of the last command. If the Sector Count Register is zero, then the automatic power-down sequence is disabled.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command E3h or Command 97h	1 1	1 0	1 0	0 1	0 0	0 1	1 1	1 1
SDH	1	X	1	D	X	X	X	X
Features Sector Count Sector Number Cylinder Low Cylinder High	Don't Care See Table Below Don't Care Don't Care Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

Sector Count Register	**Timer Value**
0	disabled
1-240	count * 5 seconds
241-251	(count - 240) * 30 minutes
252	count * 5 seconds
253	10 hours
254, 255	count * 5 seconds

4.3.19 Read Buffer (E4h)

The Read Buffer command allows the host to read Buffer 0 of the Caviar 128-KB RAM cache, for example, the 512 bytes of the first sector buffer in the base cache segment.

REGISTER	BINARY OPCODE							
	7	6	5	4	3	2	1	0
Command	1	1	1	0	0	1	0	0
SDH	1	X	1	D	X	X	X	X
Features	Don't Care							
Sector Count	Don't Care							
Sector Number	Don't Care							
Cylinder Low	Don't Care							
Cylinder High	Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

4.3.20 Check Power Mode (E5h or 98h)

The Check Power Mode command allows the host to determine the current power mode and programmed value for the spin down timer.

If the drive is in or transitioning to the Standby Power Mode, it sets BSY, sets the Sector Count Register to 00h, then clears BSY and generates an interrupt.

If the drive is in the Idle Power Mode, it sets BSY, sets the Sector Count Register to FFh, then clears BSY and generates an interrupt.

In the Cylinder Low Register, the currently programmed value for the spin down timer is returned. A value of 00h means that the timer is disabled.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command E5h or Command 98h	1 1	1 0	1 0	0 1	0 1	1 0	0 0	1 0
SDH	1	X	1	D	X	X	X	X
Features Sector Count Sector Number Cylinder Low Cylinder High	Don't Care Don't Care Don't Care Don't Care Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

4.3.21 Sleep (E6h or 99h)

Only the Sleep command causes the drive to enter the Sleep Power Mode. During sleep mode, drive interface is inactive. A Soft Reset, an AT Bus Reset or a Power On Reset are the only means for recovery from this power mode. A soft reset or AT Bus Reset when in the Sleep Mode returns the drive to the Standby Mode. Power cycling returns the drive to its default ready mode. Upon entry to the Sleep Power Mode the drive motor is stopped, BSY is cleared, an interrupt is generated and the interface becomes inactive.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command E6h or Command 99h	1 1	1 0	1 0	0 1	0 1	1 0	1 0	0 1
SDH	1	X	1	D	X	X	X	X
Features Sector Count Sector Number Cylinder Low Cylinder High	Don't Care Don't Care Don't Care Don't Care Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

4.3.22 Write Buffer (E8h)

The Write Buffer command functions identically to the Read Buffer command except that 512 bytes of data are transferred from the host to the Caviar RAM cache.

The Read and Write Buffer commands only affect the first 512 bytes of the Caviar RAM cache.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	1	1	0	1	0	0	0
SDH	1	X	1	D	X	X	X	X
Features	Don't Care							
Sector Count	Don't Care							
Sector Number	Don't Care							
Cylinder Low	Don't Care							
Cylinder High	Don't Care							

D = Drive Designation Bit (0=master, 1=slave)
X = Don't Care

4.3.23 Identify Drive (ECh)

The Identify Drive command transfers 512 bytes of data that specify the drive's parameters. The host is required to read the parameters out of the sector buffer when the Caviar sets DRQ and IRQ. Table 4-4 lists the parameters read by the host.

REGISTER	BINARY OPCODE							
	7	6	5	4	3	2	1	0
Command	1	1	1	0	1	1	0	0
SDH	1	X	1	D	X	X	X	X
Features	Don't Care							
Sector Count	Don't Care							
Sector Number	Don't Care							
Cylinder Low	Don't Care							
Cylinder High	Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

WORD	FIELD DESCRIPTION*	VALUE
0	General Configuration	0427A h
1	Number of Fixed Cylinders	3148 (AC21600) 4092 (AC32100) 4960 (AC32500)
2	Reserved	0
3	Number of Heads	16
4	Unformatted Bytes Per Track	57,600
5	Unformatted Bytes Per Sector	600
6	Sectors per Track	63
7	Minimum Size of ISG in Bytes	16
8	Reserved	0
9	Minimum PLO Bytes	14
10-19	Serial Number	WDnnnnnnnn
20	Buffer Type: Read-Ahead Cache	3
21	Controller Buffer Size in 512 Byte Blocks	256
22	Vendor Unique ECC Bytes Supported	22
23-26	Controller Firmware Revision	“nnnn”
27-46	Model Number	“WDC AC21600H” “WDC AC32100H” “WDC AC32500H”
47	Numbers of Sectors/Interrupt R/W Multiples	8010h
48	Double Word I/O	0
49	IORDY/LBA/DMA Support	2F00h[1]
50	Reserved	0
51	PIO Data Transfer Cycle Timing Mode	0280h[2]
52	Single Word DMA Data Transfer Mode	0000h[2]
53	Additional Words Valid	0003h[3]
54	Number of Current Cylinders	XX[4]
55	Number of Current Heads	XX[4]
56	Number of Current Sectors per Track	XX[4]
57-58	Current Capacity in Sectors	XX[4]
59	Current Blocking Factor	XX[5]
60-61	Total Number of Addressable Sectors	3,173,184 (AC21600) 4,124,736 (AC32100) 4,999,680 (AC32500)
62	Single Word DMA Transfer Mode Supported	00
63	Multi-Word DMA Transfer Mode Supported	0407h[6]
64	Advanced PIO Modes Supported	0003h[7]

WORD	FIELD DESCRIPTION*	VALUE
65	Min. Multi-Word DMA Transfer Cycle Time (ns)	120[8]
66	Manufacturer Recommended Multi-Word DMA Cycle Time (ns)	120[8]
67	Min. PIO Transfer Cycle Time without IORDY (ns)	160[8]
68	Min. PIO Transfer Cycle Time with IORDY (ns)	120[8]
69-255	Reserved	0

[1]Bits 15-14: Reserved
Bit 13: If set, supports ATA-2 standby timer definitions
Bit 12: Reserved.
Bit 11: If set, means IORDY supported.
Bit 10: If set, means IORDY can be disabled.
Bit 9: If set, means LBA mode supported.
Bit 8: If set, means DMA mode supported.
Bit 7-0: Vendor unique.

[2]Bits 15-8: PIO mode supported.
Bits 7-0: Vendor unique.

[3]Bits 15-2: Reserved
Bit 1: If set, means Words 64-68 are valid.
Bit 0: If set, means Words 54-58 are valid.

[4]Set to the number of heads and sectors used the last time the drive received a Set Drive Parameters Command. The number of cylinders is calculated by the drive to make full use of all available sectors on the drive. Current capacity is calculated by multiplying the current cylinders, heads, and sectors per track.

[5]Bit 15-9: Reserved
Bit 8: Always set to 1.
Bit 7-0: Current number of sectors/interrupt on read/write multiples.

[6]Bits 15-8: Multi-Word DMA mode active.
Bit 0: If set, means that Multi-Word DMA mode 0 is supported.
Bit 1: If set, means that Multi-Word DMA mode 1 is supported.
Bit 2: If set, means that Multi-Word DMA mode 2 is supported.

[7]Bits 15-1: Reserved
Bit 0: If set, means Mode 3 PIO supported.
Bit 1: If set, means Mode 4 PIO supported.

[8]IOR- and IOW- cycle times in nanoseconds.

* The data structure for the Identify Drive command contains 512 bytes of information.

Table 4-4 Identify Drive Command

4.3.24 Set Features (EFh)

The Set Features command enables or disables the features listed in the following table. Do not enable Mode 3 or Mode 4 PIO if the host system does not support I/O channel ready.

FUNCTION	FEATURES REGISTER	SECTOR COUNT REGISTER
Enable read cache	AAh	Don't care
Disable read cache	55h	Don't care
Enable write cache	02h	Don't care
Disable write cache	82h	Don't care
Select 22 byte ECC mode	44h	Don't care
Select 4 byte ECC mode	BBh	Don't care
Select 2 to 7 read segments	A2h-A7h	Don't care
PIO Default Mode	03h	00h
Disable IORDY	03h	01h
Enable Mode 3 PIO	03h	0Bh
Enable Mode 4 PIO	03h	0Ch
Enable Multi-Word DMA Mode 0	03h	20h
Enable Multi-Word DMA Mode 1	03h	21h
Enable Multi-Word DMA Mode 2	03h	22h

Note that changes made using the Set Features command are only valid while power remains applied to the drive. After power is cycled, the drive reverts to its default settings.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	1	1	0	1	1	1	1
SDH	1	X	1	D	X	X	X	X
Features Sector Count Sector Number Cylinder Low Cylinder High	AAh or 55h, 02h or 82h, 44h or BBh, A2h-A7h, 03h See table above Don't Care Don't Care Don't Care							
D = Drive Designation Bit (0=master, 1=slave) X = Don't Care								

4.3.25 Translate ID (F5h)

The Translate ID command translates the logical sector address into a physical sector address. Upon receipt of the command, the drive asserts BSY in the Status Register, performs the specified translation, updates the task file to contain the physical sector address, clears BSY, and sets IRQ to the host.

	BINARY OPCODE							
REGISTER	7	6	5	4	3	2	1	0
Command	1	1	1	1	0	1	0	1
SDH	1	0	1	D	HS3	HS2	HS2	HS0
Features	Don't Care							
Sector Count	Don't Care							
Sector Number	Logical Sector Number							
Cylinder Low	Logical Cylinder Low							
Cylinder High	Logical Cylinder High							
D = Drive Designation Bit (0=master, 1=slave) HS3-HS0 = Logical Head Select Bits								

4.4 Host I/O Read Timing

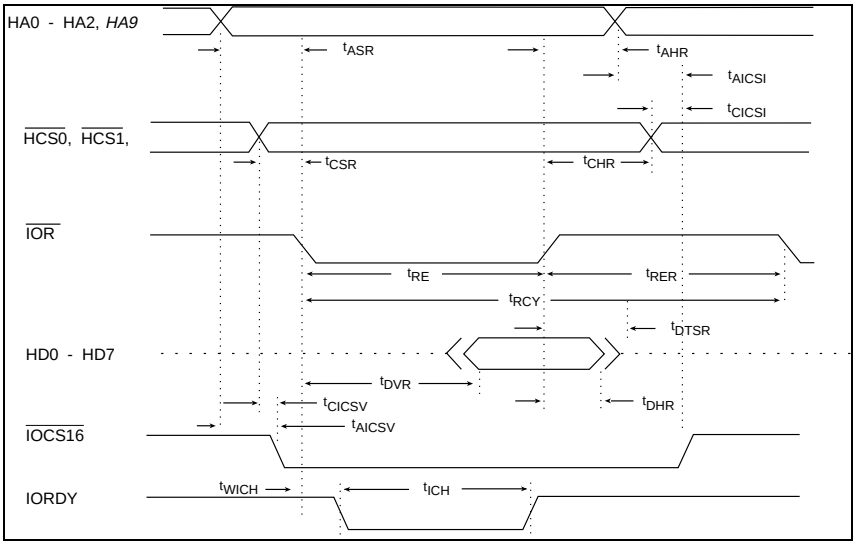

Figure 4-2. Host I/O Read Timing

Symbol	Description	Min	Max	Conditions
t_{ASR}	Address Setup to IOR- low	10		
t_{CSR}	HCS0-, HCS1- Setup to IOR- low	10		
t_{DVR}	Data valid from IOR- low		55 45	All 8-bit registers, HDRV=1 Data Port, HDRV=1, Cload=100pf
t_{RE}[1]	IOR- pulse width	65		All 8-bit and 16-bit ports
t_{DHR}	Data hold from IOR- high	5		
t_{DTSR}	Data tristate from IOR- high		20	
t_{AHR}	Address hold from IOR- high	0		
t_{CHR}	HCS0-, HCS1- Hold from IOR- high	0		
t_{RER}[1]	HCS0-, HCS1-, and IOR- inactive	20		
t_{RCY}[1]	Read cycle time	90		
t_{ICH}	IORDY pulse width		[(M+3.50) x66]+25	M=1 to 31 wait states
t_{WICH}	IORDY low to IOR- low		20	
t_{CICSV}	IOCS16- low from HCS0- low		20	
t_{AICSV}	IOCS16- low from address		20	
t_{CICSI}	IOCS16- inactive from HCS0- high		20	To tristate condition, 116DS=1
t_{AICSI}	IOCS16- inactive from address		20	To tristate condition, 116DS=0

1 The sum of the minimum IOR- pulse width requirements t_{RE} and t_{RER} will not equal the minimum cycle time t_{RCY}. Both minimum overall cycle time requirements and minimum pulse width requirements must be met.
Note 1: When the drive asserts IORDY, data is ready to be transferred.
Note 2: All units of measurement are in nanoseconds.

4.5 Host I/O Write Timing

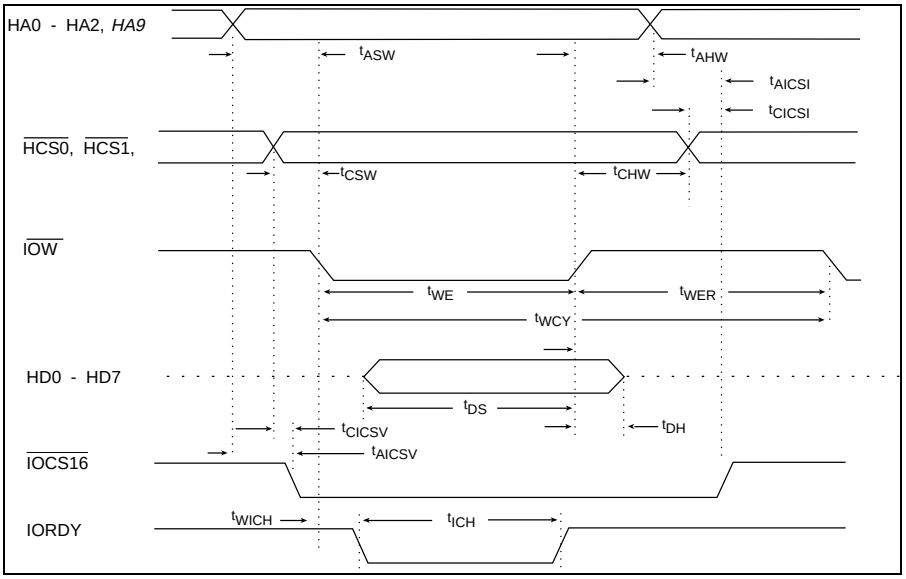

Figure 4-3. Host I/O Write Timing

Symbol	Description	Min	Max	Conditions
t_{ASW}	Address Setup to IOW- low	10		
t_{CSW}	HCS0-, HCS1- Setup to IOW- low	10		
t_{DS}	Data setup to IOW- high	20		All 8-bit and 16-bit ports
t_{WE}[1]	IOW- pulse width	65		All 8-bit and 16-bit ports
t_{DH}	Data Hold from IOW- high	5		
t_{AHW}	Address Hold from IOW- high	0		
t_{CHW}	HCS0-, HCS1-, Hold from IOW- high	0		
t_{WER}[1]	HCS0-, HCS1-, and IOW- inactive	20		
t_{WCY}[1]	Write cycle time	90		
t_{ICH}	IORDY pulse width		[(M+3.5) x66]+25	M=1 to 31 wait states
t_{WICH}	IORDY low to IOW- low		20	
t_{CICSV}	IOCS16- low from HCS0- low		20	
t_{AICSV}	IOCS16- low from address		20	
t_{CICSI}	IOCS16- inactive from HCS0- high		20	To tristate condition, 116DS=1 240pf load
t_{AICSI}	IOCS16- inactive from address		20	To tristate condition, 116DS=0 240pf load

1 The sum of the minimum IOW- pulse width requirements t_{WE} and t_{WER} will not equal the minimum cycle time t_{WCY}. Both minimum overall cycle time requirements and minimum pulse width requirements must be met.
Note: All units of measurement are in nanoseconds.

4.6 Host Multi-Word DMA Read Timing

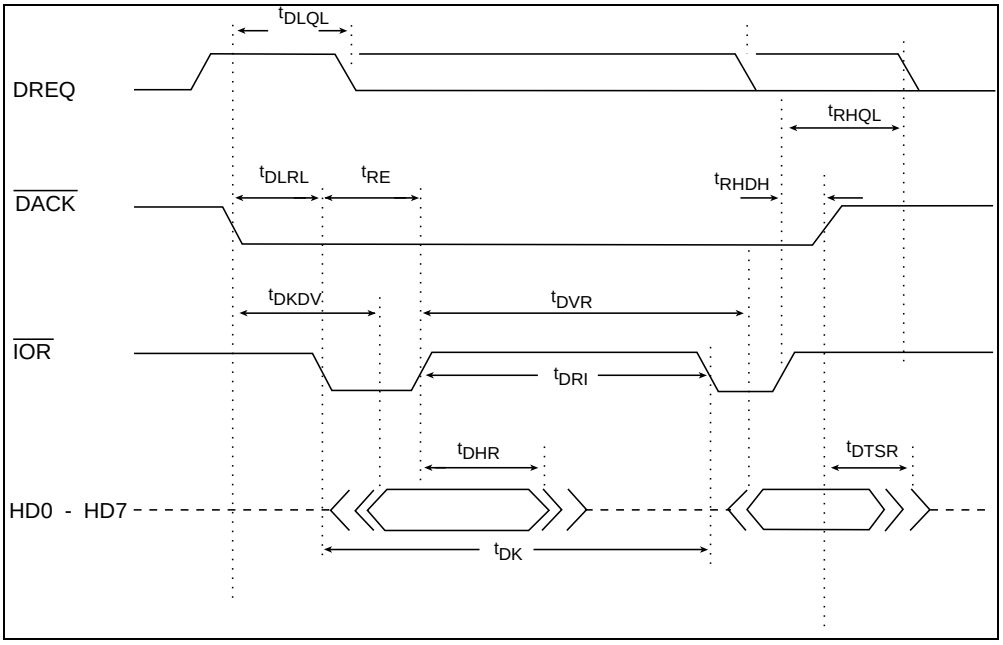

Figure 4-4. Host Multi-Word DMA Read Timing

Symbol	Description	Min	Max	Conditions
t_{DLQL}	DACK- low to DMARQ low		35	BDEN=0 or end of transfer
t_{RHQL}	IOR- high to DREQ low		240	FIFO almost/empty throttle
t_{DK}[1]	DMA- cycle time	90		
t_{DLRL}	DACK- low to IOR- low	0		
t_{RE}[1]	IOR- pulse width	65		
t_{DKDV}	Data valid from IOR- low		45	HDRV=1, Cload=100pf
t_{DHR}	Data hold from IOR- high	5		
t_{DTSR}	Data tristate from IOR- high		20	
t_{RHDH}	IOR- high to DACK- high	0		
t_{DRI}[1]	DACK- to IOR- inactive	20		Block Mode DMA
t_{DVR}	Data valid from IOR- high	70		HDRV=1, Cload=100pf

1 The sum of the minimum IOR- pulse width requirements t_{RE} and t_{DRI} will not equal the minimum cycle time t_{DK}. Both minimum overall cycle time requirements and minimum pulse width requirements must be met.

Note: All units of measurement are in nanoseconds.

4.7 Host Multi-Word DMA Write Timing

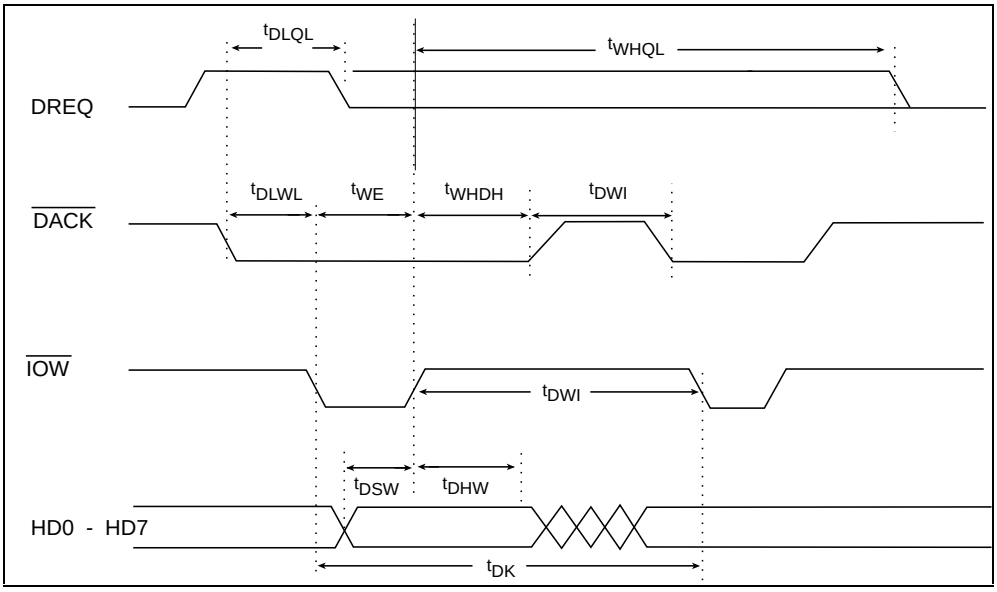

Figure 4-5. Host Multi-Word DMA Write Timing

Symbol	Description	Min	Max	Conditions
t_{DLQL}	DACK- low to DREQ low		35	BDEN=0 or end of transfer
t_{WHQL}	IOW- high to DREQ low		240	FIFO almost/empty throttle
t_{DK}[1]	DMA- cycle time	90		
t_{DLWL}	DACK- low to IOW- low	0		
t_{WE}[1]	IOW- pulse width	65		
t_{DSW}	Data setup to IOW- high	20		
t_{DHW}	Data hold from IOW- high	5		
t_{WHDH}	IOW- high to DACK- high	0		
t_{DWI}[1]	DACK- to IOW- inactive	20		Block Mode DMA

[1] The sum of the minimum IOW- pulse width requirements t_{WE} and t_{DWI} will not equal the minimum cycle time t_{DK}. Both minimum overall cycle time requirements and minimum pulse width requirements must be met.
Note: All units of measurement are in nanoseconds.

4.8 DC Electrical Specifications

Symbol	Characteristic	Min	Max	Unit	Condition
PINS: HD0 - HD15, HIRQ, DREQ					
Voh	Output High Voltage	Vdd-0.5		V	Iout= -4mA
Vol	Output Low Voltage		0.4	V	Iout=24mA (HDRV=0)
Vol	Output Low Voltage		0.4	V	Iout=15mA (HDRV=1)
PINS: IOCS16-, DASP-, PDIAG-, IORDY					
Voh	Output High Voltage	Vdd-0.5			Iout=400uA (IOCS16- only, 116DS=1)
Vol	Output Low Voltage		0.4	V	Iout=24mA
HCS0, HCS1, IOR, IOW-, HRST, DMACK					
Ipu	Pull up current	125	500	uA	Vin=0.4V, VDD=5.5V
HRST					
Ipd	Pull down current	20	200	uA	Vin=5.5V, VDD=5.5V
HA0-HA2, HD0-15, IOR, IOW, HCS0, HCS1, DMACK, PDIAG, DASP, HRST, INDEX, SCT, SRVGATE, WUS, RST					
Vih-Vil	Input Hysteresis	350		mV	
RESET, RST					
Vol	Output Low Voltage		0.4	V	Iout=8mA (VDD within spec)
AME, RWB, RGATE, NRZ0. NRZ1					
Vol	Output Low Voltage		0.4	V	Iout= -1.6mA
Voh	Output High Voltage	Vdd-0.5		V	Iout= -400uA
CLK, BA0-17, BD0-15, SCT, INDEX, SRVGATE, WUX, HA0-2, HCS0, HCS1, HD0-15, IOR-, IOW, HRST, DACK, PDIAG, DASP					
Vih	Input High Voltage	Vdd/2+ 0.3		V	
Vil	Input Low Voltage		Vdd/2+ 0.3	V	
All Pins Not Listed					
Voh	Output High Voltage	Vdd-0.3		V	Iout= -400uA
Vol	Output Low Voltage		0.4	V	Iout=1.6mA

5. INSTALLATION AND SETUP PROCEDURES

Disk drives are precision instruments that must be handled with care to prevent damage. It is important to understand that drives are typically damaged because of Electrostatic Discharge (ESD), rough handling, or shock and vibration. Refer to the Drive Handling Guide (Literature Order No. S0999) for detailed instructions on all phases of drive handling.

5.1 Unpacking

5.1.1 Handling Precautions

Western Digital products are designed to withstand normal handling during unpacking and installation. Care must be taken to avoid excessive mechanical shock or electrostatic discharge (ESD) that can permanently damage the Caviar and void the warranty. Hard drives are typically damaged because of ESD, rough handling or shock and vibration.

To avoid ESD problems wear a properly grounded wrist strap when handling the hard drive. Articles of clothing generate static electricity. Do not allow clothing to come in direct contact with the hard drive or circuit board components.

When the Caviar is not in its shipping container or installed in its proper host enclosure, it must remain in the antistatic bag. To prevent damage, do not unpack your Caviar until you are ready to install it.

5.1.2 Inspection of Shipping Container

Carefully examine the container for obvious shipping damage, such as: holes, signs of crushing, or stains. Notify the carrier and your Western Digital representative if you observe any shipment damage. Always move the shipping container in the upright position indicated by the arrows on the container.

5.1.3 Removal From Shipping Container

Remove the Caviar from the shipping container only for inspection or installation. Carefully open the box. The Caviar is always shipped in a foam-insert package. When removing the Caviar from the foam insert, follow these precautions:

- Grasp the drive by the sides only, avoid touching the circuit board components.
- Gently place the drive on its antistatic bag on a clean, level, grounded work area.
- Do not stack drives or stand the Caviar drive on its edge.

Caution: When removing the Caviar from the shipping container, be careful not to drop it. Dropping the Caviar can severely damage the head disk assembly or printed circuit board.

5.1.4 Removal From Antistatic Bag

Before removing the Caviar drive from its antistatic bag:

- Make sure that your work station is properly grounded.
- Wear a properly grounded wrist strap with good skin contact.
- Avoid contact with any component on the printed circuit board.

After attaching your wrist strap, gently remove the Caviar drive from the antistatic bag.

- Handle the Caviar drive by the sides only, avoid touching the printed circuit board.
- Handle the Caviar drive with the printed circuit board facing downward during installation.
- Do not attempt to open its sealed compartment. Failure to observe this restriction will void the warranty.

5.1.5 Moving Precautions

If it becomes necessary to move your computer, turn off the power to automatically park the heads. Parking moves the heads to a safe, non-data landing zone where they are locked into place. This helps protect the media and the heads from accidental damage due to vibration, moving or shipping.

5.2 Mounting Restrictions

5.2.1 Orientation

The Caviar can be mounted in the X, Y, or Z axis depending upon the physical design of your system. It is recommended that the drive be mounted with all four screws grounded to the chassis. If all four screws are not used, see section 5.2.3.

5.2.2 Screw Size Limitations

The Caviar is mounted to the chassis using four 6-32 screws. Recommended screw torque is 5 in-lb. Maximum screw torque is 10 in-lb.

Caution: Screws that are too long will damage circuit board components. The screw must engage no more than six threads (3/16 inch). Side mounted screws should engage a maximum of .188 inches (3/16"). Bottom mounted screws should engage a maximum of .250 inches (1/4").

5.2.3 Grounding

It is recommended that the drive be mounted with all four screws in the side grounded to the chassis. (Positions A, D, E, and H on Figure 5-1). The drive must be grounded with at least one mounting screw.

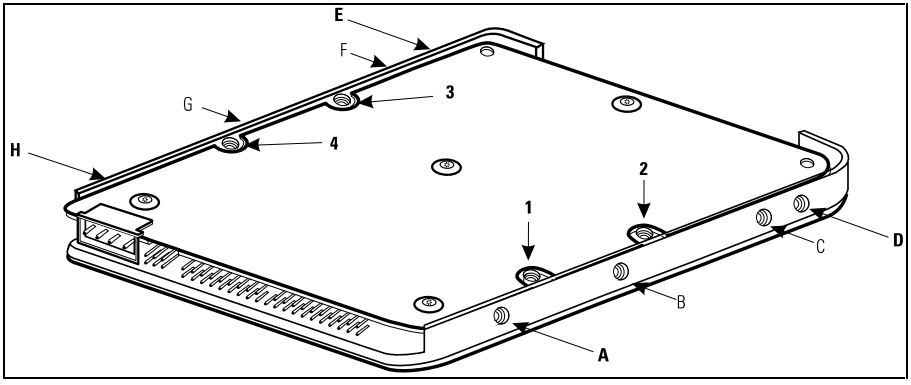

Figure 5-1. Grounding Diagram

Side mounting: Use four metal screws in A, D, E and H. If less than four screws are used, remove in this order: D, E then H. You must use a screw in position A.

Top face mounting: Use four metal screws in 1, 2, 3 and 4. If less than four screws are used, remove in this order: 2, 3 then 4. You must use a screw in position 1.

5.3 Installation Configuration

5.3.1 Determining Your Drive Configuration

You can configure the Caviar in one of two ways:

1. The drive is cabled directly to a 40-pin connector on the motherboard, or
2. The drive is cabled to an adapter card mounted in one of the expansion slots in the computer.

Both configurations use a 40-pin host interface cable.

If you are using the Caviar drive as one of two hard disk drives in the computer (dual installation), you may use either configuration. In dual installations, you must use a 40-pin host interface cable with three connectors and daisy-chain the two drives to the motherboard or adapter card.

5.3.2 Dual Installations

Dual installations require a master/slave drive configuration, where one drive is designated as the primary (master) drive and the other is designated as the secondary (slave) drive. The Caviar drive is compatible in dual installations with other IDE drives that support a master/slave configuration.

5.3.3 Jumper Settings

The Caviar drive has a jumper block (J8) located next to the 40-pin connector on the drive. The Caviar can be assigned as either a single, master, or slave drive. Refer to Figure 5-2 for an illustration of all jumper settings.

Caviar drives are shipped with a jumper shunt in the neutral storage position (across pins 5 and 3).

Single Drive Mode – If you are installing the Caviar drive as the only hard drive in the system, leave the jumper in the neutral storage position. Jumpers are not required for single drive installations. Note that even with no jumper installed, the Caviar checks the DRIVE ACTIVE/SLAVE PRESENT (DASP) signal to determine if a slave IDE drive is present.

If you have a dual installation (two hard drives), you must designate one of the drives as the master and the other as the slave drive. The jumper pins on the J8 connector need to be configured for the dual installation.

Master Drive Mode – To designate the drive as the master, place a jumper shunt on pins 5-6. With the Caviar configured as the master drive, the Caviar assumes that a slave drive is present. The jumper on pins 5-6 is optional if the slave drive follows the same protocol (Common Access Method AT Bus Attachment) as the Caviar.

Slave Drive Mode – To designate the drive as the slave, place a jumper shunt on pins 3-4. When the Caviar is configured as the slave drive, the Caviar delays spin up for three seconds after power-up reset. This feature prevents overloading of the power supply during power-up.

Cable Select (CSEL) – Caviar also supports the CSEL signal on the drive cable as a drive address selection. Place a jumper shunt on pins 1-2 to enable this option. When enabled, the drive address is 0 (Master) if CSEL is low, or 1 (Slave) if CSEL is high.

Do not install the CSEL jumper shunt when installing the Caviar drive in systems that do not support the CSEL feature.

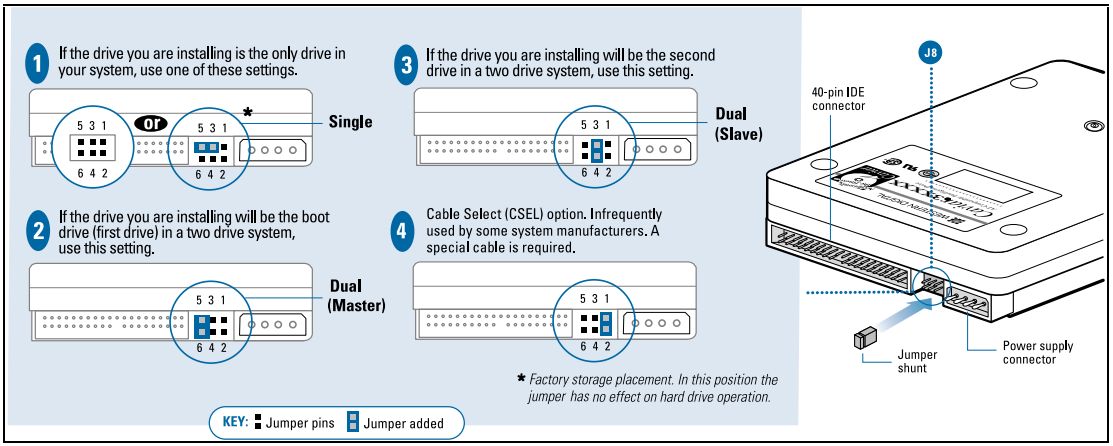

Figure 5-2. Jumper Settings

Alternate Jumper Settings for the Caviar AC32500:

On initial boot, some system BIOSs may lock up on drives that have more than 4095 cylinders (drives larger than 2.1 GB). Alternate jumper settings have been provided for the Caviar AC32500 to overcome this system BIOS limitation. These jumper settings cause the drive to report 4092 cylinders (instead of the usual 4960) in Word 1 of the Identify Drive data. The true capacity is still reported in Word 54 and Word 60-61. All other Identify Drive data remains the same. Special software is required for DOS and Windows operating systems to utilize the full capacity of the AC32500 drive.

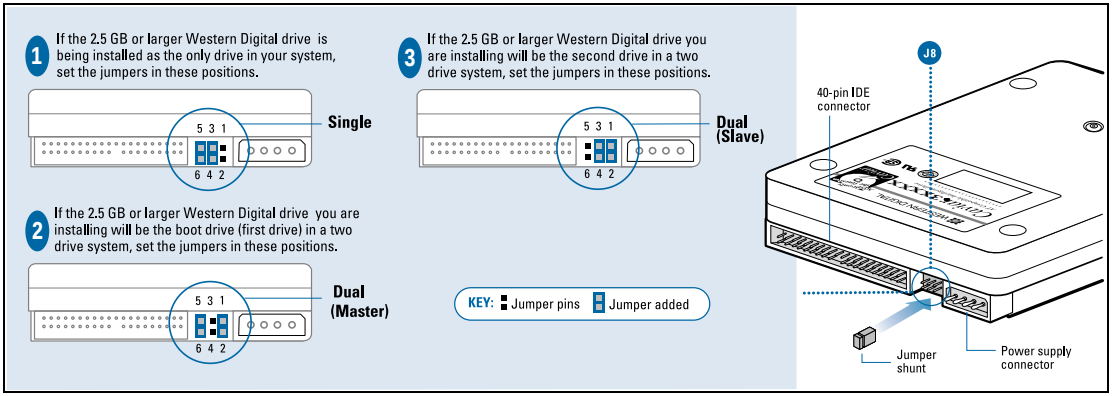

Figure 5-3. Alternate Jumper Settings for the Caviar AC32500

5.4 Installing the Caviar Drive

5.4.1 Mounting the Drive

For dual installations, it is usually easier to completely install one IDE drive in the lower position first. The order of IDE drives is unimportant if you are using two Western Digital drives. As explained previously, one must be jumpered as the master drive and the other as the slave drive. When installation is complete, the drives are daisy-chained together.

5.4.2 Cabling and Installation Steps

Make sure your interface cable is no longer than 18 inches (including daisy chaining) to minimize noise that is induced on the data and control buses. When connecting two drives, use a daisy-chain cable that has three 40-pin connectors. Connectors should be placed no more than six inches from the end of the cable. If only one drive is connected, it should be placed on the end of the cable. See Figure 5-3.

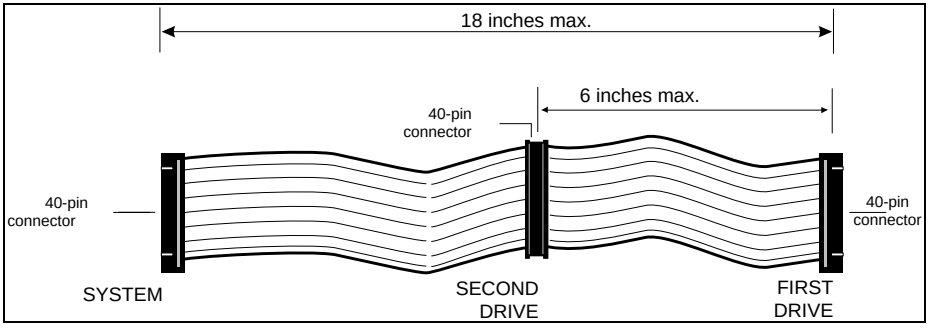

Figure 5-4. IDE Cable Connectors

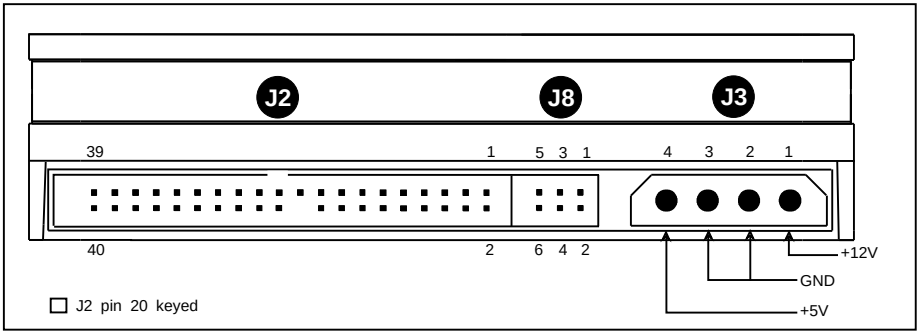

Figure 5-5. Standard Factory Connectors

Caution: You may damage the Caviar drive if the interface cable is not connected properly. To prevent incorrect connection, use a cable that has keyed connectors at both the drive and host ends. Refer to Figure 5-4 which shows pin 20 as the key. Pin 20 has been removed from the J2 connector. The female connector on the interface cable should have a plug in position 20 to prevent incorrect connection. Make sure that pin 1 on the cable is connected to pin 1 on the connectors.

The order in which you perform the following steps will vary depending on your system.

1. Attach the end of the 40-pin interface cable to the 40-pin J2 connector on the back of the Caviar hard drive as shown in Figure 5-4 and 5-5. For dual installations, connect the two drives together by using a three- connector interface cable. Match the orientation of pin socket 1 on the 40-pin IDE cable to pin 1 on the connector.
2. Thread the cable through the empty drive bay and slide in the Caviar drive.
3. Mount the Caviar drive in the drive bay using four 6-32 screws. Be sure to use the correct size screws. Do not install the screws past six threads (3/16 inch). Screws that are too long will damage the Caviar drive. For proper grounding be sure to use ALL four screws.

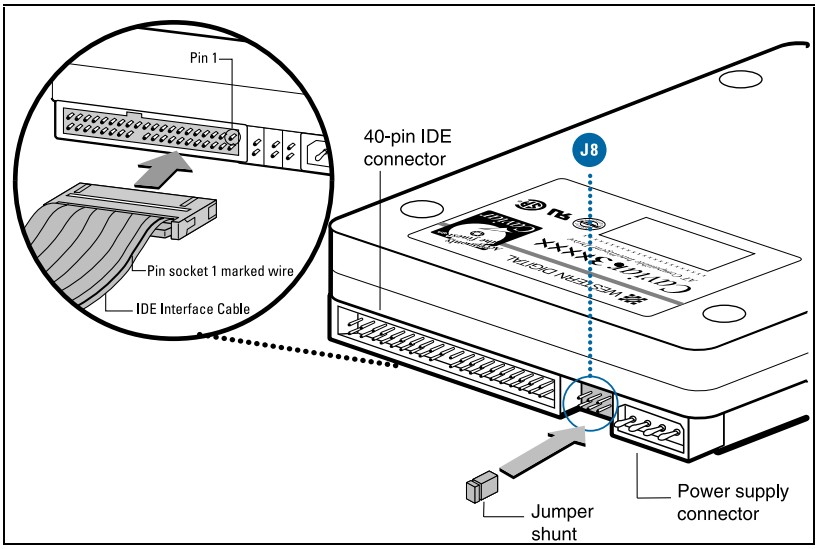

Figure 5-6. Caviar Connector Locations

Caution: Screws which are too long will damage board components. The screw must engage no more than six threads (3/16 inch.)

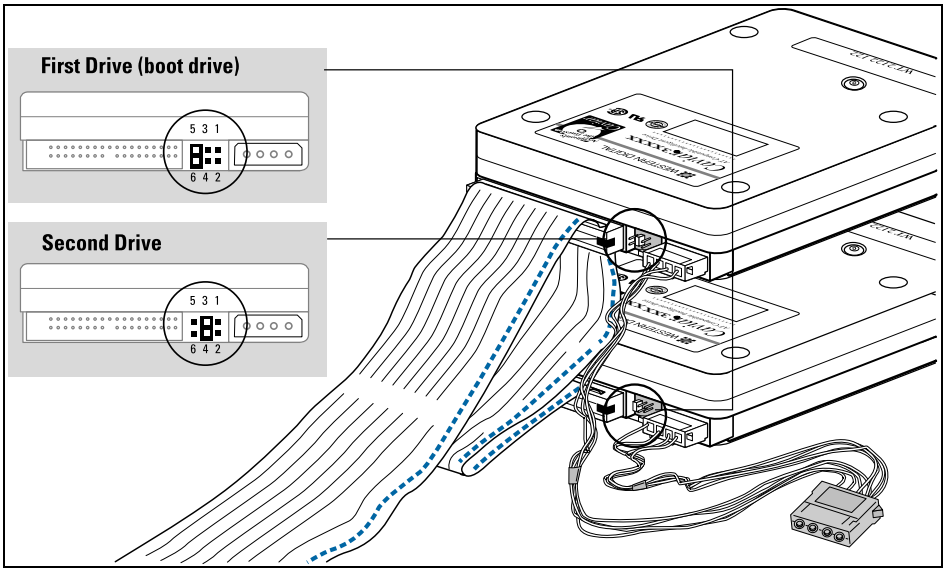

Figure 5-7. Caviar Dual Drive Cabling

4. Attach the computer's power supply cable to the 4-pin power connector J3 on the back of the Caviar drive (see Figure 5-4 and 5-5). The 4-pin connector is keyed to ensure proper insertion.

   Dual drive installations: If you do not have two internal power connectors, you will require a Y-adapter to provide power to both units. A Y-adapter can be obtained from your computer dealer or Western Digital technical support.

5. Attach the end of the 40-pin IDE cable from the Caviar hard drive to the IDE connector on the motherboard or controller card. Match pin socket 1 on the IDE cable to pin 1 on the motherboard or controller card. Figure 5-6 is an example of two Caviar drives cabled.

6. Check all cable connections. Replace the system cover according to the instructions provided in your system manual.

6. MAINTENANCE

The Caviar requires no preventative maintenance and contains no user-serviceable parts. The service and repair of the Caviar can only be performed at a Western Digital Service Center. Please Contact your Western Digital representative for warranty information and service/return procedures.

Observe the following precautions to prolong the life of the drive:

- Do not attempt to open the sealed compartment of the Caviar as this will void the warranty.
- Do not lift the Caviar by the printed circuit board.
- Avoid static discharge when handling the Caviar.
- Avoid harsh shocks or vibrations.
- Do not touch the components on the printed circuit board.
- Observe the environmental limits specified for this product.
- If it becomes necessary to move your computer system, turn off the power to automatically park the heads. Parking the heads moves them to a safe, non-data landing zone and locks them into place. This helps protect the media and the heads from accidental damage due to vibration while moving or shipping.
- To protect your data, back it up regularly. Western Digital assumes no responsibility for loss of data. For information about back-up and restore procedures, consult your operating system manual. There are also a number of utility programs available that you can use to back up your data.

7. WESTERN DIGITAL DEFECT MANAGEMENT UTILITY

All Caviar IDE drives are defect-free and low-level formatted at the factory, After prolonged use, any drive, including Caviar, may develop defects. If you continue receiving data errors in any given file at the DOS level, you can use the defect management utility WDAT_IDE.EXE to recover, relocate and rewrite the user data to the nearest spare sector and maintain a secondary defect list.

Caution: As with all format utilities, some options in the WDAT_IDE.EXE utility will overwrite user data.

8. TECHNICAL SUPPORT

You may download the Western Digital diagnostic utility WDAT_IDE from the Technical Support Bulletin Board if you have a modem.

To access the bulletin board, you require:

- A Hayes-compatible modem
- 2,400 to 28,800 Baud rate
- Format: 8 data bits, 1 stop bit, no parity

The Bulletin Board number is (714) 753-1234.

To gain access to the main menu and download this utility, follow these general steps:

1. Select S for Service and Support (drivers).
2. Select D for Downloadable Drivers.
3. Select H for Hard Drive Utilities
4. Specify WDAT_IDE.EXE.
5. To receive the software program, select CTRL-D and then transfer protocol.

On screen Help (?) is available if you have any problems. If you need additional assistance, contact Technical Support at (714) 932-4900.

9. APPENDIX

The following graphic illustrates the mechanical exploded view of the Caviar AC32100 and AC32500 drives.

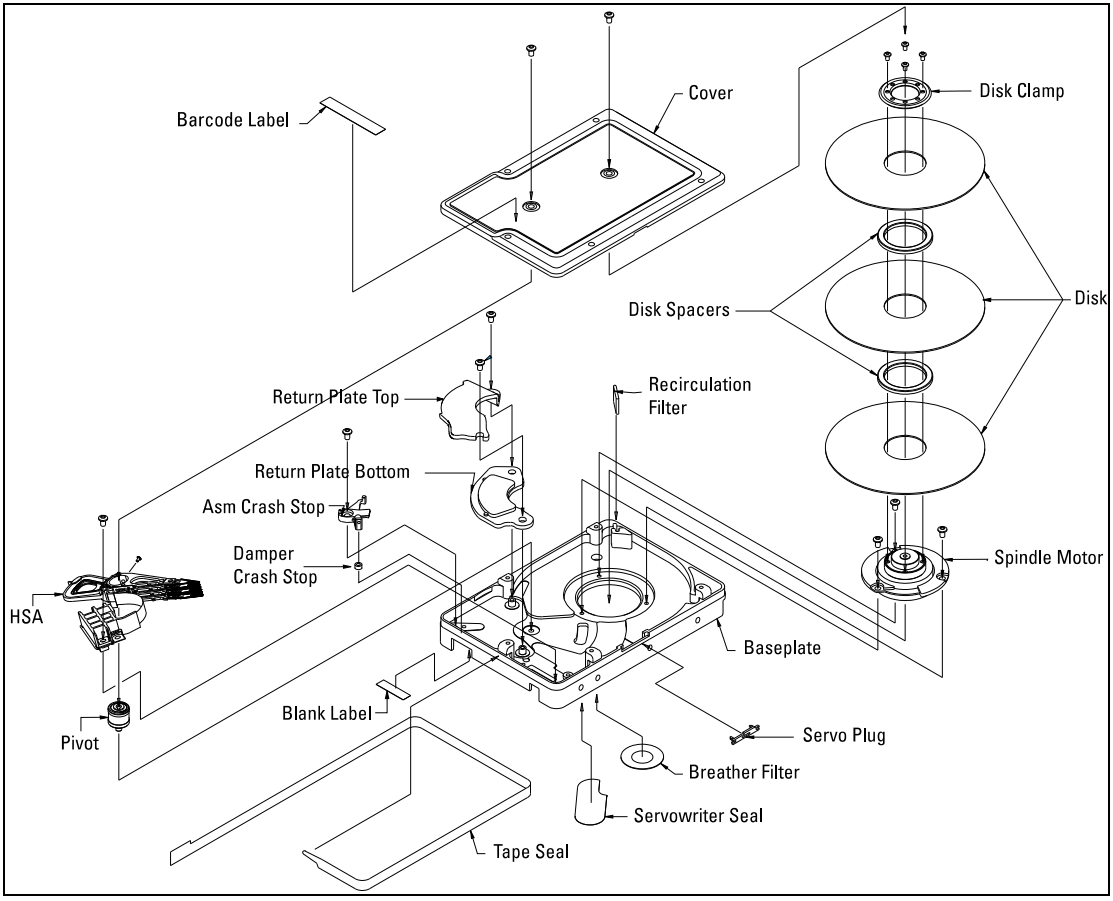

Figure 9-1. Caviar AC32100 and AC32500 HDA Assembly Drawing

10. GLOSSARY

AT Bus Attachment (ATA-2) -The interface defined by International Business Machines for the original AT disk controller. Western Digital designed the Caviar drives to be fully ATA-2 compatible.

Auto Defect Retirement - If defective sectors are found during a read or write, they are automatically mapped out and relocated.

Auto Park - Turning off the drive's power causes the Caviar drives to move the read/write heads to a safe non-data landing zone and locks them in place.

Average Seek Time - Length of time it takes the drive to move the read/write heads to a safe non-data landing zone and lock them in place.

Block - A group of bytes handled, stored, and accessed as a logical data unit, such as an individual file record.

Buffer - A temporary data storage area that compensates for a difference in data transfer rates and/or data processing rates between sender and receiver.

Correctable Error - An error that can be overcome by the use of Error Detection and Correction schemes.

Customer Configuration Code (CCC) - The CCC is located on the product label attached to the drive. The CCC is revised only when there are drive form, fit, or function changes.

Data Synchronizer = An electronic circuit that produces a clock signal that is synchronous with the incoming data stream. The clock signal is then used to decode the data.

Data Transfer Rate - The rate that digital data is transferred from one point to another, expressed in bits per second or bytes per second.

- Data Transfer Rate to Disk: The internal disk transfer rate in Mbits per second.
- Data Transfer Rate from the Buffer to the Host: Based on the transfer of buffered data in MB per second.

Dedicated Landing Zone - A designated radial zone on the disk chosen to avoid contact with the data cylinders, where contact starting and stopping occur by design.

Defect Free - A term used to describe recording surfaces that have no detectable defects.

Defect Management - A general methodology of eliminating data errors on a recording surface by mapping out known bad areas of the media.

Disk Transfer Rate - Speed at which data is transferred to and from the disk media (actual disk platter) and is a function of recording the frequency. Typical units are bits per second (BPS), or bytes per second. Modern hard drives have an increasing range of disk transfer rates from the inner diameter to the outer diameter of the disk. This is called a “zoned” recording technique.

ECC On-the-Fly - A hardware correction technique that corrects errors in the read buffer prior to host transfer without any performance penalties. These error corrections are invisible to the host system because they do not require assistance from the drive's firmware.

Embedded Servo Control - The embedded servo control concept generates accurate feedback information to the head position servo system without requiring a full data surface (which is required with a “dedicated” servo control method).

Enhanced IDE (EIDE) - Expands upon an industry accepted standard to meet the needs of improved processor speeds and bus technologies. It improves device support, provides greater than 528 MB capacity, increases data transfer rates, and provides support for non-hard drive peripherals (i. e. CD-ROMS).

Error Correction Code - A mathematical algorithm that can detect and correct errors in a data field by adding check bits to the original data.

Error Rate - The number of errors of a given type that occur when reading a specified number of bits.

FIT (Functional Integrity Testing) - A suite of tests Western Digital performs on all its drive products to ensure compatibility with different hosts, operating systems, application programs, and peripherals. This testing must be performed before the product can be released to manufacturing.

Flow Control - The ability of the drive to control the speed at which the host transfers data to or from the drive by using the IORDY signal. The host temporarily stops transferring data whenever the drive deasserts the IORDY signal. When the drive reasserts the IORDY signal, the host continues the data transfer.

Formatted Capacity - The actual capacity available to store data in a mass storage device. The formatted capacity is the gross capacity minus the capacity taken up by the overhead data required for formatting the media.

GB (Gigabyte) - Western Digital defines a gigabyte as 1,000,000,000 bytes.

Hard Error - An error that cannot be overcome by the error recovery process.

Hard Sectored - A technique that uses a digital signal to indicate the beginning of a sector on a track.

Host Transfer Rate - Speed at which the host computer can transfer data across the EIDE interface. Processor Input/Output (PIO) modes and Direct Memory Access (DMA) modes are defined in the ATA-2 industry specifications.

Index Pulse Signal - A digital pulse signal indicating the beginning of a disk revolution. An embedded servo pattern or other prerecorded information is present on the disk following index.

Landing Zone - The heads move to this location on the inner cylinders following a Park command. User data is not stored at this location.

Latency - The period of time that the read/write heads wait for the disk to rotate the data to an accessible position. For a disk rotating at 5200 RPM, the average latency is 5.8 milliseconds.

Logical Address - A storage location address that may or may not relate directly to a physical location. The logical address is usually used when requesting information from a controller. The controller performs a logical-to-physical address conversion and retrieves the data from a physical location in the storage device.

Logical Block Address - An alternative addressing methodology of identifying a given location on an EIDE drive that permits disk sizes greater than 528 MB.

Mechanical Latencies - Include both seek time and rotational latency. Mechanical latencies are the main hindrance to higher performance in modern EIDE hard drives. The time delays of mechanical latencies are one hundred times higher than electronic (non-mechanical)latencies associated with the transferring of data. Therefore, reducing mechanical latencies (a lowering of seek time and rotational latency) should be the top consideration in improving hard drive performance. *See also* Seek Time, Rotational Latency.

MB (Megabyte) - Western Digital defines a megabyte as 1,000,000 bytes.

MTBF (Mean Time Between Failures) - Average time (expressed in hours) that a component works without failure. It is calculated by dividing the total number of operating hours observed by the total number of failures. Also, the length of time a user may reasonably expect a device or system to work before an incapacitating fault occurs.

MTTR - Mean Time to Repair.

PRML (Partial Response Maximum Likelihood).- A read channel using sampled data, active equalization and Veterbi detection to accurately retrieve the user data off the disk.

Rotational Latency - The amount of delay in obtaining information from a disk drive that can be attributed to the rotation of the disk. For a disk rotating at 5200 RPM, the average rotational latency is 5.76 milliseconds. *See also* Mechanical Latency.

RPM (Revolutions per Minute) - Rotational speed of the media (disk), also known as the spindle speed. Hard drives spin at one constant speed. The slower the RPM, the higher the mechanical latencies. Disk RPM is a critical component of hard drive performance because it directly impacts the rotational latency of the disk transfer rate.

Sector - A 512-byte packet of data.

Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.) - A technology to assist the user in preventing possible system down time due to hard drive failure.

Servo Burst - Provides positioning information to the actuator arm, usually positioned between sectors or at the end of a track.

Soft Error - A data error that can be overcome by the error recovery process.

Soft Sectored - A technique that allows the controller to determine the beginning of a sector by reading the format information from the disk.

Task File - The set of I/O Host Interface Registers used to transfer status, commands, and data between the host and the drive.

Unrecoverable Error - A read error that cannot be overcome by an ECC scheme or by rereading the data when host retries are enabled.

Write Cache - A feature in CacheFlow4 that posts “command complete” prior to completing the actual write.

Zoned Recording - Increases the data density on the outer tracks of the drive where most of the sectors are located. This type of recording affords more disk capacity because there can be more sectors on the larger outer tracks than would be possible if the number of sectors per track were constant for the whole drive.

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