



Getting Results: eCache on a PC Platform

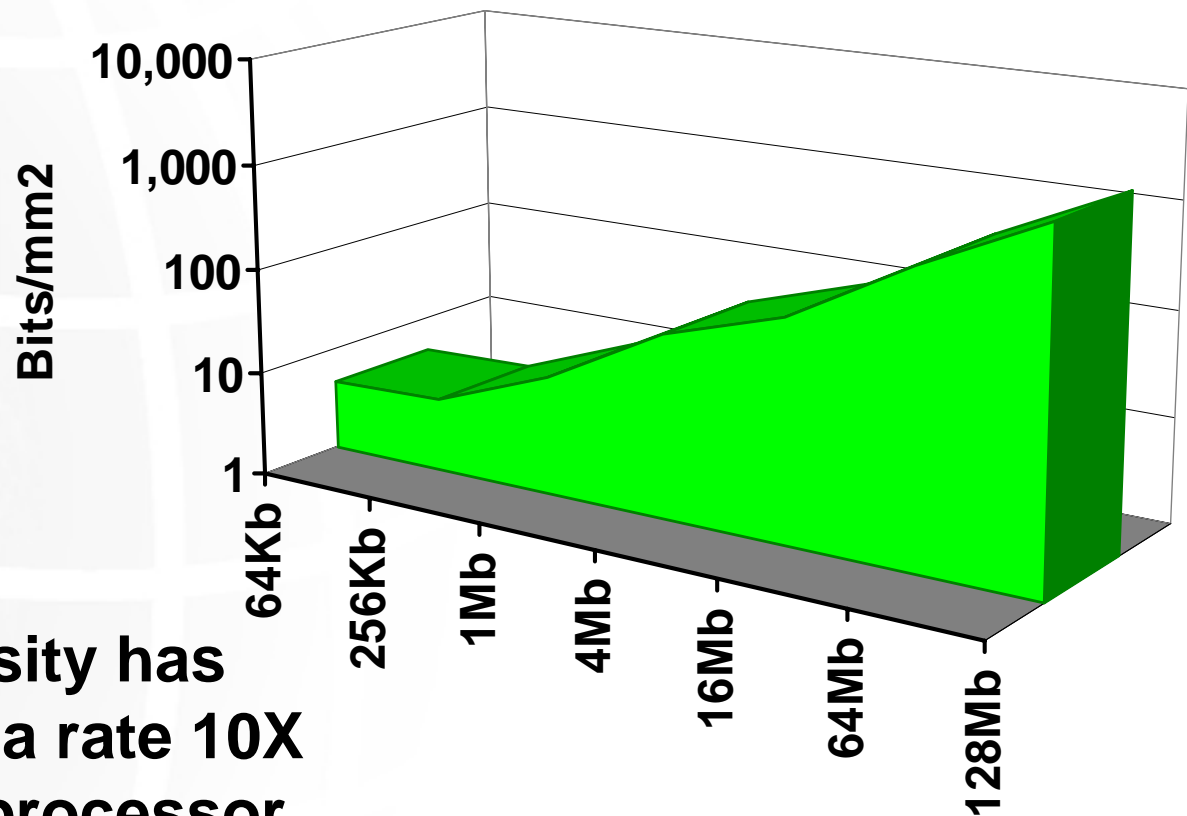
Dean A. Klein
V.P. Integrated Products
Micron Technology, Inc.



MICRON



Memory Directions



Memory density has increased at a rate 10X over that of processor performance in the past 20 years



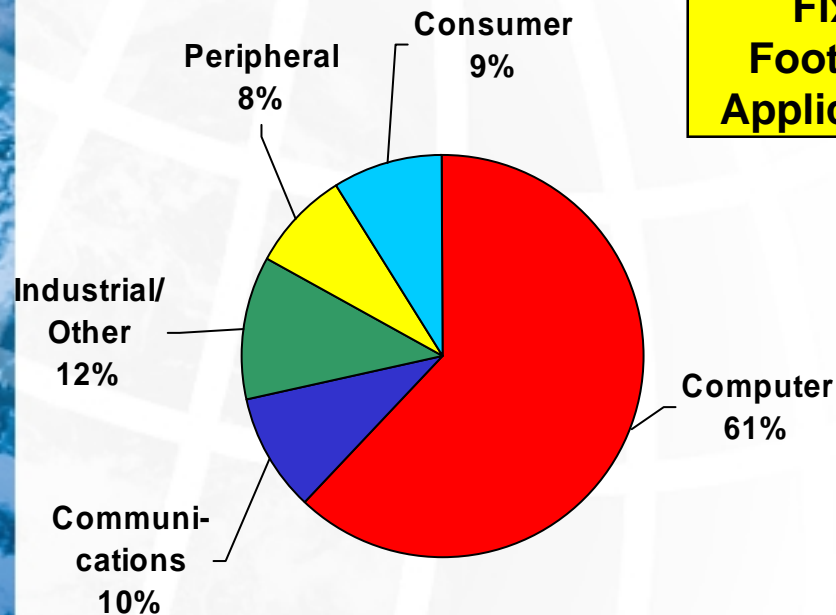
Source: Micron Technology, Inc.

MICRON



Memory Directions

1999 – \$20.7 Billion



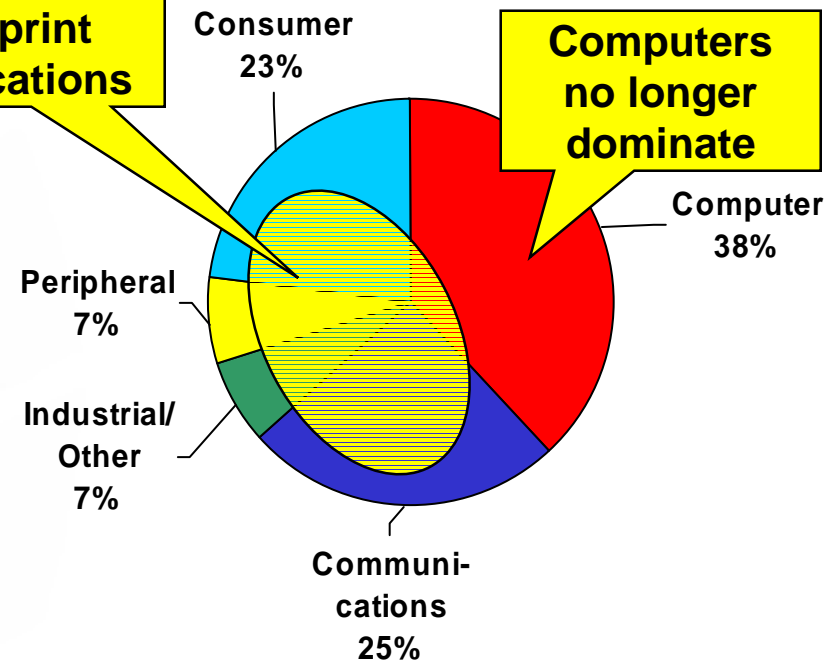
Computer – Desktop PCs, workstations, laptops, servers, etc.

Peripherals – Printers, copiers, monitors

Consumer – Camcorders, digital cameras, DVDs, set-top boxes, TVs, etc.

2004F – \$77.9 Billion

Fixed Footprint Applications



Communications – Switches, routers, LAN, hubs, cellular phones, modems, etc.

Industrial/Other – Robots, test equipment, medical equipment, automotive equipment (diagnostic equipment), GPS, and military equipment

Source: Semico Research, 1/00

MICRON



Micron eDRAM Approach

Logic + Memory

VS.

Memory + Logic

○ Memory-Centric Approach

- Greater density
- Lower cost
- Reasonable performance
- Lower power

○ Logic-Centric Approach

- Lower density
- Higher cost
- Logic-type performance





Current North Bridge Component

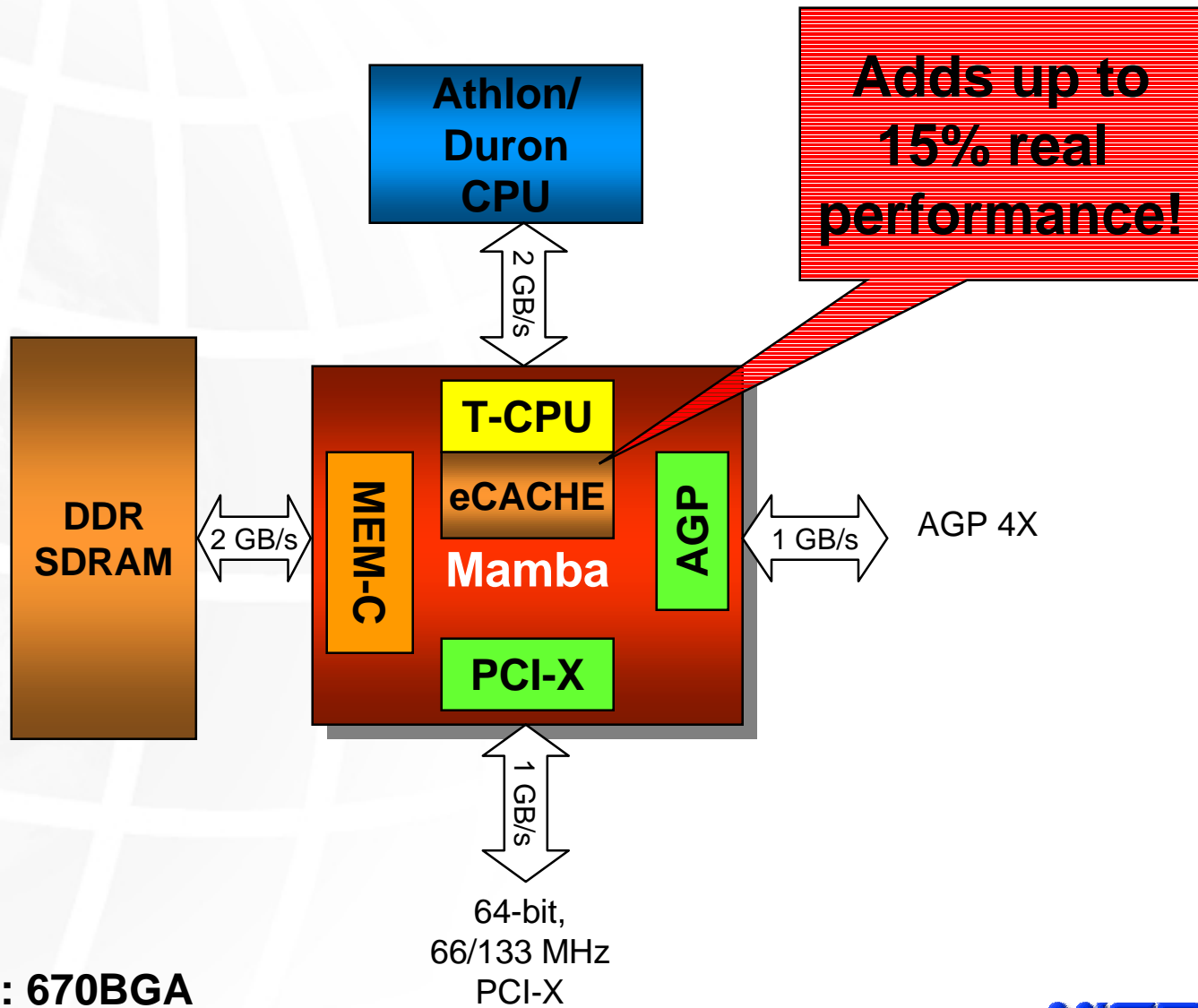
Wasted silicon wastes money!



What can we do?
eCACHE!

MICRON

Mamba



Package: 670BGA

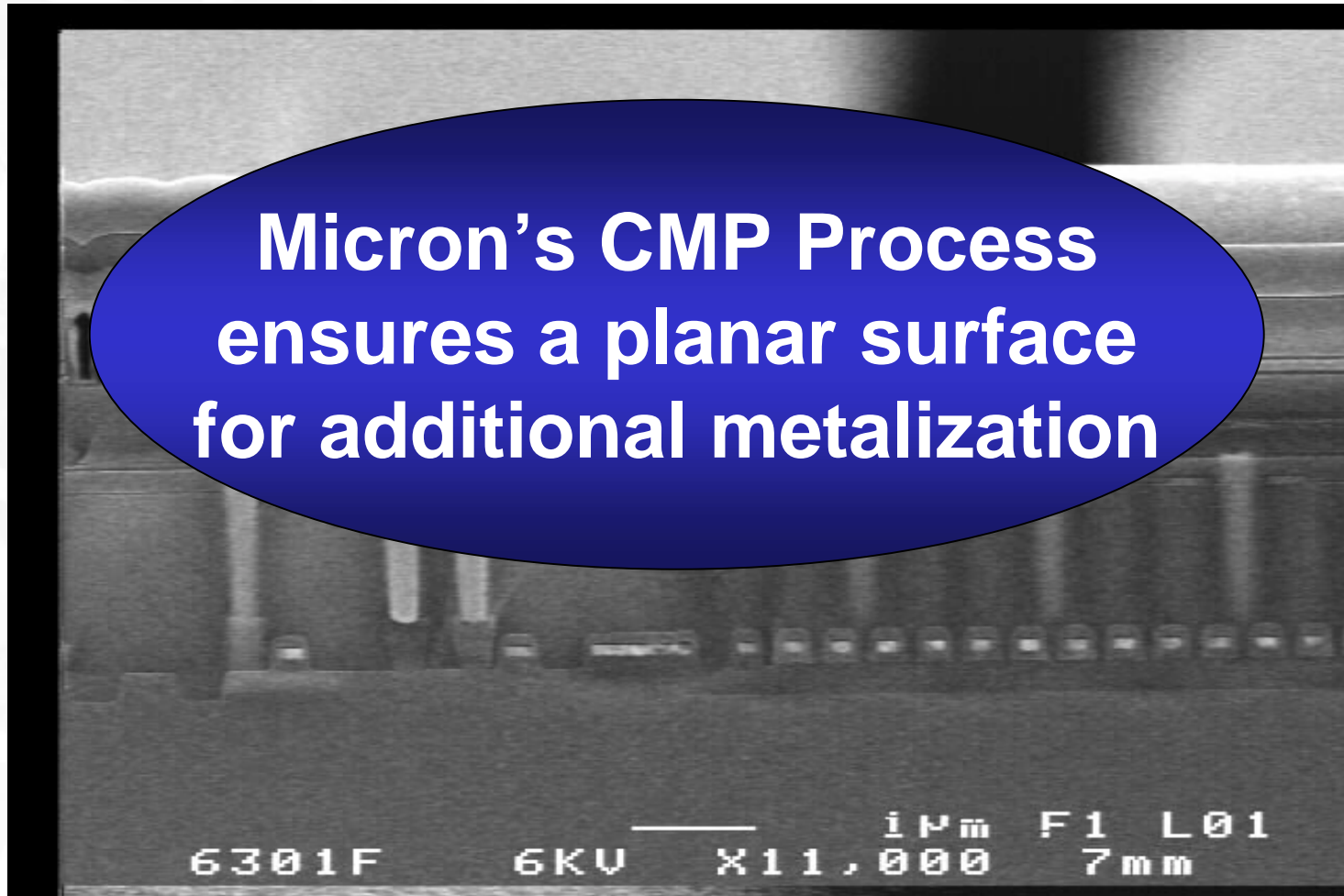


MICRON



Micron Array Edge

**Micron's CMP Process
ensures a planar surface
for additional metalization**

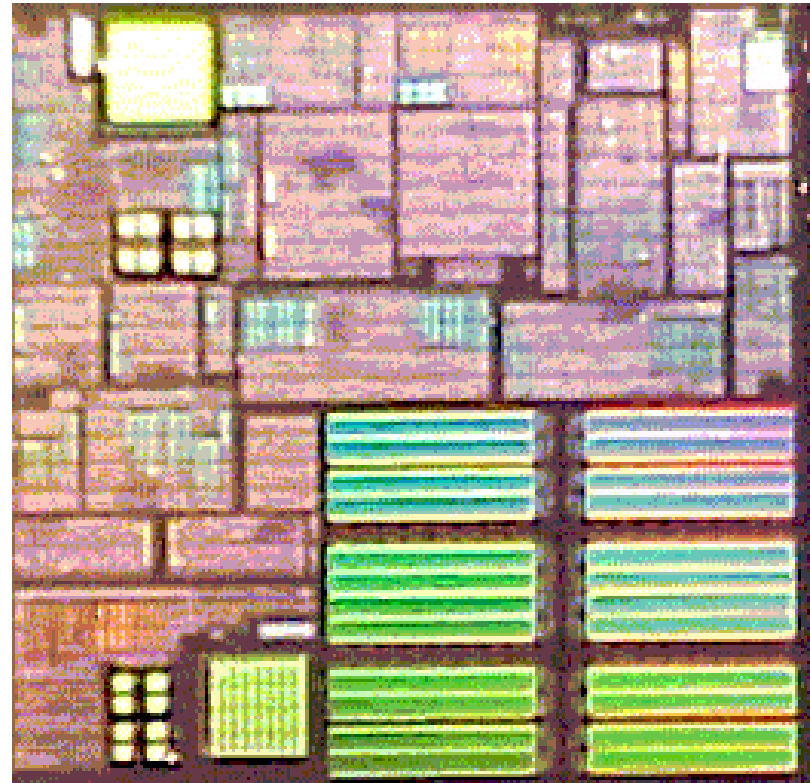


MICRON



Micron eDRAM: V4400e Statistics

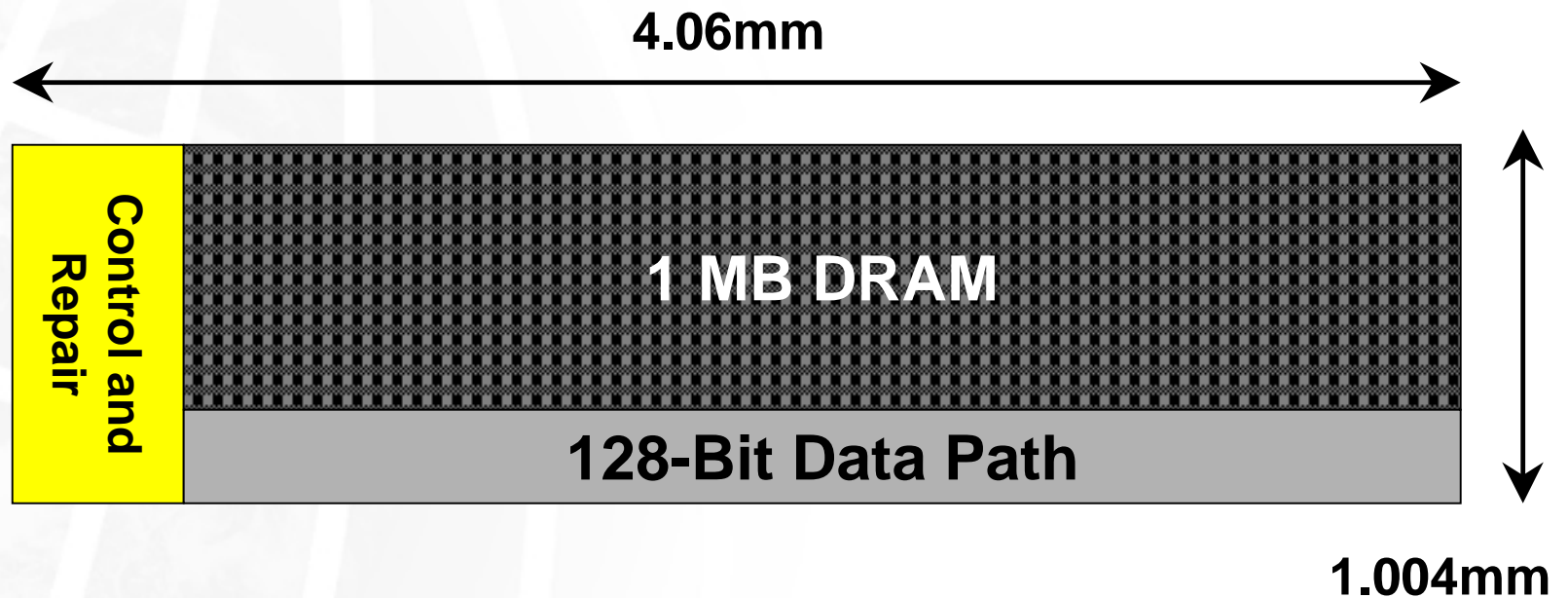
- The NVIDIA GeForce has 23M transistors
- The Intel P-III has 28M transistors
- The Intel P-4 has 42M transistors
- **V4400: Over 125M transistors!**



MICRON



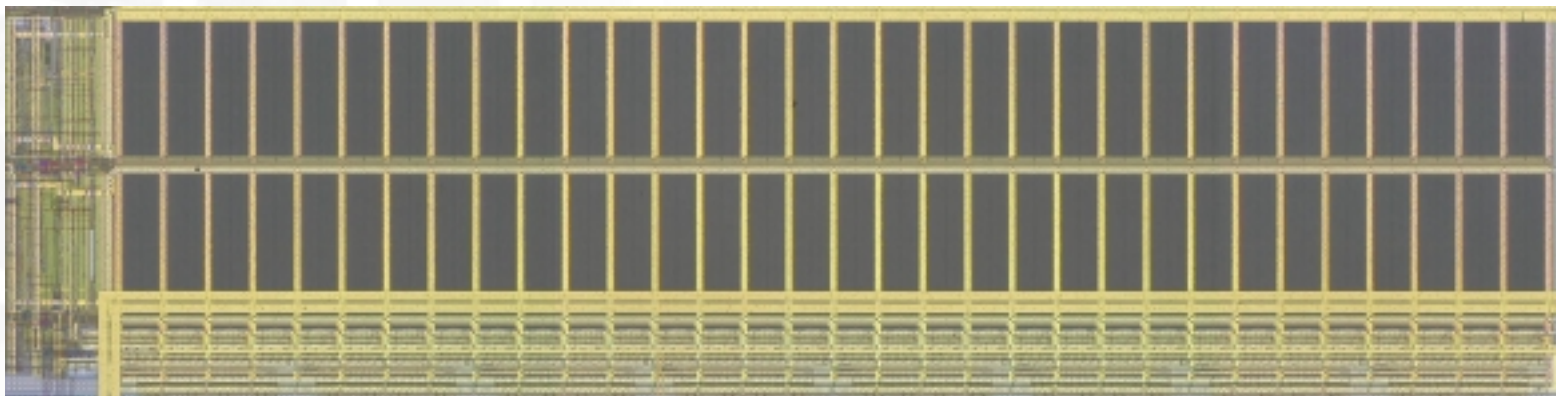
Micron's 1MB Core



MICRON



Micron's 1MB eDRAM Core

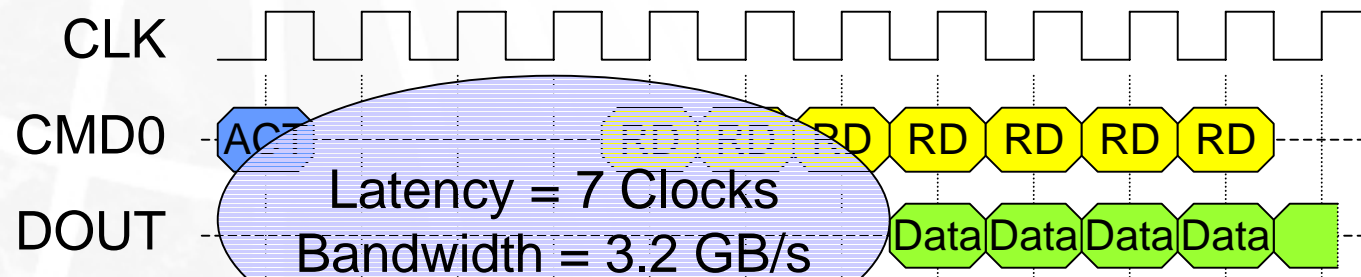


MICRON

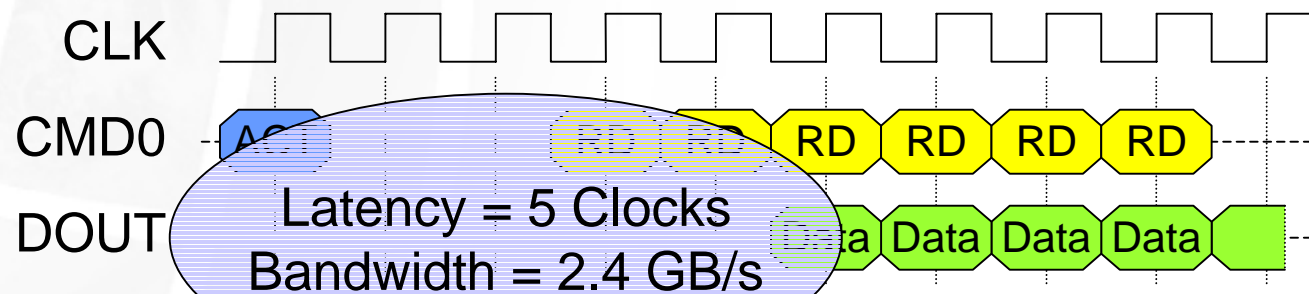


eDRAM Access

○ Standard eDRAM core

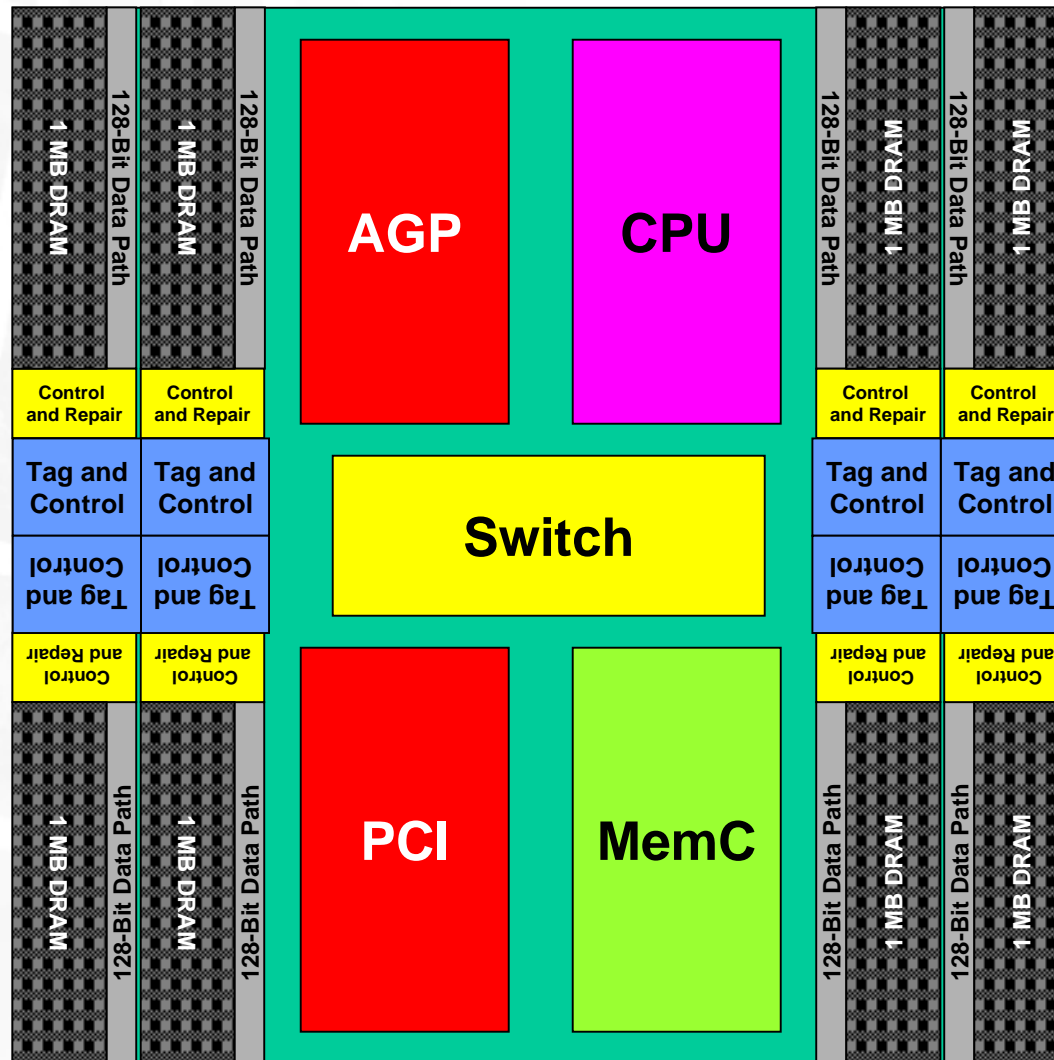


○ Mamba-enhanced eDRAM core





Mamba eCache





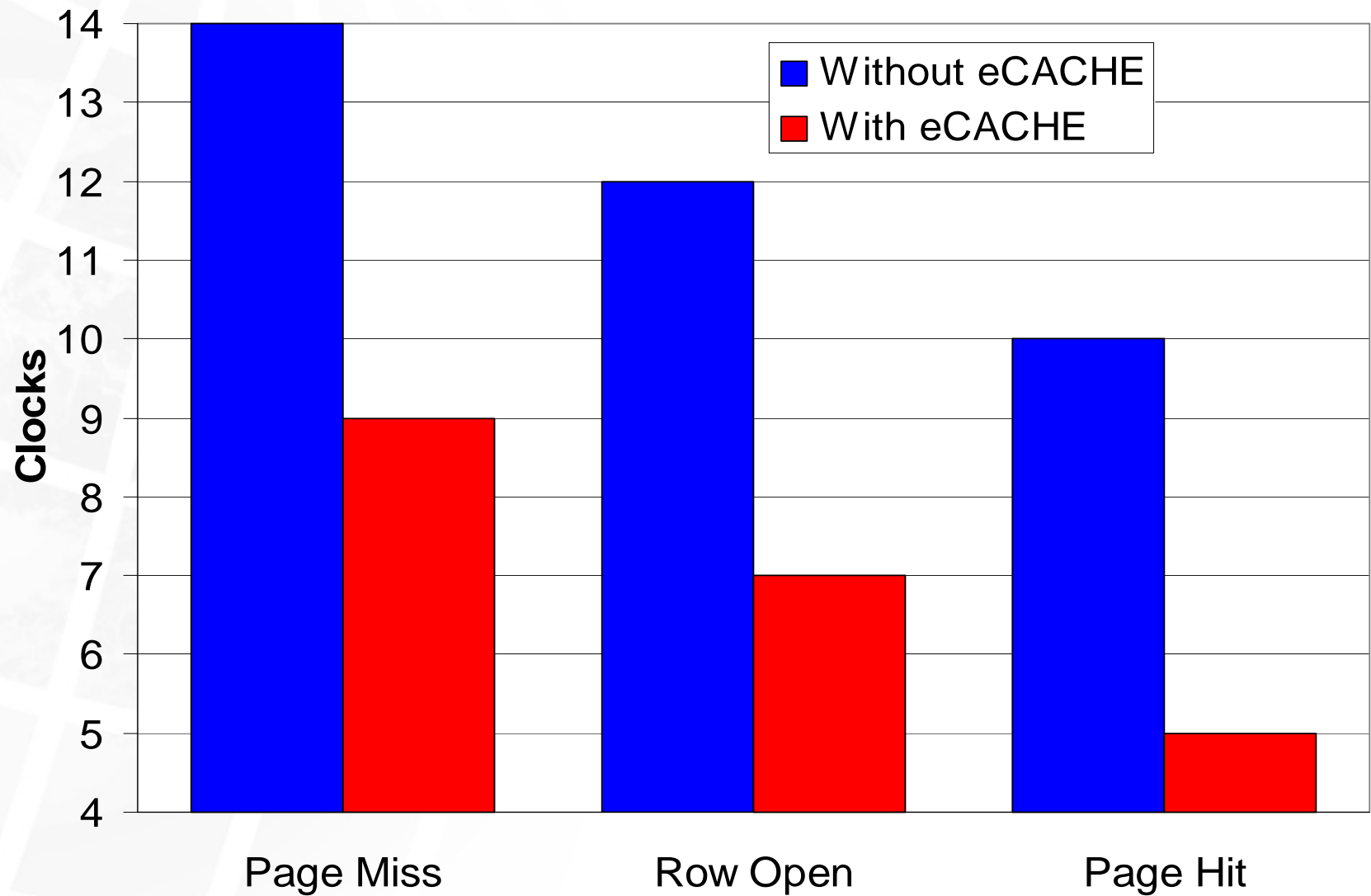
eCache Bandwidths

- eDRAM aggregate bandwidth is limited only by die size
- eCache aggregate eDRAM burst bandwidth is over 19 GB/s
- As implemented, allows simultaneous access to four arrays and four device ports, with a sustainable bandwidth from memory of 9.6 GB/s
- Command, access, refresh and precharge times can be overlapped, allowing sustained 9.6 GB/s





eCache Latency



(DRAM shown with 2-2-2 timing, 3-3-3 is worse)



MICRON



Micron eDRAM eCache

- **Embedded DRAM can be built cost effectively**
- **Embedded DRAM can improve performance both on-chip and off chip**
- **Embedded DRAM granularity allows size to be tailored to fit application**
- **Architectural decisions made with eCache allow low latency and high bandwidth**
- **Core logic architecture allows maximum utilization of eCache**





WWW.MICRONSEMI.COM



MICRON