

96x64 Polymer Light Emitting Graphics Display *Preliminary Specification*

Features

X,Y Passive addressing
Low voltage, low current operation
Bright, sun light readable
High contrast, large viewing angle
Large pixel area emission



General Description

The 96x64 Polymer Display is a thin, lightweight emissive alternative to a conventional backlit LCD display. The device is a simple sandwich-type structure, the active polymer layer lies between a semi-transparent column anode (96) and a back row cathode (64). Uniform emission is over the entire active pixel and the device is passive addressable for easy interface to multiplexed current drivers. A protective layer and cap keep the display sealed against environmental damage.

Typical Drive Parameters

Average Luminance ⁽¹⁾	200 cd/m ²
Pixel Forward Current (peak) ⁽¹⁾	0.10 mA
Forward Voltage (peak) ⁽¹⁾	6.5 V
Average Power Dissipation ^(1,2)	15 mW
Operating Temperature range	-40 to 85C

Notes:

- 1) Duty cycle of 1/64 at 200 Hz frame refresh rate. STP and humidity conditions.
- 2) 25% pixels on

Typical Characteristics

Mechanical Specifications

Parameter		Unit	Comments
Pixel Matrix	96 columns x 64 rows		Horizontal x Vertical
Pixel size	0.25 x 0.30	mm	
Pixel pitch	0.30 x 0.35	mm	
Fill factor	0.71		
Total Active Area	28.75 x 22.35	mm	
Overall dimensions	38.70 x 36.62	mm	
Icons	8		battery, power, clock, face, lock, phone, antenna, envelope
Icon Emissive Area (average)	2.0	mm ²	
Icon Area (total)	28.7 x 3	mm	located at bottom of pixel matrix
Display Contacts	169		icons are common cathode
Contact material	ITO		See package layout
Pad size	0.185 x 3.0	mm	See package layout
Pad pitch	0.30	mm	
Display thickness	2.0	mm	
Display weight	7.2	g	

Optical Specifications (see note)

parameter	min	typ	max	units	comments
Pixel Luminance		200		cd/m2	display average
Peak emission frequency		556		nm	yellow-green
Emission frequency range		525-620		nm	½ max intensity
Pixel color coordinates		0.213, 0.566			u', v' (CIE 1976)
Dark room contrast		> 1: 100			
Daylight contrast					
Viewing angle uniformity	>140			degree	
Local uniformity	1.1				
Non-local uniformity	1.3				across display

Note: optical measurements taken at 1/64 duty, 200 Hz

General Electrical Specifications

parameter	min	typ	max	units	comments
Luminance efficiency	7	10	12	cd/A	DC
Quantum efficiency				%	
Pixel Luminance efficiency		~2080		cd/m ² /mA	at 1/64 duty, 200 Hz
Voltage Temperature coefficient		- 4.0		mV/C	constant current
Column Track resistance			1.1	k Ω	
Row Track resistance			15	Ω	
Row contact resistance		2		Ω	
Pixel capacitance		25		pF	
Column capacitance		~ 1.3		nF	
Row capacitance		~ 2.7		nF	
Polymer switching speed		40		ns	Intrinsic
RC delay / rise time		~ 1.4		μ sec	All pixel in row
Reverse Voltage Breakdown		> 20		V	
Rectification Ratio		~ 5000			Current ratio at +/- 7V

Pulsed Electrical Specifications (see note)

parameter	min	typ	max	units	comments
Forward Current		0.10		mA	
Forward Voltage		6.5		V	initial
Emissive Power consumption		15		mW	average, 25% pixels on
Maximum Row current		10		mA	peak, 100% pixels on

Note: Pulsed measurements taken at 1/64 duty, 200 Hz refresh rate.

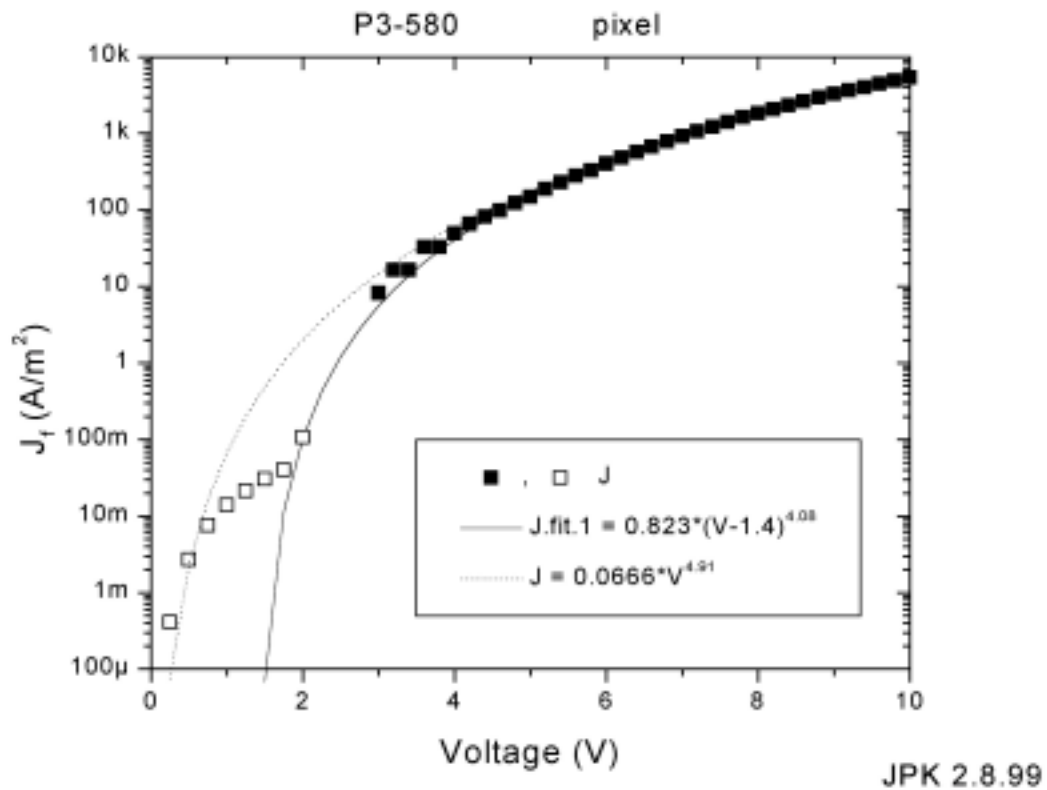


Figure 2. Typical pixel forward current – voltage characteristic in DC. Emission turn-on is about 1.8V.

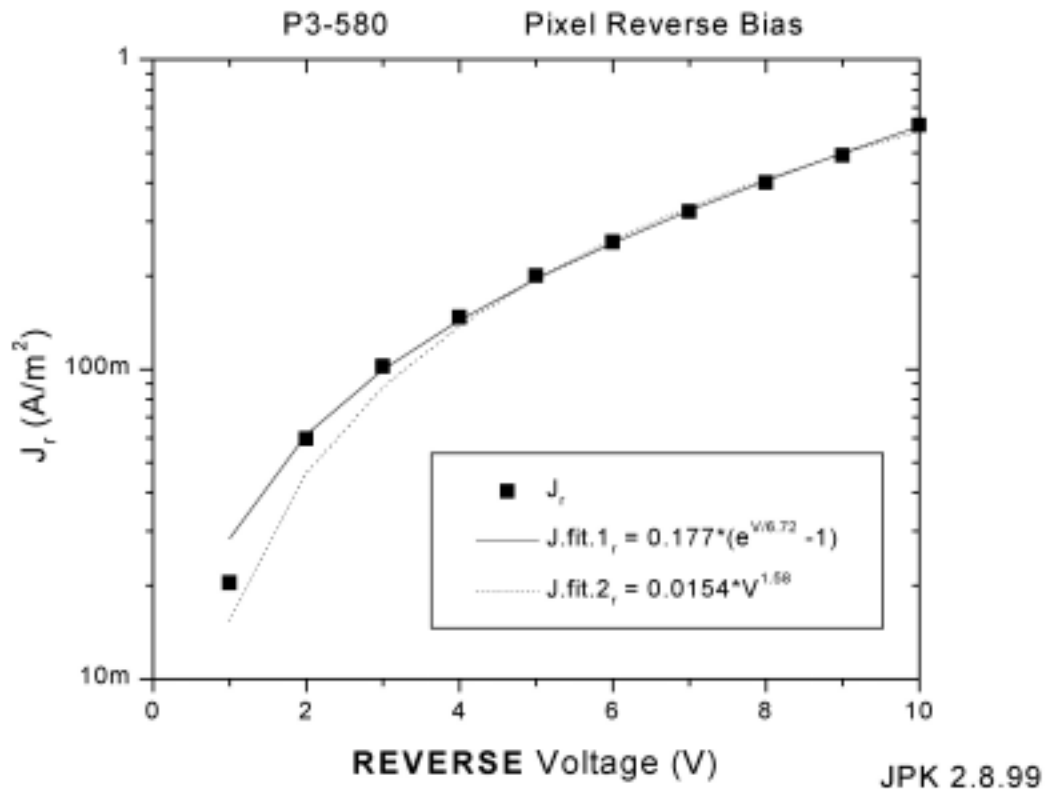
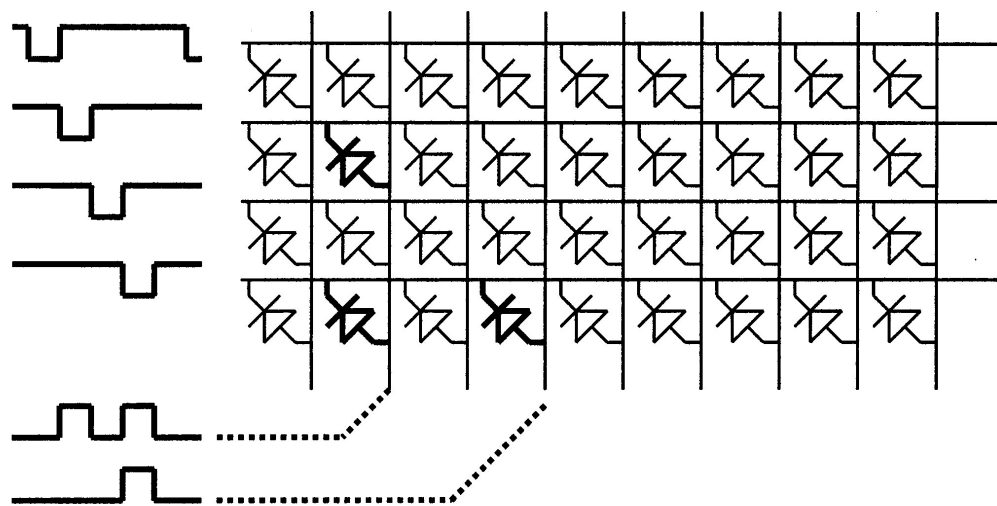


Figure 3. Typical pixel reverse current – voltage characteristic in DC. Reverse breakdown occurs at greater than 20 V.

Theory of Operation

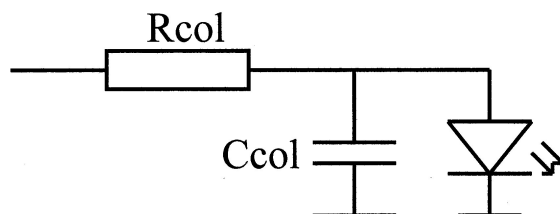
Uniax displays utilize the unique semiconductor properties of conjugated polymer chains. The polymer chains conduct in one dimension with weak link transport between chains. It is useful to think of the conduction properties of Uniax polymers as semiconductor-like, with an energy gap of roughly 2V. By matching the energy injection levels for the holes and electrons, a simple diode can be formed by sandwiching the polymer between metal anode and cathode. Above the threshold voltage, recombination causes uniform emission of light throughout the entire active region. To create an addressable display, the anodes and cathodes are structured in a grid array pattern. Finally the bare display is sealed and capped for chemical and mechanical integrity.

Functional Block Diagram



X,Y Passive Addressing Scheme.

Pixel Equivalent Circuit



$$R_{col} = 15 \, \Omega/\text{Sq}$$

$$C_{col} = 35 \, \text{nF} / \text{cm}^2$$

[illegible]

The diagram illustrates the system architecture for the Hitachi HD61830B LCD Graphics Controller. The central component is the **Hitachi HD61830B LCD Graphics Controller**. It interfaces with several external components:

- 8-bit MPU**: Connected via an 8-bit data bus (D0-7) and control signals E, RS, and RW.
- VRAM**: Connected via a 16-bit address bus (MA0-15) and an 8-bit data bus (MD0-7). Control signals WE and OE are also shown.
- Column Driver**: Receives control signals FLM and CL1 (2 lines) and power supplies Vpp and Vdd.
- Row Driver**: Receives control signals D1, CL1, and CL2 (3 lines) and power supply Vpp.
- PLED Display**: The output device, connected to the Column and Row Drivers.
- Power Converter**: Converts a 3-5V input to provide Vpp and Vdd for the other components.