

Introducing . . .

ACCEL *EDA*

Electronic
Design
Solutions
From
ACCEL Technologies

Press Spacebar to move forward, Esc to exit.

Viewing this presentation

You can view this PowerPoint presentation on ACCEL EDA at your own pace.

To move forward, press Spacebar

To move backward, press Backspace, or

To move forward, click LeftMouse

To move backward, click RightMouse

To exit at any time, press Escape

For best results, view at 800x600 SVGA

The Tour Schedule

About ACCEL Technologies
Today's Design Concerns
The ACCEL EDA Series
ACCEL EDA Highlights

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ACCEL *EDA*

About ACCEL Technologies

Founded in 1983 in San Diego, California

Entered the EDA business in 1986

Introduced Tango Series II 1988

Shipped TangoPRO for Windows in 1993

Acquired Omation in 1994, P-CAD in 1995

Introduced ACCEL EDA in 1996

We develop and market design tools to meet the present and future needs of engineering professionals worldwide who share our passion for innovation, excellence and exceptional value.

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ACCEL **EDA**

Today's Design Concerns

Software Usability

Power

Correct by Design

Manufacturability

Inter-operability

Usability

ACCEL EDA's user interface includes productivity enhancing shortcuts & features, and is configurable to your particular needs.

Status Line Editing

Speedy Query/Edit

Sub-selection

Shortcuts

Part and Component Browse

Hierarchical Design Rules

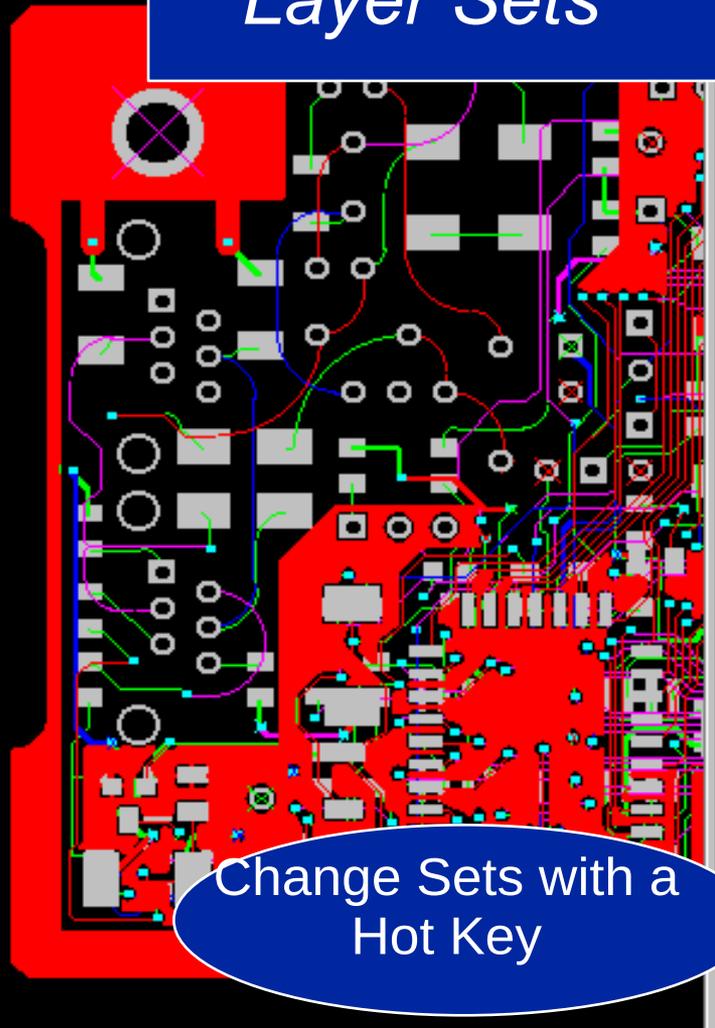
True Type Fonts

Layer Sets

Pad/Layer Ordering

Network licensing

Layer Sets



Change Sets with a Hot Key

Options Layers

Current Layer: Top Assy

Layers:

- Top Assy
- Top Silk
- Top Paste
- Top Masl
- Top
- Ground
- INT1
- INT2
- Power
- Bottom
- Bot Mask
- Bot Paste
- Bot Silk
- Bot Assy
- Board
- REF
- FAB
- Title
- ManualDim

Set Name: Top Assy

Layer Sets:

- gnd
- pwr
- solder
- alltrace
- Top Assy
- Bot Assy
- Fab

Set Contents:

- Top Assy
- Top Silk
- Board
- Top Paste
- Title

Buttons: New, Add ->, <- Remove, Enable Layers, Close

Add your own Layer Combinations

Modify Hole Range for easy Blind / Buried Via support

Options Modify Via Hole Range

Styles:	Hole Range Layers:
(Default)	Top
25R15	Ground
Buried Int1_Int2	INT1
Blind Top_Gnd	INT2
Blind Pwr_Bot	Power
Blind Top_Int2	Bottom

OK Cancel

Just pick the layer range

See the change

Power

ACCEL EDA is packed with features to tackle the most demanding designs.

Copper Pour

Split Plane Support

Shape-based

Interactive Routing

QuickRoute

Blind & Buried Vias

Orthogonal Modes

Abutment Routing

Pin and Gate Swapping

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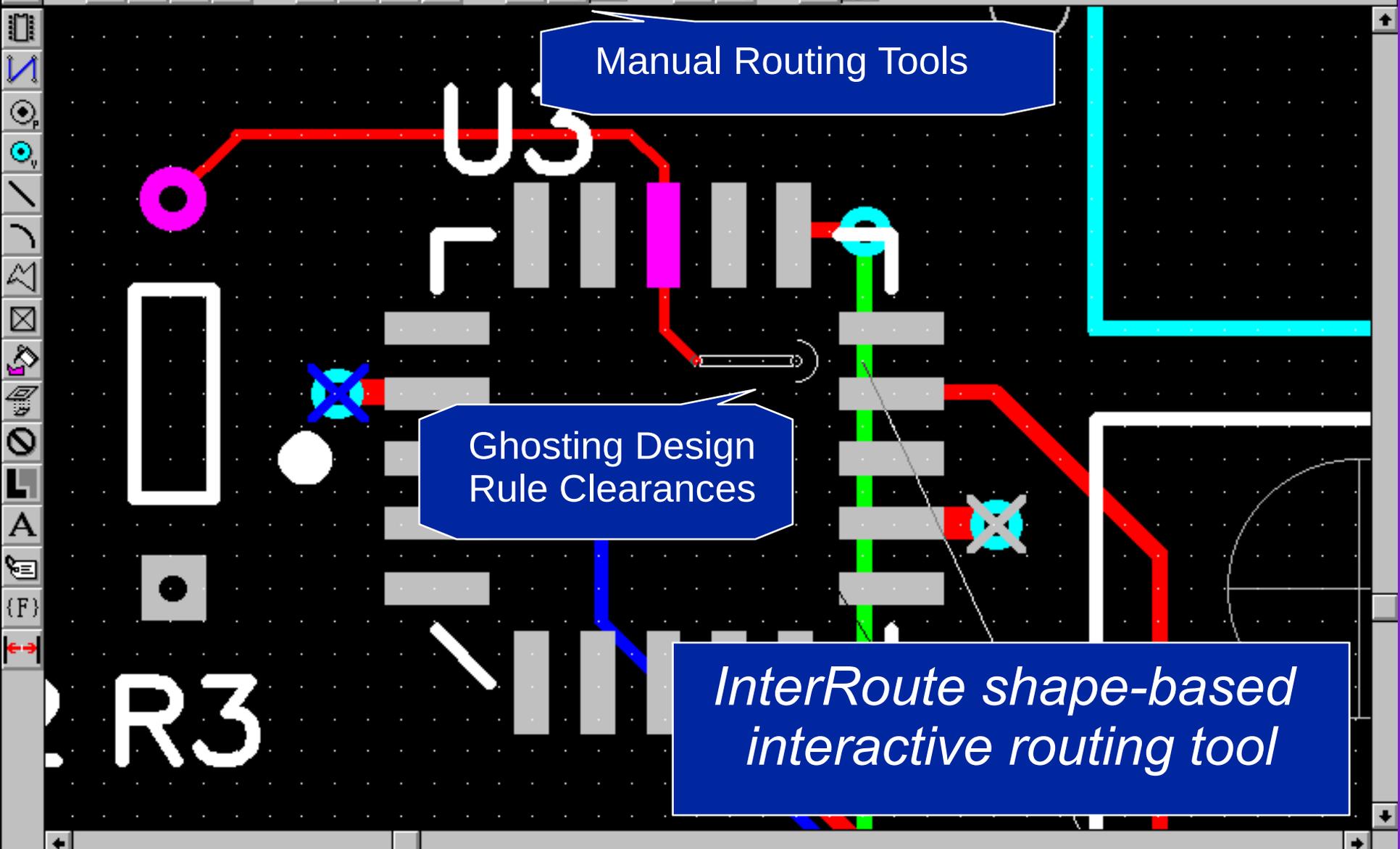
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Manual Routing Tools

Ghosting Design Rule Clearances

InterRoute shape-based interactive routing tool



SPECCTRA Router from Cooper & Chyan

Route Autorouters

Autorouter: SPECCTRA [v] Start Restart Close

Strategy

DO File [v] Output PC [v] Output Lo [v] Load [v]

Do File

DO Wiza [v] Edit as I [v]

Easy SPECCTRA command selection

SPECCTRA DO File Wizard

DO Commands: protect [v] Apply To: all wires [v]

Edit DO File

```

00000
th 8.0

clean 4
route 50 16
clean 4
filter 5
route 100 16
clean 2
delete conflicts
#
write wire $VROUTE.w
spread
miter

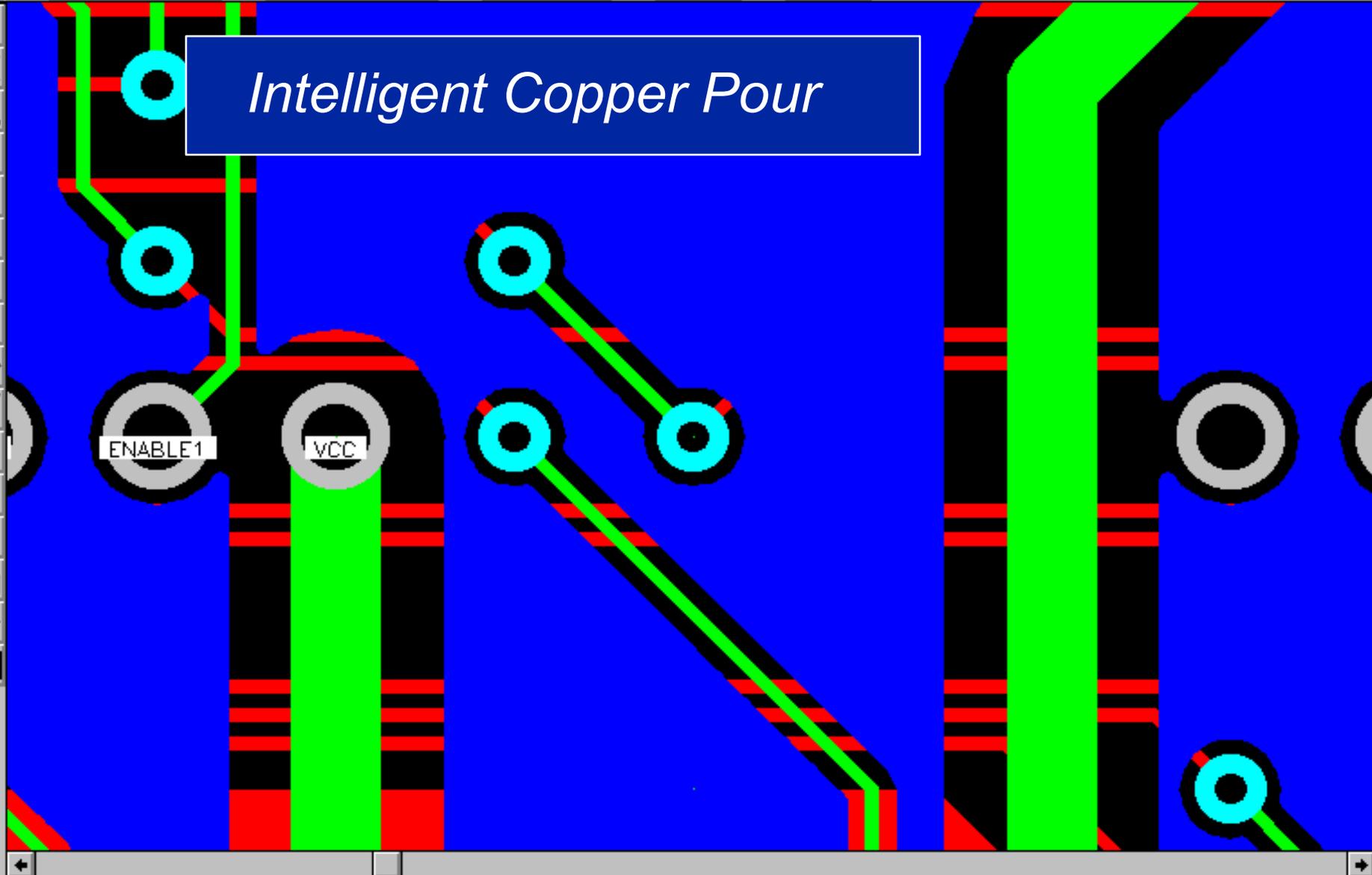
```

OK Cancel

Embedded DO File editor



Intelligent Copper Pour

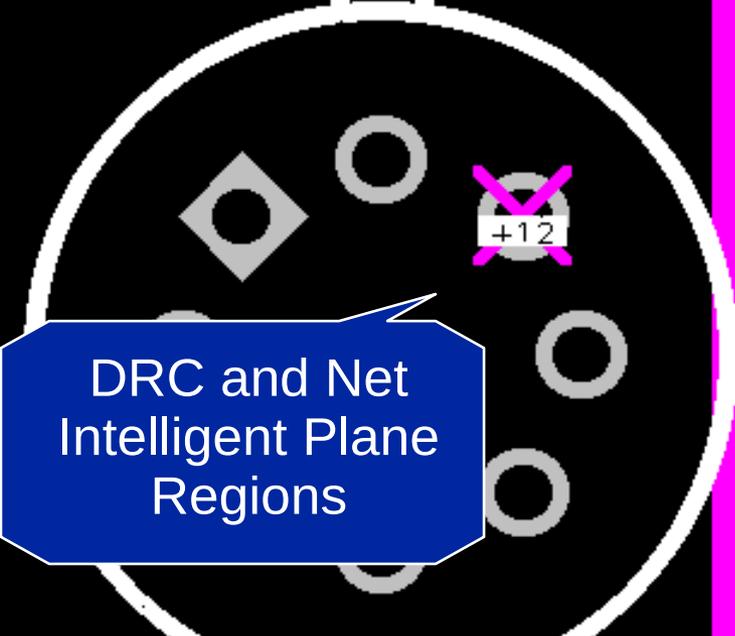


Click <Left> to single Select, <Shift><Left> for multiple, or drag for block select.

Split Plane Support

split plane
net +12

1007



DRC and Net
Intelligent Plane
Regions



split plane
net +5

U2

Correct by Design

Rules and built-in checking help eliminate errors during the design.

Resolution

Rules Checking

Plane Connections
(Thermal ties)

Apertures and Drill
Assignments

Packaging

WYSIWYG Output

On-line DRC

Net Attributes

Integrated Libraries

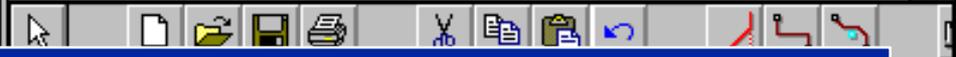
Library Management

Pattern & Symbol Creation

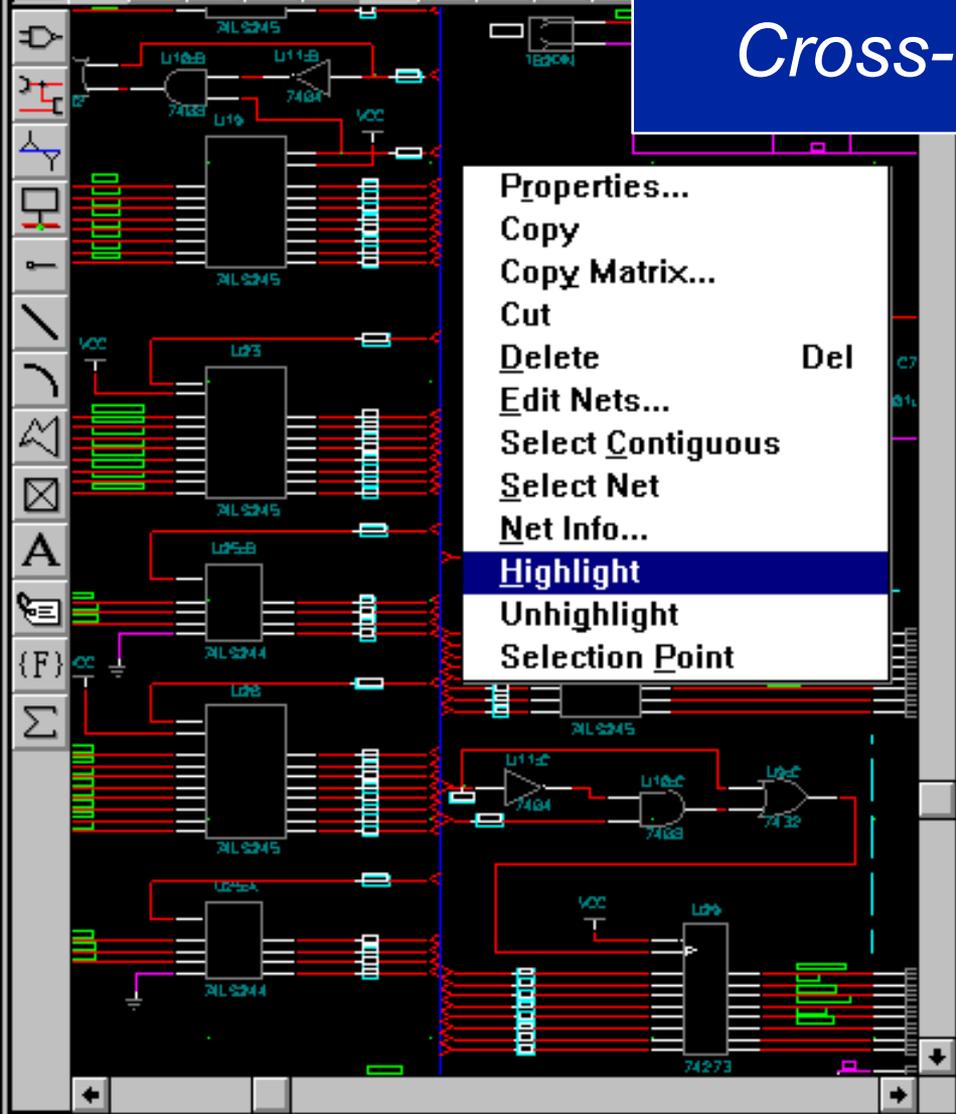
ECOs

Cross-probing

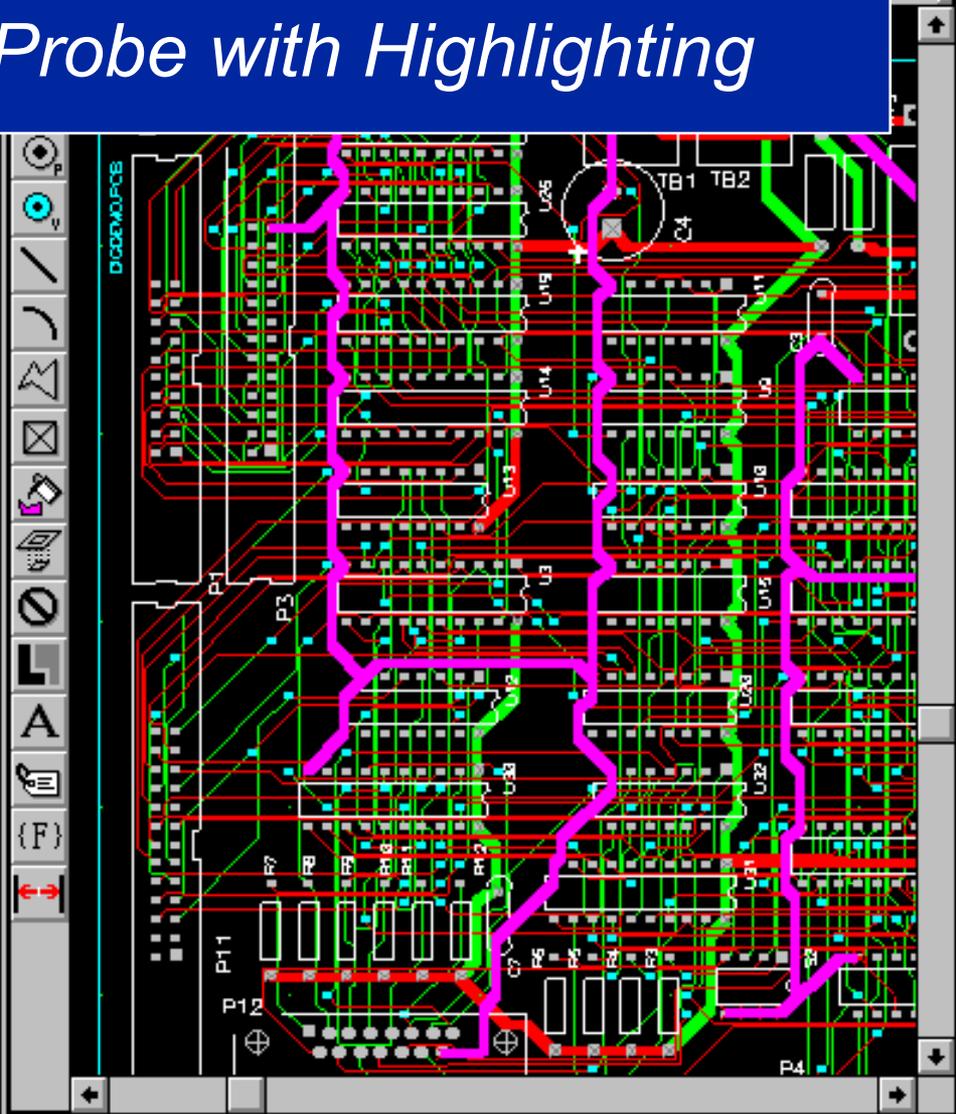
Router Integration



Cross-Probe with Highlighting



- Properties...
- Copy
- Copy Matrix...
- Cut
- Delete Del
- Edit Nets...
- Select Contiguous
- Select Net
- Net Info...
- Highlight**
- Unhighlight
- Selection Point





Symbol View: [1] SYMBOL30_N

Select Symbol...

Component Info...

Pins View...

Pattern View...

Prev. Sym.

Prev. Pin

Cross-Linked
Windows

{RefDes}

14
13
12
11
10
9
8
7
6
5
4
3

Integrated Libraries

2
1

{Type}

Pattern View: S016

RefDes

16
15
14
13
12
11
10
9
8
7
6
5
4

Type

Sym Pin #	Pin Name	Gate Eq	Pin Eq	Elec. Type
6				

Pins View

Component Info...

Pattern View...

Symbol View...

Pin Des	Gate #	Sym Pin #
6	1	6

6							
	Pin Des	Gate #	Sym Pin #	Pin Name	Gate Eq	Pin Eq	Elec. Type
4	4	1	4		1		
5	5	1	5		1		
6	6	1	6		1		

Rules Based Design Entry

Attributes on Net Classes

Options Design Rules

Net Class Net Class To Class

Net Class To Net Class Definitions:

- POWER To BUS1
- POWER To BUS2

Net Class Name: POWER

Net Class Name: BUS1

Add Definition

Rules:

LineToLineClearance=25

Modify Definition

Delete Definition

Edit Rules...

Close

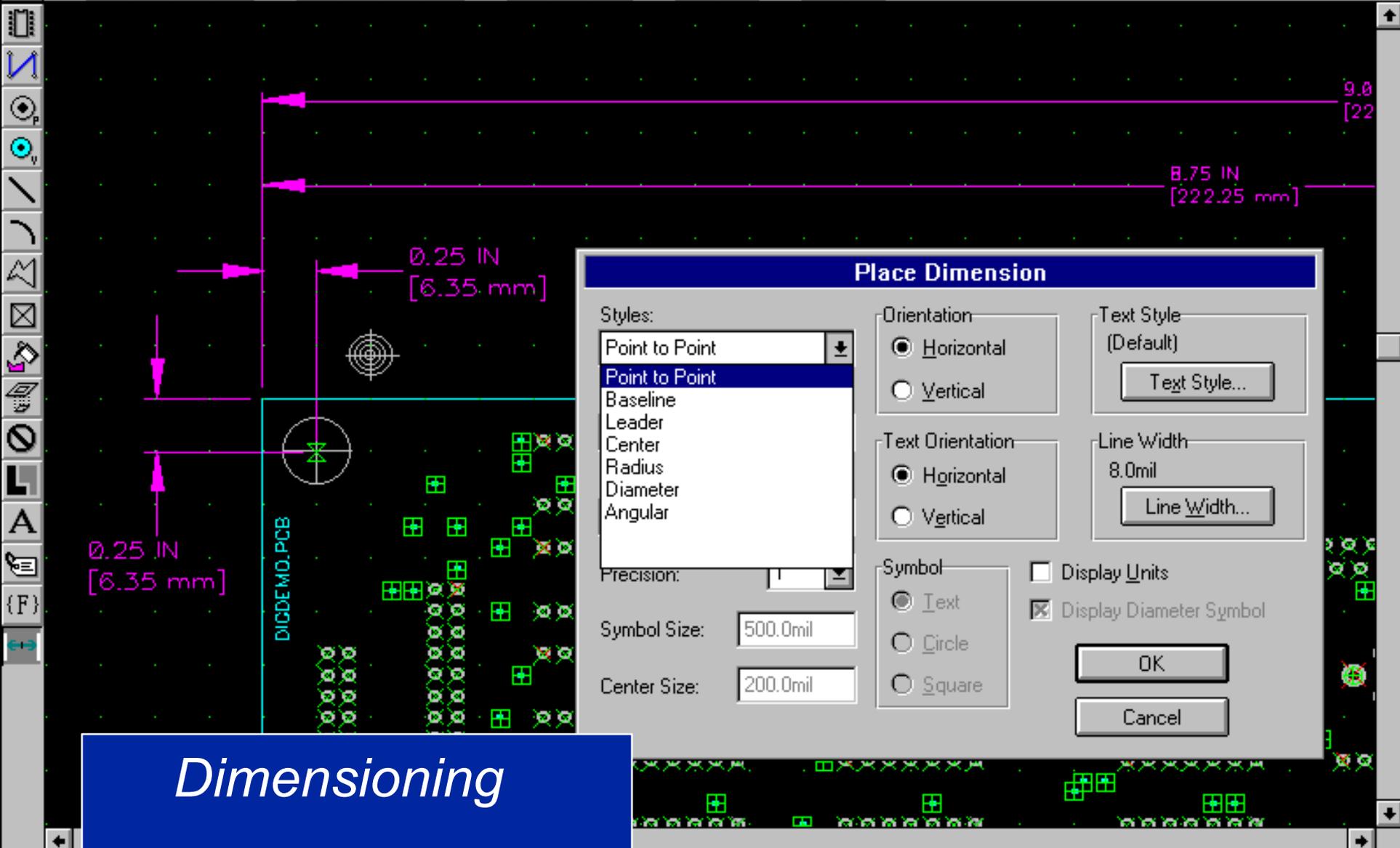
Define Rules Between Classes

Manufacturability

Speed design and reduce costs
with accurate and usable output.

Report Generation
Gerber Viewer
NC Drill and Insertion

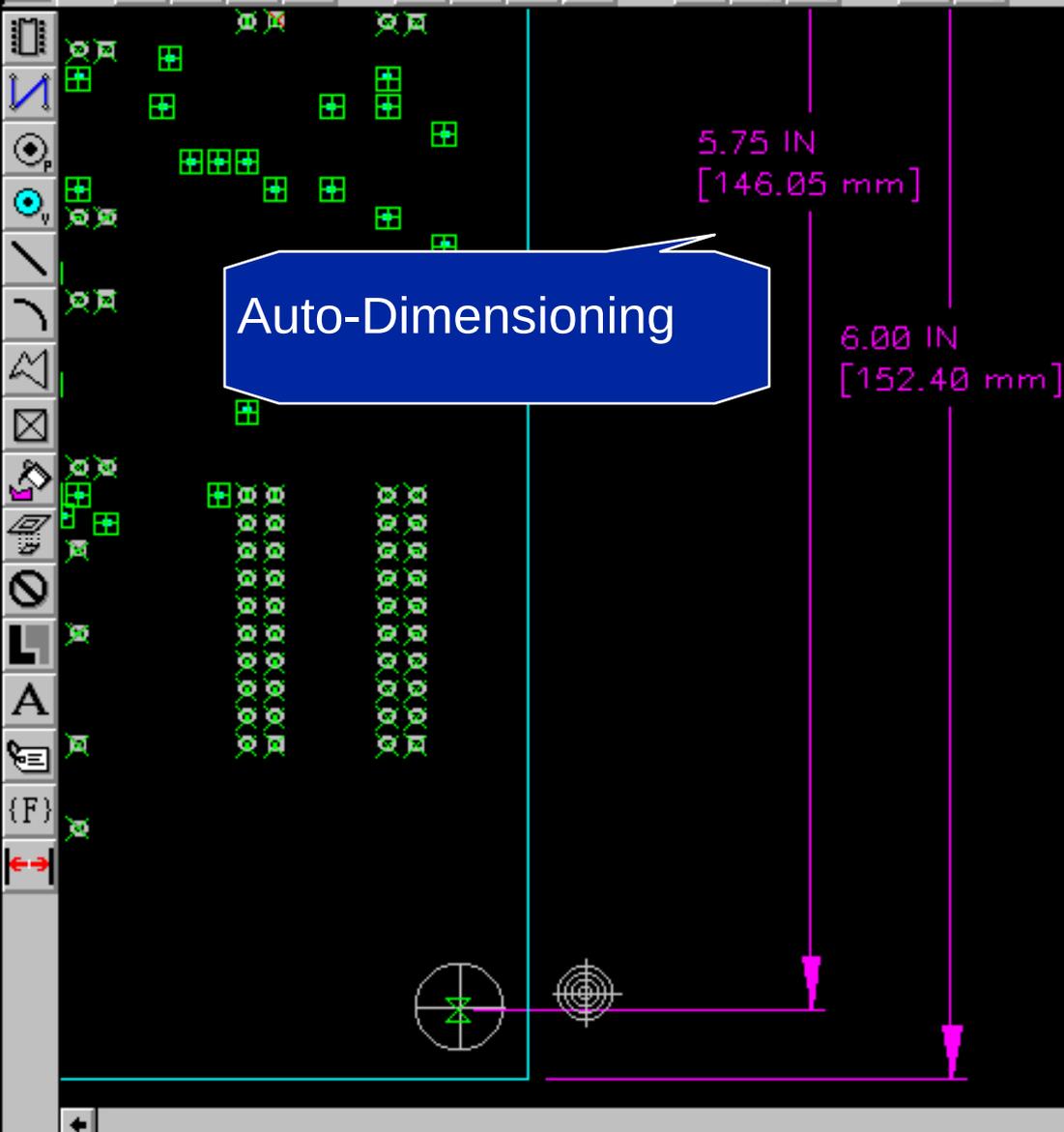
Dimensioning
DXF
Assembly and Paste Layer
Artwork



Dimensioning

Press <Left> or <Space> to display Dimension Configuration dialog.

3625.0 8100.0 Abs 25.0 Board 8.0mil



FAB and Assembly Drawings

Hole Dia (inch)	Symbol	Quantity	PTH
0.018	⊞	297	Yes
0.022	+	1	Yes
0.038	×	851	Yes
0.050	⊕	11	Yes
0.060	⊗	8	Yes
0.068	⊕	2	No
0.128	⊕	8	Yes
0.144	⊗	4	Yes

Auto-Drill Chart Creation

Inter-operability

Many ways to interface to other programs in your design environment.

Cut/Copy

Printing

Multiple Document Interface
(MDI)

ASCII Files

Application Programming
Interface (API)

Third Party Interfaces

ACCEL Pattern Wizard

Pattern Type

ARRAY

Scale View

2.

Current Units:

[mil]

Pattern Placement

4000.

X-Pos

4000.

Y-Pos

Send Pattern

Exit

Select Package Type

12

12

Number of Pads Across

100.

Pad to Pad Spacing (On Center)

6

Cutout Pads Down

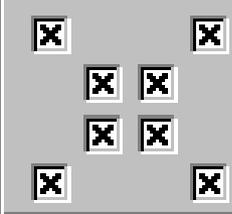
6

Cutout Pads Across

112

Total Pads

Corner Pads



Pattern Wizard for Auto-Part creation (example of API)

Pad Style

P:EX60Y60D34A

Rotate

Silkscreen Control

Silk Screen

10.

Silk Line Width

1300.

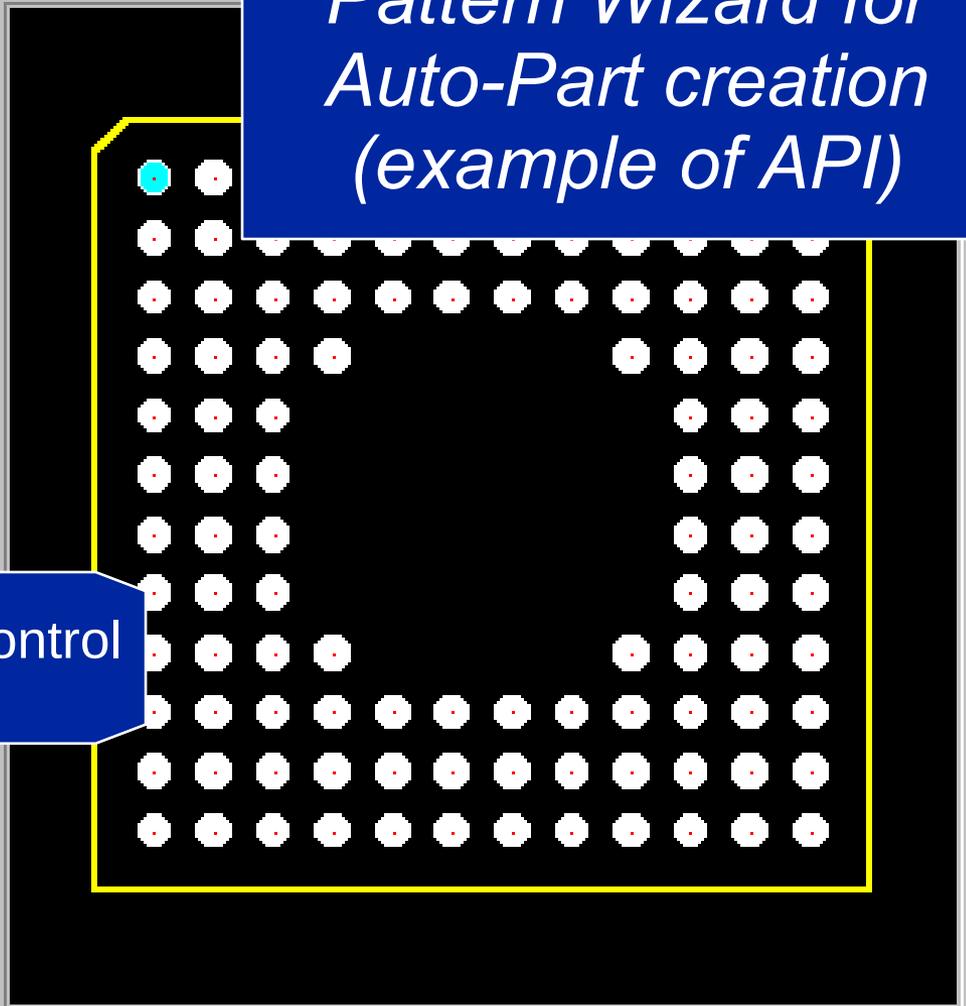
Silk Rectangle Width

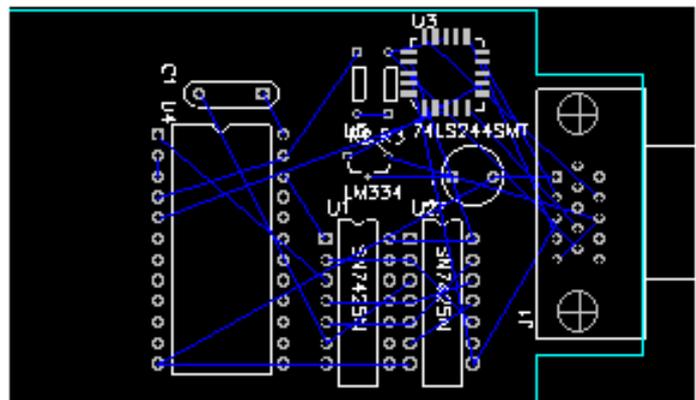
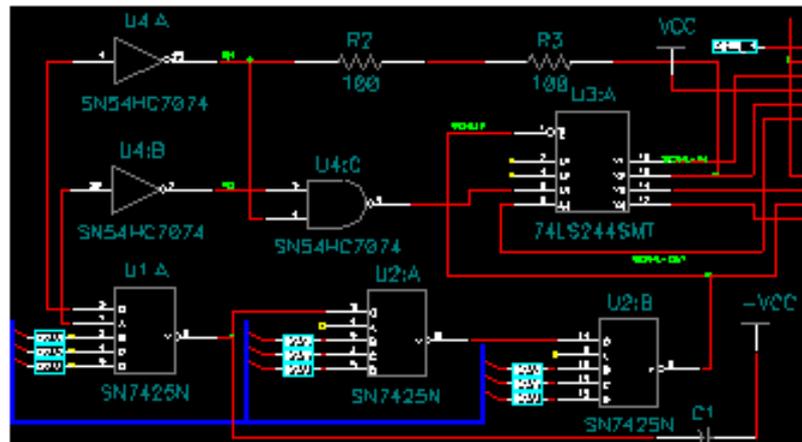
1300.

Silk Rectangle Height

Upper Left

Notch Type





; ACCEL P-CAD PCB Version 12.00 [C:\ACCEVAL\DEMO\WORD.PCB]-Mon Apr 08 13:14:10 1996

; Engineering change order #2

NetNodeDelete "NET00000" "R2-B"

NetNodeDelete "IN1" "R2-A"

CompDelete "R2"

NetNodeDelete "NET00000" "R3-A"

NetDelete "NET00000"

CompAdd "CAP300" "C2" " "

NetNodeAdd "SIGNAL1" "C2-B"

NetNodeAdd "-VCC" "C2-A"

NetAttrModify "VCC" "Width" "25"

NetAttrModify "_12" "Width" "25"

RefdesChange "U4" "U100"

RefdesChange "U5" "U101"

CompAttrAdd "U101" "ComponentHeight" "15"

Cut and Paste Graphics into Windows Programs

ACCEL EDA Highlights

Multi-function
selection tool

User programmable
hot keys

Rules based design entry

Layer sets

Cut and paste into Windows
application

DBX - ACCEL's Application
Programming Interface

Modify Hole Range - supports
blind/buried vias

Advanced copper pour

Intelligent split planes

Dimensioning

InterRoute - shape-based
interactive routing tool

Library Manager - linked views of
data

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ACCEL *EDA*

The ACCEL EDA Series

Powerful design software, and more . . .

ACCEL EDA Software

- ACCEL Schematic
- ACCEL P-CAD PCB
- ACCEL Tango PCB
- ACCEL PRO Route
- ACCEL PRO Route 2/4
- ACCEL Library Manager

Service & Support

- Printed and On-line Documentation
- Training
- Active User Groups

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ACCEL *EDA*

*from the root of your ideas
towering products grow...*

ACCEL *EDA*

Thank You

