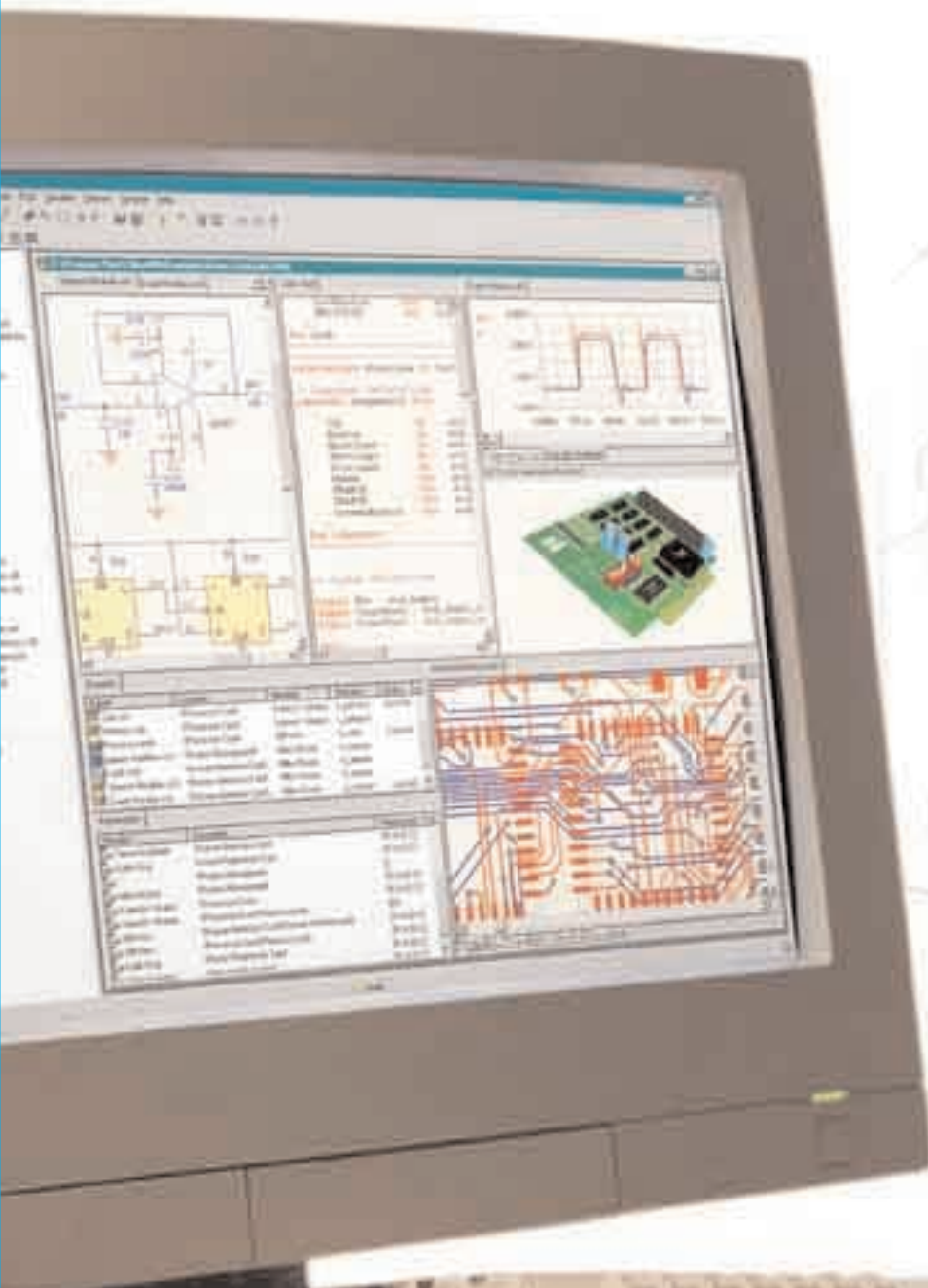


# Protel 99



# Eliminate guesswork with board signal

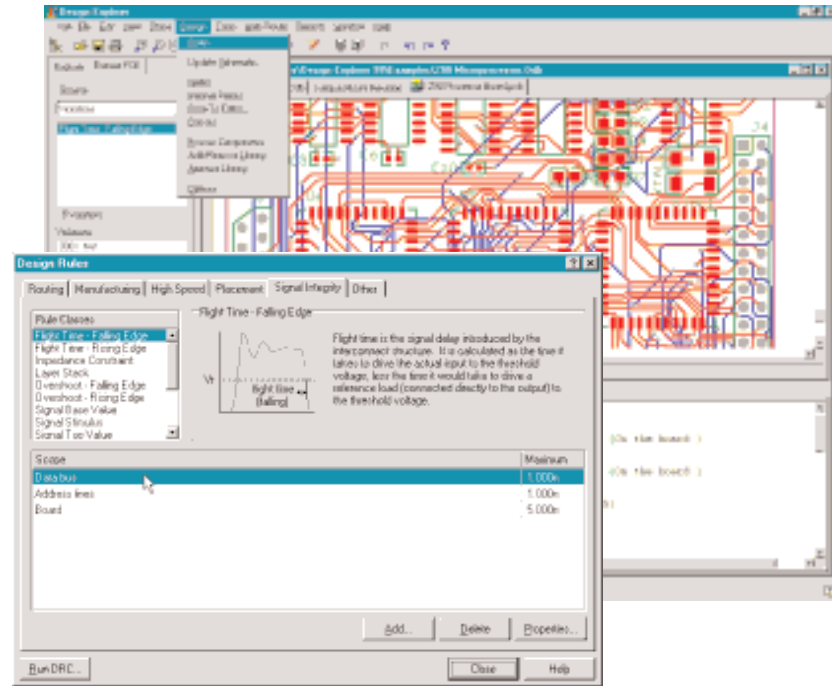
Get it right the first time and take the guesswork out of board design by including signal integrity analysis as part of your design toolbox. Protel 99's Signal Integrity Simulator is seamlessly integrated with the board layout process, providing extremely accurate board analysis. Create rules to check your whole board for crosstalk, overshoot/undershoot, flight time and impedance problems. Minimize costly post-layout changes and solve your high-speed design and EMC/EMI problems before you take your board to manufacture.

## Reduce the design time with advanced signal integrity analysis

As PCB designs become more sophisticated, with higher clock speeds, higher device switching speeds, and higher density, the need to analyze the signal integrity before the design is manufactured becomes more pressing. Propagation delays, net impedances, signal reflections and crosstalk are no longer just the domain of the high-frequency design specialist. Signal integrity problems can affect all board designs. Device manufacturers constantly produce smaller and faster devices with increasing device edge rates, and slower logic families are disappearing from manufacturers' inventories. It is becoming increasingly necessary for all designers to keep signal integrity issues in mind as they layout and route their boards.

Protel 99 includes a sophisticated Signal Integrity Simulator that provides detailed information about the real-world performance of your design. Signal integrity test parameters, such as overshoot, undershoot, impedance and signal slope requirements, are specified as standard PCB design rules. If the board fails any of the signal integrity design requirements during design rule checking, you can run Protel 99's Signal Integrity Simulator to perform full reflection or crosstalk analyses of the PCB to pinpoint the problem and examine possible solutions.

Using Protel 99's Signal Integrity Simulator you can find and correct signal integrity problems before sending your board to manufacture.



Protel 99 includes a comprehensive set of signal integrity design rules covering areas such as net impedance, overshoot, undershoot, flight time and signal slope. Signal integrity violations are then included as part of the standard board DRC report.

## Accurate results from industry-proven algorithms

Protel 99's Signal Integrity Simulator accurately models the behavior of the routed board. It uses the characteristic impedance of the traces, determined using sophisticated transmission line calculations, and I/O buffer macro-model information as input for simulations. Based on a Fast Reflection and Crosstalk simulator model, Protel 99's Signal Integrity

Simulator produces accurate simulations using industry-proven algorithms.

## Tight integration with Protel 99's PCB Editor

While you can run Protel 99's Signal Integrity Simulator at any time to examine the performance of your board in detail, tight integration with Protel 99's PCB Editor means you can easily incorporate signal integrity analysis into the normal board verification process.

Net Name	Component	Delay	Amplitude (V)	Rise/Fall Time (ns)	Signal Condition
1234	U1A	10.0	1.0	10.0	Signal Condition: OK
1235	U1A	10.0	1.0	10.0	Signal Condition: OK
1236	U1A	10.0	1.0	10.0	Signal Condition: OK
1237	U1A	10.0	1.0	10.0	Signal Condition: OK
1238	U1A	10.0	1.0	10.0	Signal Condition: OK
1239	U1A	10.0	1.0	10.0	Signal Condition: OK
1240	U1A	10.0	1.0	10.0	Signal Condition: OK
1241	U1A	10.0	1.0	10.0	Signal Condition: OK
1242	U1A	10.0	1.0	10.0	Signal Condition: OK
1243	U1A	10.0	1.0	10.0	Signal Condition: OK
1244	U1A	10.0	1.0	10.0	Signal Condition: OK
1245	U1A	10.0	1.0	10.0	Signal Condition: OK
1246	U1A	10.0	1.0	10.0	Signal Condition: OK
1247	U1A	10.0	1.0	10.0	Signal Condition: OK
1248	U1A	10.0	1.0	10.0	Signal Condition: OK
1249	U1A	10.0	1.0	10.0	Signal Condition: OK
1250	U1A	10.0	1.0	10.0	Signal Condition: OK
1251	U1A	10.0	1.0	10.0	Signal Condition: OK
1252	U1A	10.0	1.0	10.0	Signal Condition: OK
1253	U1A	10.0	1.0	10.0	Signal Condition: OK
1254	U1A	10.0	1.0	10.0	Signal Condition: OK
1255	U1A	10.0	1.0	10.0	Signal Condition: OK
1256	U1A	10.0	1.0	10.0	Signal Condition: OK
1257	U1A	10.0	1.0	10.0	Signal Condition: OK
1258	U1A	10.0	1.0	10.0	Signal Condition: OK
1259	U1A	10.0	1.0	10.0	Signal Condition: OK
1260	U1A	10.0	1.0	10.0	Signal Condition: OK
1261	U1A	10.0	1.0	10.0	Signal Condition: OK
1262	U1A	10.0	1.0	10.0	Signal Condition: OK
1263	U1A	10.0	1.0	10.0	Signal Condition: OK
1264	U1A	10.0	1.0	10.0	Signal Condition: OK
1265	U1A	10.0	1.0	10.0	Signal Condition: OK
1266	U1A	10.0	1.0	10.0	Signal Condition: OK
1267	U1A	10.0	1.0	10.0	Signal Condition: OK
1268	U1A	10.0	1.0	10.0	Signal Condition: OK
1269	U1A	10.0	1.0	10.0	Signal Condition: OK
1270	U1A	10.0	1.0	10.0	Signal Condition: OK
1271	U1A	10.0	1.0	10.0	Signal Condition: OK
1272	U1A	10.0	1.0	10.0	Signal Condition: OK
1273	U1A	10.0	1.0	10.0	Signal Condition: OK
1274	U1A	10.0	1.0	10.0	Signal Condition: OK
1275	U1A	10.0	1.0	10.0	Signal Condition: OK
1276	U1A	10.0	1.0	10.0	Signal Condition: OK
1277	U1A	10.0	1.0	10.0	Signal Condition: OK
1278	U1A	10.0	1.0	10.0	Signal Condition: OK
1279	U1A	10.0	1.0	10.0	Signal Condition: OK
1280	U1A	10.0	1.0	10.0	Signal Condition: OK
1281	U1A	10.0	1.0	10.0	Signal Condition: OK
1282	U1A	10.0	1.0	10.0	Signal Condition: OK
1283	U1A	10.0	1.0	10.0	Signal Condition: OK
1284	U1A	10.0	1.0	10.0	Signal Condition: OK
1285	U1A	10.0	1.0	10.0	Signal Condition: OK
1286	U1A	10.0	1.0	10.0	Signal Condition: OK
1287	U1A	10.0	1.0	10.0	Signal Condition: OK
1288	U1A	10.0	1.0	10.0	Signal Condition: OK
1289	U1A	10.0	1.0	10.0	Signal Condition: OK
1290	U1A	10.0	1.0	10.0	Signal Condition: OK
1291	U1A	10.0	1.0	10.0	Signal Condition: OK
1292	U1A	10.0	1.0	10.0	Signal Condition: OK
1293	U1A	10.0	1.0	10.0	Signal Condition: OK
1294	U1A	10.0	1.0	10.0	Signal Condition: OK
1295	U1A	10.0	1.0	10.0	Signal Condition: OK
1296	U1A	10.0	1.0	10.0	Signal Condition: OK
1297	U1A	10.0	1.0	10.0	Signal Condition: OK
1298	U1A	10.0	1.0	10.0	Signal Condition: OK
1299	U1A	10.0	1.0	10.0	Signal Condition: OK
1300	U1A	10.0	1.0	10.0	Signal Condition: OK

Generate a full signal integrity report for any nets on your board. The report includes comprehensive impedance and signal condition information for each net.



# integrity simulation

Signal integrity design requirements, such as net impedance, overshoot, undershoot, flight time and signal slope can be specified as design rules within the PCB Editor. When you perform a Design Rule Check (DRC) on your board, Protel 99 automatically tests these rules using the Signal Integrity Simulator algorithms. Signal integrity violations are then included as part of the standard board DRC report.

Include signal integrity rules as part of the board specification process and you'll automatically catch potential problems at the crucial layout stage, before committing to prototyping and manufacture.

And because signal integrity analysis is integrated in the PCB design rule checking process, you can use the powerful PCB Editor browse tools to quickly identify problem nets. Set the Browse mode in the PCB Editor Panel to Violations and you can quickly locate and display problem nets with full violation details.

## Perform accurate waveform analyses

To give you the full picture on your board's signal integrity performance, Protel 99's Signal Integrity

Simulator includes a powerful Wave Analyzer that displays the results of reflection and crosstalk simulations.

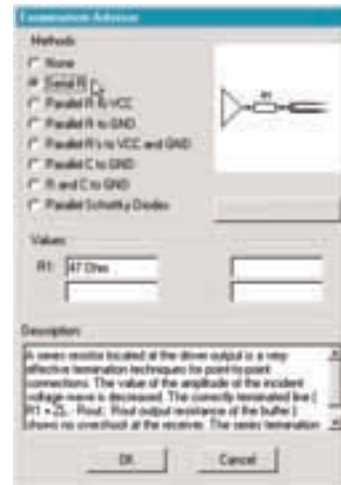
The Wave Analyzer shows the simulation results in a CRO-like graphical display. You can zoom in on any portion of a waveform, and use the versatile measurement tools to take measurements directly from the display.

## Explore termination options

Protel 99's Signal Integrity Simulator includes a powerful Termination Advisor that lets you explore the results of various termination options before modifying your board.

The Termination Advisor allows you to selectively apply different termination options for a particular node. You can then rerun the simulation to compare the effects of the different options, choosing the best solutions for your design before altering your board layout.

With Protel 99's integrated Signal Integrity Simulator, you'll save time and money by eliminating signal integrity and EMC/EMI problems on your board before prototyping and manufacture.



The integrated Termination Advisor allows you to experiment with different termination options for each connection, then run a virtual simulation using the selected termination. Find the optimal solution before modifying your board.



## Feature Highlights

- Well-proven algorithms for the accurate calculation of transmission line characteristics and simulations
- Simple to set up - define the design requirements (impedance, overshoot, undershoot, slope, flight time, etc) as PCB design rules
- No special expertise is required, the signal integrity analysis is launched directly from the PCB
- Perform a design rule check on the entire design to quickly identify nets that fail the requirements
- Perform fast simulation of reflection and crosstalk effects on selected nets
- No knowledge of SPICE or analog simulation is required, the Signal Integrity Simulator uses I/O buffer macro-models
- Oscilloscope type display of reflection and crosstalk simulation results with integrated result measurement facilities
- Quickly examine different what-if termination options with the Termination Advisor
- Extensive library of component models

## Specifications

**Device modelling:**  
I/O buffer macro-model

**Analyses:**  
Net Screening, Reflection, Crosstalk

**Integration methods:**  
Trapezoidal, Gear's Method (1st, 2nd and 3rd order)

**Termination simulations:**  
Series R, Parallel R to VCC, Parallel R to GND, Parallel R to VCC and GND, Parallel C to VCC, Parallel C to GND, Parallel Schottky diodes

**Stimulus types:**  
Single pulse, Constant level, Periodic pulses

Protel 99's Signal Integrity Simulator includes a powerful Wave Analyzer that graphically displays the results of reflection and crosstalk simulations and allows you to take measurements directly from the displayed waveforms.

