

## Contents

Help is available for menu commands in both Router mode and Placement mode. The menubar menus are listed in the following table. See [Interactive Route](#) menu and [Interactive Place](#) menu for lists of the interactive menu commands.

You can also access menu command help by clicking the Help button in a dialog box or by using the [Help] key on your keyboard. (Use the [F1] key if your keyboard does not have a [Help] key.)

The menubar contains the following menus for routing and placement.

### Router Menus

[File](#)  
[Edit](#)  
[View](#)  
[Select](#)  
[Define](#)  
[Rules](#)  
[Autoroute](#)  
[Report](#)  
[Help](#)

### Placement Menus

[File](#)  
[Edit](#)  
[View](#)  
[Select](#)  
[Define](#)  
[Rules](#)  
[Autoplace](#)  
[Report](#)  
[Help](#)

## Notes

For help on menubar commands, you can also drag the pointer to a command in a menu, and press the [Help] or [F1] key. For help on icons, buttons, or text labels in the main SPECCTRA window, you can also use the [Tab] and arrow keys to move the keyboard focus to the area of interest, and press the [Help] or [F1] key.

For help learning how to use SPECCTRA, click a subject in the Help menu. For help in the main SPECCTRA window, choose **Help - Point & Click**, and click on an icon, a button, or a text label in the window.

## Interactive Route Menu

The Interactive Route menu contains the following commands:

Setup

Select

UnSelect All Objects

Measure Mode

Edit Route Mode

Move Route Mode

Copy Route Mode

Critic Route Mode

Change Via Mode

Change Wire Mode

Cut Segment Mode

Delete

Undo

## Setup

### Sets global interactive routing controls and constraints

The Interactive Routing Setup dialog box contains the following:

**Wire Grid** sets the [wire grid](#).

**Via Grid** sets the [via grid](#).

**PCB Wire Width** sets a PCB level wire width rule. Rules at the PCB level are global rules because they apply to the entire PCB. PCB level rules have the lowest precedence in the [SPECCTRA rules hierarchy](#).

**PCB Clearance** sets a PCB level clearance rule. Rules at the PCB level are global rules because they apply to the entire PCB. PCB level rules have the lowest precedence in the [SPECCTRA rules hierarchy](#).

**Pointer Style** sets the pointer style to one of the following:

**90 deg crosshair** displays orthogonal crosshairs.

**45 deg crosshair** displays both 90 and 45-degree crosshairs if Snap Angle is set to 45 degrees or All.

**Arrow only** displays the pointer without crosshairs. This is the default pointer style.

**Redundant Power Net Wiring** controls whether EditRoute allows redundant wires and vias on power nets. If Redundant Power Net Wiring is not checked (default), EditRoute eliminates wire loops and extra vias during interactive routing. Click this check box if you need redundant wires and vias to increase current capacity to a power connection, or if you need to enclose a pin or via with a shield.

**Show Timing/Length Rule Constraints** controls whether EditRoute displays length rule indicators as you are editing a wire with a length rule. The two types of indicators are as follows:

**Meter** displays the current wire length relative to the minimum or maximum length rules of the wire.

**Octagons** displays an octagon showing the minimum or maximum length rule of the wire you are editing.

**Snap Angle** controls whether the pointer snaps to any angle, or snaps to a 45 or 90 degree angle when you are routing. The default is 45 degrees.

**Via Assistance** controls whether visual assistance is available to search for legal via locations. When you are routing a connection, you add a via by clicking twice in the same location. If the Snap option is checked (default), the cursor snaps to the closest via site when you click twice near a legal via location. If Display is checked, nearby legal via sites are displayed when you click twice at a location that is not a legal via site. If None is checked, via assistance is not available.

**Snap to Pin Origin** controls whether the cursor snaps to pin origins. If Snap to Pin Origins is checked (default), a wire snaps to the origin of noncircular pins when you click anywhere inside the pin. If Snap to Pin Origin is not checked, a connection to a noncircular pin is considered complete if it is simply within the boundary of the pin shape. Wires always snap to the origins of circular pins, regardless of how this control is set.

**Push routing** lets you route between existing wires and automatically push them aside in order to comply with wire-to-wire clearance rules. Push routing reduces the need to interrupt routing when existing wires block a path. Push routing is on by default.

**Note**

Redundant wires and vias on power connections are not automatically protected. Use one of the protect commands on the Edit menu to prevent the autorouter from eliminating redundant wires and vias on power connections.

## Interactive Place Menu

The Interactive Place menu contains the following commands:

Setup

Select

UnSelect All Objects

Measure Mode

Place Components

Move Comp Mode

Push Comp Mode

Pivot Comp Mode

Flip Comp Mode

Trade Comp Mode

Align Comp Mode

Swap

Undo

## Place Components - XY Location

### **Interactively places components at exact locations**

The Place Components dialog box allows you to pick a component and specify the exact point where you want to place its origin. You can also choose the side of the PCB where you want to place the component and set the component's orientation.

Use the [Filter](#) data entry box or the Components [list](#) to pick the component you want to place.

**X** is the X coordinate of the point where you want to place the component.

**Y** is the Y coordinate of the point where you want to place the component.

**Front** means to place the component on the front side of the PCB.

**Back** means to place the component on the back side of the PCB.

**Rotation** is the angle in degrees at which you want to rotate the component. Rotation is counterclockwise with respect to a view facing the component's mounting surface.

## Place Components - Place List Mode

### Places components from a defined list

The Place Component List dialog box allows you to place components from either an unordered list or an ordered list of component reference designators.

- To place components from an unordered list pick the components using the [Filter](#) data entry box or the Components [list](#).
- To place components from an ordered list, you enter the component reference designators in the Comp List data entry box.

After you click Apply or OK in the dialog box, SPECCTRA attaches the first component to the pointer. Move the pointer inside the PCB boundary, and click at the point where you want to place the component. SPECCTRA attaches the next component in the list to the pointer.

After you place a component, SPECCTRA attaches another component to the pointer.

- If you defined an ordered list, SPECCTRA attaches components in the order you entered them in the Comps List data entry box.
- If you defined an unordered list, SPECCTRA attaches the components in reverse of the order components are specified in the design file.

This process continues until you have placed all the components in the list or you press [RB] and choose **Exit To Move Comp Mode** from the Place List Mode menu.

### To place components from an unordered list

1. Press [RB] and choose **Place Components - By List Mode** from the Interactive Place menu.
2. Click the Unordered Components button.
3. Use A or B:
  - A. Enter a component reference designator or a wildcard in the Filter data entry box..
  - B. Click one or more component reference designators in the Components list.
4. Click Apply or OK.

### To place components from an ordered list

1. Press [RB] and choose **Place Components - By List Mode** from the Interactive Place menu.
2. Click the Ordered Components button.
3. Enter component reference designators, separated by a blank space, in the Comp List data entry box.
4. Click Apply or OK.

## Snap Grid

### **Sets the pointer snap grid in the interactive drawing modes**

The Snap Grid dialog box defines the grid points to which the lines snap when you are drawing a fence in Draw Fence mode, a room in Draw Room mode, a keepout area in Draw Keepout mode, or a placement boundary in Draw Place Boundary mode. This grid is used only for interactive area editing such as drawing rooms for placement or fences for routing. The default snap grid is 0, which means no snap grid is used.



## Define Room

### Assigns a unique name to and an optional side to a room

Use the Define Room dialog box in [Draw Room mode](#) to assign a unique name to the room you have drawn. A room is an area of the PCB that you define to control where SPECCTRA places components. You can control placement in a room on one surface or on both surfaces.

You draw a room by setting [LB] to Draw Room mode and clicking at points within the PCB boundary until you have drawn a closed rectangle or polygon.

To open the Define room dialog box, press [RB] and choose Add Polygon as Room. You must assign a unique name to the room. You can also specify whether the room applies to the front, back, or both sides of the PCB.

**Room ID** is a unique name used to identify the room when you assign rules. If you try to assign a room ID that is already defined, SPECCTRA reports an error.

**Side** specifies one or both sides of the PCB. The options are

**Both**, which means the room is on both sides of the PCB.

**Front**, which means the room is only on the front side of the PCB.

**Back**, which means the back is only on the back side of the PCB.

### Notes

Room names must be unique.

To define a room by specifying the X,Y coordinates for each corner, use [Define - Room](#).

To disband a room use [Define - Forget Rooms](#).

## Select

**Sets [LB] to select a certain type of routing object**

The Select submenu choices are

Select - Comp Mode

Select - Net Mode

Select - Wire Mode

Select - Guide Mode

## Select

**Sets [LB] to select a certain type of placement object**

The Select submenu choices are

Select - Comp Mode

Select - Gate Mode

Select - Subgate Mode

Select - Pin Mode

Select - Terminator Mode

## UnSelect All Objects

### **Unselects all selected objects**

After you click Unselect All Objects on the right mouse button menu, all selected objects are no longer in the select color (yellow if you use the default color map).

### **Note**

When all objects are unselected they are available for automatic routing and placement operations. If one or more objects are selected, only those objects are available for automatic routing and placement operations.

## Delete

### **Sets [LB] to delete wires or nets or to repair nets**

The commands on the Delete menu remove wire segments and nets. The Delete menu contains the following commands:

[Segment Mode](#)

[Wire Mode](#)

[Net Mode](#)

[Repair Net Mode](#)

## Place Components

**Sets [LB] to place components interactively at locations you choose**

The Place Components submenu choices are

[Place Connect Mode](#)

[Guided Place Overlap Allowed Mode](#)

[Guided Place Connect Mode](#)

[XY Location](#)

[Place List Mode](#)

## Swap

**Sets [LB] to swap equivalent gates, subgates, pins, or terminators.**

The Swap submenu choices are

Gate Mode

Sub-Gate Mode

Pin Mode

Terminator Mode

## Starting SPECCTRA

You start SPECCTRA by double-clicking the SPECCTRA icon in the SPECCTRA group.

The [Startup dialog box](#) appears. You must specify a design file to start a new session or a session file to restart a previous session. You can also specify a do file a routes file, and other options.

You can also bypass the Startup dialog box and start SPECCTRA by specifying using the **specctra** command with command line switches. For more information on starting SPECCTRA, see the *SPECCTRA User's Reference* manual.

### Note

You can run a do file when you start SPECCTRA or at any time during the SPECCTRA session. To run a do file after you start SPECCTRA, click [File - Execute Do File](#).



## Startup dialog box

When the Startup dialog box appears, you must specify a design file to start a new session or a session filename to restart a previous session. You can also specify a [do file](#), a [routes file](#), and other options. To see the other options, click the More Options button.

To enter the name of a file, you can do either of the following:

- Click the data entry box, and type the path and filename
- Click the Browse button, and choose a filename in the dialog box that appears

SPECCTRA automatically checks the check box for the option when you enter or choose a filename. To disable the option, you can remove the check from the check box or delete the filename from the data entry box.

For general information about specifying filenames in SPECCTRA, see Chapter 1 in the *SPECCTRA User's Reference* manual. See Chapter 2 in this manual for general information about starting SPECCTRA and using startup options.

### To start SPECCTRA using the Startup dialog box

1. Enter the name of your design file or session file in the Design/Session File data entry box.
2. If you want to use routing information from a previous session, enter the name of a routes file or a wires file in the Wires/Routes File data entry box.
3. If you want to start the session by performing commands listed in a do file, enter the name of your do file in the Do File data entry box.
4. Click the More Options button to expand the Startup dialog box if you want to use any other options.
5. Click the [Add License](#) button if you need to install licenses before starting SPECCTRA.
6. Click the Start SPECCTRA button.

If you specify a do file, SPECCTRA starts by performing the commands listed in the file.

Click on the following topics to find out information about the fields in the Startup dialog box.

[Startup exclamation point](#)

[Design/Session File](#)

[Wires/Routes File](#)

[Do File](#)

[No Graphics](#)

[Quit After Do File](#)

[No Preroutes](#)

[Don't Strip Orphan Shapes](#)

[Simplify Polygons](#)

[Show Usage](#)

[Password File](#)

[Did File](#)

[Message Output File](#)

[Status File](#)

[Color Mapping File](#)

[Add Licenses button](#)

## **Startup exclamation point**

Displays messages if SPECCTRA could not start with the information in the Startup dialog box .

## Design/Session File

Names the SPECCTRA design file or session file.

## Wires/Routes File

Names the wires file or routes file.

## Do File

Names the do file that will run once the autorouter starts.

## No Graphics

Runs SPECCTRA without the Graphical User Interface (GUI). Graphics are not displayed. Use this option to run SPECCTRA by performing commands listed in a [do file](#).

## Quit After Do File

Exits the autorouter after the do file finishes running.



## No Preroutes

Deletes prerouted wires defined in the design file.

## Don't Strip Orphan Shapes

Does not remove orphan shapes defined in the design file. By default, SPECCTRA removes all shapes that are not assigned to a net.

## **Simplify Polygons**

Changes 1-inch or smaller polygons to simple rectangles.

## Show Usage

Lists all command line switches.

## **Password File**

Specifies a password file. The default is sp.pas in the directory where you loaded SPECCTRA.

## Did File

Names the did file.

## **Message Output File**

Sends prompts and messages to this file, in addition to sending them to the output window.  
This is useful when you run SPECCTRA unattended with a batch script.

## Status File

Names the file where routing status information is saved. Default: monitor.sts



## Color Mapping File

Names the color map file used to change the color scheme built into the autorouter. If you do not use this option, the autorouter looks for the file color.std in the SPECCTRA directory. If color.std does not exist, the autorouter uses an internal color map. Default: color.std

## **Add Licenses button**

Displays the [Add Licenses dialog box](#) , which you use to add passwords to the password file.

## Add License dialog box

The Add License dialog box is used to add SPECCTRA node-locked licenses to the license file on UNIX systems. Use the license information sheet sent with the software to enter the correct information in the dialog box.

Click on the following topics to get information about the Add License dialog box.

[Exclamation point](#)

[Password file](#)

[Host ID](#)

[Feature](#)

[Model](#)

[Version](#)

[Expiration date](#)

[Password key](#)

### Note

This dialog box is for adding node-locked licenses only. You must use the SPECCTRA installation script to add network licenses. See the installation instructions provided with your SPECCTRA software shipment for details.

## Add\_Password dialog box

Use the Add\_Password dialog box to add SPECCTRA licenses to the password file on Windows and Windows NT systems. Use the license information sheet sent with the software to enter the correct information in the dialog box.

Click on the following topics to get information about the Add\_Password dialog box.

[Exclamation point](#)

[Password file](#)

[Host ID](#)

[Feature](#)

[Model](#)

[Version](#)

[Expiration date](#)

[Password key](#)

## **Exclamation point**

Displays error messages about license information entered in the Add Licenses dialog box.

## License file

Displays the name of the license file to be edited. The license file is set in the Startup dialog box.

## **Password file**

Displays the name of the password file to be edited. The password file is set in the Startup dialog box.

## Host ID

The identification number for the system where your SPECCTRA software is installed.

On a Windows or Windows NT system, this is the label on the security key.



## Feature

The license feature name. The following table shows license feature names and the SPECCTRA configurations.

Feature	Configuration
ViewBase	Base SPECCTRA license
RouteBase	Base AutoRoute license for maximum 255 signal layers
Route2	Base AutoRoute license for maximum 2 signal layers and 4000 component pins
Route4P	Base AutoRoute license for maximum 4 signal layers and 4000 component pins
RouteADV	AutoRoute ADV option
RouteDFM	AutoRoute DFM option
RouteHYB	AutoRoute HYB option
Route FST	AutoRoute FST option
EditBase	Base EditRoute license
EditFST	EditRoute FST option
PlaceBase	Base AutoPlace licenses
IPlaceBase	

## Model

The SPECCTRA model number as it appears on the license information sheet.

## Version

The SPECCTRA software version number.

## Expiration date

The license expiration date in the format MM/DD/YYYY.

## **Password key**

The password as it appears on the license information sheet.

## **File Menu**

### **Reads and writes files, and exits SPECCTRA**

Most of the File menu commands bring up a dialog box that contains a data entry box and a Browse button. You can use the keyboard to type all or part of a directory path and filename. You can also click the Browse button to open the file selector dialog box, and use the pointer to choose the directory and the file you want.

The File menu commands are

Read

Write

Execute Do File

Autosave

Bestsave

Did File

Status File

Placement Mode

Quit

## File - Read

### Loads a wires, routes, or colormap file

A [wires file](#) and a [routes file](#) contain routing information from a previous routing session. A colormap file maps colors and fill patterns to objects. The File - Read menu commands are

[Wires](#)

[Routes](#)

[Colormap](#)

### Note

A wires file is created by using the **File - Write - Wires** command. A routes file is created by using the **File - Write - Routes** command.

## **File - Read - Wires**

### **Loads a SPECCTRA wires file**

The wires file is a text file that contains wire and via information. The wires file is used to load the wiring from a previous routing session.

If the wires you read have paths and shapes that are identical to existing wires, the duplicates in the wires file are discarded.

The Read Wires dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Note**

The difference between a routes file and a wires file is that the routes file can be used to return the routed wires to your PCB layout system and the wires file cannot.

## **File - Read - Routes**

### **Loads a SPECCTRA routes file**

The routes file is a text file that contains net, path, wire, and via information. The routes file serves two purposes:

- To return the routed wires to the PCB layout system
- To restore the routed wires from a previous autorouting session in the current autorouting session

The Read Routes dialog box contains a data entry box, a Browse button, and the following option. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

**ECO Mode (Ignore Net Names)**, which ignores net names in the Net\_out section of the routes file so that an engineering change can be made using the routes file. When ECO mode is on, SPECCTRA determines net names according to the wires, pins, and vias in the design. The default is off (SPECCTRA does not ignore net names).

If the wires you read from the routes file have paths and shapes that are identical to existing wires, the duplicates in the routes file are discarded.

### **Note**

The difference between a routes file and a wires file is that the routes file can be used to return the routed wires to your PCB layout system and the wires file cannot.



## File - Read - Colormap

### Loads a SPECCTRA color map file

A [color map](#) file is a text file that defines colors used in the SPECCTRA work area and assigns colors and fill patterns to design objects and graphical features.

The Read Colormap dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

You can read a color map file containing any number of definitions or assignments. You can also assign user-defined fill patterns. An example of a color map file follows.

```
(colors
  (color 0 black    170 210 255)
  (color 1 blue     0   0 255)
  (color 2 green    0 255   0)
  (color 3 violet  175   0 175)
  (color 4 red     255   0   0)
  ...
  (set_color background black)
  (set_color via violet)
  (set_color via_keepout red)
  (set_color pin blue)
  (set_color area green)
  ...
  (set_pattern background solid)
  (set_pattern via solid)
  (set_pattern pin solid)
  (set_pattern keepout slantrightpat)
  ...)
```

You can create your own fill patterns by using a bitmap editor. Make sure the bitmap file has the .bit filename extension, and copy it into either the directory where you start SPECCTRA or the cfg directory under the SPECCTRA installation directory. For example, to assign a fill pattern defined in the bitmap file named dotpat.bit to signal layer 1, add the following line to your color map file:

```
(set_pattern signal 1 dotpat)
```

You can also specify a color map file when you start SPECCTRA, either by using the -c switch or by using a file named color.std in the directory where you start SPECCTRA. See chapter 2 in the *SPECCTRA User's Reference* manual for details.

If you do not specify a color map file, SPECCTRA uses colors and fill patterns defined and mapped in the design file, or internal defaults. See the *SPECCTRA Design Language Reference* manual for details about default colors and fill patterns.

**See also**

[File - Write Colormap](#)

## **File - Write**

### **Saves design data in text files**

The File - Write menu commands are

Wires

Routes

Network

Conflicts

Padstacks

Corners

Session

Colormap

## File - Write - Wires

### **Saves wiring in a wires file**

The [wires file](#) includes wire and via information.

The Write Wires dialog box contains a data entry box, a Browse button, and the following options. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

**Include Testpoints** adds testpoint records to the wires file.

**Write Only Selected Wires** saves wire and via information for only the selected wires.

### **Notes**

You can load a wires file with your design file when you start SPECCTRA by entering the filename in the Startup dialog box or by using the -w command line switch. See the *SPECCTRA User's Reference* manual for more information about command line switches.

A routes file is the suggested means for saving wiring for subsequent autorouting sessions.

## File - Write - Routes

### **Saves all wiring in a routes file**

The [routes file](#) contains wire and via information. This file contains the wiring data that you merge with your original PCB layout.

The Write Routes dialog box contains a data entry box, a Browse button, and the following options. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

**Include Testpoints** adds testpoint records to the routes file.

**Include Guides** adds guide information to the routes file so that, if any connections are not routed, the host system can determine the topology used in SPECCTRA.

**Write Only Selected Wires** places only the selected wires in the routes file.

### **Note**

The routes file is the suggested means for saving and reloading the wiring in subsequent autorouting sessions. You can load a routes file with your design file when you start SPECCTRA by entering the filename in the Startup dialog box or by using the -w command line switch. See the *SPECCTRA User's Reference* manual for more information about command line switches.

## **File - Write - Network**

### **Saves the netlist in a text file**

The network file contains the netlist. It includes net names and fromtos (pin to pin connections). The network file is used for checking and documentation purposes.

The Write Network dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Tip**

You can view a summary of the network data in a report by clicking [Report - Network](#).

## **File - Write - Conflicts**

### **Saves conflicts in a text file**

The conflicts file lists crossover and clearance conflicts. Each conflict occupies a separate line and is enclosed in parentheses. Conflicts are marked as either a cross (crossing) or near (clearance) type and include the X,Y location in database units.

The Write Conflict dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Tip**

You can view a summary of the conflicts in a report by clicking [Report - Conflicts](#).

## File - Write - Padstacks

### **Saves padstack data in a text file**

The padstack file contains definitions of all padstacks included in your SPECCTRA design file. This file lists the via, pin, and SMD padstacks from the library section of the design file.

Each padstack is identified by the *padstack* keyword, which is followed by a name or id. Each padstack shape is identified by a keyword such as circle, rect, or poly, and accompanied by a layer id and dimensions, which are represented in database units.

The Write Padstacks dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Tip**

You can view a summary of padstack information by clicking [Report - Padstacks](#).

### **Note**

For additional information on the design file, see the *Design Language Reference* manual.

## **File - Write - Corners**

### **Saves the corners data in a text file**

The corners file identifies layer and X,Y coordinate locations of 90-degree wire corners. X,Y coordinates are in database units (DBUs). You can use the resolution statement at the beginning of the corners file to convert DBUs into working units. If you want to convert DBUs to working units, divide X,Y coordinate values by the resolution value.

The Write Corner dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Tip**

You can view a corners report by clicking [Report - Corners](#).



## File - Write - Session

### **Saves all SPECCTRA session information in a session file**

A session file contains the original design filename as well as placement, floor plan, swap, netlist, and route data generated during a SPECCTRA session. The session file provides a convenient way to track and load all data associated with a SPECCTRA placement or routing session. The session file can be loaded instead of a design file when you start SPECCTRA, but the design file must be available.

The **File - Write - Session** dialog box contains a data entry box to enter a filename, a data entry box with a check box to include a comment in your session file, and a Browse button.

The Write Session dialog box contains a data entry box, a Browse button, and the following option. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

**Include Comment** adds a comment to the session file. The comment is added at the near the beginning of the session file for documentation purposes.

### **Note**

The session file does not include any rule changes you make during the session. If you start SPECCTRA with a session file to restart the session, you must set the rules again to establish the previous session conditions.

## File-Write-Colormap

### **Saves all current SPECCTRA color map data in a text file**

You can use a [color map](#) file to save the current color definitions for the SPECCTRA work area and the current colors and fill patterns assigned to design objects and graphical features.

The Write Colormap dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Notes**

Use this command to save colors or fill patterns you loaded when you started SPECCTRA or by using [File - Read - Colormap](#) during the session. See Chapter 2 in the *SPECCTRA User's Reference* manual for details about starting SPECCTRA with a color map file.

SPECCTRA uses colors and fill patterns from the design file, or internal defaults, if you do not use a color map file. See the *SPECCTRA Design Language Reference* manual for information about color and fill pattern definitions and defaults.

## **File Menu**

### **Reads and writes files, and exits SPECCTRA**

Most of the File menu commands bring up a dialog box that contains a data entry box and a Browse button. You can use the keyboard to type all or part of a directory path and filename. You can also click the Browse button to open the file selector dialog box, and use the pointer to choose the directory and the file you want.

The File menu commands are

Read

Write

Execute Do File

Did File

Routing Mode

Quit

## **File - Read**

### **Loads a placement or floor plan file**

A placement file is created by using the **File - Write - Placement** command. A floor plan file is created by using the **File - Write - Floor Plan** command. The File - Read menu commands are

[Placement](#)

[Floor Plan](#)

[Colormap](#)

## **File - Read - Placement**

### **Loads a SPECCTRA placement file**

The placement file contains placement information. The placement file serves two purposes:

- To return the placement information to the PCB layout system
- To restore placement information from a previous placement session

If you have results from multiple placement trials, you can load your design first and then read each placement file.

The Read Placement dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Tip**

When you're placing a more difficult PCB, you can apply different rules and constraints over several placement trials, and save the results of each trial in a separate placement file.

## **File - Read - Floor Plan**

### **Loads a SPECCTRA floor plan file**

The SPECCTRA floor plan file is a text file that contains information for room and cluster definitions. All existing rooms and clusters are deleted when a new floor plan file is read.

The Read Floor Plan dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Tip**

When you are placing a difficult PCB, you can create several different floor plans and save the floor plan for each trial in a separate file.

## **File - Write**

### **Saves design data in text files**

The File - Write menu commands are

[Placement](#)

[Floor Plan](#)

[Session](#)

[Colormap](#)

## **File - Write - Placement**

### **Saves all component placements to a placement file**

The placement file includes the X,Y coordinate location, and the side (mounting surface), rotation, and lock status, for each component in the design. This file contains the placement information that gets merged with your original PCB layout. Placement information is written for each instance of a component image.

The Write Placement dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Note**

Use a placement file to save the current component placement information for use in a subsequent SPECCTRA session. When you are placing a difficult PCB, you can apply different rules and constraints over several placement trials and save the results of each trial in a separate placement file.



## **File - Write - Floor Plan**

### **Saves all room and cluster data in a floor plan file.**

The floor plan file is a text file that contains the data needed to define clusters and rooms. Room rules are cluster assignments, component assignments, height restrictions, and power dissipation limits.

The Write Floor Plan dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Note**

Use a floor plan file to save current cluster and room definitions for use in a subsequent placement session.

## **File - Execute Do File**

### **Runs a do (command) file**

The do file contains a sequence of SPECCTRA commands. Each line in the do file consists of a single command. SPECCTRA executes the commands in sequence, from the start of the file to the end of the file. If a command or keyword is misspelled, or a syntax error is encountered, execution of the do file is terminated.

The Execute Do File dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

### **Note**

The filename extension that usually identifies a do file is .do, but you can use any filename or extension.

## File - Autosave

### Controls whether a wires file is written after every routing pass

The Autosave dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

When autosave is enabled, a wires file is written after every routing pass. Autosave can add time to an autorouting session if you're routing a large design that is converging slowly. The default is disabled.

### Tip

Use [File - Bestsave](#) instead of Autosave as a more efficient way to save intermediate results during an autorouting session.

## File - Bestsave

### Controls whether a wires file is written after routing results improve

The Bestsave dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

When bestsave is enabled, a wires file is written at the end of a routing pass if routing improved as compared to the previous save. SPECCTRA uses the following method to determine whether routing has improved.

$$\text{pass score} = (\text{crossing violations} + \text{clearance violations} + \text{crosstalk violations} + \text{length violations} + (2 \times \text{unroutes}))$$

If the current pass score is lower than the previous best pass score, routing is saved.

You can use the wires file created by the **File - Bestsave** to recover your work in the event of a system failure. The default is disabled.

## File - Did File

### **Controls whether a did file is created during a SPECCTRA session**

The Did File dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

When Enable is specified in the Did File dialog box, every command you try to execute in SPECCTRA is recorded into a [did file](#). The default is disable.

You can edit a did file to create a script, called a [do file](#), that you can use later to run another SPECCTRA session.

## File - Status File

### **Sets the path, filename, and update interval of the status file**

The [status file](#) contains routing status information. SPECCTRA updates this file at regular intervals. You use this status file to analyze routing results. The default status filename is monitor.sts.

The Status File dialog box contains a data entry box and a Browse button. You can enter a path and filename in the data entry box, or click the Browse button and choose a filename in the file selection dialog box that appears.

The Update Interval determines the frequency of updates to the status file. SPECCTRA automatically updates the status file after every 100 connections or the end of a pass.

### **Note**

The default update interval of 100 minimizes the impact on performance while producing sufficient routing status data to analyze results. Smaller update intervals can affect performance by forcing the autorouter to write status results more frequently. If you reduce the interval, routing time increases.

## **File - Placement Mode**

### **Changes from Routing mode to Placement mode.**

**File - Placement Mode** changes the Graphical User Interface to the placement menubar, toolbar, and status area. If you have a license for the placement tool, you can use Placement Mode to automatically or interactively place or relocate components.

### **Note**

Clicking the Place icon on the toolbar also changes from Routing mode to Placement mode.

## File - Routing Mode

**Changes from Placement mode to Routing mode.**

**File - Routing Mode** changes the Graphical User Interface to the routing menubar, toolbar, and status area. If you have a license for automatic or interactive routing, you can use Routing Mode to route wires between placed components.

### Note

Clicking the Routing icon on the toolbar also changes from Placement mode to Routing mode.



## File - Quit

### Exits SPECCTRA

When you click **File - Quit**, a message popup displays and prompts you to confirm (Quit) or cancel (Don't Quit). If you click Quit, SPECCTRA immediately exits. If you click Don't Quit, you return to SPECCTRA.

If you click **File - Quit** when an automatic operation is in progress, the operation pauses, the message popup appears, and you're prompted to confirm or cancel. If you click Don't Quit, the message popup closes and the operation resumes. If you click Quit, SPECCTRA immediately exits without saving the routing or placement data.

### Tip

Make sure you save your placement data, floor plan data, and routed wires before you use **File - Quit**.

## Edit Menu

**Deletes, restores, fixes, unfixes, protects, and unprotects objects**

The Edit menu commands are

[Undo](#)

[Redo](#)

[Delete Wires](#)

[Delete All Fences](#)

[Delete All Wirebonds](#)

[\[Un\] Fix Nets](#)

[\[Un\] Fix Nets By Class List](#)

[\[Un\] Protect Wires By Net](#)

[\[Un\] Protect All Testpoints](#)

[\[Un\] Protect Wires By Class List](#)

[\[Un\] Protect Wires By Layer List](#)

## Edit Menu

**Deletes and restores objects, and locks and unlocks components**

The Edit menu commands are

Undo

Redo

Delete Wires

Delete All Wirebonds

[Un]Lock Components

[Un]Lock Components Mode

## Edit - Undo

### Reverses an interactive editing operation

You can reverse a single interactive editing operation by clicking **Edit - Undo**. You can reverse a series of interactive editing operations by entering a series of undo commands or by using a shortcut key. The shortcut keys are [F3] or [Undo] on your keyboard.

The interactive routing and editing operations that you can reverse are

- Edit Route
- Move Route
- Copy Route
- Critic Route
- Change Via
- Change Wire
- Cut Segment
- Delete Segment
- Delete Wire
- Delete Net

**Repair Net** cannot be reversed with **Edit - Undo**.

### Note

The **undo** keyboard command is the same as **Edit - Undo**.

## Edit - Redo

**Reapplies an interactive routing or editing operation that was reversed by the Edit - Undo command**

Using **Edit - Redo**, you can immediately redo an operation that you reversed by clicking **Edit - Undo**. You can redo a series of undo operations by entering multiple redo commands or by using a shortcut key. The shortcut keys are [Shift][F3] or [Shift][Undo].

The interactive routing and editing operations that you can reapply are

- Edit Route
- Move Route
- Copy Route
- Critic Route
- Change Via
- Change Wire
- Cut Segment
- Delete Segment
- Delete Wire
- Delete Net

### Note

The **redo** keyboard command is the same as **Edit - Redo**.

## Edit - Delete Wires

The Edit - Delete Wires menu commands are:

[By Selected Nets](#)

[All Wires](#)

[By Net List](#)

[Conflict Wires](#)

[Conflict Wire Segments](#)

[Incomplete Wires](#)

[Redundant Wires](#)

## Edit - Delete Wires - By Selected Nets

### **Deletes all selected wires**

You can delete all wires on one or more nets by selecting the nets and then using **Edit - Delete Wires - By Selected Nets**. You can use one of the **Select - Nets** commands to select the nets.

Wires and vias that are protected, and wires and vias attached to fixed nets, are not deleted.

## **Edit - Delete Wires - All Wires**

### **Deletes all wires**

Wires and vias that are protected or belong to fixed nets are not deleted.



## Edit - Delete Wires - By Net List

### **Deletes specific wires from the netlist**

This command removes wires and vias attached to specific nets. The Delete Wires By Net List dialog box contains a [Filter](#) and a [Nets list](#).

Wires and vias that are protected or attached to fixed nets are not deleted.

## Edit - Delete Wires - Conflict Wires

### **Deletes connections involved in conflicts**

This command deletes complete pin-to-pin connections rather than individual segments involved in conflicts. It deletes one of the two wires involved in each conflict.

#### **Note**

See also [Edit - Delete Wires - Conflict Wire Segments](#) and [Autoroute - Postroute - Filter Routing](#)

## Edit - Delete Wires - Conflict Wire Segments

### **Deletes wire segments involved in conflicts**

This command deletes only a segment involved in a conflict rather than the entire pin-to-pin connection. It deletes one of the two segments involved in each conflict.

#### **Note**

See also [Edit - Delete Wires - Conflict Wires](#) and [Autoroute - Postroute - Filter Routing](#)

## **Edit - Delete Wires - Incomplete Wires**

### **Deletes incomplete connections**

This command removes partially routed connections. Incomplete connections can be created in the PCB layout system or by deleting wire segments involved in conflicts. SPECCTRA doesn't remove incomplete connections when you load the design.

## **Edit - Delete Wires - Redundant Wires**

### **Deletes redundant wires on the same net**

If you are routing interactively, you can create redundant wires on the same net. Use this command to delete the redundant wires.

## Edit - Undo

### Reverses an interactive placement command operation

You can reverse a single interactive placement operation by clicking **Edit - Undo**. You can reverse a series of interactive placement operations by entering a series of undo commands or by using a shortcut key. The shortcut keys are [F3] or [Undo] on your keyboard.

You can reverse the following commands:

- align
- lock
- place
- push
- relocate (pivot, flip, and move)
- trade
- unlock
- unplace

When you use **Edit - Undo**, the command it reverses is saved in memory. You can use **Edit -Redo** to reapply a command reversed by **Edit - Undo**.

### Note

The **undo** keyboard command is the same as **Edit - Undo**.

## Edit - Redo

**Reapplies an interactive placement command operation that was reversed by the Edit - Undo command**

Using **Edit - Redo**, you can immediately redo an operation that you reversed by clicking **Edit - Undo**. You can redo a series of undo operations by entering multiple redo commands or by using a shortcut key. The shortcut keys are [Shift][F3] or [Shift][Undo].

You can reapply the following commands:

- align
- lock
- place
- push
- relocate (pivot, flip, and move )
- trade
- unlock
- unplace

When you use **Edit - Undo**, the command it reverses is saved in memory. **Edit - Redo** reapplies that command and clears it from memory.

### Note

The **redo** keyboard command is the same as **Edit - Redo**.

## Edit - [Un]Lock Components

### Locks or unlocks component locations, gates, and pins

Locking components in position prevents inadvertent movement or swapping during automatic and interactive placement operations. Locked components cannot be moved by any SPECCTRA operation. Locked gates, subgates, and pins cannot be swapped. When a component is locked, the displayed outline of the component is changed to a thicker line width.

The [Un] Lock Components dialog box is used to lock and unlock components. This dialog box contains the following:

**Selected** locks or unlocks selected components.

**All** locks or unlocks all components.

**By List** locks or unlocks components you mark in the [Components list](#) box. You can use the [filter](#) to choose components in the Components list.

### Action

**Lock** locks the components after you click Apply or OK.

**Unlock** unlocks the components after you click Apply or OK.

### Lock Type

**Position** locks the location of the components.

**Gate** prevents gates from being swapped.

**SubGate** prevents subgates from being swapped.

**Pin** prevents pins from being swapped.



## Edit - Delete All Fences

### **Removes all routing fences**

A fence is an area that controls how the enclosed connections are routed. A fence can be either [hard](#) or [soft](#).

### **Note**

See also [Define - Draw Fence Mode](#) [Define - Fence](#) and [Soft - Fence](#).

## Edit - Delete All Wirebonds

### **Deletes all wirebond sites and attached wires**

This command deletes all bond sites and wires that were created by using **AutoRoute - Pre Route - Wirebonds**.

### **Note**

See also [Autroute - Pre Route - Wirebonds](#).

## Edit - [Un] Fix Nets

### Fixes or unfixes nets

Fixing completely isolates a net. Once a net is fixed, the autorouter can neither move any part of the net (same as protect) nor route to any point on the net. If you fix a net that is completely or partially routed, the wires cannot be deleted, or ripped up and rerouted. Wires of fixed nets are treated as keepouts and cannot be involved in conflicts.

The [Un] Fix Nets by List dialog box is used to fix and unfix selected nets marked in the Nets listing. This dialog box contains the following:

**Selected** fixes or unfixes selected nets.

**By List** fixes or unfixes nets you mark in the [Nets list](#). You can use the [filter](#) to choose nets in the Nets list.

### Action

**Fix** fixes the nets after you click Apply or OK.

**Unfix** unfixes the nets after you click Apply or OK.

## Edit - [Un] Fix Nets By Class List

### Fixes or unfixes nets defined in a class

Fixed nets are hidden from the autorouter. When a class of nets is fixed, the autorouter can't move wires or vias attached to the nets, and can't route to wires and vias attached to the nets. If you fix a class of nets that is completely or partially routed, the wires cannot be deleted and cannot be ripped up and rerouted. Wires attached to fixed net classes are treated as keepouts and cannot be involved in conflicts.

The [Un] Fix Nets by Class List dialog box is used to fix and unfix nets defined as a class. This dialog box contains the following:

[Filter data entry box](#)

[Classes list](#)

### Action

**Fix** fixes the nets after you click Apply or OK.

**Unfix** unfixes the nets after you click Apply or OK.

## Edit - [Un] Protect Wires By Net

### Protects, unprotects, and "soft protects" nets

The paths of protected wires and the locations of protected vias cannot be changed by the autorouter. However, the autorouter can route to a protected via, a protected wire at its terminals, or if tjunctions are allowed, to a protected wire segment. For example, you can fanout a component, protect the fanout wires and vias, and then route the PCB. Wires are routed to fanout vias even though they are protected.

The [Un] Protect Wires By Net dialog box is used to protect, unprotect, and "soft protect" nets. If a net is set to "soft", the autorouter can push and shove it to make room when space is needed but cannot reroute the connection.

The [Un]Protect Wires By Net dialog box contains the following:

**All** protects all nets

**Selected** protects nets you previously selected

**By List** protects nets that you choose from a [Nets list](#). You can use the [filter](#) to choose nets in the Nets list.

### Action

**Protect** protects nets.

**Soft Protect** sets nets to "soft," which means it can be pushed and shoved by the autorouter.

**UnProtect** unprotects nets.

**Wiring Attributes** determines whether wires with the fanout, bus, and testpoint attributes are protected or unprotected. The following attributes are assigned when a wire or via is added with a particular command:

**Bus** is assigned when wires are created by using  
**AutoRoute - Pre Route - Bus Routing.**

**Fanout** is assigned when wires are created by using  
**AutoRoute - Pre Route - Fanout.**

**Test** is assigned when wires are created by using  
**AutoRoute - Post Route - Testpoints.**

### Note

Protect and unprotect functions apply to routed wires only. See [Edit - \[Un\] Fix Nets](#) and [Edit - \[Un\] Fix Nets By Class List](#) to control the routing of nets and fromtos.

## Edit - [Un] Protect All Testpoints

### Protects and unprotects testpoints

A testpoint is a pin or via assigned to each net for testing purposes. Testpoints are created by [AutoRoute - Post Route - Testpoints](#).

The [Un] Protect All Testpoints dialog box is used to protect and unprotect test vias and through-pin testpoints, and contains the following choices:

#### Action

**Protect** protects test vias and through-pin testpoints.

**Unprotect** unprotects test vias and through-pin testpoints.

## Edit - [Un] Protect Wires By Class List

### **Protects, unprotects, and "soft protects" wires assigned to one or more classes**

The paths of wires and locations of vias in a protected class cannot be changed by the autorouter. However, the autorouter can route to a protected via, a protected wire at its terminals, or if tjunctions are allowed, to a protected wire segment. For example, you can fanout a component, protect the fanout wires and vias, and then autoroute. Wires are routed to fanout vias even though they are protected.

The [Un] Protect Wires By Class List dialog box is used to protect, unprotect, and "soft protect" wires and vias attached to nets in the class. If a wire is set to "soft", the autorouter can push and shove it to make room when space is needed. This dialog box contains the following:

[Filter data entry box](#)

[Classes list](#)

#### **Action**

**Protect** protects wires in a class.

**Soft Protect** sets wires in a class to "soft," which means the wires can be pushed and shoved by the autorouter.

**UnProtect** unprotects wires in a class.

**Wiring Attributes** specifies whether wires with the bus, fanout, and test attributes are protected or unprotected. The following attributes are assigned when a wire is created with a particular command:

**Bus** is assigned when wires are created by using **AutoRoute - Pre Route - Bus Routing**

**Fanout** is assigned when wires are created by using **AutoRoute - Pre Route - Fanout**

**Test** is assigned when wires are created by using **AutoRoute - Post Route - Testpoints**

## Edit - [Un] Protect Wires By Layer List

### **Protects, unprotects, or "soft protects" wires assigned on one or more layers**

The paths of protected wires and the locations of protected vias cannot be changed by the autorouter. However, the autorouter can route to a protected via, a protected wire at its terminals, or if tjunctions are allowed, to a protected wire segment. For example, you can fanout a component, protect the fanout wires and vias, and then autoroute. Wires are routed to fanout vias even though they are protected.

The [Un] Protect Wires By Layer List dialog box is used to protect, unprotect, and "soft protect" wires and vias on a layer. If a wire is set to "soft", the autorouter can push and shove it to make room when space is needed. This dialog box contains the following:

[Filter data entry box](#)

[Layers list](#)

#### **Action**

**Protect** protects wires by layer.

**Soft Protect** sets wires on a layer to "soft," which means wires on the layer can be pushed and shoved by the autorouter.

**Unprotect** unprotects wires by layer.

**Wiring Attributes** specifies whether wires on the layer with bus, fanout, and test attributes are protected or unprotected. The following attributes are assigned when a wire is created with a particular command:

**Bus** is assigned when wires are created by using **AutoRoute - Pre Route - Bus Routing**

**Fanout** is assigned when wires are created by using **AutoRoute - Pre Route - Fanout**

**Test** is assigned when wires are created by using **AutoRoute - Post Route - Testpoints**



## View Menu

**Alters or repaints the work area display, displays the layer panel, and sets the mouse mode to measure**

The View menu commands are

Highlight

Unroutes

Layers

Repaint

All

Fit Selected Comps/Nets

Previous

Shadow Mode

Zoom In

Zoom Out

Split View

Component Labels

Measure Mode

## View - Highlight

Highlighting only graphically emphasizes objects. The highlighting has no affect on how SPECCTRA processes the object.

The View - Highlight menu provides a range of choices for highlighting different PCB objects. The menu commands are

Highlight Mode

Component Nets

Off

Components By List

Nets By List

Wires By Shielding

Bends

Pins

SMD Pads Without Fanouts

Nets Without Testpoints

Incomplete Wires

Redundant Wires

Last Loads of Nets

Off Grid

### Note

You can change the default highlight color (white) by defining the highlight color in a [color map file](#). Use [File - Read - Colormap](#) after you create the color map file.

## View - Highlight - Highlight Mode

### Sets the left mouse button to highlight mode

After you set highlight mode, *Highlight* displays in the mode status area. Pins, wires, and vias on a net are highlighted graphically when you click them. Guides are also highlighted if you click a pin, wire, or via of a net that has unrouted connections.

### Notes

If you click a highlighted object when you are in Highlight Mode, the object is no longer highlighted.

Turn off highlighting by clicking **View - Highlight - Off**.

## View - Highlight - Component Nets

**Provides two methods for highlighting the nets attached to a component**

You can highlight nets attached to a component by using Highlight Comp Net mode or by choosing a component in a component list. The Component Nets menu commands are

[Highlight Comp Mode](#)

[By Component List](#)

## View - Highlight - Component Nets - Highlight Comp Mode

### Sets the left mouse button to highlight component net mode

After you click **View - Highlight - Component Nets - Highlight Comp Mode**, *Highlight Comp Net* appears in the mode status area.

When you click on a component in Highlight Comp Mode, the guides and wires of the nets attached to that component are highlighted as well as all component pins, wires, and vias of the attached nets. Power nets are not highlighted.

If you click a highlighted object when you are in Highlight Comp Mode, the object is no longer highlighted.

### Note

To turn off all highlighting, click **View - Highlight - Off**.

## View - Highlight - Component Nets - By Component List

### Highlights nets attached to components by picking from a list

When you choose Highlight in the Action area of the Highlight Component Nets dialog box, click a component reference designator in the Components list, and click Apply or OK, all parts of the net including guides, wires, pins, and vias are highlighted. Power nets are not highlighted.

The Highlight Component Nets dialog box contains a [Filter data entry box](#) and a [Components list](#) of components in your design.

**Highlight** graphically emphasizes the specified components after you click Apply or OK.

**Unhighlight** removes the graphic emphasis on the specified components after you click Apply or OK.

### Notes

This does not change the left button mouse mode.

To turn off all highlighting, click [View - Highlight - Off](#).

## **View - Highlight - Off**

**Removes highlighting and restores all highlighted objects to normal display status**

When you click **View - Highlight - Off**, all highlighted objects are reset to normal display status and the screen repaints.

## View - Highlight - Components By List

### Highlights components by picking from a list of reference designators

When you choose Highlight in the Action area of the Highlight Components dialog box, click a component reference designator in the Components list, and click OK or Apply, outlines and pins of the components marked in the list are highlighted.

The Highlight Components dialog box includes a [Filter data entry box](#) and a [Components list](#).

### Action

**Highlight** graphically emphasizes the specified components after you click Apply or OK.

**Unhighlight** removes the graphic emphasis on the specified components after you click Apply or OK.

### Notes

This does not change the left button mouse mode.

To turn off all highlighting, click [View - Highlight - Off](#).



## View - Highlight - Nets By List

### Highlights or unhighlights nets from a list of nets

When you apply the Highlight Nets dialog box with Highlight on, all pins, wires, vias, components, and guides attached to nets marked in the list are highlighted.

The Highlight Nets dialog box includes a [Filter](#) and a [Nets list](#).

### Action

**Highlight** graphically emphasizes the specified nets after you click Apply or OK.

**Unhighlight** removes the graphic emphasis on the specified nets after you click Apply or OK.

### Notes

This command does not change the left button mouse mode.

To turn off all highlighting, click [View - Highlight - Off](#).

## View - Highlight - Wires By Shielding

**Highlights all wires with shields or all wires that are missing their shields.**

Use this command to see shielded wires or wires that are supposed to be shielded but are missing their shields. The View - Highlight - Wires By Shielding menu commands are

- Wires With Shields
- Wires Missing Shields

### Notes

To turn off all highlighting, click [View - Highlight - Off](#).

## View - Highlight - Bends

### Highlights wires with 90- or 45-degree bends

Use this command to see 90- or 45-degree corners after using the **miter** or **recorner** command. The View - Highlight - Bends menu commands are

- 90-degree bends
- 45-degree bends

### Notes

To turn off all highlighting, click [View - Highlight - Off](#).

## View - Highlight - Pins

### Highlights component pins

You can highlight a pin on a specific component or a pin on all components. The Highlight Pins dialog box contains the following:

**By Component Pin**, in which you enter the reference designator and the pin number of the pin you want to highlight.

**By Image Pin**, in which you enter the pin number that you want to highlight. Pins with that number in the image description of the design file are highlighted.

### Action

**Highlight** graphically emphasizes the specified pins after you click Apply or OK.

**Unhighlight** removes the graphic emphasis on the specified pins after you click Apply or OK.

### Note

To turn off all highlighting, click [View - Highlight - Off](#).

## View - Highlight - SMD Pads Without Fanouts

### Highlights SMD pads that are missing a wire with the fanout property

This command visually identifies fanout failures that occurred during the last fanout command. After you click [Autoroute - Pre Route - Fanouts](#), the autorouter attaches the fanout property to fanout wires and vias. Use **View - Highlight - SMD Pads Without Fanouts** to highlight pads that didn't fan out during the last fanout command.

### Notes

**View - Highlight - SMD Pads Without Fanouts** highlights single pin nets that are not fanned out.

To turn off all highlighting, click [View - Highlight - Off](#).

## View - Highlight - Nets Without Testpoints

### Highlights all nets without a testpoint

This command visually identifies testpoint failures. **View - Highlight - Nets Without Testpoints** is available with the DFM option.

You can use [Autoroute - Post Route - Testpoints](#) to add a testpoint to each net in your design. After you add testpoints, you can check for testpoint failures by using **View - Highlight - Nets Without Testpoints**.

### Notes

**View - Highlight - Nets Without Testpoints** does not highlight power nets, single pin nets, and unused pins.

To turn off all highlighting, click [View - Highlight - Off](#).

## View - Highlight - Incomplete Wires

### Highlights dangling wires that don't complete a connection

Incomplete wires occur when you delete wire segments or stop the autorouter while it is routing. You can highlight incomplete wires to determine their location.

#### Notes

To turn off all highlighting, click [View - Highlight - Off](#).

To delete incomplete wires, see [Edit - Delete Wires - Incomplete Wires](#)

## View - Highlight - Redundant Wires

### Highlights extra wire segments and vias on power nets

In the interactive routing tool, you can allow redundant power wiring. This can add extra wire segments and vias on power nets. You can highlight these power nets to determine their location.

### Notes

To turn off all highlighting, click [View - Highlight - Off](#).

To delete redundant wires, see Edit - [Delete Wires - Redundant Wires](#)



## View - Highlight - Last Loads of Nets

**Highlights component pins which were the last on a net to be assigned a load property**

This command is useful for swapping ECL terminator pins. If you used the **order daisy** command and assigned source, load, and terminator properties, you can use **View - Highlight - Last Loads of Nets** to highlight the last load pins on the net and see how they connect to the terminator pins. Use [Autoplace - Automatic Swap](#) to swap the terminator pins.

### Notes

To turn off all highlighting, click [View - Highlight - Off](#).

You can also use the keyboard command **rule reorder daisy** to swap terminator pins.

## View - Highlight - Off Grid

### Highlights routing objects that are off-grid

The **View - Highlight - Off Grid** command displays a cascade-menu from which you can choose the off-grid components, pins, wires, and vias for highlighting. If you want to highlight all off-grid objects, click **All** on the menu.

The View - Highlight - Off Grid menu choices are

**Components**, which highlights components whose origins are not on a placement grid

**Pins**, which highlights all pins that are not on a wire grid

**Wires**, which highlights all wires that are not on a wire grid

**Vias**, which highlights all vias that are not on the via grid

**All**, which highlights all off-grid objects

### Note

To turn off all highlighting, click [View - Highlight - Off](#).

## View - Unroutes

### Controls how unroutes display

Your choices on the View - Unroutes menu are

**All** displays all unroutes

**Placed** displays unroutes for all placed components

**Last** displays unroutes for the last component placed (using **View - Unroutes** in the placement environment)

**Front** displays unroutes for components on the front side of the PCB

**Back** displays unroutes for components on the back side of the PCB

**Between** displays unroutes between components on the front and back sides of the PCB

**Selected** displays unroutes for all selected components

**Highlighted** displays unroutes for all highlighted components

**Off** turns off the display of unroutes

## View - Layers

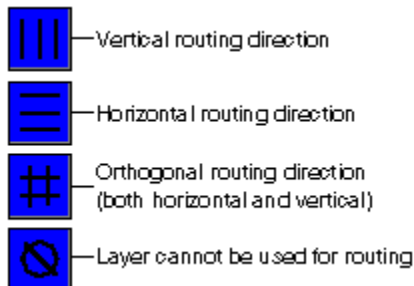
### Controls layer visibility, selection for routing, and routing direction

When you click **View - Layers**, the layer panel appears.



The layer panel indicates the status of signal, power, and system layers. Each row of buttons represents a layer of the design or a system layer. The buttons control whether the layer is selected for routing, the layer's route direction, and whether it's visible.

Layer selection and routing direction are controlled by a single button. When you click this button, the button graphic changes to one of four images. The button graphics and their meanings are



The button labeled S determines whether objects can be selected on the layer. When the S is visible, objects on the layer can be selected. If the S is not visible, objects on the layer cannot be selected.

Layer visibility is controlled by clicking the layer ID button, which is labeled with the layer name. Each time you click a layer ID button, layer visibility toggles to the opposite state.

### Note

The All Signal Layers button changes the visibility and selectability of all signal layers.

## View - Repaint

### **Refreshes the work area of the SPECCTRA window**

Click **View - Repaint** to refresh all objects displayed in the work area, or click the Repaint icon on the [tool bar](#).

When you repaint, all visible layers are redrawn, but the layer set as primary in the layer panel is drawn last so it displays on top of all others.

## **View - All**

### **Displays the entire design**

**View - All** changes the view so that the entire design fits within the work area of the SPECCTRA window.

## View - Fit Selected Comps/Nets

**Displays the area of the design that contains selected nets and components**

**View - Fit Selected Comps/Nets** changes the view so that the selected nets and components fit within the work area of the SPECCTRA window. Use the commands on the Select menu to select objects.



## View - Previous

### **Displays the previous view**

**View - Previous** changes the view to the display you saw before you used **View - All**, **View - Zoom In**, or **View - Zoom Out**. It also changes the display to the previous view before you used the middle mouse button to zoom in or out or to pan to a new location.

## View - Shadow Mode

**Displays selected nets and components in their "normal" colors and dims all unselected objects**

The Shadow Mode dialog box contains the following:

**Normal Mode**, which displays objects according to their layer color. In Normal Mode, selected objects appear in the select color (yellow if you use the default color map).

**Shadow Mode**, which displays selected objects in their layer color and unselected objects in a dimmed color, based on the Brightness percentage specified.

**Brightness**, which sets the percentage of color that appears in dimmed objects in Shadow Mode. If you set the brightness to zero, the objects do not appear. If you set the brightness to 100, the objects appear in their "normal" colors.

### Tip

Shadow Mode is useful to use in dense designs to view selected nets.

## View - Zoom In

**Changes the view so that you see more detail**

**View - Zoom In** magnifies the display in the work area so you can see more detail. The display is magnified to twice its previous size, but only half as much of the design fits in the work area.

## View - Zoom Out

**Changes the view so that you see more of the design**

**View - Zoom Out** reduces the display in the work area so you can see more of the design. The display is reduced to half its previous size, but twice as much of the design fits in the work area.

## View - Split View

### Controls whether layers are displayed as a composite or in separate panels

Unless you change to split view, SPECCTRA displays all layers as a single composite overlay. Using **View - Split View**, you can view layers in up to eight separate panels. If the number of visible layers is more than the number of panels, layers overlay in one or more panels.

#### Note

**View - All**, and **View - Previous**, and Zoom and pan operations are disabled when split view is set to a number greater than one.

## View - Component Labels

**Displays component reference designators, pin IDs, image IDs, logical part IDs, and physical part IDs**

The View Component Labels dialog box contains the following:

**View Labels**, which displays or does not display the specified labels.

**Ref Des**, which are the component reference designators

**Ref Des and Pin IDs**, which are the component reference designators and the pin IDs

**Image ID**, which are the image IDs

**Logical Part ID**, which are the logical parts

**Physical Part ID**, which are the physical parts

You can turn on and off the labels on the front, back, or both sides of the PCB.

### Note

If you turn off **View Labels**, the layer that contains the labels is turned off. The Component Labels layer in the layer panel shows that the layer is off.

## View - Measure Mode

### Sets the left mouse button mode to Measure mode

You can measure distance between two points or extract information about objects and design rule violations. After you click **View - Measure Mode**, *Measure* appears in the mode status area.

### To measure the distance between two points

1. Click **View - Measure Mode**.
2. Drag the pointer between the two points you want to measure.
3. Release [LB] and read the Delta distance in the output window.

The distance between the points also displays beside the delta symbol next to the coordinate readout near the bottom of the SPECCTRA window.

### To display information about objects

1. Click **View - Measure Mode**.
2. Click an object.

The object can be a component, pin, wire, via, keepout, or room.
3. Read the information about the object in the output window.

### To display information about a clearance or crossover violation

1. Click **View - Measure Mode**.
2. Click the [violation symbol](#).
3. Read the information about the object in the output window.

## Select Menu

### Selects and unselects design objects

By using the Select Menu, you can control which nets and [fromtos](#) are routed and edited, which layers they are routed on, and which vias the autorouter can use.

When signal layers and vias are selected, they are available for routing. When components, nets, wires, and fromtos are selected, only those objects are available for routing. Objects not selected are not used in routing.

When the autorouter reads in your design file, all signal layers and vias that are not spares are selected. All components, nets, and fromtos are unselected. In this case, the autorouter tries to route all nets, using all signal layers and vias that are not spares. If you select a net, class of nets, fromto, group of fromtos, balanced pair, or some routed wires, the autorouter tries to route only those selected objects. If you unselect all objects, the autorouter tries to route all nets.

The Select menu commands are

[Components](#)

[Fit](#)

[Nets](#)

[Wires](#)

[Shields](#)

[Vias For Routing](#)

[Guides](#)

[Pairs](#)

[Groups](#)

[UnSelect All Routing Objects](#)



## Select Menu

### Selects and unselects placement design objects

By using the Select Menu, you can select objects for exclusive processing. You can control which components, images, image families, logical parts, and physical parts are processed during automatic placement operations, and are used in defining clusters, assigning properties and rules, and generating reports. You can also control which gates, subgates, pins, or terminators are swapped during swapping operations and included in placement conflict reports. Selected rooms are also included in reports.

In addition, you can select components or images before defining clusters or rooms, before assigning properties, and before checking place rules.

The Select menu commands are

[Components](#)

[Families](#)

[Fit](#)

[Images](#)

[Nets](#)

[Rooms](#)

[Component Clusters](#)

[Gates](#)

[Subgates](#)

[Pins](#)

[Terminators](#)

[Physical Parts](#)

[Logical Parts](#)

[Unselect All Placement Objects](#)

## Select - Components

### **Selects and unselects components for rule assignments, property definitions, or automatic operations**

For autorouting, when you select components you control which nets and wires are routed. The autorouter routes or reroutes wires that have at least one end connected to a selected component. Unrouted nets connected to pins of selected components are also routed.

For automatic placement operations, when you select components you control which components are placed, interchanged, or rotated. You can also select components before performing tasks such as defining clusters or rooms, assigning properties, learning and applying small component patterns, generating component reports, unplacing components, and checking placement rule violations.

The commands on the Select - Components menu are

[Sel Comp Mode](#)

[Select All](#)

[By List](#)

[By Property](#)

[By Side](#)

[Unselect All](#)

## Select - Components - Select All

### Selects all components in the design

When you [select](#) components, SPECCTRA highlights the components with the select color (yellow when you use the default color map), and displays their reference designators. All pins, wires, and guides attached to the components are also selected.

#### Note

To unselect all components, use [Select - Components - Unselect All](#).

## Select - Components - By List

### Selects and unselects components from a list

When you [select](#) components, SPECCTRA highlights the components with the select color (yellow when you use the default color map), and displays their reference designators. A component reference designator is the component's reference name as it appears in the placement section of the SPECCTRA design file. All pins, wires, and guides attached to the components are also selected.

For autorouting, when you select components you control which nets and wires are routed. The autorouter routes only wires and nets connected to pins of the selected components and to other pins and vias on the same nets.

For automatic placement operations, when you select components you control which components are placed, interchanged, or rotated. You can also select components before performing tasks such as defining clusters or rooms, assigning properties, learning and applying small component patterns, generating component reports, unplacing components, and checking placement rule violations.

The [Un] Select Components dialog box contains the following:

[Filter](#) and [Components list](#), which you use to choose component reference designators.

### Action

**Select** identifies components for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

## Select - Components - By Property

### Selects and unselects components with specified properties

Use the [Un] Select Components by Property dialog box to select all components that have certain image or component properties. SPECCTRA checks all the components in the design, and selects only those components that have the specified properties.

When you select components, SPECCTRA highlights the components with the select color (yellow when you use the default color map), and displays their reference designators. All pins, wires, and guides attached to the components are also selected.

For autorouting, when you select components you control which nets and wires are routed. The autorouter routes only wires and nets connected to pins of the selected components and to other pins and vias on the same nets.

For automatic placement operations, when you select components you control which components are placed, interchanged, or rotated. You can also select components before performing tasks such as defining clusters or rooms, assigning properties, learning and applying small component patterns, generating component reports, unplacing components, and checking placement rule violations.

The properties you can specify are

#### Component Type

**Capacitor**, which is any small component defined as a capacitor in the design file or in SPECCTRA. Small components that have only power pins are automatically defined as capacitors in SPECCTRA.

**Discrete**, which is any small component defined as a discrete in the design file or in SPECCTRA.

**Small**, which is any component that has three pins or less, including components defined as capacitors or discrete.

**Large**, which is any component that has more than three pins.

**Maximum Height**, which is the maximum height assigned to a component or its image.

**Power Dissipation**, which is the power dissipation value assigned to a component or its image.

**Electrical Value**, which is a property assigned to a component in the design file or in SPECCTRA. This property usually identifies some electrical characteristic of the component.

**Part Number**, which is the part number assigned to a component in the design file.

#### Action

**Select** identifies components for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

#### Notes

A value of -1 means the property is unspecified. If you do not want SPECCTRA to search for a specific property, click its check box to turn it off.

Properties assigned to an individual component take precedence over properties assigned to its image.

You can define properties for images and components in SPECCTRA, but you cannot change properties defined in the design file. You define properties for individual components using [Define - Component Properties](#). You define properties for the instances of an image using [Define - Image Properties](#).

## Select - Components - By Side

### Selects and unselects components on the front, back, or both sides of the PCB

When you [select](#) components, SPECCTRA highlights the components with the select color (yellow when you use the default color map), and displays their reference designators. All pins, wires, and guides attached to the components are also selected.

For autorouting, when you select components you control which nets and wires are routed. The autorouter routes only wires that are connected on at least one end to a selected component. Unrouted nets connected to selected components are also routed.

For automatic placement operations, when you select components you control which components are placed, interchanged, or rotated. You can also select components before performing tasks such as defining clusters or rooms, assigning properties, learning and applying small component patterns, generating component reports, unplacing components, and checking placement rule violations.

Use the [Un] Select All Components by Side dialog box to select or unselect all components on one or both sides of the PCB. The sides you can choose are

#### Side

**Front**, which means select all components on the front side of the PCB.

**Back**, which means select all components on the back side of the PCB.

**Both**, which means select all components on both sides of the PCB.

#### Action

**Select** identifies components for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

## Select - Components - Unselect All

### **Unselects all components**

All components in the design are unselected. All pins, wires, and guides attached to components are also unselected.



## Select - Fit

**Selects nets and components, and displays the area of the design that contains the selected nets and components**

**Select - Fit** lets you select nets and components, then changes the view so that the selected objects fit within the graphic display area.

**Select - Fit** also displays the design in Normal Mode (default) or Shadow Mode. In Normal Mode, selected objects appear in a "select" color (yellow when you use the default color map) and unselected objects appear in the color of their layer. In Shadow Mode, selected nets and components appear in their "normal" colors and unselected objects appear in a dimmed color.

The Select Fit dialog box contains the following:

[Filter](#) and [nets list](#), which you use to select nets.

[Filter](#) and [components list](#), which you use to select components.

**Shadow Mode** button, which displays the Shadow Mode dialog box. The Shadow Mode dialog box contains the following:

**Normal Mode**, which displays objects according to the color of their layer. In Normal Mode, selected objects appear in a yellow when you use the default color map.

**Shadow Mode**, which displays selected objects in their layer color and unselected objects in a dimmed color, based on the Brightness percentage specified.

**Brightness**, which sets the percentage of color that appears in dimmed objects. If you set the brightness to zero, the objects do not appear. If you set the brightness to 100, the objects appear in their "normal" colors.

### Note

See also [View - Fit Selected Comps/Nets](#).

**Select - Fit** is similar to **Select - Components - By List** and **Select - Nets - By List**, which let you select components and nets, and **View - Fit Selected Comps/Nets**, which changes the view so that the selected nets and components fit within the work area of the SPECCTRA window.

### Tip

Shadow Mode is useful to use in dense designs to view selected nets and components.

## Select - Nets

### Selects and unselects nets

You don't need to select all nets before you begin placing components and routing. When one or more nets are selected, SPECCTRA processes only the selected nets. If nothing is selected, all nets are processed by SPECCTRA.

The commands on the Select - Nets menu are

[Sel Net Mode](#)

[Select All](#)

[By List](#)

[By Class](#)

[With Timing Rules](#)

[Unselect All](#)

## Select - Nets

### Selects and unselects nets

You do not need to select all nets before you begin placing components and routing. When one or more nets are selected, SPECCTRA processes only the selected nets. If nothing is selected, all nets are processed by SPECCTRA.

The commands on the Select - Nets menu are

[Sel Net Mode](#)

[Select All](#)

[By List](#)

[With Timing Rules](#)

[Unselect All](#)

## Select - Nets - Select All

### Selects all nets in the design

This command selects all guides, vias, wires, and pins with nets attached.

### Notes

To unselect all nets, use Select - Nets - Unselect All.

If one or more nets are selected, only those nets are processed during routing and placement operations. To process all nets, select or unselect all nets.

## Select - Nets - By List

### Selects and unselects nets from the PCB netlist

Use the [Un] Select Nets dialog box to select or unselect nets. All pins, vias, wires, and guides in the net are selected or unselected.

The [Un] Select Nets dialog box contains the following:

Filter and Nets list, which you use to identify the nets you want to select or unselect.

### Action

**Select** identifies nets for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

### Note

If one or more nets are selected, only those nets are processed during routing and placement operations. To process all nets, select or unselect all nets.

## Select - Nets - By Class

### Selects and unselects classes of nets

Use the [Un] Select Nets By Class dialog box to select or unselect nets in one or more [classes](#). All pins, vias, wires, and guides in the net are selected or unselected.

The [Un] Select Nets By Class dialog box contains the following:

[Filter Classes list](#), which you use to identify one or more classes of nets to select or unselect.

### Action

**Select** identifies classes of nets for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

### Note

If one or more nets are selected, only those nets are processed during routing and placement operations. To process all nets, select or unselect all nets.

## Select - Nets - With Timing Rules

### Selects nets assigned length or timing rules

Timing rules are defined in terms of time or length units. You can use **Rules - Net - Timing** to assign a timing rule to a net.

### Notes

If one or more nets are selected, only those nets are processed during routing and placement operations. To process all nets, select or unselect all nets.

To unselect all nets, use [Select - Nets - Unselect All](#).

## Select - Nets - Unselect All

### Unselects all nets on the PCB

**Select - Nets - Unselect All** unselects all selected nets. All pins with nets assigned, guides, wires, and vias are unselected. If all nets are unselected, they are processed during routing or placement operations.

### Note

You can use **Select - Nets - Unselect All** to unselect guides and fromtos.



## Select - Wires

### Select and unselect guides and wires

Use the Select - Wires menu to control whether both unrouted connections (guides) and routed connections (wires) are selected.

The commands on the Select - Wires menu are

[Sel Wire Mode](#)

[Select All](#)

[By Layer List](#)

[Unselect All](#)

## Select - Wires - Select All

### Selects all wires

**Select - Wires - Select All** [selects](#) all wires. This command also selects component pins, guides, and vias connected to the wires.

### Note

To unselect all wires, use [Select - Wires - Unselect All](#).

## Select - Wires - By Layer List

### Selects and unselects all wires on particular layers

Use **Select - Wires - By Layer List** if you want to select wiring on specific layers. Only routed wires on these layers are selected. Guides and component pins are not selected.

Use the [Un] Select Layer Wires dialog box to select or unselect layers. It contains the following:

Filter and Layers list, which you use to identify one or more layers to select or unselect.

### Action

**Select** identifies wiring on specific layers to be used for routing operations after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

### Note

**Select - Wires - By Layer List** is often used with [Edit - Delete Wires - By Selected Nets](#).

## Select - Wires - Unselect All

### Unselects all wires

**Select - Wires - Unselect All** unselects all wires. This command also unselects component pins, pins with nets attached, guides, and vias connected to the wires.

## Select - Shields

### Selects or unselects shielded nets

You can use Select - Shields to select or unselect all nets that have assigned shields. When shielded nets are selected, SPECCTRA processes only the selected nets. If nothing is selected, all nets are processed by SPECCTRA.

The commands on the Select - Shields menu are

Select All

Unselect All

## Select - Shields - Select All

### Selects all nets that have assigned shields

This command also selects all guides, vias, wires, and pins attached to the nets .

#### Notes

If only shielded nets are selected, they are the only nets are processed during routing and placement operations.

To unselect all shielded nets, use Select - Shields - Unselect All.

## Select - Shields - Unselect All

**Unselects all nets that have assigned shields**

All guides, wires, vias, and pins attached to the nets are also unselected.

## Select - Vias For Routing

### **Determines which vias can and cannot be available for routing**

Selected vias are available for autorouting. If a via is unselected, it cannot be used unless assigned to a net by a [use vias](#) wiring rule or specified with the [Autoroute - Post Route - Testpoints](#) command. Vias defined as spares in the design are unselected.

The commands on the Select - Vias menu are

[Select All](#)

[By List](#)

[Unselect All](#)



## Select - Vias For Routing - Select All

### **Makes all vias in the design available for autorouting**

On some layout systems, not all of the vias defined in the design are made available for autorouting. By default in SPECCTRA, the design file selects only those vias that are available for routing on the layout system. You can override the design file by selecting all vias in the design.

### **Note**

To unselect all vias for autorouting, use [Select - Vias - Unselect All](#) .

## Select - Vias For Routing - By List

### Determines which vias can and cannot be used by the autorouter

The [Un]Select Vias dialog box either selects or unselects vias for autorouting. Any via that is selected can be used by the autorouter for autorouting. Vias that are not selected cannot be used, unless they are specified by a [use vias](#) wiring rule or the **Autoroute - Post Route - Testpoints** command.

Use the [Un] Select Vias dialog box contains the following:

[Filter](#) and [Vias list](#), which you use to identify one or more vias to select or unselect.

### Action

**Select** identifies vias that can be used for autorouting after you click Apply or OK.

**Unselect** identifies vias that cannot be used for autorouting after you click Apply or OK.

### Note

Use **Report - Vias** to display a report that shows which vias are selected and unselected.

## Select - Vias For Routing - Unselect All

### Determines which vias are not available for autorouting

Unselected vias are not available for autorouting, unless they are specified by a [use vias](#) wiring rule or by the **Autoroute - Post Route - Testpoints** command. You can unselect all vias just before you select only those vias that you want to use for autorouting.

## Select - Guides

### Selects and unselects pin-to-pin connections that are not routed

There are several methods you can use to select [guides](#). The commands on the Select - Guides menu are

[Sel Guide Mode](#)

[Select All](#)

[By Degree](#)

[By Length](#)

[By Area](#)

[By Crossing](#)

[Unselect All](#)

## Select - Guides - Select All

**Selects all pin-to-pin connections that are not routed**

You can select all guides to apply some special operation to the unrouted connections.

### Note

To unselect all guides, use [Select - Guides - Unselect All](#).

## Select - Guides - By Degree

**Selects and unselects unrouted pin-to-pin connections with guides that lie within the specified range of angles**

The [Un]Select Guides by Degree dialog box selects or unselects all pin-to-pin guides that lie within the minimum and maximum angles specified. Degrees are referenced from the positive X axis by sweeping from zero in a counter-clockwise direction.

The [Un]Select Guides by Degree dialog box contains the following:

### **Degree**

**Minimum** specifies the minimum angle.

**Maximum** specifies the maximum angle.

### **Action**

**Select** identifies guides for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

## Select - Guides - By Length

**Selects and unselects unrouted pin-to-pin connections according to their length**

The [Un]Select Guides by Length dialog box selects or unselects unrouted connections with lengths that fall within specified minimum and maximum lengths. Lengths must be scaled for the current working units. Use the unit indicator at the bottom right corner of the window to determine the current working units.

The [Un]Select Guides by Length dialog box contains the following:

### Length

**Minimum** specifies the minimum length.

**Maximum** specifies the maximum length.

### Action

**Select** identifies guides for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

## Select - Guides - By Area

**Selects and unselects unrouted pin-to-pin connections that lie completely within an area**

If a guide is selected, it is available for routing. The [Un]Select Guides by Area dialog box selects and unselects connections that lie completely within the area you specify.

The [Un]Select Guides by Area dialog box contains the following:

### Rectangle

**From Vertex** determines one corner of the rectangular area.

**To Vertex** determines the diagonally opposite corner of the rectangular area.

### Action

**Select** identifies guides for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

### Note

The guide is selected or unselected only if both pins of the guide are within the area.



## Select - Guides - By Crossing

**Selects and unselects unrouted pin-to-pin connections that cross a line defined by two vertexes.**

The [Un]Select Guides by Crossing dialog box selects or unselects connections that cross a line defined by two vertexes.

The [Un]Select Guides by Crossing dialog box contains the following:

### Line

**From Vertex** specifies the X,Y coordinates for one endpoint of the line.

**To Vertex** specifies the X,Y coordinates for the other endpoint of the line.

### Action

**Select** identifies guides for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

## Select - Guides - Unselect All

**Unselects all pin-to-pin connections that are not routed**

If you selected guides to perform some special operation to the unrouted connections, you can unselect the guides by using **Select - Guides - Unselect All**.

## Select - Pairs

### Selects and unselects nets defined as differential pairs

The commands on the Select - Pairs menu are

[Select All](#)

[By List](#)

[Unselect All](#)

#### Note

The [Define - Net Pair](#) command assigns two nets for balanced pair routing. Pair rules and definitions are followed only when the [FST](#) option is installed.

## Select - Pairs - Select All

### Selects all defined differential pairs

A net pair is two nets that must be routed as a balanced or differential pair. Net pairs are assigned by using [Define - Net Pair](#).

## Select Pairs By List

### Selects and unselects differential pairs from a list

A net pair is two nets that must be routed as a balanced or differential pair. Net pairs are assigned by using [Define - Net Pair](#).

Use the [Un] Select Nets dialog box to select or unselect differential pairs. All pins, vias, wires, and guides in both nets of the differential pair are selected or unselected.

The [Un] Select Net Pairs dialog box contains the following:

[Filter](#) and [Net Pairs list](#), which you use to identify one or more differential pairs to select or unselect.

### Action

**Select** identifies differential pairs for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

### Note

If one or more differential pairs are selected, only those nets are processed during routing and placement operations.

## Select - Pairs - Unselect All

### Unselects all net pairs

A net pair is two nets that must be routed as a balanced or differential pair. Net pairs are assigned by using [Define - Net Pair](#).

## Select - Groups

### Selects and unselects groups of fromtos

A group is one or more [fromtos](#) that you define by using the **Define - Group** command.

The commands on the Select - Groups menu are

[Select All](#)

[By List](#)

[Unselect All](#)

## Select - Groups - Select All

### Selects all groups of fromtos

A group consists of one or more fromtos, which are pin-to-pin connections. You define a group by using the [Define - Group](#) command.

Use **Select - Groups - Select All** to select all groups. When objects are selected, only those objects are processed during autorouting operation. This command is useful for routing only a subset of all connections.



## Select - Groups - By List

### Selects and unselects groups from a list

A group consists of one or more fromtos, which are pin-to-pin connections. You define a group by using the [Define - Group](#) command.

The [Un]Select Groups dialog box lists the names of the group you defined with the **Define - Group** command. The group names appear in Groups list box.

The [Un]Select Groups dialog box contains the following:

[Filter](#) and [Groups list](#), which you use to identify one or more groups of nets to select or unselect.

### Action

**Select** identifies the group of fromtos for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

### Note

If one or more groups are selected, only those nets are processed during routing and placement operations.

## Select - Groups - Unselect All

### Unselects all selected groups

A group consists of one or more fromtos, which are pin-to-pin connections. You define a group by using the **Define - Group** command.

Use **Select - Groups - Unselect All** to unselect all selected fromtos in all groups.

## Select - UnSelect All Routing Objects

### **Unselects all selected objects**

The autorouter processes all objects in the design, unless some objects are selected. When some objects are selected, only those objects are considered during autorouting operations. All routing objects can be unselected by using **Select - UnSelect All Routing Objects** to assure that all are processed during autorouting.

## Select - Families

### Selects and unselects image families

A family is one or more images that are defined in the design file or by the [Define - Image Properties](#) command. You can define spacing rules between image families. Family to family spacing rules take [precedence](#) over other spacing rules, except image to image spacing rules.

The [Un]Select Families By List dialog box contains the following:

[Filter](#) and [Families list](#), which you use to identify one or more families of images to select or unselect.

### Action

**Select** identifies image families for exclusive processing by placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

## Select - Images

### Selects and unselects images

When you [select](#) images, you control which images are processed during automatic placement operations, and are used in defining clusters, assigning properties and rules, and generating reports.

[Images](#) are defined in the library section of the SPECCTRA design file. All instances of an image are selected.

The commands on the Select - Images menu are

[Sel Image Mode](#)

[Select All](#)

[By List](#)

[Unselect All](#)

## Select - Images - Select All

### Selects all images

When you [select](#) all images, you select all instances of all [images](#) in the design.

SPECCTRA highlights all instances of the selected images with the select color (yellow when you use the default color map), and displays their component reference designators. All attached pins, wires, and guides are also selected.

### Note

To unselect all images use [Select - Images - Unselect All](#).

## Select - Images - By List

### Selects and unselects images from a list

When you [select](#) an [image](#), you select all instances of that image in the design.

SPECCTRA highlights all instances of the selected images with the select color (yellow when you use the default color map), and displays their component reference designators. All attached pins, wires, and guides are also selected.

When you select images, you control which images are processed during automatic placement operations, and are used in defining clusters, assigning properties and rules, and generating reports.

The [Un] Select Images dialog box contains the following.

[Filter](#) and [Images list](#), which you use to choose image IDs. An image ID is the image's library name as it appears in the library section of the SPECCTRA design file.

### Action

**Select** identifies images for exclusive processing after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

## Select - Images - Unselect All

### **Unselects all selected images**

When you unselect all selected images, all instances of the images are unselected. All attached pins, wires, and guides are also unselected.

#### **Note**

To select all images, use [Select - Images - Select All](#).



## Select - Rooms

### Selects rooms for room reports and unselects rooms

A room is an area of the PCB in which you can assign placement rules, define height and power dissipation constraints, and include or exclude specific components and clusters. Rooms can be defined using [Define - Draw Room Mode](#) or [Define - Room](#).

When you select one or more rooms, you can use the [Report - Rooms](#) command to generate a list of contents for those rooms.

The commands on the Select - Rooms menu are

[Sel Room Mode](#)

[Select All](#)

[By List](#)

[Unselect All](#)

## Select - Rooms - Select All

### Selects all rooms

When a [room](#) is selected, its boundary is highlighted with the select color (yellow when you use the default color map).

### Notes

To unselect all rooms use [Select - Rooms - Unselect All](#).

## Select - Rooms - By List

### Selects or unselects rooms from a list

When a [room](#) is selected, its boundary is highlighted with the select color (yellow when you use the default color map).

When you select one or more rooms, you can use the [Report - Rooms](#) command to generate a list contents for the selected rooms.

The [Un] Select Rooms dialog box contains the following:

[Filter](#) and a [Rooms list](#), which you use to choose room IDs. A room ID is the name you assign when you define the room.

### Action

**Select** identifies rooms for exclusive processing by routing and placement commands after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

### Note

You can define rooms by using [Define - Draw Room Mode](#) or [Define - Room](#).

## Select - Rooms - Unselect All

**Unselects all selected rooms**

### Note

To select all rooms use [Select - Rooms - Select All](#).

## Select - Component Clusters

### Selects and unselects component clusters

A cluster is a group of components that you want to place together or in the same area of the PCB. You can select a cluster for exclusive processing by placement operations.

Clusters are created by using [Define - Cluster](#) or [Autoplace - Cluster Components](#) . You can use the [Report - Clusters](#) command to generate a list of components in the selected clusters.

The commands on the Select - Component Clusters menu are

[Select All](#)

[By List](#)

[Unselect All](#)

## Select - Component Clusters - Select All

### Selects all component clusters

When you select a [component cluster](#), you select every component in the cluster. The components are highlighted with the select color (yellow when you use the default color map), and their reference designators are displayed. All pins, wires, and guides attached to the components are also selected.

### Note

To unselect all clusters use [Select - Component Clusters - Unselect All](#).

## Select - Component Clusters - By List

### Selects or unselects clusters from a list

When you select a [component cluster](#), you select every component in the cluster. SPECCTRA highlights the components with the select color (yellow when you use the default color map), and displays their component reference designators. All attached pins, wires, and guides are also selected.

You can select a cluster for exclusive processing by placement operations.

The [Un] Select Clusters dialog box contains the following:

[Filter](#) and a [Clusters list](#), which you use to choose cluster IDs. A cluster ID is the name you assign when you define the cluster in [Define - Cluster](#) or the name automatically assigned by SPECCTRA when you use [Autoplace - Cluster Components](#) .

### Action

**Select** identifies clusters for exclusive processing after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

## Select - Component Clusters - Unselect All

### **Unselects all selected clusters**

All components in the selected [clusters](#) are unselected. All their attached pins, wires, and guides are also unselected.

### **Note**

To select all clusters use [Select - Component Clusters - Select All](#) .



## Select - Gates

### Selects and unselects gates for swapping

When you [select](#) gates, you can control which [gates](#) are swapped during swapping operations and included in placement conflict reports.

The commands on the Select - Gates menu are

[Select Gate Mode](#)

[Select All](#)

[Select Eq Gate Mode](#)

[Unselect All](#)

### Note

If gate definitions are not included in your design file, you cannot select gates. SPECCTRA displays the warning "Place: No Logical Part is defined" in the output window.

## Select - Gates - Select All

### Selects all gates

When you select gates, SPECCTRA highlights the gate pins with the select color (yellow when you use the default color map). The attached wires and guides are also selected.

### Note

To unselect all gates, use Select - Gates - Unselect All.

## Select - Gates - Unselect All

### Unselects all selected gates

All selected gate pins are unselected. Their attached wires and guides are also unselected.

#### Note

To select all gates, use Select - Gates - Select All.

## Select - Subgates

### Selects and unselects subgates for swapping

When you [select](#) subgates, you can control which [subgates](#) are swapped during swapping operations and included in placement conflict reports.

The commands on the Select - Subgates menu are

[Sel Subgate Mode](#)

[Select All](#)

[Sel Eq Subgate Mode](#)

[Unselect All](#)

### Note

If subgate definitions are not included in your design file, you cannot select subgates. SPECCTRA displays the warning "Place: No Logical Part is defined" in the output window.

## Select - Subgates - Select All

### Selects all the subgates in the design

When you select [subgates](#), SPECCTRA highlights the subgate pins with the select color (yellow when you use the default color map). The attached wires and guides are also selected.

#### Note

To unselect all subgates, use [Select - Subgates Unselect All](#)

## Select - Subgates - Unselect All

### Unselects all selected subgates

All selected [subgate](#) pins are unselected. Their attached wires and guides are also unselected.

#### Note

To select all subgates, use [Select - Subgates - Select All](#).

## Select - Pins

### Selects and unselects pins for swapping

When you [select](#) pins before performing automatic pin swapping, only the selected pins are swapped.

The commands on the Select - Pins menu are

[Sel Pin Mode](#)

[Select All](#)

[Sel Eq Pin Mode](#)

[Unselect All](#)

#### Note

You cannot select a pin unless it is included as part of a gate definition in the design file. You cannot swap a pin unless it has a gate pin swap code in the design file. SPECCTRA displays the warning "Place: No Logical Part is defined" in the output window.

## Select - Pins - Select All

### Selects all the pins

When you [select](#) pins, SPECCTRA highlights the pins with the select color (yellow when you use the default color map). The attached wires and guides are also selected.

### Note

To unselect all pins use [Select - Pins - Unselect All](#).



## Select - Pins - Unselect All

### **Unselects all selected pins**

All selected pins are unselected. Their attached wires and guides are also unselected.

#### **Note**

To select all pins use [Select - Pins - Select All](#).

## Select - Terminators

### Selects and unselects terminators for swapping

When you [select](#) terminators before performing automatic terminator swapping, only the selected [terminator](#) pins are swapped.

The commands on the Select - Terminators menu are

[Sel Terminator Mode](#)

[Select All](#)

[Unselect All](#)

#### Note

You cannot select a terminator pin unless it is included as part of a gate definition in the design file. SPECCTRA displays the warning "Place: No Logical Part is defined" in the output window.

## Select - Terminators - Select All

### Selects all the terminators

When you [select](#) terminators, SPECCTRA highlights the terminator pins with the select color (yellow when you use the default color map). The attached wires and guides are also selected.

### Note

To unselect all terminators use [Select - Terminators - Unselect All](#).

## Select - Terminators - Unselect All

### **Unselects all selected terminators**

All selected terminators are unselected. Their attached wires and guides are also unselected.

#### **Note**

To select all terminators use [Select - Terminators - Select All](#).

## Select - Physical Parts

### Selects and unselects physical parts

You can control which [physical parts](#) are processed during automatic placement operations, and are used in defining clusters, assigning properties and rules, and generating reports.

When you [select](#) a [physical part](#) you select all instances of that part in the design.

The commands on the Select - Physical Parts menu are

[Sel Physical Part Mode](#)

[Select All](#)

[By List](#)

[Unselect All](#)

## Select - Physical Parts - Select All

### Selects all physical parts

When you [select](#) all [physical parts](#), you select all instances of all physical parts in the design.

SPECCTRA highlights all instances of the selected parts with the select color (yellow when you use the default color map), and displays their component reference designators. All attached pins, wires, and guides are also selected.

### Note

To unselect all physical parts use [Select - Physical Parts - Unselect All](#).

## Select - Physical Parts - By List

### Selects and unselects physical parts by part ID

When you [select](#) a [physical part](#), you select all instances of that part in the design.

SPECCTRA highlights all instances of the selected parts with the select color (yellow when you use the default color map), and displays their component reference designators. All attached pins, wires, and guides are also selected.

You can control which physical parts are processed during automatic placement operations, and are used in defining clusters, assigning properties and rules, and generating reports.

The [Un]Select Physical Parts dialog box contains the following:

[Filter](#) data entry box and a [Physical Parts list](#), which you use to choose the physical part IDs. A physical part ID is the part's library name as it appears in the part library section of the SPECCTRA design file.

### Action

**Select** identifies physical parts for exclusive processing after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

## Select - Physical Parts - Unselect All

### **Unselects all selected physical parts**

When you unselect all selected [physical parts](#), you unselect all instances of all physical parts in the design. All attached pins, wires, and guides are also unselected.

#### **Note**

To select all physical parts use [Select - Physical Parts - Select All](#).



## Select - Logical Parts

### Selects and unselects logical parts

You can control which [logical parts](#) are processed during automatic placement operations, and are used in defining clusters, assigning properties and rules, and generating reports.

When you [select](#) a [logical part](#), you select all instances of that part in the design.

The commands on the Select - Logical Parts menu are

[Sel Logical Part Mode](#)

[Select All](#)

[By List](#)

[Unselect All](#)

## Select - Logical Parts - Select All

### Selects all logical parts

When you [select](#) all [logical parts](#), you select all instances of all logical parts in the design.

SPECCTRA highlights all instances of the selected parts with the select color (yellow when you use the default color map), and displays their component reference designators. All attached pins, wires, and guides are also selected.

### Note

To unselect all logical parts use [Select - Logical Parts - Unselect All](#).

## Select - Logical Parts - By List

### Selects and unselects logical parts by part ID

When you [select](#) a [logical part](#), you select all instances of that part in the design.

SPECCTRA highlights all instances of the selected parts with the select color (yellow when you use the default color map), and displays their component reference designators. All attached pins, wires, and guides are also selected.

When you select logical parts for automatic placement, you control which components SPECCTRA places, interchanges, or rotates. You can also select logical parts before defining clusters.

The [Un]Select Logical Parts dialog box contains the following:

[Filter](#) data entry box and a [Logical Parts list](#), which you use to choose the logical part IDs. A logical part ID is the part's library name as it appears in the part library section of the SPECCTRA design file.

### Action

**Select** identifies logical parts for exclusive processing after you click Apply or OK.

**Unselect** removes the select identifier after you click Apply or OK.

## Select - Logical Parts - Unselect All

### Unselects all selected logical parts in the design

Every instance of every [logical part](#) in the design is unselected. All attached pins, wires, and guides are also unselected.

### To unselect all logical parts

- Click **Select - Logical Parts - Unselect All**.

### Note

To select all logical parts use [Select - Logical Parts - Select All](#).

## Select - Unselect All Placement Objects

### **Unselects all selected objects**

Placement objects include components, images, rooms, clusters, gates, subgates, and pins. During initial placement and interchange operations, SPECCTRA processes and operates on the selected components. If no objects are selected, SPECCTRA processes and operates on all placement objects. All placement objects can be unselected to assure that all components are considered during initial placement and interchange.

## Define Menu

**Defines associations between nets, sets the left mouse button mode, assigns daisy chain properties to pins, and disbands previously defined classes and net rules**

The Define menu commands are described in the following table.

Command	Description
<a href="#"><u>Class</u></a>	Defines a net class
<a href="#"><u>Group</u></a>	Defines a group of fromtos
<a href="#"><u>Net Pair</u></a>	Defines a differential net pair
<a href="#"><u>Pin Attributes</u></a>	Assigns source, load, and terminator attributes, and the expose property to pins on a net
<a href="#"><u>Fence</u></a>	Defines a route keepin area, which can be used for example to separate analog and digital signals
<a href="#"><u>Draw Fence Mode</u></a>	Sets [LB] to Draw Fence mode
<a href="#"><u>Keepout</u></a>	Defines a keepout area
<a href="#"><u>Draw Keepout Mode</u></a>	Sets [LB] to Draw Keepout mode
<a href="#"><u>Region</u></a>	Defines a region and the rules that apply to the region
<a href="#"><u>Assign Pin</u></a>	
<a href="#"><u>Forget Classes</u></a>	Disbands net classes and all associated rules
<a href="#"><u>Forget Groups</u></a>	Disbands a group
<a href="#"><u>Forget Nets</u></a>	Disbands all rules associated with nets
<a href="#"><u>Forget Keepouts</u></a>	Disbands a keepout area
<a href="#"><u>Forget Regions</u></a>	Disbands a region

## Define Menu

**Defines clusters, rooms, keepouts, component and image properties, and component associations; disbands previously defined clusters, rooms, keepouts, and associations.**

The Define menu commands are described in the following table.

Command	Description
---------	-------------

<u>Cluster</u>	Assigns components to a cluster
<u>Room</u>	Assigns the X and Y coordinates for a room
<u>Draw Room Mode</u>	Sets the left mouse button [LB] mode to draw rooms
<u>Keepout</u>	Defines a keepout area
<u>Draw Keepout Mode</u>	Sets [LB] to Draw Keepout mode
<u>Place Boundary</u>	Defines the area within which you can place components
<u>Draw Place Boundary Mode</u>	Sets [LB] to Draw Place Boundary mode
<u>Component Properties</u>	Assigns component properties such as component type, maximum height, power dissipation, or electrical value
<u>Image Properties</u>	Assigns image properties such as image type, maximum height, or power dissipation
<u>Associate Components</u>	Links a large component with one or more small components
<u>Associate Components Mode</u>	Sets [LB] to Associate Components mode
<u>Forget Clusters</u>	Disbands clusters and all associated rules
<u>Forget Rooms</u>	Disbands rooms and all associated rules
<u>Forget Keepouts</u>	Disbands a keepout area
<u>Disassociate Components</u>	Disbands component associations

## Define - Class

**Creates a net class that consists of one or more nets from the PCB netlist and**

## removes nets from a class

A class is a set of nets that you define by choosing the nets and assigning a Class ID (name). Once a class is defined, you can apply rules or operate on all nets in the class by using the Class ID.

The Define Class dialog box contains the following:

**Class ID** is the class name used to identify the set of nets. This data entry box contains the default Class ID (class1) or the last class name you defined. If you try to use a Class ID that is already defined, an error is written to the output window.

[Nets list](#) and [Filter](#) are used to choose the nets you want to add to a class.

**Add to Class** button adds the nets you chose in the Nets list to the class that you specified in the Class ID data entry box. After you click this button, the net names appear in the Nets in Class list.

[Nets in Class list](#) and [Filter](#) are use to choose the nets you want to remove from a class.

**Remove from Class** button removes the net(s) you chose in the Nets in Class list box from the class. After you click this button, the net name(s) are removed from the Nets in Class list.

## Notes

Class names must be unique.

You can assign a net to more than one class.



## Define - Group

### **Creates a group of fromtos and removes fromtos from a group**

A group is a set of [fromtos](#) that you define by choosing the fromtos and assigning a Group ID (name). Once a group is defined, you can apply rules or operate on all fromtos in the group by using the Group ID.

The Define Group dialog box contains the following:

**Pick Net** button displays the Pick Active Net for Fromto dialog box, which you use to choose the net that contains the fromto(s) you want to place in a group. This dialog box contains a [Filter](#) and an [Items list](#). After you click OK or Apply, the fromtos for the net appear in the Fromtos in Net list.

**Group ID** is the group name used to identify the set of fromtos. This data entry box contains the default Group ID (group1) or the last group name you defined. If you try to use a Group ID that is already defined, an error is written to the output window.

[Fromtos in Net list](#) and [Filter](#) are used to choose the fromtos you want to add to a group.

**Add to Group** button adds the fromtos you chose in the Fromtos in Net list to the group that you specified in the Group ID data entry box. After you click this button, the fromto names appear in the Fromtos in Group list.

[Fromtos in Group list](#) and [Filter](#) are use to choose the fromtos you want to remove from a group.

**Remove from Group** button removes the fromto(s) you chose in the Fromtos in Group list box from the group. After you click this button, the fromto name(s) are removed from the Fromtos in Group list.

### **Notes**

Group names must be unique.

You can assign a fromto to more than one group.

## Define - Net Pair

**Defines two nets as a differential or balanced pair, and disbands a differential pair**

When two nets are defined as a pair, they are routed with the same path topology and maintain a specified gap, except when they connect to pins or diverge to avoid obstacles.

The Define Net Pairs dialog box contains the following:

### By Lists

[Net 1 list](#) and [Filter](#) are used to choose one of nets in the differential pair.

[Net 2 list](#) and [Filter](#) are used to choose the other net in the differential pair.

**Set Gap** determines the gap maintained between the differential pair wires. When the Set Gap check box is checked, the value entered in the data entry box is the gap maintained. Otherwise, a wire to wire clearance rule is used to determine the gap.

**Wildcard for Net 1** and **Wildcard for Net 2** data entry boxes let you use a question mark (?) as a wildcard character to define more than one differential pair. You enter the string with the wildcard character in each data entry box and click the Define button next to the data entry boxes. For example, if you enter A?+ in the Wildcard for Net 1 data entry box and A?- in the Wildcard for Net 2 dialog box then click the Define button, A1+ and A1-, A2+ and A2-, A3+ and A3- are defined as differential pairs.

**Define** button defines the two nets you chose in the Net 1 list and Net 2 list as a differential pair. After you click Define, the two nets are listed in the Net Pairs list.

[Net Pairs list](#) and [Filter](#) is used to choose a net pair that you want to disband.

**Forget** button disbands the association between the two nets that you chose in the Net Pairs list.

### Notes

If the nets you choose are too far apart or do not follow the same topology, they are not defined as a differential pair. A warning message appears in the output window.

You can reset the gap to the default clearance rule by using -1 in the Set Gap data entry box.

Differential pair rules are followed only when the [FST](#) option is installed.

## Define - Pin Attributes

### Assigns source, load, terminator, and expose properties to component pins

The **Define - Pin Attributes** command provides an efficient way to specify large numbers of daisy-chained nets in source-load-terminator format. It also lets you assign an expose property, which marks through-pins as requiring fanout. When a through-pin is assigned the expose property, the autorouter connects to the outermost layers. If the autorouter needs to use an internal layer, it will connect to a fanout via.

The Define Pin Attributes dialog box contains the following:

**Pick Net** button displays the Pick Active Net for Fromto dialog box, which you use to choose the net that contains the pin(s) to which you want to assign properties. This dialog box contains a [Filter](#) and an [Items list](#). After you click OK or Apply, the pins appear in the Pins on Net list.

[Pins on Net list](#) and [Filter](#) are used to choose the pins to which you will assign properties.

#### Assign Selected Pin(s) to:

**Expose** assigns the expose property to the pins you chose in the **Pins on Net** list.

**No expose** removes the expose property from the pins you chose in the **Pins on Net** list.

**Source** assigns the source attribute to the pin.

**Load** assigns the load attribute to the pin.

**Terminator** assigns the terminator attribute to the pin.

#### Note

Source, load, and terminator pin properties are not used unless the associated nets are ordered as daisy chain. See Net Ordering under [Rule - Net - Wiring](#) for more information.

## Define - Fence

### Defines a route keepin region

**Define - Fence** lets you define a fence by specifying coordinates. A fence is an area that controls how the enclosed connections are routed. The way in which connections are routed in a fence region depends on whether the fence is set to [soft type](#) or [hard type](#). Use [Autoroute - Setup](#) to set the fence type.

The Define Fence dialog box contains data entry boxes, in which you specify the X and Y coordinates of diagonally opposite corners.

### Notes

You can define multiple fences, but when fences overlap, they are merged to form a single polygonal fence region.

Hard and soft fence types cannot coexist. Either all fences in a design are hard or all are soft.

Another way to create a fence is by using [Define - Draw Fence Mode](#).

## Define - Draw Fence Mode

### Sets the left mouse button [LB] to Draw Fence mode

**Define - Draw Fence Mode** lets you define a fence by drawing the fence with the mouse. A fence is an area that controls how the enclosed connections are routed. The way in which connections are routed in a fence region depends on whether the fence is set to [soft type](#) or [hard type](#). Use [Autoroute - Setup](#) to set the fence type.

### To draw a rectangular routing fence

1. Click **Define - Draw Fence Mode**.

The left mouse button [LB] is set to Draw Fence Mode, which is indicated in the Mode Status area at the bottom of the window.

2. Click one corner of the region you want to enclose with a fence.
3. Drag the pointer to the diagonally opposite corner of the region you want to create.
4. Release [LB].
5. Click [RB] and slide the pointer to **Define Polygon as Fence**.

### Notes

When [LB] is set to Draw Fence mode, you can create a polygonal fence by clicking each corner of the fence region. Use the right mouse button to display a menu of commands for editing, defining, or deleting the fence. If you create a polygonal fence, you must use **Define Polygon as Fence** on the right button menu to define the polygon as a fence.

Hard and soft fence types cannot coexist. Either all fences in a design are hard or all are soft.

Another way to create a fence is by using [Define - Fence](#).

## Define - Keepout

### Defines an area where objects are prohibited

The Define Keepout dialog box contains the following:

**Keepout ID** is the name used to identify the keepout area. This data entry box contains the default Keepout ID (keepout1) or the last keepout name you defined. If you try to use a Keepout ID that is already defined, an error is written to the output window. If this data entry box is blank when you click Apply or OK, SPECCTRA assigns a Keepout ID for you.

#### Type:

**Via** prohibits vias in the keepout area.

**Wire** prohibits wires in the keepout area.

**Bend** prohibits bends in wires in the keepout area.

**Place** prohibits components in the keepout area.

**All** prohibits vias, wires, and components in the keepout area.

#### On:

**All Signal Layers** places the keepout on all signal layers.

**Specify** lets you choose a layer for the keepout by using the Pick Layer button. The Pick Layer button displays the Pick Active Layer for Rules dialog box, which contains an [Item list](#) and [Filter](#).

#### Outline:

**Polygon** lets you define a polygonal area by entering the coordinates of each vertex.

**Rectangle** lets you define a rectangular area by entering the coordinates of two opposite corners.

#### Note

Another way to define a keepout is to use [Define - Keepout](#).

## Define - Draw Keepout Mode

### Sets the left mouse button [LB] to Draw Keepout mode

A keepout is an area where specified objects, such as wires or components, are prohibited.

After you click **Define - Draw Keepout Mode**, you can draw a keepout area by clicking one corner of the keepout area and dragging the pointer to the diagonally opposite corner of the area. To define the polygon as a keepout, click **Define Polygon as Keepout** from the right mouse button menu. The Add Polygon as Keepout dialog box appears. It contains the following:

**Keepout ID** is the name used to identify the keepout area. This data entry box contains the default Keepout ID (keepout1) or the last keepout name you defined. If you try to use a Keepout ID that is already defined, an error is written to the output window. If this data entry box is blank when you click Apply or OK, SPECCTRA assigns a Keepout ID for you.

#### Type:

**Via** prohibits vias in the keepout area.

**Wire** prohibits wires in the keepout area.

**Bend** prohibits bends in wires in the keepout area.

**Place** prohibits components in the keepout area.

**All** prohibits vias, wires, and components in the keepout area.

#### On:

**All Signal Layers** places the keepout on all signal layers.

**Specify** lets you choose a layer for the keepout by using the Pick Layer button. The Pick Layer button displays the Pick Active Layer for Rules dialog box, which contains an [Item list](#) and [Filter](#).

#### Notes

When [LB] is set to Draw Keepout mode, you can create a polygonal keepout by clicking each corner of the keepout area. Use the right mouse button to display a menu of commands for editing and defining the keepout. If you create a polygonal keepout, you must use **Define Polygon as Keepout** on the right button menu to define the polygon as a keepout area.

Another way to define a keepout is to use [Define - Keepout](#).

## Define - Region

### **Defines a rectangular area of the PCB**

After you define a region, you can assign region rules to the region by using [Rules - Region](#). Region rules have the highest precedence in the [rule hierarchy](#) and, therefore, override all other rules.

The Define Region dialog box contains the following:

**Region ID** is the region name. This data entry box contains the default Region ID (region1) or the last region name you defined. If you try to use a Region ID that is already defined, an error is written to the output window.

**All Signal Layers** creates the region on all signal layers.

**Specify** creates the region on the layer you specify by using the Pick Layer button. The Pick Layer button displays the Pick Active Layer for Rules dialog box, which contains an [Item list](#) and [Filter](#).

### **Bounding Box**

**Vertex 1** defines the X, Y coordinate of one corner of the region.

**Vertex 2** defines the X, Y coordinate of the opposite corner of the region.



## Define - Assign Pin

### Assigns source, load, terminator, and expose properties to component pins

The **Define - Assign Pin** command provides an efficient way to specify large numbers of daisy-chained nets in source-load-terminator format. It also lets you assign an expose property, which marks through-pins as requiring fanout. When a through-pin is assigned the expose property, the autorouter connects to the outermost layers. If the autorouter needs to use an internal layer, it will connect to a fanout via.

The Assign Pin dialog box includes the following:

#### Assign

**Expose** forces connections to pin to be routed on the external surfaces of the PCB. The expose property applies to through-pins only.

**No expose** turns off the expose property on a pin.

**Source** assigns the source property to pins for daisy-chain routing.

**Load** assigns the load property to pins for daisy-chain routing.

**Terminator** assigns the terminator property to pins for daisy-chain routing.

**On Components** contains a [filter](#) and a [Components list](#), which you use to specify the component reference designator(s) that contains the pins to assign properties.

#### Assign To

**All Pins**, which assigns the property to all pins on the component

**Pin List**, where you specify a pin number in the data entry box

**Pin Range**, which lets you specify more than one pin by using the following:

**Pin Number Prefix**, which is a non-numeric character or character string that represents a pin number prefix

**Pin Number Suffix**, which is a non-numeric character or character string that represents a pin number suffix

**Beginning Pin**, which is the pin number of the first pin in the list

**Ending Pin**, which is the pin number of the last pin in the list

**Increment**, which determines the pins included between the Beginning Pin and the Ending Pin

#### Notes

Source, load, and terminator pin properties are not used unless the associated nets are ordered as daisy chain.

You can also assign properties to component pins by using [Define - Pin Attributes](#).

## Define - Forget Classes

**Disbands net classes, including class names and all rules assigned to the classes**

Net classes are defined using the **Define - Class** command. If you want to disband a net class, use **Define - Forget Classes**. The Forget Classes dialog box contains a [Filter](#) and a [Classes lists](#), which you use to choose the class that you want to disband.

### Note

Rules assigned by net are not removed by **Define - Forget Classes**.

## Define - Forget Groups

### Disbands groups

You can define a group of [fromtos](#) by using the **Define - Group** command. After you define a group, you can apply routing rules to it. If you want to disband the group, use the **Define - Forget Groups** command. When you disband one or more groups of fromtos, all group rules (including ordering) that were assigned to the group(s) no longer apply.

The Forget Groups dialog box contains a [Filter](#) and a [Groups lists](#), which you use to choose the groups that you want to disband.

## Define - Forget Nets

### **Removes all rules assigned to one or more nets**

The Forget Nets dialog box contains a [Filter](#) and a [Nets lists](#), which you use to choose the nets from which you want to remove rules.

#### **Note**

Rules assigned by class are not removed by **Define - Forget Nets**.

## Define - Forget Keepouts

### Disbands keepout areas

A keepout is an area where objects are prohibited. You define a keepout area by using **Define - Keepout** or **Define - Draw Keepout Mode**.

If you want to disband one or more keepout areas, use **Define - Forget Keepout**. The Forget Keepouts dialog box contains a [Filter](#) and a [Keepouts lists](#), which you use to choose the Keepout ID(s) of the keepouts that you want to disband.

## Define - Forget Regions

### **Disbands regions, including all rules assigned to the regions**

A region is a rectangular area of the PCB that you define with **Define - Region**. After you define a region, you can assign rules to the region. Region rules have the highest precedence in the [rule hierarchy](#) and, therefore, override all other rules.

If you want to disband one or more regions, use **Define - Forget Regions**. The Forget Regions dialog box contains a [Filter data entry box](#) and a [Regions lists](#), from which you choose the region ID(s) of the regions that you want to disband.

## Define - Cluster

### Creates a cluster consisting of two or more components

A cluster is a group of components that you can refer to by using a unique ID. You define a cluster by choosing the constituent components, choosing the cluster type, and assigning a cluster ID (name). Once a cluster is defined, you can manipulate all components in the cluster, or assign them to a room, by using the ID.

The Define Cluster dialog box contains the following:

**Cluster ID** is the cluster name used to identify the group of components. This data entry box contains the default cluster ID (cluster1) or the name of last cluster you defined. If you try to use a cluster name that is already defined, an error is reported in the output window.

**Selected** defines a cluster containing all selected components. You can select components by using the **Select - Components** commands.

**Specified** lets you choose the components you want in the cluster. If you use this option, use the [Filter](#) data entry box and the Components [list](#) to specify components.

The Cluster Type determines what kind of cluster you define. SPECCTRA recognizes four types of clusters:

**Super**, which is a group of components with fixed positions and orientations with respect to one another. The super cluster is treated as a single component and is sometimes called a super component.

**Floor Plan**, which is a group of components you want to include in or exclude from a room.

**Piggyback Super**, which is a super cluster in which the components are permitted to overlap when placed without violating spacing rules. Place and lock the components before you define the cluster.

**Piggyback**, which is a group of components that can overlap when placed without violating spacing rules. Place and lock the components before you define the cluster.

### Notes

Cluster names must be unique.

You must preplace the components in a piggyback or super piggyback cluster before performing automatic placement.

You can use the **define cluster** command in the command entry area to assign place rules to a super cluster or a super piggyback cluster.

You can use [Autoplace - Cluster Components](#) if you want to form clusters automatically from signal nets or power nets.

To disband a cluster, use [Define - Forget Clusters](#).

## Define - Room

**Defines the X and Y coordinates of each corner of a room, assigns an ID, and assigns the PCB side**

A room is an area that you define to control where SPECCTRA places components on the PCB. You can control placement in a room on one surface or on both surfaces.

The Define Room dialog box includes the following:

**Room ID** is the name used to identify the room. This data entry box contains the default Room ID (room1) or the last room name you defined. If you try to use a room name that is already defined, an error is reported in the output window.

### Side:

**Both (signal)** defines the room on both the front and back sides of the PCB. This is the default.

**Front** defines the room on the front (top) side of the PCB.

**Back** defines the room on the back (bottom) side of the PCB.

### Outline:

**Polygon** defines the room as a polygon, in which you enter the X,Y coordinates for each corner point, separated by blank spaces.

**Rectangle** defines the room as a rectangle, in which you enter the X and Y coordinate values for two diagonal corners of the rectangle (the lowest and highest X and Y values). This is the default.

### Notes

Room names must be unique.

You can also use the [Define - Draw Room Mode](#) to define a room.

To disband a room, use [Define - Forget Rooms](#).



## Define - Draw Room Mode

### Sets the left mouse button [LB] to Draw Room mode

A room is an area that you define to control where SPECCTRA places components on the PCB. You can control placement in a room on one surface or on both surfaces.

After you click **Define - Draw Room Mode**, you can draw a room area by clicking each corner of the room, then click **Define Polygon as Room** from the right mouse button menu. The Add Polygon as Room dialog box appears. It contains the following:

**Room ID** is the name used to identify the room. This data entry box contains the default Room ID (room1) or the last room name you defined. If you try to use a room name that is already defined, SPECCTRA reports an error.

#### Side:

**Both (signal)** defines the room on both the front and back sides of the PCB. This is the default.

**Front** defines the room on the front (top) side of the PCB.

**Back** defines the room on the back (bottom) side of the PCB.

#### Notes

Room names must be unique.

When [LB] is set to Draw Room mode, you can create a polygonal room by pressing [RB] and removing the check from the Orthogonal check box before you start drawing the room.

To define a room by specifying the X,Y coordinates for each corner use [Define - Room](#).

To disband a room use [Define - Forget Rooms](#).

## Define - Place Boundary

### **Defines a placement boundary**

A placement boundary is an area of the PCB within which you can place components.

The Define Boundary dialog box includes the following:

#### **Outline:**

**Path** defines the placement boundary as a path, in which you enter the X,Y coordinates for each vertex, separated by blank spaces.

**Rectangle** defines the placement boundary as a rectangle, in which you enter the X and Y coordinate values for two diagonal corners of the rectangle (the lowest and highest X and Y values). This is the default.

## Define - Draw Place Boundary

### Sets the left mouse button [LB] to Draw Place Boundary mode

A placement boundary is an area of the PCB within which you can place components.

After you click **Define - Draw Place Boundary Mode**, you can draw a placement boundary by clicking each corner of the boundary, then click **Define Polygon as Boundary** from the right mouse button menu.

### Notes

When [LB] is set to Draw Place Boundary mode, you can create a polygonal room by pressing [RB] and removing the check from the Orthogonal check box before you start drawing the room.

To define a placement boundary by specifying the X,Y coordinates for each corner use [Define - Place Boundary](#).

When you define a new placement boundary, SPECCTRA automatically deletes the old placement boundary. If no placement boundary is defined, SPECCTRA uses the routing boundary as the boundary for placing components.

## Define - Component Properties

### **Assigns component type and other properties to individual components.**

You can assign any component properties that are not defined for the component in the design file. Component properties consist of component type, physical properties, and electrical value.

The Define Component Properties dialog box contains the following:

#### **Component Types:**

**Large**, which is any component that has more than three pins.

**Small**, which is any component that has three pins or less, including components defined as capacitors or discrete.

The large and small component types are determined by the number of pins. Components assigned the capacitor or discrete component type are also treated as small components.

The large component type cannot be changed, and you can't change the component type of a small component if it's defined in the design file. You can assign the capacitor type or the discrete type to small components, but you can't assign the large type to small components.

**Discrete**, which is any small component defined as a discrete in the design file or in SPECCTRA. Use the Discrete component type to differentiate certain small images (besides decoupling capacitors) from other small images.

**Capacitor**, which is any small component defined as a capacitor in the design file or in SPECCTRA. Small components that have only power pins are automatically defined as capacitors in SPECCTRA. Use the Capacitor component type to identify decoupling capacitors when you want to place them separately from other small images.

The physical and electrical properties are

**Maximum Height**, which is the maximum height assigned to a component.

**Power Dissipation**, which is the power dissipation value assigned to a component.

**Electrical Value**, which is a label that describes some electrical characteristic of the component.

#### **On Components:**

**Selected** assigns the component properties to selected components. You select components by using a **Select - Components** command.

**By List** lets you choose components by using the [Components list](#) and [Filter](#).

#### **Notes**

A value of -1 means the property is unspecified. If you do not want SPECCTRA to assign a property, click its check box to turn it off.

Properties assigned to an individual component take precedence over properties assigned to its image. You can define properties for the instances of an image using [Define - Image Properties](#).

You can define properties for images and components in SPECCTRA, but you can't change properties defined in the design file.

SPECCTRA treats a small component with pins connected only to power nets as a

decoupling capacitor. If such a component is not assigned the Capacitor component type in the design file, SPECCTRA assigns it automatically; however, you can change the type to Small or Discrete.

## Define - Image Properties

**Assigns image type, physical properties, and family names to component images.**

You can assign properties to an image that are not defined in the design file. Image properties consist of image type and physical properties.

The Define Image Properties dialog box contains the following:

### Image Type:

**Capacitor**, which is any small component defined as a capacitor in the design file or in SPECCTRA. Use the Capacitor image type to identify decoupling capacitors when you want to place them separately from other small components.

**Discrete**, which is any small image defined as a discrete in the design file or in SPECCTRA. Use the Discrete image type to differentiate certain small components (besides decoupling capacitors) from other small components.

**Small**, which is any component that has three pins or less, including components defined as capacitors or discrete.

**Large**, which is any component that has more than three pins.

The large and small component types are determined by the number of pins. Components assigned the capacitor or discrete component type are also treated as small components.

The large image type cannot be changed, and if the image type for a small component is defined in your design file, it can't be changed. You can assign the capacitor type or the discrete type to small images, but you can't assign the large type to small images.

**Maximum Height**, which is the maximum height assigned to an image.

**Power Dissipation**, which is the power dissipation value assigned to an image.

### Family:

**Add to Family**, which is the name of the image family to which you want to add the specified or selected images. This name can define a new family, or it can specify an existing family. The default is family1 or the name of the last family you defined..

**Reset Family**, which is the name of the image family from which you want to remove the specified or selected images.

**Selected Images** assigns the image properties to selected images. You select components by using a **Select - Images** commands.

**Specified Images** lets you choose images by using the [Images list](#) and [Filter](#).

### Notes

A value of -1 means the property is unspecified. If you do not want SPECCTRA to assign a property, click its check box to turn it off.

Properties assigned to an individual component take precedence over properties assigned to its image. You can define properties for individual components using [Define - Component Properties](#).

You can define properties for images and components in SPECCTRA, but you can't change properties defined in the design file.

## Define - Associate Components

### **Creates an association between a large component and one or more small components**

You can create component associations to link small components with a large component. SPECCTRA places the small components as close as possible to the power pins of the large component.

The Associate Components dialog box contains separate [Filter](#) and Components [lists](#) for large and small components. You choose a single component from the Large Component list, and one or more components from the Small Component list.

### **Notes**

Once you have created a component association, you can't use its components in another association unless you first disband the current association. You can use [Define - Disassociate Components](#) to break the links between a large component and all its small component associates.

## Define - Forget Clusters

**Disbands component clusters, including cluster names and all rules assigned to the clusters**

The Forget Clusters dialog box contains a [Filter](#) data entry box and a Clusters [list](#).

### Note

Place rules assigned to a super cluster are removed by **Define - Forget Clusters**. Place rules assigned to individual images or components in the cluster are not removed.



## Define - Forget Rooms

**Disbands rooms, including room names and all rules assigned to the rooms**

The Forget Rooms dialog box contains a [Filter](#) data entry box and a Rooms [list](#).

### Note

Place rules assigned to a room or an image set in a room are removed by **Define - Forget Rooms**. Place rules assigned to individual images or components in the room are not removed.

## Define - Disassociate Components

### Disbands associations between large and small components

To disband a component association, you specify the reference designator of the large component. SPECCTRA breaks the links between the large component and all its small component associates.

The Disassociate Components dialog box contains a [Filter](#) data entry box and a Component [list](#).

#### Note

Once you have created a component association by using [Define - Associate Components](#), you can't use its components in another association unless you first disband the current association.

## Rules Menu

### Sets routing rules

You can assign different rules to a net or to connections in a net and rely on SPECCTRA to determine which rule has precedence during autorouting. [SPECCTRA rules are hierarchical](#). This means that certain rules have precedence over others.

Routing rules are assigned through commands on the Rules menu. These commands are listed according to their precedence, from lowest to highest. PCB level rules have the lowest precedence and region rules have the highest. Using the Rules menu, you can also control routing costs, fromto sorting (scheduling), and rule checking.

The commands on the Rules menu are

[PCB](#)

[Layer](#)

[Class](#)

[Class Layer](#)

[Net](#)

[Selected Net](#)

[Net Layer](#)

[Group](#)

[Group Layer](#)

[Fromto](#)

[Fromto Layer](#)

[Class to Class](#)

[Class to Class Layer](#)

[Padstack](#)

[Region](#)

[Costs](#)

[Sorting](#)

[Check Rules](#)

## Rules Menu

### Sets placement rules

You can assign different rules to an image set, an image, a component, or a room, and rely on SPECCTRA to determine which rule has precedence during placement and interchange operations. SPECCTRA rules are hierarchical. This means that certain rules have precedence over others. The basic SPECCTRA rule hierarchy from highest to lowest precedence is:

**Image-image**, which are pad edge and body edge spacing rules between two images.

**family-family**, which are pad edge and body edge spacing rules between the images in an image family and the images in one or more other families.

**Room image set**, which are rules for images of a certain type (large, small, capacitor, or discrete) within a room.

**Room**, which are rules for all images in a room.

**Super cluster**, which are rules for components in a super cluster.

**Component**, which are rules for an individual component.

**Image**, which are rules for all instances of an image.

**Image Set**, which are rules for images of a certain type (large, small, capacitor, or discrete).

**PCB**, which are rules for all images in the design.

Super cluster rules are set by using the **define cluster** or **place\_rule** command in the command area. Other placement rules can be assigned through the Rules menu.

The commands on the Rules menu are

[PCB](#)

[Image Set](#)

[Image](#)

[Component](#)

[Room](#)

[Family to Family](#)

[Image to Image](#)

[Check Rules](#)

## Rules - PCB

### Sets routing rules at the PCB level

PCB level rules are global rules that have the lowest [precedence](#) in the SPECCTRA rules hierarchy. Rules at other levels, such as layer, class, net, or fromto, override conflicting PCB rules.

The commands on the Rules - PCB menu are

[Clearance](#)

[Wiring](#)

[Time/Length Factor](#)

[Crosstalk](#)

[Noise](#)

[Wire Grid](#)

[Via Grid](#)

[Smart Grid](#)

[Via Keepout Grid](#)

## Rules - PCB - Clearance

### Sets routing clearance and wire width rules at the PCB level

You can set object-to-object clearance rules with the PCB Clearance Rules dialog box, which contains the following:

**Wire Width** sets the width of wires.

**Same Net Checking** controls checking of rule violations on the same net.

**All** sets all object-to-object clearance rules to the same value.

Each object type can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

**SMD-Via Same Net** sets the PCB clearance between SMD pads and vias on the same net. A -1 means the clearance is not specified.

**Buried-Via Gap** sets the PCB clearance between buried vias. A -1 means the clearance is not specified.

**Antipad Gap** sets the PCB clearance between antipads. A -1 means the clearance is not specified.

**SMD Escape** sets the maximum SMD escape distance that is used when the SMD mounting layer is unselected and not available for routing. A -1 means the SMD escape distance is not specified.

**Via-Via Same Net** sets the PCB clearance between vias on the same net. A -1 means the clearance is not specified.

**Pad-to-Turn Gap** sets the PCB clearance between a pad (through-pin) and the first turn. A -1 means the clearance is not specified.

**SMD-to-Turn Gap** sets the PCB clearance between a SMD pad and the first turn. A -1 means the clearance is not specified.

## Rules - PCB - Wiring

### **Sets wiring rules that control how connections are routed**

You assign PCB level wiring rules in the PCB Wiring Rules dialog box, which contains the following:

**Junctions** controls the occurrence of tjunctions for starburst nets. The options are

[T-Junctions](#)

[Junction Type](#)

**Vias** controls the placement of vias under SMD pads. The options are

[Via at SMD](#)

[Via at SMD Grid](#)

[Via at SMD Fit](#)

[Net Ordering](#) controls how nets are ordered for routing.

[Limit Cross](#) sets limits on crossing conflicts.

[Limit Bends](#) sets limits on bends.

[Limit Vias](#) sets limits on vias.

[Limit Way](#) sets limits on wrong way routing.

[Max Stagger](#) sets the maximum wire lengths for mixed layers.

[Min Shield](#) sets the minimum wire length for shielding.

[Stub Length](#) sets the stub lengths for daisy-chain nets.

## Rules - PCB - Time/Length Factor

### Sets the time conversion factor used to calculate timing delays for wires

The PCB [Time/Length Factor](#) value sets a time conversion factor at the PCB level. This ratio of time per unit length is a multiplier used to calculate effective wire lengths from delay times. It is used for all delay to length conversions unless different Time/Length Factor values are specified at the layer, class, net, or group levels. The length is measured in the current measurement units.

For example, if your measurement unit is mil, and you set a time conversion factor of 10, each mil of wire length is equivalent to 10 time units (usually nanoseconds). A delay rule of 1000 is equivalent to a length rule of 100 mils (1000/10). Make sure you use consistent time units throughout your design.

When the time conversion factor is zero, all timing delay rules are ignored. The timing delay rules are set by using the TIME option in the following commands:

[Rules - Class - Timing](#)

[Rules - Net - Timing](#)

[Rules - Selected Net - Timing](#)

[Rules - Group - Timing](#)

[Rules - Fromto - Timing](#)

### Notes

Rules are hierarchical. If a time conversion factor is set more than once, one time conversion factor rule takes [precedence](#) over another time conversion factor rule. For example, if you set a class layer timing rule and a net layer timing rule, the net layer timing rule takes precedence over the class layer timing rule.

You can set the time conversion factor for specific layers by using the following commands:

[Rules - Layer - Time/Length Factor](#)

[Rules - Class Layer - Timing](#)

[Rules - Net Layer - Timing](#)

[Rules - Group Layer - Timing](#)

[Rules - Fromto Layer - Timing](#)

A time conversion factor for a layer takes [precedence](#) over the time conversion factor at the PCB level.



## Rules - PCB - Crosstalk

### Sets routing rules that control parallel and tandem segment crosstalk

Parallel segment and tandem segment crosstalk rules control the distances wires can be routed in parallel with a given gap. Parallel segment rules apply between wires routed on the same layer. Tandem segment rules apply between wires routed on one layer and two adjacent signal layers.

The PCB Crosstalk Rules dialog box contains the following:

**Turn Off** disables all parallel or tandem crosstalk rules that were set at the PCB level. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** sets the minimum edge-to-edge distance between parallel or tandem wire segments. Parallel or tandem wires with gaps less than the entered value are considered as violations if they are parallel for a distance that exceeds the Length value. Parallel and tandem wires with gaps equal to or greater than the Gap value are ignored.

**Length** sets the maximum parallel or tandem distance above which a violation will occur. Parallel and tandem wire lengths that are equal to or less than the Length value are ignored.

You can enter multiple length and gap rules to approximate a crosstalk curve that varies as a function of these parameters.

#### Note

The parallel segment and tandem segment rules are followed only when the [FST](#) option is installed.

## Rules - PCB - Noise

### Sets routing rules that control parallel and tandem noise coupling

Parallel noise and tandem noise rules control routing by calculating noise coupling between parallel and tandem wires. Parallel noise rules apply to wires routed on the same layer. Tandem noise rules apply to wires routed on adjacent layers.

**Max Noise** sets the PCB level rule that determines the maximum noise that can be coupled onto a net before a violation occurs. The PCB level max noise rule is followed when max noise is not overridden by a higher precedence rule. The Max Noise value and Weight values must be entered in the same units (volts, millivolts, microvolts). These values are usually entered in units of millivolts, but any electrical unit can be used.

**Turn Off** disables all parallel or tandem noise rules that were set at the PCB level. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** sets the edge-to-edge distance between wires. Parallel or tandem wires with gaps less than this value, and with lengths that exceed the Threshold value, are included in coupled noise calculations.

**Threshold** sets the minimum parallel or tandem wire length considered when calculating parallel or tandem coupled noise.

**Weight** specifies the noise transmitted per unit of wire length and is expressed in electrical units such as millivolts. The unit of wire length is the unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value applies per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise coupling curve that varies as a function gap and length.

### Note

The parallel noise and tandem noise rules are followed only when the [FST](#) option is installed.

## Rules - PCB - Wire Grid

### Sets the PCB wire grid

The PCB wire grid is used for all signal layers unless separate wire grids are defined for individual layers. You must enter the grid value in the current measurement units. If you want to route without a grid, set the grid value to 0.

### Notes

If you set the PCB wire grid after you set the Smart Grid, the PCB wire grid overrides the Smart Grid setting.

To set a wire grid for individual layers, use [Rules - Layer - Wire Grid](#).

## Rules - PCB - Via Grid

### Sets PCB via grids

You can set a single grid for all vias in the design by using the All button, or you can set separate via grids by choosing a via from the Via List.

The Via Grid dialog box contains the following:

**Grid** is the spacing between grid points. Enter these in the current measurement units.

### For Via

**All** specifies one via grid.

**From List** specifies separate via grids. If this option is on, click a via ID in the [Via list](#) or use the [Filter data entry box](#) to specify a via ID.

## Rules - PCB - Smart Grid

### Sets the wire grid and the minimum via grid used for autorouting

The Smart Grid dialog box contains the following:

**Wire Grid**, in which you enter a value that is the grid spacing used throughout the autorouting session for routing wires.

**Via Grid**, in which you enter a value that is the via grid used after the first three routing passes. The via grid value should be an even multiple of the wire grid value, and both values must be scaled for the current measurement units.

During the initial three routing passes or until routing completion is 50%, the autorouter calculates a via grid that allows the routing of two wires between adjacent vias. After the third routing pass is completed, the via grid is set to the final spacing value that you enter in the Via Grid data entry box.

The formula used to calculate the initial via grid is

$$\text{initial via grid} = \text{via diameter} + 2(\text{wire width} + \text{wire-to-via clearance}) + \text{wire-to-wire clearance}$$

Smart Grid is designed to avoid via barriers and better distribute vias during the early routing passes and is the preferred method for setting wire and via grids for autorouting.

## Rules - PCB - Via Keepout Grid

### **Reserves via grid points so they are not used for adding vias**

Via keepout grid points are referenced to the 0,0 coordinates of your design. These grid points are reserved, until you restore the via keepout grid to unspecified by entering a value of 0.

The Via Keepout Grid dialog box contains the following:

**Grid**, in which you enter the grid value in the current measurement units.

## Rules - Layer

### Sets routing rules by layer

Layer rules override conflicting PCB rules. Rules at other levels, such as class, net, or fromto, override conflicting layer rules. Layer rules are near the bottom of the [precedence rule level](#).

The commands on the Rules - Layer menu are

[Clearance](#)

[Wiring](#)

[Time/Length Factor](#)

[Crosstalk](#)

[Noise](#)

[Noise Weight](#)

[Wire Grid](#)

[Costing](#)

## Rules - Layer - Clearance

### Sets wire width and clearance rules for layers

The Layer Clearance Rules dialog box contains the following:

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer to assign clearance rules.

**Wire Width** sets the width of wires routed on the layer.

**All** sets all object-to-object clearance rules for the layer to the same value.

You can set a clearance rule for each object on a layer. Each type of object can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The basic object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

**SMD-Via Same Net** sets the clearance between SMD pads and vias on the same net on the layer.

**Via-Via Same Net** sets the clearance between vias on the same net on the layer.

**Buried-Via Gap** sets the clearance between buried vias on the layer.

**Pad-to-Turn Gap** sets the clearance between a pad (through-pin) and the first turn on the layer.

**Antipad Gap** sets the clearance between antipads on the layer.

**SMD-to-Turn Gap** sets the clearance between a SMD pad and the first turn on the layer.



## Rules - Layer - Wiring

### Sets wiring rules for layers

You assign layer wiring rules in the Layer Wiring Rules dialog box, which contains the following:

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer to assign wiring rules.

**Vias** controls the placement of vias under SMD pads. The options are

[Via at SMD](#)

[Via at SMD Grid](#)

[Via at SMD Fit](#)

[Limit Cross](#) sets limits on crossing conflicts.

[Limit Bends](#) sets limits on bends.

[Limit Vias](#) sets limits on vias.

[Limit Way](#) sets limits on wrong way routing.

[Max Stagger](#) sets the maximum wire lengths for mixed layers.

[Stub Length](#) sets the stub lengths for daisy-chain nets.

[Length Factor](#) is used to calculate wire lengths.

### Note

If you do not assign wiring rules for a layer, the autorouter uses default rules for that layer.

## Rules - Layer - Time/Length Factor

**Sets the time conversion factor used to calculate timing delays for wires in a specific layer**

The Layer Time/Length Factor dialog box contains the following:

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer to assign a time/length factor.

[Time/Length Factor](#) value specifies time per unit length for a single layer. This time conversion factor is a multiplier used to calculate effective wire delay times on a layer. The length is measured in the current measurement units.

The layer time conversion factor is used for all delay to length conversions in the layer unless different time conversion factors are set at a higher [precedence level](#). The length is measured in the current measurement units.

For example, if your measurement unit is mil, and you set a time conversion factor of 10, each mil of wire length is equivalent to 10 time units (usually nanoseconds). If you entered a delay rule of 1000, the delay is equivalent to a length rule of 100 mils (1000/10). Make sure you use consistent time units throughout your design.

When the time conversion factor is zero, all timing delay rules in the layer are ignored.

The timing delay rules are set by using the TIME option in the following commands:

[Rules - Class - Timing](#)

[Rules - Net - Timing](#)

[Rules - Selected Net - Timing](#)

[Rules - Class - Timing](#)

[Rules - Group - Timing](#)

[Rules - Fromto - Timing](#)

### Notes

Rules are hierarchical. If a time conversion factor is set more than once, one time conversion factor rule takes [precedence](#) over another time conversion factor rule. For example, if you set a class layer timing rule and a net layer timing rule, the net layer timing rule takes precedence over the class layer timing rule.

You can set the time conversion factor for specific layers by using the following commands:

[Rules - Layer - Time/Length Factor](#)

[Rules - Class Layer - Timing](#)

[Rules - Net Layer - Timing](#)

[Rules - Group Layer - Timing](#)

[Rules - Fromto Layer - Timing](#)

A time conversion factor for a layer takes [precedence](#) over setting the time conversion factor at the PCB level. See also [Rules - PCB - Time/Length Factor](#).

## Rules - Layer - Crosstalk

### Sets parallel and tandem segment layer rules to control crosstalk

Parallel and tandem segment rules control the distances wires can be routed in parallel with a given gap. Parallel segment rules apply between wires routed on the specified layer. Tandem segment rules apply between wires routed on the specified layer and two adjacent signal layers.

The Layer Crosstalk Rules dialog box contains the following:

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer to assign parallel and tandem segment crosstalk rules.

**Turn Off** disables all parallel or tandem crosstalk rules that were set for the layer. When you click Turn Off, parallel or tandem rules for the layer are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel or tandem wire segments. When parallel wires are separated by a distance that is less than the Gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function of gap and length.

### Notes

Parallel and tandem segment crosstalk rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem segment crosstalk rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Crosstalk](#)

[Rules - Class - Crosstalk](#)

[Rules - Class Layer - Crosstalk](#)

[Rules - Net - Crosstalk](#)

[Rules - Selected Net - Crosstalk](#)

[Rules - Net Layer - Crosstalk](#)

[Rules - Group - Crosstalk](#)

[Rules - Group Layer - Crosstalk](#)

[Rules - Fromto - Crosstalk](#)

[Rules - Fromto Layer - Crosstalk](#)

[Rules - Class to Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

## Rules - Layer - Noise

### Sets parallel and tandem layer rules to control noise coupling

Parallel noise and tandem noise rules control routing by calculating noise coupling between parallel and tandem wires. Parallel noise rules apply to wires routed on the same layer. Tandem noise rules apply to wires routed on adjacent layers.

The Layer Noise Rules dialog box contains the following:

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer to assign parallel and tandem noise rules.

**Turn Off** disables all parallel noise or tandem noise rules that were set for the active layer. When you click Turn Off, corresponding parallel or tandem rules for the layer are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the longest distance wires can be parallel, before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between the parallel wires is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the amount of noise transmitted per unit of wire length and expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value applies per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise coupling curve that varies as a function of gap and length.

### Notes

Parallel noise rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem noise rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Noise](#)

[Rules - Class - Noise](#)

[Rules - Class Layer - Noise](#)

[Rules - Net - Noise](#)

[Rules - Selected Net - Noise](#)

[Rules - Net Layer - Noise](#)

[Rules - Group - Noise](#)

[Rules - Group Layer - Noise](#)

[Rules - Fromto - Noise](#)

[Rules - Fromto Layer - Noise](#)

[Rules - Class to Class - Noise](#)

### Rules - Class to Class Layer - Noise

To adjust the noise weight of nets by layer, use Rules - Layer - Noise Weight.

## Rules - Layer - Noise Weight

### Adjusts the noise weight of nets by layer

Layer noise weight is used to factor different PCB layer characteristics into coupled noise calculations. The amount of noise transmitted by a net routed on an internal layer can be different from the amount of noise transmitted if the net is routed on an external layer. The layer noise weight factors are defined to adjust the noise weights of nets according to the layers on which they are routed. Layer noise weight is defined for pairs of signal layers, which can be the same layer or adjacent layers.

When a power layer separates signal layers, the power layer is assumed to act as a perfect shield to transmitted noise. Therefore, power layers should not be included in layer noise weight pairs, and signal layers separated by a power layer should not be assigned layer noise weight factors.

The Layer Noise Weight dialog box contain the following:

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer to assign a noise weight.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the same layer or an adjacent layer.

**Weight** sets the noise weight factor for the layer pair.

### Notes

To set noise rules by layer, start by setting one parallel or tandem noise value using [Rules - Layer - Noise](#). Then use **Rules - Layer - Noise Weight** to adjust the parallel and tandem noise values for other layers. *Parallel* noise is from a layer to itself. *Tandem* noise is from one layer to an adjacent layer.

Layer noise weight rules are followed only when the [FST](#) option is installed.

## Rules - Layer - Wire Grid

### Sets a wire grid for all layers or for individual layers

When you set a wire grid, all new routing and rerouting conforms to the grid except in which pin entries or exits are off grid. Connections that are already routed before you set the grid might not be on the current grid unless they are rerouted. The Layer Wire Grid dialog box contains the following:

**Grid** sets the wire grid spacing. Grid values must be scaled for your current measurement units. Enter a value of 0 to route without a grid.

#### For Layer:

**All** sets the grid for all layers. When All is checked, the grid is set for all layers.

**From List** sets the grid for the layers that you choose by using the [Layer list](#) and [Filter](#).

## Rules - Layer - Costing

### Sets the cost to use a layer for routing or allow wrong way routing on a layer

The **Rules - Layer - Costing** command influences how much

- A layer is used for routing
- Wrong way routing is used in place of vias

The Layer Costing dialog box contains the following:

#### Cost Type

**Length** controls how much a layer is used for routing. When Cost Value is set to a value other than Off, the setting determines how much the layer is used for routing.

**Wrong Way** controls how much wrong way routing is used in place of vias. When Wrong Way is checked, the Cost Value affects how much wrong way routing is used on the layer.

**Cost Value** sets the cost for the layer to Off (default), Free, Low, Medium, High, or Forbidden. When cost is Free, the cost type is allowed without a cost value. When cost is Forbidden, the selected cost type is prohibited. The Low, Medium, and High cost values provide a range of intermediate costs between the extremes. If the Cost Value is set to Off (default), the cost is unspecified.

#### Notes

When you set a cost, you override corresponding default costs that change dynamically as routing completion and other conditions change.

You can also prohibit routing on a layer by unselecting it in the [Layer panel](#) or with the **unselect layer\_wires** command.



## Rules - Class

### Sets routing rules for defined classes of nets

Setting [class](#) rules is a convenient way of assigning rules to a number of nets at the same time.

Class rules override conflicting PCB and layer rules. Rules at other levels, such as net, group, or fromto, override conflicting class rules in the [SPECCTRA rules hierarchy](#).

The command on the Rules - Class menu are

[Clearance](#)

[Wiring](#)

[Timing](#)

[Shielding](#)

[Crosstalk](#)

[Noise](#)

## Rules - Class - Clearance

### Sets routing clearance and width rules for a class of nets

A class must be defined before you can assign rules to the class. See [Define - Class](#) for help on defining a class of nets.

The Class Clearance Rules dialog box contains the following:

**Pick Class** displays the [Pick Active Class for Rules](#) dialog box in which you choose the class to assign clearance rules.

**Wire Width** sets the width of wires for the class of nets.

**All** sets all object-to-object clearance rules for the class to the same value.

You can set a clearance rule for each object attached to the nets in a class. Each type of object can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The basic object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

You can also assign the following class rules:

**SMD-Via Same Net** sets the clearance rule between SMD pads and vias on the same net.

**Via-Via Same Net** sets the clearance rule between vias on the same net.

**Buried-Via Gap** sets the clearance rule between buried vias.

**Pad-to-Turn Gap** sets the clearance rule between a pad (through-pin) and the first turn.

**Antipad Gap** sets the clearance rule between antipads.

**SMD-to-Turn Gap** sets the clearance rule between a SMD pad and the first turn.

## Rules - Class - Wiring

### Sets routing rules for a class of nets

A class must be defined before you can assign rules to the class. See [Define - Class](#) for help on defining a class of nets.

You assign rules to a class of nets and control how they are routed by using the Class Wiring Rules dialog box. You can assign different wiring rule values for each class.

If you do not assign wiring rules for a class, the autorouter uses default rules for that class.

The Class Wiring Rules dialog box contains the following:

**Pick Class** displays the [Pick Active Class for Rules](#) dialog box in which you choose the class to assign wiring rules.

**Junctions** controls the occurrence of tjunctions for starburst nets.

[T-Junction](#)

[Junction Type](#)

**Vias** controls the placement of vias under SMD pads.

[Via at SMD](#)

[Via at SMD Grid](#)

[Via at SMD Fit](#)

[Net Ordering](#) controls how nets are ordered for routing.

[Net Priority](#) determines when a net is scheduled for routing with respect to other nets.

[Limit Cross](#) sets limits on crossing conflicts.

[Limit Vias](#) sets limits on vias.

[Limit Bends](#) sets limits on bends.

[Limit Way](#) sets limits on wrong way routing.

[Max Stagger](#) sets the maximum wire lengths for mixed layers.

[Stub Length](#) sets the stub lengths for daisy-chain nets.

[Use Vias](#) is used with the [Vias list](#) and [Filter](#) to determine the vias to use for routing the class.

[Max Total Vias \(per Net\)](#) sets the maximum number of vias.

[Effective Via Length](#) determines the amount added to wire length calculations by each through-via.

[Use Layers](#) is used with the [Layers list](#) and [Filter](#) to select the routing layers for the class.

## Rules - Class - Timing

### Sets timing rules for a class of nets

After you define a class of nets by using [Define - Class](#), you can set the timing rules for all the nets in the class. You control timing by LENGTH or TIME. The Class Timing Rules dialog box contains the following:

**Pick Class** displays the [Pick Active Class for Rules](#) dialog box in which you choose the class to assign timing rules.

To control the routing patterns for wires in a class of nets, use

[Length Gap](#)

[Length Amplitude](#)

**LENGTH** specifies timing rules in the current measurement units, usually inches or mils. The LENGTH options are

[Min Length](#)

[Max Length](#)

[Specify as Ratios](#)

[Match Net](#)

[Length Tolerance](#)

[Match Fromto](#)

[Length Tolerance](#)

**TIME** specifies timing rules in time units, usually picoseconds or nanoseconds. You must set the Time/Length Factor for timing rules to apply. All delay rules must use the same time units. The TIME options are

[Time/Length Factor](#)

[Min Delay](#)

[Max Delay](#)

[Match Net](#)

[Delay Tolerance](#)

[Match Fromto](#)

[Delay Tolerance](#)

### Notes

You cannot set both length and delay rules for the same class of nets. If you try to set both rules, only the last one specified is used.

Timing rules are followed only when the [FST](#) option is installed.

## Rules - Class - Shielding

**Turns shielding on and off, chooses the power net that attaches to the shield, and sets shield width and gap rules to a class of nets**

**Pick Class** displays the [Pick Active Class for Rules](#) dialog box in which you choose the class of nets to be shielded.

**Shielding** determines whether shielding is turned on or turned off when you apply the dialog box. If the Shielding option button is checked, shielding is turned on when the dialog box is applied. Shielding is turned off (unspecified) for the class of nets, when the dialog box is applied and the Shielding option button is not checked.

The [Shield Net list](#) and the [Filter](#) are used to choose which power net attaches to the shield. You can choose only one power net to shield the nets in the class.

**Shield Width** sets the width for the shield wire. The width value must be entered for your current measurement units. A value of -1 means that shield width is unspecified, in which case, the shield wire width defaults to the same width as the signal wire being shielded.

**Shield Gap** sets the edge-to-edge distance between the shield wire and the signal wires being shielded. A value of -1 means that the shield gap is unspecified. In this case, the gap defaults to the wire-to-wire clearance rule for the signal nets being shielded.

### Note

Shield rules are followed only when the [FST](#) option is installed.

You can set shield rules at other [precedence levels](#) by using the following commands:

[Rules - Net - Shielding](#)

[Rules - Selected Net - Shielding](#)

[Rules - Group - Shielding](#)

[Rules - Fromto - Shielding](#)

## Rules - Class - Crosstalk

**Sets parallel segment and tandem segment rules to control crosstalk between nets in a class and between nets in the class and all other nets**

Parallel and tandem segment rules control the distances wires can be routed in parallel with a given gap. Parallel segment rules apply between wires routed on the same layer. Tandem segment rules apply between wires routed on a layer and two adjacent signal layers.

The Class Crosstalk Rules dialog box contains the following:

**Pick Class** displays the [Pick Active Class for Rules](#) dialog box in which you choose the class to assign parallel segment and tandem segment crosstalk rules.

**Turn Off** disables all parallel or tandem crosstalk rules that were set for the active class. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel wire segments. When parallel wires are separated by a distance that is less than the gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance that wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function of gap and length.

### Note

Parallel segment and tandem segment crosstalk rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem segment crosstalk rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Crosstalk](#)

[Rules - Layer - Crosstalk](#)

[Rules - Class Layer - Crosstalk](#)

[Rules - Net - Crosstalk](#)

[Rules - Selected Net - Crosstalk](#)

[Rules - Net Layer - Crosstalk](#)

[Rules - Group - Crosstalk](#)

[Rules - Group Layer - Crosstalk](#)

[Rules - Fromto - Crosstalk](#)

[Rules - Fromto Layer - Crosstalk](#)

[Rules - Class to Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

## Rules - Class - Noise

**Sets parallel noise and tandem noise rules to control noise coupling between the nets in a class and between the nets in a class and all other nets**

Parallel noise and tandem noise rules control routing by calculating noise coupling between parallel and tandem wires. Parallel noise rules apply to wires routed on the same layer. Tandem noise rules apply to wires routed on adjacent layers.

The Class Coupled Noise Rules dialog box contains the following:

**Pick Class** displays the [Pick Active Class for Rules](#) dialog box in which you choose the class to assign parallel noise and tandem noise rules.

**Turn Off** disables all parallel or tandem noise rules that were set for the active class. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Max Noise** sets the maximum noise that can be coupled onto each net in the class before wires involved in the calculations are rerouted to reduce calculated noise below the maximum value. A Max Noise value of -1 resets the maximum noise rule for the class of nets to unspecified.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the longest distance that wires can be parallel, before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the noise transmitted per unit of wire length and is expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value applies per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise curve that varies as a function of gap and length.

### Note

Parallel noise and tandem noise rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem noise rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Noise](#)

[Rules - Layer - Noise](#)

[Rules - Class Layer - Noise](#)

[Rules - Net - Noise](#)

[Rules - Selected Net - Noise](#)

[Rules - Net Layer - Noise](#)

[Rules - Group - Noise](#)

Rules - Group Layer - Noise

Rules - Fromto - Noise

Rules - Fromto Layer - Noise

Rules - Class to Class - Noise

Rules - Class to Class Layer - Noise



## Rules - Class Layer

### **Sets routing rules for a class of nets on a particular layer**

Class layer rules override conflicting PCB, layer, and class rules. Rules at other levels, such as net, group, or fromto, override conflicting class layer rules in the [SPECCTRA rules hierarchy](#).

The commands on the Rules - Class Layer menu are

[Clearance](#)

[Timing](#)

[Crosstalk](#)

[Noise](#)

## Rules - Class Layer - Clearance

### **Sets routing clearance and width rules for a class of nets on a specific layer**

The Class Layer Clearance Rules dialog box contains the following:

**Pick Class** displays the [Pick Active Class for Rules](#) dialog box in which you choose the class to assign clearance and width rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Wire Width** sets the width of wires for the class of nets.

**All** sets all object-to-object clearance rules for the class to the same value.

You can set a clearance rule for each object attached to the nets in a class. Each type of object can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The basic object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

You can also assign the following class layer rules:

**SMD-Via Same Net** sets the clearance rule between SMD pads and vias on the same net.

**Via-Via Same Net** sets the clearance rule between vias on the same net.

**Pad-to-Turn Gap** sets the clearance rule between a pad (through-pin) and the first turn.

**SMD-to-Turn Gap** sets the clearance rule between a SMD pad and the first turn.

## Rules - Class Layer - Timing

### Sets timing rules for a class of nets on a specific layer

The Class Layer Clearance Rules dialog box contains the following:

**Pick Class** displays the [Pick Active Class for Rules](#) dialog box in which you choose the class to assign timing rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

[Length Gap](#) determines the edge-to-edge distance maintained between adjacent segments when the autorouter uses an accordion, trombone, or serpentine pattern.

[Length Amplitude](#) determines the maximum height of an accordion routing pattern.

[Time/Length Factor](#) sets a time conversion factor for wire lengths.

### Note

Timing rules are followed only when the [FST](#) option is installed.

## Rules - Class Layer - Crosstalk

### Sets parallel and tandem segment class layer rules to control crosstalk

Parallel and tandem segment rules control the distances wires can be routed in parallel with a given gap. Parallel segment rules apply between wires routed on the specified layer. Tandem segment rules apply between wires routed on the specified layer and two adjacent signal layers.

Class layer rules apply to a class of nets on a specific layer. The Class Layer Crosstalk Rules dialog box contains the following:

**Pick Class** displays the [Pick Active Class for Rules](#) dialog box in which you choose the class to assign parallel and tandem segment rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Turn Off** disables all parallel or tandem crosstalk rules that were set for the class. When you click Turn Off, parallel or tandem rules for the layer are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel or tandem wire segments. When parallel wires are separated by a distance that is less than the Gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function of gap and length.

### Notes

Parallel and tandem segment crosstalk rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem segment crosstalk rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Crosstalk](#)

[Rules - Layer - Crosstalk](#)

[Rules - Class - Crosstalk](#)

[Rules - Net - Crosstalk](#)

[Rules - Selected Net - Crosstalk](#)

[Rules - Net Layer - Crosstalk](#)

[Rules - Group - Crosstalk](#)

[Rules - Group Layer - Crosstalk](#)

[Rules - Fromto - Crosstalk](#)

[Rules - Fromto Layer - Crosstalk](#)

[Rules - Class to Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

## Rules - Class Layer - Noise

**Sets parallel noise and tandem noise rules to control noise coupling on a specific layer between the nets in a class and between the nets in a class and all other nets**

Parallel noise and tandem noise rules control routing by calculating noise coupling between parallel and tandem wires. Parallel noise rules apply to wires routed on the same layer. Tandem noise rules apply to wires routed on adjacent layers.

The Class Layer Noise Rules dialog box contains the following:

**Pick Class** displays the [Pick Active Class for Rules](#) dialog box in which you choose the class to assign parallel noise and tandem noise rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Turn Off** disables all parallel or tandem noise rules that were set for the active class. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the longest distance that wires can be parallel, before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the noise transmitted per unit of wire length and is expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value applies per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise curve that varies as a function of gap and length.

### Note

Parallel noise and tandem noise rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem noise rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Noise](#)

[Rules - Layer - Noise](#)

[Rules - Class - Noise](#)

[Rules - Net - Noise](#)

[Rules - Selected Net - Noise](#)

[Rules - Net Layer - Noise](#)

[Rules - Group - Noise](#)

[Rules - Group Layer - Noise](#)

Rules - Fromto - Noise

Rules - Fromto Layer - Noise

Rules - Class to Class - Noise

Rules - Class to Class Layer - Noise

## Rules - Net

### Sets routing rules for nets

Net rules override conflicting PCB, layer and class rules. Rules at other levels, such as group, fromto, or class to class, override conflicting net rules in the [SPECCTRA rules hierarchy](#).

The commands on the Rules - Net menu are

[Clearance](#)

[Wiring](#)

[Timing](#)

[Shielding](#)

[Crosstalk](#)

[Noise](#)

## Rules - Net - Clearance

### Sets routing clearance and width rules for nets

You can set a clearance rule for each object attached to a net. Each type of object can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The Net Clearance Rules dialog box contains the following:

**Pick Net** displays the [Pick Active Net for Rules](#) dialog box in which you choose the net to assign clearance rules.

**Wire Width** sets the wire width rule.

**All** sets all net clearance rules to the same value.

Each object type can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

**SMD-Via Same Net** sets the clearance between SMD pads and vias on the same net.

**Via-Via Same Net** sets the clearance between vias on the same net.

**Buried-Via Gap** sets the clearance between buried vias.

**Pad-to-Turn Gap** sets the clearance between a pad (through-pin) and the first turn.

**Antipad Gap** sets the clearance between antipads.

**SMD-to-Turn Gap** sets the clearance between a SMD pad and the first turn.



## Rules - Net - Wiring

### Sets routing rules for nets

You assign rules to individual nets of your design and control how they are routed by using the Net Wiring Rules dialog box. You can assign different wiring rule values to each net. The Net Wiring Rules dialog box contains the following:

**Junctions** controls the occurrence of tjunctions for starburst nets.

[T-Junctions](#)

[Junction Type](#)

**Vias** controls the placement of vias under SMD pads.

[Via at SMD](#)

[Via at SMD Grid](#)

[Via at SMD Fit](#)

[Net Ordering](#) controls how nets are ordered for routing.

[Net Priority](#) determines when a net is scheduled for routing with respect to other nets.

[Limit Cross](#) sets limits on crossing conflicts.

[Limit Vias](#) sets limits on vias.

[Limit Bends](#) sets limits on bends.

[Limit Way](#) sets limits on wrong way routing.

[Max Stagger](#) sets the maximum wire lengths for mixed layers.

[Stub Length](#) sets the stub lengths for daisy-chain nets.

[Use Vias](#) is used with the [Vias list](#) and [Filter](#) to determine the vias to use for routing the class.

[Max Total Vias \(per Net\)](#) sets the maximum number of vias.

[Effective Via Length](#) determines the amount added to wire length calculations by each through-via.

[Use Layers](#) is used with the [Layers list](#) and [Filter](#) to select the routing layers for the class.

### Note

If you do not assign wiring rules for a net, the autorouter uses default rules for that net.

## Rules - Net - Timing

### Sets timing rules for a net

You can control timing by LENGTH or TIME. The Net Timing Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose the net to assign timing rules.

To control the routing patterns for wires, use

[Length Gap](#)

[Length Amplitude](#)

**LENGTH** specifies timing rules in the current measurement units, usually inches or mils. The LENGTH options are

[Min Length](#)

[Max Length](#)

[Specify as Ratios](#)

[Match Fromto](#)

[Length Tolerance](#)

**TIME** specifies timing rules in time units, usually picoseconds or nanoseconds. You must set the Time/Length Factor for timing rules to apply. All delay rules must use the same time units. The TIME options are

[Time/Length Factor](#)

[Min Delay](#)

[Max Delay](#)

[Match Fromto](#)

[Delay Tolerance](#)

### Notes

You cannot set both length and delay rules for the same class of nets. If you try to set both rules, only the last one specified is used.

Timing rules are followed only when the [FST](#) option is installed.

You must set the Time/Length Factor for timing rules to apply. All delay rules must use the same time units.

## Rules - Net - Shielding

**Turns shielding on and off, chooses the power net that will serve as the shield, and sets shield width and gap rules for a net**

The Net Shielding Rules dialog box contains the following

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose the net to be shielded.

**Shielding** determines whether shielding is turned on or turned off when you apply the dialog box. If the Shielding option button is checked, shielding is turned on when the dialog box is applied. Shielding is turned off (unspecified), when the dialog box is applied and the Shielding option button is not checked.

The [Shield Net list](#) and the [Filter](#) are used to choose which power net attaches to the shield. You can choose only one power net.

**Shield Width** sets the width for the shield wire. The width value must be entered for your current measurement units. A value of -1 means that shield width is unspecified, in which case, the shield wire width defaults to the same width as the signal wire being shielded.

**Shield Gap** sets the edge-to-edge distance between the shield wire and the signal wires being shielded. A value of -1 means that the shield gap is unspecified, in which case, the gap defaults to the wire-to-wire clearance rule for the signal nets being shielded.

### Note

Shield rules are followed only when the [FST](#) option is installed.

You can set shield rules at other [precedence levels](#) by using the following commands:

[Rules - Class - Shielding](#)

[Rules - Selected Net - Shielding](#)

[Rules - Group - Shielding](#)

[Rules - Fromto - Shielding](#)

## Rules - Net - Crosstalk

### Sets parallel segment and tandem segment rules to control crosstalk for a net

Parallel and tandem segment rules control the distances wires can be routed in parallel with a given gap. Parallel segment rules apply between wires routed on the same layer. Tandem segment rules at the net level apply between the specified net and wires routed on two adjacent signal layers.

The Net Crosstalk Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose nets to assign parallel segment and tandem segment rules.

**Turn Off** disables all parallel or tandem crosstalk rules that were set for the active net. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel wire segments. When parallel wires are separated by a distance that is less than the gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance that wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function gap and length.

### Notes

Parallel segment and tandem segment crosstalk rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem segment crosstalk rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Crosstalk](#)

[Rules - Layer - Crosstalk](#)

[Rules - Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

[Rules - Selected Net - Crosstalk](#)

[Rules - Net Layer - Crosstalk](#)

[Rules - Group - Crosstalk](#)

[Rules - Group Layer - Crosstalk](#)

[Rules - Fromto - Crosstalk](#)

[Rules - Fromto Layer - Crosstalk](#)

[Rules - Class to Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

## Rules - Net - Noise

### Sets parallel noise and tandem noise rules to control noise coupling between nets

Parallel noise rules control parallel length and gap between wires on the same layer. Tandem noise rules control parallel length and gap between wires on two adjacent layers. The Net Noise Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose nets that must follow parallel noise and tandem noise rules.

**Max Noise** sets the maximum noise that can be coupled onto a net before wires involved in the calculations are rerouted to reduce the noise calculation below the maximum value. A Max Noise value of -1 resets the maximum noise rule for the net to unspecified.

**Turn Off** disables all parallel or tandem noise rules that were set for the active net. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the minimum distance that wires can be parallel or tandem before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the noise transmitted per unit of wire length and is expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value applies per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise coupling curve that varies as a function gap and length.

### Note

Parallel noise and tandem noise rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem noise rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Noise](#)

[Rules - Layer - Noise](#)

[Rules - Class - Noise](#)

[Rules - Class Layer - Noise](#)

[Rules - Selected Net - Noise](#)

[Rules - Net Layer - Noise](#)

[Rules - Group - Noise](#)

[Rules - Group Layer - Noise](#)

[Rules - Fromto - Noise](#)

Rules - Fromto Layer - Noise

Rules - Class to Class - Noise

Rules - Class to Class Layer - Noise

## Rules - Selected Net

### Sets routing rules for selected nets

Net rules override conflicting PCB, layer and class rules. Rules at other levels, such as group, fromto, or class to class, override conflicting net rules in the [SPECCTRA rules hierarchy](#).

The commands on the Rules - Selected Net menu are

[Clearance](#)

[Wiring](#)

[Timing](#)

[Shielding](#)

[Crosstalk](#)

[Noise](#)

## Rules - Selected Net - Clearance

### Sets routing clearance and width rules for selected nets

Before you assign rules, you must select the net(s) by using one of the [Select - Nets](#) commands or the Select Net button on the tool bar

The Selected Net Clearance Rules dialog box contains the following:

**Wire Width** sets the wire width rule.

**All** sets all net clearance rules to the same value.

You can set a clearance rule for each type of object on a selected net. Each object type can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

**SMD-Via Same Net** sets the clearance between SMD pads and vias on the same net.

**Via-Via Same Net** sets the clearance between vias on the same net.

**Buried-Via Gap** sets the clearance between buried vias.

**Pad-to-Turn Gap** sets the clearance between a pad (through-pin) and the first turn.

**Antipad Gap** sets the clearance between antipads.

**SMD-to-Turn Gap** sets the clearance between a SMD pad and the first turn.

### Note

**Rules - Selected Net - Clearance** applies only to nets. If individual pin-to-pin (fromto) connections are selected, the rules do not apply.



## Rules - Selected Net - Wiring

### Sets routing rules for selected nets

Before you assign rules, you must select the net(s) by using one of the [Select - Nets](#) commands or the Select Net button on the tool bar

You assign rules for selected nets and control how they are routed by using the Selected Net Wiring Rules dialog box. You can assign different wiring rule values for each net. The Net Wiring Rules dialog box contains the following:

**Junctions** controls the occurrence of tjunctions for starburst nets.

[T-Junctions](#)

[Junction Type](#)

**Vias** controls the placement of vias under SMD pads.

[Via at SMD](#)

[Via at SMD Grid](#)

[Via at SMD Fit](#)

[Net Ordering](#) controls how nets are ordered for routing.

[Net Priority](#) determines when a net is scheduled for routing with respect to other nets.

[Limit Cross](#) sets limits on crossing conflicts.

[Limit Vias](#) sets limits on vias.

[Limit Bends](#) sets limits on bends.

[Limit Way](#) sets limits on wrong way routing.

[Max Stagger](#) sets the maximum wire lengths for mixed layers.

[Stub Length](#) sets the stub lengths for daisy-chain nets.

[Use Vias](#) is used with the [Vias list](#) and [Filter](#) to determine the vias to use for routing the class.

[Max Total Vias](#) sets the maximum number of vias.

[Effective Via Length](#) determines the amount added to wire length calculations by each through-via.

[Use Layers](#) is used with the [Layers list](#) and [Filter](#) to select the routing layers for the class.

### Notes

Selected net wiring rules are assigned to all nets that are currently selected.

**Rules - Selected Net - Wiring** applies only to nets. If individual pin-to-pin (fromto) connections are selected, the rules do not apply.

The autorouter uses default values (or rules assigned at a lower precedence level) for any rules you do not assign.

## Rules - Selected Net - Timing

### Sets timing rules for selected nets

Before you assign rules, you must select the net(s) by using one of the [Select - Nets](#) commands or the Select Net button on the tool bar

You can control timing by LENGTH or TIME. The Selected Net Timing Rules dialog box contains the following:

To control the routing patterns for wires, use

[Length Gap](#)

[Length Amplitude](#)

**LENGTH** specifies timing rules in the current measurement units, usually inches or mils. The LENGTH options are

[Min Length](#)

[Max Length](#)

[Specify as Ratios](#)

[Match Fromto](#)

[Length Tolerance](#)

**TIME** specifies timing rules in time units, usually picoseconds or nanoseconds. You must set the Time/Length Factor for timing rules to apply. All delay rules must use the same time units. The TIME options are

[Time/Length Factor](#)

[Min Delay](#)

[Max Delay](#)

[Match Fromto](#)

[Delay Tolerance](#)

### Notes

You cannot set both length and delay rules for the same net. If you try to set both rules, only the last one specified is used.

Timing rules are followed only when the [FST](#) option is installed.

You must set the Time/Length Factor for timing rules to apply. All delay rules must use the same time units.

Remember to select the net to which you want to apply the rule. Use one of the [Select - Nets](#) commands before you use **Rules - Selected Net - Timing**.

**Rules - Selected Net - Timing** applies only to nets. If individual pin-to-pin (fromto) connections are selected, the rules do not apply.

## Rules - Selected Net - Shielding

**Turns shielding on or off for selected nets, chooses the power net that will serve as the shield, and sets shield width and gap rules for selected nets**

Before you assign rules, you must select the net(s) by using one of the [Select - Nets](#) commands or the Select Net button on the tool bar

The Selected Net Shielding Rules dialog box contains the following:

**Shielding** determines whether shielding is turned on or turned off when you apply the dialog box. If the Shielding option button is checked, shielding is turned on when the dialog box is applied. Shielding is turned off (unspecified), when the dialog box is applied and the Shielding option button is not checked.

The [Shield Net list](#) and the [Filter](#) are used to choose which power net attaches to the shield. You can choose only one power net.

**Shield Width** sets the width for the shield wire. The width value must be entered for your current measurement units. A value of -1 means that shield width is unspecified, in which case, the shield wire width defaults to the same width as the signal wire being shielded.

**Shield Gap** sets the edge-to-edge distance between the shield wire and the signal wires being shielded. A value of -1 means that the shield gap is unspecified. In which case, the gap defaults to the wire-to-wire clearance rule for the signal nets being shielded.

### Notes

**Rules - Selected Net - Shielding** applies only to nets. If individual pin-to-pin (fromto) connections are selected, the rules do not apply.

Shield rules are followed only when the [FST](#) option is installed.

You can set shield rules at other [precedence levels](#) by using the following commands:

[Rules - Class - Shielding](#)

[Rules - Net - Shielding](#)

[Rules - Group - Shielding](#)

[Rules - Fromto - Shielding](#)

## Rules - Selected Net - Crosstalk

### Sets parallel segment and tandem segment rules to control crosstalk

Before you assign rules, you must select the net(s) by using one of the [Select - Nets](#) commands or the Select Net button on the tool bar

Parallel segment rules control parallel length and gap between wires on the same layer. Tandem segment rules control parallel length and gap between the selected net and wires on two adjacent signal layers. The Selected Crosstalk Rules dialog box contains the following:

**Turn Off** disables all parallel or tandem crosstalk rules that were set for the active net. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel wire segments. When parallel wires are separated by a distance that is less than the gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance that wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function gap and length.

### Notes

**Rules - Selected Net - Crosstalk** applies only to nets. If individual pin-to-pin (fromto) connections are selected, the rules do not apply.

Parallel segment and tandem segment crosstalk rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem segment crosstalk rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Crosstalk](#)

[Rules - Layer - Crosstalk](#)

[Rules - Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

[Rules - Net - Crosstalk](#)

[Rules - Net Layer - Crosstalk](#)

[Rules - Group - Crosstalk](#)

[Rules - Group Layer - Crosstalk](#)

[Rules - Fromto - Crosstalk](#)

[Rules - Fromto Layer - Crosstalk](#)

[Rules - Class to Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

## Rules - Selected Net - Noise

### Sets parallel noise and tandem noise rules to control noise coupling between nets

Before you assign rules, you must select the net(s) by using one of the [Select - Nets](#) commands or the Select Net button on the tool bar

Parallel noise rules control parallel length and gap between wires on the same layer. Tandem noise rules control parallel length and gap between wires on adjacent layers.

The Selected Net Coupled Noise Rules dialog box contains the following:

**Max Noise** sets the maximum noise that can be coupled onto selected nets before the wires involved in the calculations are rerouted to reduce calculated noise below the maximum value. A Max Noise value of -1 resets a maximum noise rule to unspecified.

**Turn Off** disables all parallel or tandem noise rules that were set for the selected net or nets. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the minimum distance that wires can be parallel, before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the noise transmitted per unit of wire length and is expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value applies per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise curve that varies as a function of gap and length.

### Notes

**Rules - Selected Net - Noise** applies only to nets. If individual pin-to-pin (fromto) connections are selected, the rules do not apply.

Parallel noise and tandem noise rules are followed only when the [FST](#) option is installed.

## Rules - Net Layer

### **Sets routing rules for nets on a specific layer**

Net layer rules override conflicting PCB, layer, class, and net rules. Rules at other levels, such as group, fromto, or class to class, override conflicting net layer rules in the [SPECCTRA rules hierarchy](#).

The command on the Rules - Net Layer menu are

[Clearance](#)

[Timing](#)

[Crosstalk](#)

[Noise](#)

## Rules - Net Layer - Clearance

### **Sets routing clearance and width rules for nets on a specific layer**

The Net Layer Clearance Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose nets to assign clearance and width rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Wire Width** sets the wire width rule.

**All** sets all net clearance rules to the same value.

You can set a clearance rule for each type of object on a net. Each object type can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

**SMD-Via Same Net** sets the clearance between SMD pads and vias on the same net.

**Via-Via Same Net** sets the clearance between vias on the same net.

**Pad-to-Turn Gap** sets the clearance between a pad (through-pin) and the first turn.

**SMD-to-Turn Gap** sets the clearance between a SMD pad and the first turn.

## Rules - Net Layer - Timing

### Sets timing rules for nets on a specific layer

The Net Layer Clearance Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose nets to assign timing rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

[Length Gap](#) determines the edge-to-edge distance maintained between adjacent segments when the autorouter uses an accordion, trombone, or serpentine pattern.

[Length Amplitude](#) determines the maximum height of an accordion routing pattern.

[Time/Length Factor](#) sets a time conversion factor for wire lengths.

### Note

Timing rules are followed only when the [FST](#) option is installed.



## Rules - Net Layer - Crosstalk

### Sets crosstalk rules for nets on a specific layer

Parallel segment rules control parallel length and gap between wires on the same layer. Tandem segment rules control parallel length and gap between wires on the selected layer and wires on two adjacent signal layers.

The Net Layer Crosstalk Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose nets to assign crosstalk rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Turn Off** disables all parallel or tandem crosstalk rules that were set for the active net. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel wire segments. When parallel wires are separated by a distance that is less than the gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance that wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function gap and length.

### Notes

Parallel and tandem segment crosstalk rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem segment crosstalk rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Crosstalk](#)

[Rules - Layer - Crosstalk](#)

[Rules - Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

[Rules - Net - Crosstalk](#)

[Rules - Selected Net - Crosstalk](#)

[Rules - Group - Crosstalk](#)

[Rules - Group Layer - Crosstalk](#)

[Rules - Fromto - Crosstalk](#)

[Rules - Fromto Layer - Crosstalk](#)

[Rules - Class to Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

## Rules - Net Layer - Noise

### Sets noise rules for nets on a specific layer

Parallel noise and tandem noise rules control routing by calculating noise coupling between parallel and tandem wires. Parallel noise rules apply to wires routed on the same layer. Tandem noise rules apply to wires routed on adjacent layers.

The Net Layer Noise Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose nets to assign timing rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Turn Off** disables all parallel or tandem noise rules that were set for the active class. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the longest distance that wires can be parallel, before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the noise transmitted per unit of wire length and is expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value applies per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise curve that varies as a function of gap and length.

### Notes

Parallel and tandem noise rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem noise rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Noise](#)

[Rules - Layer - Noise](#)

[Rules - Class - Noise](#)

[Rules - Net - Noise](#)

[Rules - Selected Net - Noise](#)

[Rules - Group - Noise](#)

[Rules - Group Layer - Noise](#)

[Rules - Fromto - Noise](#)

[Rules - Fromto Layer - Noise](#)

[Rules - Class to Class - Noise](#)

## Rules - Class to Class Layer - Noise

## Rules - Group

### **Sets routing rules for groups of fromtos**

Group rules override conflicting PCB, layer, class, and net rules. Rules at other levels, such as fromto and class-to-class, override conflicting group rules in the [SPECCTRA rules hierarchy](#).

The command on the Rules - Group menu are

[Clearance](#)

[Wiring](#)

[Timing](#)

[Shielding](#)

[Crosstalk](#)

[Noise](#)

## Rules - Group - Clearance

### Sets wire width and clearance rules for a group of fromtos

Before you assign rules to a group of [fromtos](#), you must define the group by using the [Define - Group](#) command.

The Group Clearance Rules dialog box contains the following:

**Pick Group** displays the [Pick Active Group for Rules](#) dialog box in which you choose groups to assign width and clearance rules.

**Wire Width** sets the wire width rule.

**All** sets all net clearance rules to the same value.

You can set a clearance rule for each object attached to a group of fromtos. Each object type can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

**SMD-Via Same Net** sets the clearance between SMD pads and vias on the same net.

**Via-Via Same Net** sets the clearance between vias on the same net.

**Pad-to-Turn Gap** sets the clearance between a pad (through-pin) and the first turn.

**Antipad Gap** sets the clearance between antipads.

**SMD-to-Turn Gap** sets the clearance between a SMD pad and the first turn.

## Rules - Group - Wiring

### Sets wiring rules for a group of fromtos

Before you assign rules to a group of [fromtos](#), you must define the group by using the [Define - Group](#) command.

You assign rules to a group of fromtos and control how they are routed by using the Group Wiring Rules dialog box, which contains the following:

**Pick Group** displays the [Pick Active Group for Rules](#) dialog box in which you choose groups to assign wiring rules.

**Vias** controls the placement of vias under SMD pads. The options are

[Via at SMD](#)

[Via at SMD Grid](#)

[Via at SMD Fit](#)

[Limit Cross](#) sets limits on crossing conflicts.

[Limit Vias](#) sets limits on vias.

[Limit Bends](#) sets limits on bends.

[Limit Way](#) sets limits on wrong way routing.

[Max Stagger](#) sets the maximum wire lengths for mixed layers.

[Use Vias](#) is used with the [Vias list](#) and [Filter](#) to determine the vias to use for routing the group.

[Max Total Vias \(per Net\)](#) sets the maximum number of vias.

[Effective Via Length](#) determines the amount added to wire length calculations by each through-via.

[Use Layers](#) is used with the [Layers list](#) and [Filter](#) to select the routing layers for the group.

## Rules - Group - Timing

### Sets timing rules for a group of fromtos

After you define a group of fromtos by using the [Define - Group](#) command, you can set the timing rules for all the fromtos in the group. You control timing by LENGTH or TIME in the Group Timing Rules dialog box, which contains the following options.

**Pick Group** displays the [Pick Active Group for Rules](#) dialog box in which you choose nets to assign timing rules.

To control the routing patterns for wires, use

[Length Gap](#)

[Length Amplitude](#)

**LENGTH** specifies timing rules in the current measurement units, usually inches or mils. The LENGTH options are

[Min Length](#)

[Max Length](#)

[Min Total Length](#)

[Max Total Length](#)

[Specify as Ratios](#)

[Match Fromto](#)

[Length Tolerance](#)

**TIME** specifies timing rules in time units, usually picoseconds or nanoseconds. You must set the Time/Length Factor for timing rules to apply. All delay rules must use the same time units. The TIME options are

[Time/Length Factor](#)

[Min Delay](#)

[Max Delay](#)

[Min Total Delay](#)

[Max Total Delay](#)

[Match Fromto](#)

[Delay Tolerance](#)

### Notes

You cannot set both length and delay rules for the same group of fromtos. If you try to set both rules, only the last one specified is used.

Timing rules are followed only when the [FST](#) option is installed.

You must set the Time/Length Factor for timing rules to apply.

## Rules - Group - Shielding

**Turns shielding on and off, chooses the power net that attaches to the shield, and sets shield width and gap rules for a group of fromtos**

Before you assign rules to a group of [fromtos](#), you must define the group by using the [Define - Group](#) command.

The Group Shielding Rules dialog box contains the following:

**Pick Group** displays the [Pick Active Group for Rules](#) dialog box in which you choose the group to shield.

**Shielding** determines whether shielding is turned on or turned off when you apply the dialog box. If the Shielding option button is checked, shielding is turned on when the dialog box is applied. Shielding is turned off (unspecified) for the group, when the dialog box is applied with the Shielding option button not checked.

The [Shield Net list](#) and the [Filter](#) are used to choose which power net attaches to the shield. You can choose only one power net to shield the group of fromtos.

**Shield Width** sets the width for the shield wire. The width value must be entered for your current measurement units. A value of -1 means that shield width is unspecified. In this case, the shield wire width defaults to the same width as the signal wire being shielded.

**Shield Gap** sets the edge-to-edge distance between the shield wire and the signal wires being shielded. A value of -1 means that the shield gap is unspecified. In this case, the gap defaults to the wire-to-wire clearance rule for the signal nets being shielded.

### Note

Shield rules are followed only when the [FST](#) option is installed.



## Rules - Group - Crosstalk

### Sets parallel segment and tandem segment rules to control crosstalk for a group of fromtos

Before you assign rules to a group of [fromtos](#), you must define the group by using the [Define - Group](#) command.

Parallel segment rules control parallel length and gap between wires on the same layer. Tandem segment rules control parallel length and gap between wires on two adjacent signal layers.

The Group Crosstalk Rules dialog box contains the following:

**Pick Group** displays the [Pick Active Group for Rules](#) dialog box in which you choose the group to assign parallel segment and tandem segment crosstalk rules.

**Turn Off** disables all parallel or tandem crosstalk rules that were set for the active group. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel wire segments. When parallel wires are separated by a distance that is less than the gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance that wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function of gap and length.

### Notes

Parallel segment and tandem segment crosstalk rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem segment crosstalk rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Crosstalk](#)

[Rules - Layer - Crosstalk](#)

[Rules - Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

[Rules - Net - Crosstalk](#)

[Rules - Selected Net - Crosstalk](#)

[Rules - Net Layer - Crosstalk](#)

[Rules - Group Layer - Crosstalk](#)

[Rules - Fromto - Crosstalk](#)

[Rules - Fromto Layer - Crosstalk](#)

[Rules - Class to Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

## Rules - Group - Noise

### Sets parallel noise and tandem noise rules to control noise coupling for a group of fromtos

Before you assign rules to a group of [fromtos](#), you must define the group by using the [Define - Group](#) command.

Parallel noise rules control parallel length and gap between wires on the same layer. Tandem noise rules control parallel length and gap between wires on adjacent layers. The Group Coupled Noise Rules dialog box contains the following:

**Pick Group** displays the [Pick Active Group for Rules](#) dialog box in which you choose the group to assign parallel and tandem noise rules.

**Turn Off** disables all parallel or tandem noise rules that were set for the active group. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the longest distance wires can be parallel, before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the noise transmitted per unit of wire length and is expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value is considered per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting fromto.

Multiple gap, threshold, and weight rules can be entered to approximate a noise curve that varies as a function of gap and length.

### Notes

Parallel noise and tandem noise rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem noise rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Noise](#)

[Rules - Layer - Noise](#)

[Rules - Class - Noise](#)

[Rules - Net - Noise](#)

[Rules - Selected Net - Noise](#)

[Rules - Net Layer - Noise](#)

[Rules - Group Layer - Noise](#)

[Rules - Fromto - Noise](#)

[Rules - Fromto Layer - Noise](#)

Rules - Class to Class - Noise

Rules - Class to Class Layer - Noise

## Rules - Group Layer

### **Sets routing rules for a group of fromtos on a specific layer**

Group layer rules override conflicting PCB, layer, class, class layer, net, net layer, and group rules. Rules at other levels, such as fromto and class-to-class, override conflicting group layer rules in the [SPECCTRA rules hierarchy](#).

The commands on the Rules - Group Layer menu are

[Clearance](#)

[Timing](#)

[Crosstalk](#)

[Noise](#)

## Rules -Group Layer -Clearance

### **Sets clearance and width rules for a group of fromtos on a specific layer**

The Group Layer Clearance Rules dialog box contains the following:

**Pick Group** displays the [Pick Active Group for Rules](#) dialog box in which you choose the group to assign width and clearance rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Wire Width** sets the width of wires for the group of fromtos.

**All** sets all object-to-object clearance rules for the group of fromtos to the same value.

You can set a clearance rule for each object attached to the [fromtos](#) in the group. Each type of object can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The basic object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

**SMD-Via Same Net** sets the clearance rule between SMD pads and vias on the same net.

**Via-Via Same Net** sets the clearance rule between vias on the same net.

**Pad-to-Turn Gap** sets the clearance rule between a pad (through-pin) and the first turn.

**SMD-to-Turn Gap** sets the clearance rule between a SMD pad and the first turn.

## Rules - Group Layer - Timing

### Sets timing rules for a group of fromtos on a specific layer

The Group Layer Timing Rules dialog box contains the following:

**Pick Group** displays the [Pick Active Group for Rules](#) dialog box in which you choose the group to assign timing rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

[Length Gap](#) determines the edge-to-edge distance maintained between adjacent segments when the autorouter uses an accordion, trombone, or serpentine pattern.

[Length Amplitude](#) determines the maximum height of an accordion routing pattern.

[Time/Length Factor](#) sets a time conversion factor for wire lengths.

### Note

Timing rules are followed only when the [FST](#) option is installed.

## Rules - Group Layer - Crosstalk

### Sets crosstalk rules for a group of fromtos on a specific layer

Parallel and tandem segment rules control the distances wires can be routed in parallel with a given gap. Parallel segment rules apply between wires routed on the specified layer. Tandem segment rules apply between wires routed on the specified layer and two adjacent signal layers.

Group layer rules apply to a group of fromtos on a specific layer. The Group Layer Crosstalk Rules dialog box contains the following:

**Pick Group** displays the [Pick Active Group for Rules](#) dialog box in which you choose the group to assign crosstalk rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Turn Off** disables all parallel or tandem crosstalk rules that were set for the group on the specified layer. When you click Turn Off, parallel or tandem rules for the layer are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel or tandem wire segments. When parallel wires are separated by a distance that is less than the Gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function of gap and length.

### Notes

Parallel and tandem segment crosstalk rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem segment crosstalk rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Crosstalk](#)

[Rules - Layer - Crosstalk](#)

[Rules - Class - Crosstalk](#)

[Rules - Class Layer - Crosstalk](#)

[Rules - Net - Crosstalk](#)

[Rules - Selected Net - Crosstalk](#)

[Rules - Net Layer - Crosstalk](#)

[Rules - Group - Crosstalk](#)

[Rules - Fromto - Crosstalk](#)

[Rules - Fromto Layer - Crosstalk](#)

[Rules - Class to Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

## Rules - Group Layer - Noise

**Sets parallel noise and tandem noise rules to control noise coupling on a specific layer between the fromtos in a group and between the fromtos in a group and all other nets**

Parallel noise and tandem noise rules control routing by calculating noise coupling between parallel and tandem wires. Parallel noise rules apply to wires routed on the same layer. Tandem noise rules apply to wires routed on adjacent layers.

The Group Layer Noise Rules dialog box contains the following:

**Pick Group** displays the [Pick Active Group for Rules](#) dialog box in which you choose the group to assign parallel and tandem noise rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Turn Off** disables all parallel or tandem noise rules that were set for the active group. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the longest distance that wires can be parallel, before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the noise transmitted per unit of wire length and is expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value applies per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise curve that varies as a function of gap and length.

### Note

Parallel noise and tandem noise rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem noise rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Noise](#)

[Rules - Layer - Noise](#)

[Rules - Class - Noise](#)

[Rules - Class Layer - Noise](#)

[Rules - Net - Noise](#)

[Rules - Selected Net - Noise](#)

[Rules - Net Layer - Noise](#)

[Rules - Group - Noise](#)



Rules - Fromto - Noise

Rules - Fromto Layer - Noise

Rules - Class to Class - Noise

Rules - Class to Class Layer - Noise

## Rules - Fromto

### Sets routing rules for fromtos

A fromto is a pin-to-pin connection on a net. You can set rules for individual fromtos.

Fromto rules override conflicting PCB, layer, class, class layer, net, net layer, group, and group layer rules. Rules at other levels, such as fromto layer, class-to-class, and class-to-class layer, override conflicting fromto rules in the [SPECCTRA rules hierarchy](#).

The commands on the Rules - Fromto menu are

[Clearance](#)

[Wiring](#)

[Timing](#)

[Shielding](#)

[Crosstalk](#)

[Noise](#)

## Rules - Fromto - Clearance

### Sets routing clearance and width rules for fromtos

The Fromto Clearance Rules dialog box contains the following:

**Pick Net** displays the [Pick Active Net for Rules](#) dialog box in which you choose the net that contains the [fromto](#).

**Pick Fromto** displays the [Pick Active Fromto for Rules](#) dialog box in which you choose the fromto to assign width and clearance rules.

**Wire Width** sets the wire width rule.

**All** sets all fromto clearance rules to the same value.

You can set a clearance rule for each object attached to a fromto. Each type of object can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

**SMD-Via Same Net** sets the clearance between SMD pads and vias on the same net.

**Via-Via Same Net** sets the clearance between vias on the same net.

**Pad-to-Turn Gap** sets the clearance between a pad (through-pin) and the first turn.

**Antipad Gap** sets the clearance between antipads.

**SMD-to-Turn Gap** sets the clearance between a SMD pad and the first turn.

## Rules - Fromto - Wiring

### Sets wiring rules for fromtos

You assign rules to individual [fromtos](#) and control how they are routed by using the Fromto Wiring Rules dialog box. You can assign different wiring rule values to each fromto. The Fromto Wiring Rules dialog box contains the following:

**Pick Net** displays the [Pick Active Net for Rules](#) dialog box in which you choose the net that contains the [fromto](#).

**Pick Fromto** displays the [Pick Active Fromto for Rules](#) dialog box in which you choose the fromto to assign wiring rules.

**Junctions** controls the occurrence of tjunctions for starburst nets. The options are

[T-Junctions](#)

[Junction Type](#)

**Vias** controls the placement of vias under SMD pads. The options are

[Via at SMD](#)

[Via at SMD Grid](#)

[Via at SMD Fit](#)

[Fromto Priority](#) determines when a fromto is scheduled for routing with respect to other fromtos.

[Limit Cross](#) sets limits on crossing conflicts.

[Limit Vias](#) sets limits on vias.

[Limit Bends](#) sets limits on bends.

[Limit Way](#) sets limits on wrong way routing.

[Max Stagger](#) sets the maximum wire lengths for mixed layers.

[Stub Length](#) sets the stub lengths for daisy-chain nets.

[Use Vias](#) is used with the [Vias list](#) and [Filter](#) to determine the vias to use for routing the class.

[Max Total Vias \(per Net\)](#) sets the maximum number of vias.

[Effective Via Length](#) determines the amount added to wire length calculations by each through-via.

[Use Layers](#) is used with the [Layers list](#) and [Filter](#) to select the routing layer for the fromtos.

## Rules - Fromto - Timing

### Sets timing rules for fromtos

You can control the timing of individual [fromtos](#) by LENGTH or TIME. The Fromto Timing Rules dialog box contains the following options.

**Pick Net** displays the [Pick Active Net for Rules](#) dialog box in which you choose the net that contains the [fromto](#).

**Pick Fromto** displays the [Pick Active Fromto for Rules](#) dialog box in which you choose the fromto to assign timing rules.

To control the routing patterns for wires, use

[Length Gap](#)

[Length Amplitude](#)

**LENGTH** specifies timing rules in the current measurement units, usually inches or mils. The LENGTH options are

[Min Length](#)

[Max Length](#)

[Specify as Ratios](#)

[Match Fromto](#)

[Length Tolerance](#)

**TIME** specifies timing rules in time units, usually picoseconds or nanoseconds. You must set the Time/Length Factor for timing rules to apply. All delay rules must use the same time units. The TIME options are

[Time/Length Factor](#)

[Min Delay](#)

[Max Delay](#)

[Match Fromto](#)

[Delay Tolerance](#)

### Notes

You cannot set both length and delay rules for the same class of nets. If you try to set both rules, only the last one specified is used.

Timing rules are followed only when the [FST](#) option is installed.

You must set the Time/Length Factor for timing rules to apply. All delay rules must use the same time units.

## Rules - Fromto - Shielding

**Sets shielding rules between fromtos**

**Turns shielding on and off, chooses the power net that will serve as the shield, and sets shield width and gap rules for fromtos**

The Fromto Shielding Rules dialog box contains the following

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose the net that contains the [fromto](#) to be shielded.

**Pick Fromto** displays the [Pick Active Fromto for Rules](#) dialog box in which you choose the [fromto](#) to be shielded.

**Shielding** determines whether shielding is turned on or turned off when you apply the dialog box. If the Shielding option button is checked, shielding is turned on when the dialog box is applied. Shielding is turned off (unspecified), when the dialog box is applied and the Shielding option button is not checked.

The [Shield Net list](#) and the [Filter](#) are used to choose which power net attaches to the shield. You can choose only one power net.

**Shield Width** sets the width for the shield wire. The width value must be entered for your current measurement units. A value of -1 means that shield width is unspecified. In this case, the shield wire width defaults to the same width as the signal wire being shielded.

**Shield Gap** sets the edge-to-edge distance between the shield wire and the signal wires being shielded. A value of -1 means that the shield gap is unspecified. In this case, the gap defaults to the wire-to-wire clearance rule for the signal nets being shielded.

### Notes

Shield rules are followed only when the [FST](#) option is installed.

You can set shield rules at other [precedence levels](#) by using the following commands:

[Rules - Class - Shielding](#)

[Rules - Net - Shielding](#)

[Rules - Selected Net - Shielding](#)

[Rules - Group - Shielding](#)

## Rules - Fromto - Crosstalk

### Sets crosstalk rules for fromtos

Parallel and tandem segment rules control the distances wires can be routed in parallel with a given gap. Parallel segment rules apply between wires routed on the same layer. Tandem segment rules at the fromto level apply between the specified [fromto](#) and wires routed on two adjacent signal layers.

The Fromto Crosstalk Rules dialog box contains the following

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose the net that contains the [fromto](#).

**Pick Fromto** displays the [Pick Active Fromto for Rules](#) dialog box in which you choose the fromto to assign parallel and tandem segment crosstalk rules.

**Turn Off** disables all parallel or tandem crosstalk rules that were set for the active net. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel wire segments. When parallel wires are separated by a distance that is less than the gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance that wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function gap and length.

### Notes

Parallel segment and tandem segment crosstalk rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem segment crosstalk rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Crosstalk](#)

[Rules - Layer - Crosstalk](#)

[Rules - Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

[Rules - Selected Net - Crosstalk](#)

[Rules - Net - Crosstalk](#)

[Rules - Net Layer - Crosstalk](#)

[Rules - Group - Crosstalk](#)

[Rules - Group Layer - Crosstalk](#)

[Rules - Fromto Layer - Crosstalk](#)

[Rules - Class to Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

## Rules - Fromto - Noise

### Sets parallel noise and tandem noise rules to control noise coupling for fromtos

Parallel noise rules control parallel length and gap between wires on the same layer. Tandem noise rules control parallel length and gap between wires on adjacent layers.

The Fromto Noise Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose the net that contains the [fromto](#).

**Pick Fromto** displays the [Pick Active Fromto for Rules](#) dialog box in which you choose the fromto to assign parallel and tandem noise rules.

**Max Noise** sets the maximum noise that can be coupled onto a net before wires involved in the calculations are rerouted to reduce the noise calculation below the maximum value. A Max Noise value of -1 resets the maximum noise rule for the net to unspecified.

**Turn Off** disables all parallel or tandem noise rules that were set for the active net. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the minimum distance that wires can be parallel or tandem before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the noise transmitted per unit of wire length and is expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value applies per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise coupling curve that varies as a function gap and length.

### Note

Parallel and tandem noise rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem noise rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Noise](#)

[Rules - Layer - Noise](#)

[Rules - Class - Noise](#)

[Rules - Class Layer - Noise](#)

[Rules - Net - Noise](#)

[Rules - Selected Net - Noise](#)



Rules - Net Layer - Noise

Rules - Group - Noise

Rules - Group Layer - Noise

Rules - Fromto Layer - Noise

Rules - Class to Class - Noise

Rules - Class to Class Layer - Noise

## Rules - Fromto Layer

### **Sets routing rules for fromtos on a specific layer**

Fromto layer rules override conflicting PCB, layer, class, class layer, net, net layer, group, group layer, and fromto rules. Rules at other levels, such as class-to-class, class-to-class layer, and padstack, override conflicting fromto layer rules in the [SPECCTRA rules hierarchy](#).

The commands on the Rules - Fromto Layer menu are

[Clearance](#)

[Timing](#)

[Crosstalk](#)

[Noise](#)

## Rules - Fromto Layer - Clearance

### **Sets routing clearance and width rules for fromtos on a specific layer**

The Fromto Layer Clearance Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose the net that contains the [fromto](#).

**Pick Fromto** displays the [Pick Active Fromto for Rules](#) dialog box in which you choose the [fromto](#) to assign clearance and width rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Wire Width** sets the wire width rule.

**All** sets all clearance rules to the same value.

You can set a clearance rule for each type of object on a fromto. Each object type can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

**SMD-Via Same Net** sets the clearance between SMD pads and vias on the same net.

**Via-Via Same Net** sets the clearance between vias on the same net.

**Pad-to-Turn Gap** sets the clearance between a pad (through-pin) and the first turn.

**SMD-to-Turn Gap** sets the clearance between a SMD pad and the first turn.

## Rules - Fromto Layer - Timing

### Sets timing rules for fromtos on a specific layer

The Fromto Layer Timing Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose the net that contains the [fromto](#).

**Pick Fromto** displays the [Pick Active Fromto for Rules](#) dialog box in which you choose the fromto to assign timing rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

[Length Gap](#) determines the edge-to-edge distance maintained between adjacent segments when the autorouter uses an accordion, trombone, or serpentine pattern.

[Length Amplitude](#) determines the maximum height of an accordion routing pattern.

[Time/Length Factor](#) sets a time conversion factor for wire lengths.

### Note

Timing rules are followed only when the [FST](#) option is installed.

## Rules - Fromto Layer - Crosstalk

### Sets crosstalk rules for fromtos on a specific layer

Parallel segment rules control parallel length and gap between wires on the same layer. Tandem segment rules control parallel length and gap between wires on the selected layer and wires on two adjacent signal layers.

The Fromto Layer Clearance Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose the net that contains the [fromto](#).

**Pick Fromto** displays the [Pick Active Fromto for Rules](#) dialog box in which you choose the fromto to assign parallel and tandem segment crosstalk rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Turn Off** disables all parallel or tandem crosstalk rules that were set for the active net. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel wire segments. When parallel wires are separated by a distance that is less than the gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance that wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function gap and length.

### Notes

Parallel and tandem segment crosstalk rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem segment crosstalk rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Crosstalk](#)

[Rules - Layer - Crosstalk](#)

[Rules - Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

[Rules - Net - Crosstalk](#)

[Rules - Selected Net - Crosstalk](#)

[Rules - Group - Crosstalk](#)

[Rules - Group Layer - Crosstalk](#)

[Rules - Fromto - Crosstalk](#)

[Rules - Class to Class - Crosstalk](#)

[Rules - Class to Class Layer - Crosstalk](#)

## Rules - Fromto Layer - Noise

### Sets noise rules for fromtos on a specific layer

Parallel noise and tandem noise rules control routing by calculating noise coupling between parallel and tandem wires. Parallel noise rules apply to wires routed on the same layer. Tandem noise rules apply to wires routed on adjacent layers.

The Fromto Layer Noise Rules dialog box contains the following:

**Pick Net** displays the [Pick Net for Rules](#) dialog box in which you choose the net that contains the **fromto**.

**Pick Fromto** displays the [Pick Active Fromto for Rules](#) dialog box in which you choose the fromto to assign parallel and tandem noise rules.

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

**Turn Off** disables all parallel or tandem noise rules that were set for the active layer and fromto. When you click Turn Off, the corresponding parallel or tandem rules are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the longest distance that wires can be parallel, before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the noise transmitted per unit of wire length and is expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value applies per each mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise curve that varies as a function of gap and length.

### Notes

Parallel and tandem noise rules are followed only when the [FST](#) option is installed.

You can set parallel and tandem noise rules at other [precedence levels](#) by using the following commands:

[Rules - PCB - Noise](#)

[Rules - Layer - Noise](#)

[Rules - Class - Noise](#)

[Rules - Net - Noise](#)

[Rules - Selected Net - Noise](#)

[Rules - Group - Noise](#)

[Rules - Group Layer - Noise](#)

[Rules - Fromto - Noise](#)

Rules - Class to Class - Noise

Rules - Class to Class Layer - Noise

## Rules - Class to Class

### **Sets routing rules between classes of nets**

Class to class rules override conflicting PCB, layer, class, class layer, net, net layer, group, group layer, fromto, and fromto layer rules. Rules at other levels, such as class-to-class layer, padstack, and region, override conflicting class to class rules in the [SPECCTRA rules hierarchy](#).

The commands on the Rules - Class to Class menu are

[Clearance](#)

[Crosstalk](#)

[Noise](#)



## Rules - Class to Class - Clearance

### Sets clearance rules between classes of nets

Clearance rules apply between nets of the classes marked in one list and those marked in the other list. Class to class rules are inter-class, not intra-class, unless the same class name is marked in both Classes lists.

The Class to Class Clearance Rules dialog box contains the following:

Classes list and Filter, which you use to choose one class of nets.

Classes list and Filter, which you use to choose the other class of nets. You can choose the same class name in the second Classes list that you chose in the first classes list.

**All** sets all clearance rules to the same value.

You can set a clearance rule for each object attached to a class of nets. Each object type can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

### Note

Class to class clearance rules are followed only when the FST option is installed.

## Rules - Class to Class - Crosstalk

### Sets parallel and tandem crosstalk rules between classes of nets

Crosstalk rules apply between nets of the classes marked in one list and those marked in the other. Class to class rules are inter-class, not intra-class, unless the same class name is marked in both Classes lists.

Parallel rules control parallel length and gap between wires on the same layer. Tandem rules control parallel length and gap between wires on two adjacent signal layers.

The Class to Class Crosstalk Rules dialog box contains the following:

[Classes list](#) and [Filter](#), which you use to choose one class of nets.

[Classes list](#) and [Filter](#), which you use to choose the other class of nets. You can choose the same class name in the second Classes list that you chose in the first classes list.

**Turn Off** disables all parallel or tandem crosstalk rules that were set between the active classes. When you click Turn Off, corresponding parallel or tandem rules for the classes are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel wire segments. When parallel wires are separated by a distance that is less than the gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance that wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

### Notes

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function of gap and length.

Class to class crosstalk rules are followed only when the [FST](#) option is installed.

## Rules - Class to Class - Noise

### Sets parallel and tandem noise rules between classes of nets

Parallel noise rules control parallel length and gap between wires on the same layer. Tandem noise rules control parallel length and gap between wires on adjacent layers.

Noise rules apply between the classes marked in one list and those marked in the other. Class to class rules are inter-class, not intra-class, unless the same class name is marked in both Classes lists.

The Class to Class Noise Rules dialog box contains the following:

[Classes list](#) and [Filter](#), which you use to choose one class of nets.

[Classes list](#) and [Filter](#), which you use to choose the other class of nets. You can choose the same class name in the second Classes list that you chose in the first classes list.

**Uni-directional (A to B only)** controls whether net classes in the Classes lists are noise transmitters or noise receivers. When Uni-directional is checked, nets can be either transmitters or receivers but not both. Nets that belong to marked classes in the left list are considered noise transmitters to the net classes marked in the right list. Nets that belong to classes marked in the right list are considered noise receivers from net classes marked in the left list.

**Turn Off** disables all parallel or tandem noise rules that were set for the active class. When you click Turn Off, corresponding parallel or tandem rules for the class are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the longest distance wires can be parallel, before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the amount of noise per unit of wire length that is transmitted by the net and expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value is considered per each 1 mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise curve that varies as a function of gap and length.

### Note

Class to Class parallel and tandem noise rules are followed only when the [FST](#) option is installed.

## Rules - Class to Class Layer

### **Sets routing rules between classes on a specific layer**

In the [SPECCTRA rules hierarchy](#), class to class layer rules override conflicting rules at other levels, except padstack and region rules.

The commands on the Rules - Class to Class Layer menu are

[Clearance](#)

[Crosstalk](#)

[Noise](#)

## Rules - Class to Class Layer - Clearance

### Sets clearance rules between classes on a specific layer

Clearance rules apply between nets of the classes marked in one list and those marked in the other list. Class to class rules are inter-class, not intra-class, unless the same class name is marked in both Classes lists.

The Class to Class Layer Clearance Rules dialog box contains the following:

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

[Classes list](#) and [Filter](#), which you use to choose one class of nets.

[Classes list](#) and [Filter](#), which you use to choose the other class of nets. You can choose the same class name in the second Classes list that you chose in the first classes list.

**All** sets all clearance rules to the same value.

You can set a clearance rule for each object attached to a class of nets. Each object type can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Area**, which is a keepout region or the PCB boundary
- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Wire**, which is the shape that completes a connection

### Note

Class to class layer clearance rules are followed only when the [FST](#) option is installed.

## Rules - Class to Class Layer - Crosstalk

### Sets crosstalk rules between classes on a specific layer

Crosstalk rules apply between nets of the classes marked in one list and those marked in the other. Class to class rules are inter-class, not intra-class, unless the same class name is marked in both Classes lists.

Parallel rules control parallel length and gap between wires on the same layer. Tandem rules control parallel length and gap between wires on two adjacent signal layers.

The Class to Class Layer Crosstalk Rules dialog box contains the following:

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

[Classes list](#) and [Filter](#), which you use to choose one class of nets.

[Classes list](#) and [Filter](#), which you use to choose the other class of nets. You can choose the same class name in the second Classes list that you chose in the first classes list.

**Turn Off** disables all parallel or tandem crosstalk rules that were set between the active classes. When you click Turn Off, corresponding parallel or tandem rules for the classes are immediately turned off. You do not need to click Apply or OK.

**Gap** is the minimum edge-to-edge distance between parallel wire segments. When parallel wires are separated by a distance that is less than the gap value, and the wires are parallel for a distance that exceeds the Length value, the wires are rerouted during subsequent routing passes to correct the condition.

**Length** is the maximum distance that wire segments can be parallel before a violation occurs. When wires are parallel over a distance that exceeds the Length value, and the edge-to-edge distance between them is less than the Gap value, the wires are rerouted during subsequent routing passes to correct the condition.

Multiple length and gap rules can be entered to approximate a crosstalk curve that varies as a function of gap and length.

### Note

Class to class layer crosstalk rules are followed only when the [FST](#) option is installed.

## Rules - Class to Class Layer - Noise

### Sets noise rules between classes on a specific layer

Parallel noise rules control parallel length and gap between wires on the same layer. Tandem noise rules control parallel length and gap between wires on adjacent layers.

Noise rules apply between the classes marked in one list and those marked in the other. Class to class rules are inter-class, not intra-class, unless the same class name is marked in both Classes lists.

The Class to Class Layer Noise Rules dialog box contains the following:

**Pick Layer** displays the [Pick Active Layer for Rules](#) dialog box in which you choose the layer.

[Classes list](#) and [Filter](#), which you use to choose one class of nets.

[Classes list](#) and [Filter](#), which you use to choose the other class of nets. You can choose the same class name in the second Classes list that you chose in the first classes list.

**Uni-directional (A to B only)** controls whether net classes in the Classes lists are noise transmitters or noise receivers. When Uni-directional is checked, nets can be either transmitters or receivers but not both. Nets that belong to marked classes in the left list are considered noise transmitters to the net classes marked in the right list. Nets that belong to classes marked in the right list are considered noise receivers from net classes marked in the left list.

**Turn Off** disables all parallel or tandem noise rules that were set for the active layer. When you click Turn Off, corresponding parallel or tandem noise rules for the layer are immediately turned off. You do not need to click Apply or OK.

**Gap** is the edge-to-edge distance between parallel wires, below which noise coupling calculations are performed. When the edge-to-edge distance between parallel wires is less than the Gap value, and the wires are parallel for a distance that exceeds the Threshold value, noise coupling calculations are performed.

**Threshold** is the longest distance wires can be parallel, before they are included in noise coupling calculations. When wires are parallel over a distance that exceeds the Threshold value, and the edge-to-edge distance between them is less than the Gap value, the wires are included in noise coupling calculations.

**Weight** is the amount of noise per unit of wire length that is transmitted by the net and expressed in electrical units such as millivolts. The unit of wire length is the measurement unit in effect at the time you apply the rule. For example, if your measurement unit is mils, the weight value is considered per each 1 mil of length. Noise coupling calculations are made by multiplying parallel and tandem lengths by the weight value of the transmitting net.

Multiple gap, threshold, and weight rules can be entered to approximate a noise curve that varies as a function of gap and length.

### Note

Parallel and tandem noise rules are followed only when the [FST](#) option is installed.

## Rules - Padstack

### **Sets routing rules for padstacks**

In the [SPECCTRA rules hierarchy](#), the padstack clearance rule overrides conflicting clearance rules at other levels, except a region clearance rule.

The command on the Rules - Padstack menu is

[Clearance](#)



## Rules - Padstack - Clearance

### Sets clearance rules for padstacks

The Padstack Clearance Rules dialog box contains the following:

**Pick Padstack** displays the [Pick Active Padstack for Rules](#) dialog box in which you choose the padstack you want to assign clearance rules.

**All** sets all padstack clearance rules to the same value.

You can set a clearance rule for each object type attached to a padstack. Each object type can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Pin**, which is a through-pin
- **SMD**, which is an SMD pad
- **Via**, which is a blind, buried, or through-via
- **Area**, which is a keepout region or the PCB boundary
- **Wire**, which is the shape that completes a connection

### Notes

Padstack clearance rules are followed only when the [FST](#) option is installed.

Padstack rules are used to set the drill clearance. For via padstacks, setting the via to via clearance rule for a padstack enables certain vias to have a larger clearance.

If more than one via to via clearance rule is applied, the largest clearance is followed.

## Rules - Region

### **Sets rules to a rectangular area of the PCB**

In the [SPECCTRA rules hierarchy](#), a region clearance rule overrides all other clearance rules.

The command on the Rules - Region menu is

[Clearance](#)

### **Note**

Region rules are followed only when the [FST](#) option is installed.

## Rules - Region - Clearance

### Sets clearance and width rules to a rectangular area of the PCB

You can assign region rules to all layers of the PCB or to individual layers, depending how you defined the region when you used [Define - Region](#). Region rules have the highest precedence in the rule hierarchy and, therefore, override all other clearance rules.

The Region Clearance Rules dialog box contains the following:

**Pick Region** displays the [Pick Active Region for Rules](#) dialog box in which you choose the region you want to assign clearance rules.

**All** sets all object-to-object clearance rules to the same value.

Each object type can have a separate rule with respect to each of the other object types. For example, you can set separate via-to-wire, via-to-pin, and via-to-via rules. The object types are

- **Area** is a keepout region or the PCB boundary.
- **Pin** is a through-pin.
- **SMD** is an SMD pad.
- **Via** is a blind, buried, or through-via.
- **Wire** is the shape that completes a connection.

#### Note

Region rules are followed only when the [FST](#) option is installed.

## Rules - Costs

### **Sets cost and tax values that determine how connections are autorouted**

Cost and tax settings determine routing behavior. The autorouter maintains an internal set of costs, which change over the course of an autorouting session. The internal costs are proprietary and not published. The types of cost or tax values you can set are

**Wrong-way routing** controls the cost of routing horizontally on a vertical layer or vertically on a horizontal layer.

**Crossings** controls the cost of crossing conflicts.

**Vias** controls the cost to use vias.

**Off-grid routing** controls the cost to route off-grid (when a wire grid is defined).

**Off-center SMD exit** controls the cost to exit an SMD pad off-center.

**Long-side SMD exit** controls the cost to exit the side of SMD pads.

**Via-wire-squeeze** controls the cost to route with wire to via conflicts.

The range of cost values you can use is from 0 to 100. A cost value of 100 usually prohibits the associated routing behavior. A value of 0 usually removes any penalty from the corresponding routing behavior.

When a cost value in the Costs dialog box is -1, the autorouter's internal value is used. If you set a cost to some value other than -1, that cost overrides the internal value and remains in effect until you change it again or reset it by reentering -1.

The Costs dialog box is for expert users. You can rely on the autorouter's internal cost management for most designs. If you need to influence routing behavior by adjusting costs, try applying a tax factor instead of a cost to influence routing behavior. Tax is a multiplier or factor that applies to the autorouter's internal cost parameters.

## Rules - Sorting

**Determines how all connections are scheduled for routing**

The Sorting dialog box contains the following:

**Smart** schedules connections based on congestion. Smart sort is the default method for scheduling connections.

**Random** schedules connections randomly, without regard to length or other individual characteristics.

**By Manhattan length - Shortest first** schedules shorter connections before longer connections.

**By Manhattan length - Longest first** schedules longer connections before shorter connections.

**By Manhattan area - Smallest first** schedules connections according to the area bounded by their Manhattan lengths. Smaller Manhattan areas are scheduled before larger Manhattan areas.

**By Manhattan area - Largest first** schedules connections according to the area bounded by their Manhattan lengths. Larger Manhattan areas are scheduled before smaller Manhattan areas.

## Rules - Check Rules

### Checks the design for any current rule conflicts or violations

You can check for routing conflicts and rule violations, or you can check for both routing and placement conflicts and rule violations. The Check Rule menu commands are

**All** checks both routing rule conflicts and placement rule violations.

**Routing** checks only routing conflicts and rule violations. When you check routing rules, the current wiring is examined against current rules.

- Crossing conflicts are marked graphically with a diamond shape.
- Clearance conflicts are marked graphically with a bounding rectangle.
- Length rule violations are marked graphically with a yellow dashed line.
- Crosstalk violations are marked graphically with a white rectangle.

A common use of Check Rules is to determine the effects of a rule change on the current placement or the finished routing. You do this by applying the rule changes you want to check and clicking **Rules - Check Rules - Routing**. Examine the conflicts or violations created by the rules change and determine whether to keep the rule changes or reset them to their previous values.

When you start a rules check for all rules, the current component positions and orientations are examined against current placement rules. Components that violate current rules are indicated by a thick-lined bounding box with diamond-shaped markers at each corner of the component's bounding box.

## Rules - PCB

### **Sets placement rules at the PCB level**

The commands on the Rules - PCB menu are

[Spacing](#)

[Permitted Orientations](#)

[Permitted Sides](#)

[Placement Grids](#)

[Opposite Sides](#)

## Rules - PCB - Spacing

### Sets component spacing rules at the PCB level

PCB is the lowest precedence rule level. Rules at other levels such as image set, image, component, or room override conflicting PCB rules.

You can set the same spacing rule for all objects, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All object-to-object spacing rules can be set with the PCB Spacing Rules dialog box. The dialog box contains two matrixes of data entry boxes, one for the front side of the PCB and the other for the back side of the PCB. Each data entry box represents one object-to-object spacing rule.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

A value of -1 means a rule is unspecified. A positive value in the All data entry box overrides a value of -1 in any of the matrix data entry boxes. A positive value in any of the matrix data entry boxes overrides a positive value in the All data entry box.

### Note

Spacing rules set in the PCB Spacing Rules dialog box override the global PCB Spacing Rule in the Setup dialog box.



## Rules - PCB - Permitted Orientations

### Sets component orientation rules at the PCB rule level

PCB is the lowest precedence rule level. Rules at other levels such as image set, image, component, or room override conflicting PCB rules.

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees, or as horizontal or vertical. You can also permit different orientations for the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

If the largest horizontal and vertical arrays have the same number of pins, an image's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the image's orientation is unspecified.

The orientation options are

**No rule**, which means the rule is unspecified.

**Horizontal**, which means components can be aligned with the X axis.

**Vertical**, which means components can be aligned with the Y axis.

**Specified by Degree**, which means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees. If you click Specified by Degree, all four rotation angles (0, 90, 180, and 270) are permitted by default. Remove the check from the check box of any angle you do not want to permit.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Note

Components with square footprints (same number of pins on all four sides) can be rotated to any permitted orientation if you specify a horizontal or vertical rule. If you specify the permitted orientation rules by degrees, SPECCTRA follows the rules exactly for square components.

## Rules - PCB - Permitted Sides

### Sets permitted side rules at the PCB rule level

PCB is the lowest precedence rule level. Rules at other levels such as image set, image, component, or room override conflicting PCB rules.

Permitted side rules determine the sides of the PCB on which components can be placed. Use the PCB Permitted Side Rules dialog box to assign permitted side rules for all components. The permitted side options are

**Both** means components can be placed on either side of the PCB.

**Front** means components can be placed only on the front side of the PCB.

**Back** means components can be placed only on the back side of the PCB.

### Notes

If you do not set permitted side rules, placement is permitted on both sides of the PCB by default.

PCB permitted side rules apply to all component packages. If you want to apply separate permitted side rules for SMD and through-pin components, use the image set permitted side rules.

## Rules - PCB - Placement Grids

### **Defines grids for SMD and through-pin components**

SPECCTRA does not require you to define a placement grid for automatic placement. You can define a placement grid if it is required by your design or manufacturing rules.

The Placement Grids dialog box allows you to define a single grid for all components or separate SMD and through-pin (PTH) grids. The default placement grid is 0, which means no grid is defined. The PTH grid spacing value must be a multiple of the SMD grid spacing value; otherwise, SPECCTRA resets the PTH grid to 0.

**All** specifies the grid spacing for both SMD and through-pin placement grids

**SMD** specifies the grid spacing for the SMD placement grid

**PTH** specifies the grid spacing for the through-pin placement grid

### **Notes**

The placement grids you define by using **Rules - PCB - Placement Grids** override the placement grid defined in the [Setup](#) dialog box.

## Rules - PCB - Opposite Sides

### Sets opposite side rules at the PCB rule level

PCB is the lowest precedence rule level. Rules at other levels such as image set, image, component, or room override conflicting PCB rules.

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side.

By default, all opposite side placement is permitted. Use the PCB Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed on the opposite side of other large components.

**Large\_Small** permits large components to be placed on the opposite side of small components and small components to be placed on the opposite side of large components.

**Small\_Small** permits small components to be placed on the opposite side of other small components.

### Notes

PCB opposite side rules apply to all component packages. If you want to apply separate opposite side rules for SMD and through-pin components, use the image set permitted side rules.

## Rules - Image Set

### **Sets placement rules for image property types**

The image property types are large, small, capacitor, and discrete. You can apply different rules for each type. The commands on the Rules - Image Set menu are

[Large](#)

[Small](#)

[Capacitor](#)

[Discrete](#)

## Rules - Image Set - Large

### **Sets placement rules for large images**

The commands on the Rules - Image Set - Large menu are

[Spacing](#)

[Permitted Orientations](#)

[Permitted Sides](#)

[Opposite Sides](#)

## Rules - Image Set - Large - Spacing

### Sets spacing rules for large images

SPECCTRA uses the number of component pins to differentiate large and small images. Large images have more than three pins.

You can set the same spacing rule for all large images, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- PTH is a through-pin component package
- SMD is a surface-mounted device package
- Area is a keepout region, a placement keepout, or the PCB boundary

All large image object-to-object spacing rules can be set with the Image Set Large Spacing Rules dialog box. The dialog box contains two tables of data entry boxes, one for SMD spacing and the other for PTH spacing. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Note

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image Set - Large - Permitted Orientations

### Sets component orientation rules for large images

SPECCTRA uses the number of component pins to differentiate large and small images. Large images have more than three pins.

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees, or as horizontal or vertical. You can also permit different orientations for SMD and through-pin components, or on the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

If the largest horizontal and vertical arrays have the same number of pins, an image's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the image's orientation is unspecified.

The orientation options are

**No rule** means the rule is unspecified.

**Horizontal** means components can be aligned with the X axis.

**Vertical** means components can be aligned with the Y axis.

**Specified by Degree** means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

Components with square footprints (same number of pins on all four sides) can be rotated to any permitted orientation if you specify a horizontal or vertical rule. If you specify the permitted orientation rules by degrees, SPECCTRA follows the rules exactly for square components.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.



## Rules - Image Set - Large - Permitted Sides

### Sets permitted side rules for large images

SPECCTRA uses the number of component pins to differentiate large and small images. Large images have more than three pins.

Permitted side rules determine the sides of the PCB on which components can be placed. Use the Image Set Large Permitted Side Rules dialog box to assign permitted side rules for all large components. You can permit different sides for SMD and through-pin component packages. The permitted side options are

**Both** means the image instances can be placed on either side of the PCB.

**Front** means the image instances can be placed only on the front side of the PCB.

**Back** means the image instances can be placed only on the back side of the PCB.

### Notes

If you do not set permitted side rules for an image set large, placement is permitted on both sides of the PCB by default.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image Set - Large - Opposite Sides

### Sets opposite side rules for large images

SPECCTRA uses the number of component pins to differentiate large and small images. Large images have more than three pins.

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side. You can set the same opposite side rule for all component packages, or you can set separate rules for SMD and PTH components.

By default, all opposite side placement is permitted. Use the Image Set Large Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed on the opposite side of other large components.

**Large\_Small** permits large components to be placed on the opposite side of small components and small components to be placed on the opposite side of large components.

**Small\_Small** permits small components to be placed on the opposite side of other small components.

Small\_Small is ignored when opposite side rules are set for large images.

### Notes

If you do not set opposite side rules for an image set large, all opposite side placements of those components are permitted by default.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image Set - Small

### **Sets placement rules for small images**

The commands on the Rules - Image Set - Small menu are

[Spacing](#)

[Permitted Orientations](#)

[Permitted Sides](#)

[Opposite Sides](#)

## Rules - Image Set - Small - Spacing

### Sets spacing rules for all small images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less.

You can set the same spacing rule for all small image instances, or you can set separate rules for each small image type with respect to each of the other small image types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All small image object-to-object spacing rules can be set with the Image Set Small Spacing Rules dialog box. The dialog box contains two tables of data entry boxes, one for SMD spacing and the other for PTH spacing. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Note

Small image set spacing rules apply to all small images, including those assigned the capacitor or discrete property. However, capacitor and discrete image spacing rules override conflicting small image set rules.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image Set - Small - Permitted Orientations

### Sets component orientation rules for small images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less.

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees, or as horizontal or vertical. You can also permit different orientations for SMD and through-pin components, or on the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

If the largest horizontal and vertical arrays have the same number of pins, an image's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the image's orientation is unspecified.

The orientation options are

**No rule** means the rule is unspecified.

**Horizontal** means components can be aligned with the X axis.

**Vertical** means components can be aligned with the Y axis.

**Specified by Degree** means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

Small image set permitted orientation rules apply to all small images, including those assigned the capacitor or discrete property. However, capacitor and discrete image rules override conflicting small image set rules.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image Set - Small - Permitted Sides

### Sets permitted side rules for small images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less.

Permitted side rules determine the sides of the PCB on which components can be placed. Use the Image Set Small Permitted Side Rules dialog box to assign permitted side rules for all small components. You can permit different sides for SMD and through-pin component packages. The permitted side options are

**Both** means the image instances can be placed on either side of the PCB.

**Front** means the image instances can be placed only on the front side of the PCB.

**Back** means the image instances can be placed only on the back side of the PCB.

### Notes

If you do not set permitted side rules for an image set small, placement is permitted on both sides of the PCB by default.

Small image set permitted side rules apply to all small components, including those assigned the capacitor or discrete property. However, capacitor and discrete image rules override conflicting small image set rules.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image Set - Small - Opposite Sides

### Sets opposite side rules for small images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less.

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side. You can set the same opposite side rule for all component packages, or you can set separate rules for SMD and PTH components

By default, all opposite side placement is permitted. Use the Image Set Small Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed on the opposite side of other large components.

**Large\_Small** permits large components to be placed on the opposite side of small components and small components to be placed on the opposite side of large components.

**Small\_Small** permits small components to be placed on the opposite side of other small components.

Large\_Large is ignored when opposite side rules are set for small images.

### Notes

If you do not set opposite side rules for an image set small, opposite side placement of those components is permitted by default.

Small image set opposite side rules apply to all small images, including those assigned the capacitor or discrete property. However, capacitor and discrete image set rules override conflicting small image set rules.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image Set - Capacitor

### **Sets placement rules for capacitor images**

The commands on the Rules - Image Set - Capacitor menu are

[Spacing](#)

[Permitted Orientations](#)

[Permitted Sides](#)

[Opposite Sides](#)



## Rules - Image Set - Capacitor - Spacing

### Sets spacing rules for all capacitor images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Capacitor images are small images assigned the capacitor property either in the design file or in SPECCTRA.

You can set the same spacing rule for all capacitor image instances, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All capacitor image object-to-object spacing rules can be set with the Image Set Capacitor Spacing Rules dialog box. The dialog box contains two tables of data entry boxes, one for SMD spacing and the other for PTH spacing. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Notes

Image set spacing rules take precedence over PCB spacing rules. Rules at other levels such as image, component, or room override conflicting image set rules.

SPECCTRA treats small components with pins connected only to power nets as decoupling capacitors. If these components are not assigned the capacitor property in the design file, SPECCTRA assigns it automatically. You can override the automatic assignment and assign the small or discrete property. Small image set rules apply to capacitor images when capacitor image set rules are not specified.

## Rules - Image Set - Capacitor - Permitted Orientations

### Sets component orientation rules for capacitor images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Capacitor images are small images assigned the capacitor property either in the design file or in SPECCTRA.

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees, or as horizontal or vertical. You can also permit different orientations for SMD and through-pin components, or on the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

The orientation options are

**No rule** means the rule is unspecified.

**Horizontal** means components can be aligned with the X axis.

**Vertical** means components can be aligned with the Y axis.

**Specified by Degree** means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

SPECCTRA treats small components with pins connected only to power nets as decoupling capacitors. If these components are not assigned the capacitor property in the design file, SPECCTRA assigns it automatically. You can override the automatic assignment and assign the small or discrete property. Small image set rules apply to capacitor images when capacitor image set rules are not specified.

## Rules - Image Set - Capacitor - Permitted Sides

### Sets permitted side rules for capacitor images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Capacitor images are small images assigned the capacitor property either in the design file or in SPECCTRA.

Permitted side rules determine the sides of the PCB on which components can be placed. Use the Image Set Capacitor Permitted Side Rules dialog box to assign permitted side rules for all capacitors. You can permit different sides for SMD and through-pin component packages. The permitted side options are

**Both** means the image instances can be placed on either side of the PCB.

**Front** means the image instances can be placed only on the front side of the PCB.

**Back** means the image instances can be placed only on the back side of the PCB.

### Notes

If you do not set permitted side rules for an image set capacitor, placement is permitted on both sides of the PCB by default.

SPECCTRA treats small components with pins connected only to power nets as decoupling capacitors. If these components are not assigned the capacitor property in the design file, SPECCTRA assigns it automatically. You can override the automatic assignment and assign the small or discrete property. Small image set rules apply to capacitor images when capacitor image set rules are not specified.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image Set - Capacitor - Opposite Sides

### Sets opposite side rules for capacitor images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Capacitor images are small images assigned the capacitor property either in the design file or in SPECCTRA.

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side. You can set the same opposite side rule for all component packages, or you can set separate rules for SMD and PTH components

By default, all opposite side placement is permitted. Use the Image Set Capacitor Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed on the opposite side of other large components.

**Large\_Small** permits large components to be placed on the opposite side of small components and small components to be placed on the opposite side of large components.

**Small\_Small** permits small components to be placed on the opposite side of other small components.

Large\_Large is ignored when opposite side rules are set for capacitors.

### Notes

If you do not set opposite side rules for an image set capacitor, opposite side placement of those components is permitted by default.

SPECCTRA treats small components with pins connected only to power nets as decoupling capacitors. If these components are not assigned the capacitor property in the design file, SPECCTRA assigns it automatically. You can override the automatic assignment and assign the small or discrete property. Small image set rules apply to capacitor images when capacitor image set rules are not specified.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, and room override conflicting image set rules.

## Rules - Image Set - Discrete

### Sets placement rules for discrete images

The commands on the Rules - Image Set - Discrete menu are

Spacing

Permitted Orientations

Permitted Sides

Opposite Sides

## Rules - Image Set - Discrete - Spacing

### Sets spacing rules for all discrete images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Discrete images are small images assigned the discrete property either in the design file or in SPECCTRA.

You can set the same spacing rule for all discrete image instances, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All discrete image object-to-object spacing rules can be set with the Image Set Discrete Spacing Rules dialog box. The dialog box contains two tables of data entry boxes, one for SMD spacing and the other for PTH spacing. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Note

The discrete property is used to differentiate certain small images that are not decoupling capacitors but that you want to place separately from other small components. Small image set rules apply to discrete images if the discrete image set rules are unspecified.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image Set - Discrete - Permitted Orientations

### Sets component orientation rules for discrete images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Discrete images are small images assigned the discrete property either in the design file or in SPECCTRA.

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees, or as horizontal or vertical. You can also permit different orientations for SMD and through-pin components, or on the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

If the largest horizontal and vertical arrays have the same number of pins, an image's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the image's orientation is unspecified.

The orientation options are

**No rule** means the rule is unspecified.

**Horizontal** means components can be aligned with the X axis.

**Vertical** means components can be aligned with the Y axis.

**Specified by Degree** means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

The discrete property is used to differentiate certain small images that are not decoupling capacitors but that you want to place separately from other small components. Small image rules apply to discrete images if the discrete image set rules are unspecified.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image Set - Discrete - Permitted Sides

### Sets permitted side rules for discrete images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Discrete images are small images assigned the discrete property either in the design file or in SPECCTRA.

Permitted side rules determine the sides of the PCB on which components can be placed. Use the Image Set Discrete Permitted Side Rules dialog box to assign permitted side rules for all discrete components. You can permit different sides for SMD and through-pin component packages. The permitted side options are

**Both** means the images can be placed on either side of the PCB.

**Front** means the images can be placed only on the front side of the PCB.

**Back** means the images can be placed only on the back side of the PCB.

### Notes

If you do not set permitted side rules for a component package, placement is permitted on both sides of the PCB by default.

The discrete property is used to differentiate certain small images that are not decoupling capacitors but that you want to place separately from other small components. Small image set rules apply to discrete images if the discrete image set rules are unspecified.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.



## Rules - Image Set - Discrete - Opposite Sides

### Sets opposite side rules for discrete images

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Discrete images are small images assigned the discrete property either in the design file or in SPECCTRA.

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side. You can set the same opposite side rule for all component packages, or you can set separate rules for SMD and PTH components

By default, all opposite side placement is permitted. Use the Image Set Discrete Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed on the opposite side of other large components.

**Large\_Small** permits large components to be placed on the opposite side of small components and small components to be placed on the opposite side of large components.

**Small\_Small** permits small components to be placed on the opposite side of other small components.

Large\_Large is ignored when opposite side rules are set for discrete images.

### Notes

If you do not set opposite side rules for a component package, all opposite placements of those components are permitted by default.

The discrete property is used to differentiate certain small images that are not decoupling capacitors but that you want to place separately from other small components. Small image set rules apply to discrete images if the discrete image set rules are unspecified.

Image set rules take precedence over PCB rules. Rules at other levels such as image, component, or room override conflicting image set rules.

## Rules - Image

### **Sets placement rules for specific images**

The commands on the Rules - Image menu are

Spacing

Permitted Orientations

Permitted Sides

Site Grid

Opposite Sides

## Rules - Image - Spacing

### Sets spacing rules for specific images

You can set a single spacing rule for an image, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All image object-to-object spacing rules can be set with the Image Spacing Rules dialog box. The dialog box contains two matrixes of data entry boxes, one for the front side of the PCB and the other for the back side of the PCB. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

Image spacing rules are assigned to the active image. The image ID of the active image is displayed at the top of the Image Spacing Rules dialog box. You can use the Pick Active Image dialog box to change the active image.

The Image Spacing Rules dialog box contains the following:

**Pick Image** opens the Pick Active Image dialog box if you want to change the active image. Enter the image ID or a wildcard in the Filter data entry box or click the image ID in the Images list. Click OK in the Pick Active Image dialog box.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Notes

Image spacing rules take precedence over image set and PCB spacing rules. Rules at other levels such as component, room, or room image set override conflicting image rules.

Image rules apply to all instances of an image unless specific instances have been assigned different component rules. If you do not assign spacing rules for an image, SPECCTRA uses default rules or rules set at a lower precedence level.

## Rules - Image - Permitted Orientations

### Sets component orientation rules for specific images

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees or as horizontal or vertical. You can also permit different orientations for the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

If the largest horizontal and vertical arrays have the same number of pins, an image's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the image's orientation is unspecified.

All permitted orientation rules can be set with the Permitted Image Orientation Rules dialog box. Image orientation rules are assigned to the active image. The image ID of the active image is displayed at the top of the Permitted Image Orientation Rules dialog box. You can use the Pick Active Image dialog box to change the active image.

The Permitted Image Orientation Rules dialog box contains the following:

**Pick Image** opens the Pick Active Image dialog box if you want to change the active image. Enter the image ID or a wildcard in the Filter data entry box. or click the image ID in the Images list. Click OK in the Pick Active Image dialog box.

The orientation options for the FRONT and BACK sides of the PCB are

**No Rule** means the rule is unspecified.

**Horizontal** means components can be aligned with the X axis.

**Vertical** means components can be aligned with the Y axis.

**Specified by Degree** means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

Components with square footprints (same number of pins on all four sides) can be rotated to any permitted orientation if you specify a horizontal or vertical rule. If you specify the permitted orientation rules by degrees, SPECCTRA follows the rules exactly for square components.

Permitted image orientation rules take precedence over image set and PCB rules. Rules at other levels such as component, room, or room image set override conflicting image rules.

Image rules apply to all instances of an image unless specific instances have been assigned higher precedence rules. If you do not assign rules for an image, SPECCTRA uses default

rules or rules set at a lower precedence level.

## Rules - Image- Permitted Sides

### Sets permitted side rules for specific images

Permitted side rules determine the sides of the PCB on which components can be placed. Use the Permitted Image Side Rules dialog box to assign permitted side rules for all instances of an image.

Image permitted side rules are assigned to the active image. The image ID of the active image is displayed at the top of the Permitted Image Side Rules dialog box. You can use the Pick Active Image dialog box to change the active image.

The Permitted Image Side Rules dialog box contains the following:

**Pick Image** opens the Pick Active Image dialog box if you want to change the active image. Enter the image ID or a wildcard in the [Filter](#) data entry box or click the image ID in the [Images list](#). Click OK in the Pick Active Image dialog box.

**Both** means the image instances can be placed on either side of the PCB.

**Front** means the image instances can be placed only on the front side of the PCB.

**Back** means the image instances can be placed only on the back side of the PCB.

### Notes

If you do not set permitted side rules, placement is permitted on both sides of the PCB by default.

Permitted image side rules take precedence over image set and PCB rules. Rules at other levels such as component, room, or room image set override conflicting image rules.

Image rules apply to all instances of an image unless specific instances have been assigned different component rules. If you do not assign rules for an image, SPECCTRA uses default rules or rules set at a lower precedence level.

## Rules - Image - Site Grid

### **Defines component-to-component grid spacing for images**

Image site grids establish a regular spacing pattern between multiple component instances of an image. When you define a site grid for an image, the image site grid supersedes the placement grid.

You can use image site grids with or without placement grids. You specify both X (horizontal) and Y (vertical) values for an image site grid. However, if you defined a placement grid, both the X and Y values must be multiples of the placement grid value. Otherwise, SPECCTRA resets the site grid to 0.

If you defined separate SMD and PTH placement grids

- A site grid for an SMD image must be a multiple of the SMD placement grid.
- A site grid for a through-pin image must be a multiple of the PTH placement grid (if one is defined) or of the SMD placement grid (if a PTH placement grid is not defined).

The current placement grid value is displayed at the top of the Image Site Grid dialog box.

The Image Site Grid dialog box also contains the following:

**X** specifies the horizontal grid spacing value.

**Y** specifies the vertical grid spacing value.

Filter and an Images list that you use to choose image IDs. An image ID is the image's library name as it appears in the library section of the SPECCTRA design file.

### **Notes**

You can define placement grids using Rules - PCB - Placement Grids. You can also define a single placement grid for all components using Autoplace - Setup.

## Rules - Image - Opposite Sides

### Sets opposite side rules for specific images

Opposite sides rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side.

By default, all opposite side placement is permitted. Use the Image Opposite Side Rules dialog box to constrain opposite side placement based on image size.

Image opposite side rules are assigned to the active image. The image ID of the active image is displayed at the top of the Image Opposite Side Rules dialog box. You can use the Pick Active Image dialog box to change the active image.

The Image Opposite Side Rules dialog box contains the following:

**Pick Image** to open the Pick Active Image dialog box if you want to change the active image. Enter the image ID or a wildcard in the [Filter](#) data entry box or click the image ID in the [Images list](#). Click OK in the Pick Active Image dialog box.

**Large\_Large** permits large components to be placed on the opposite side of other large components.

**Large\_Small** permits large components to be placed on the opposite side of small components and small components to be placed on the opposite side of large components.

**Small\_Small** permits small components to be placed on the opposite side of other small components.

Large\_Large is ignored when opposite side rules are set for a small, capacitor, or discrete image. Small\_Small is ignored when opposite side rules are set for a large image.

### Notes

Image opposite side rules take precedence over image set and PCB rules. Rules at other levels such as component, room, or room image set override conflicting image rules.

Image rules apply to all instances of an image unless specific instances have been assigned higher precedence rules. If you do not assign rules for an image, SPECCTRA uses default rules or rules set at a lower precedence level.



## Rules - Family to Family

### **Sets pad edge and body edge spacing rules between two or more families of images**

Family-to-family spacing rules override conflicting spacing rules assigned to at all image sets, images, components, or rooms, but are overridden by conflicting image-to-image spacing rules.

You can set a single family-to-family spacing rule for an image family with respect to other families, or you can set separate Pad-to-Pad, Pad-to-Body, and Body-to-Body rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- Pad Edge, which is the edge of a pin shape
- Body Edge, which is the edge of the component body

All family-to-family spacing rules can be set with the Family-to-Family Spacing Rules dialog box. The dialog box contains two matrixes of data entry boxes, one for the front side of the PCB and the other for the back side of the PCB. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

Family-to-family spacing rules are assigned to one image family with respect to one or more other families. The Family-to-Family Spacing Rules dialog box contains a Family I list and a Family II list. Use the [Filter](#) Family I [list](#) on the left to choose one image family. Then use the [Filter](#) Family II [list](#) on the right to choose the other families. You can choose the same family name in the Family II list that you chose in the Family I list.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### **Note**

Family to family spacing rules apply to all instances of the images in specified families.

## Rules - Image to Image

### Sets pad edge and body edge spacing rules between two or more images

Image-to-image spacing rules have the highest precedence in the spacing rule hierarchy. They override conflicting spacing rules at all other levels such as image set, image, component, or room.

You can set a single image-to-image spacing rule for an image with respect to other images, or you can set separate Pad-to-Pad, Pad-to-Body, and Body-to-Body rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- Pad Edge, which is the edge of a pin shape
- Body Edge, which is the edge of the component body

All image-to-image spacing rules can be set with the Image to Image Spacing Rules dialog box. The dialog box contains two matrixes of data entry boxes, one for the front side of the PCB and the other for the back side of the PCB. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

Image-to-image spacing rules are assigned to one image with respect to one or more other images. The Image to Image Spacing Rules dialog box contains an Image list and an Images list. Use the [Filter Image list](#) on the left to choose one image. Then use the [Filter Images list](#) on the right to choose the other images. You can choose the same image name in the Images list that you chose in the Image list.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Note

Image-to-image spacing rules apply to all instances of the specified images.

## Rules - Component

### **Sets placement rules for individual components**

The commands on the Rules - Component menu are

Spacing

Permitted Orientations

Permitted Sides

Opposite Sides

## Rules - Component - Spacing

### Sets spacing rules for components

You can set a single spacing rule for a component, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All component object-to-object spacing rules can be set with the Component Spacing Rules dialog box. The dialog box contains two matrixes of data entry boxes, one for the front side of the PCB and the other for the back side of the PCB. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

Component spacing rules are assigned to the active component. The reference designator of the active component is displayed at the top of the Component Spacing Rules dialog box. You can use the Pick Active Component dialog box to change the active component. Enter the component reference designator or a wildcard in the [Filter](#) data entry box or click the component reference designator in the [Components list](#). Click OK in the Pick Active Component dialog box.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Notes

Component spacing rules take precedence over image, image set, and PCB spacing rules. Rules at other levels such as room or room image set override conflicting component rules.

Component rules override rules assigned to the component's image. If you do not assign rules for a component, SPECCTRA uses default rules or rules set at a lower precedence level.

## Rules - Component - Permitted Orientations

### Sets orientation rules for individual components

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees or as horizontal or vertical. You can also permit different orientations for the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The component footprints are analyzed during automatic placement to determine the correct orientations:

- If a component has more pins in a horizontal array than in any vertical array, the component is horizontal.
- If a component has more pins in a vertical array than in any horizontal array, the component is vertical.

If the largest horizontal and vertical arrays have the same number of pins, a component's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the component's orientation is unspecified.

All permitted orientation rules can be set with the Permitted Component Orientation Rules dialog box. Component orientation rules are assigned to the active component. The reference designator of the active component is displayed at the top of the Permitted Component Orientation Rules dialog box.

You can use the Pick Active Component dialog box to change the active component. Enter the component reference designator or a wildcard in the [Filter](#) data entry box or click the component reference designator in the [Components list](#). Click OK in the Pick Active Component dialog box.

The orientation options for the FRONT and BACK of the PCB are

**No rule** means the rule is unspecified.

**Horizontal** means components can be aligned with the X axis.

**Vertical** means components can be aligned with the Y axis.

**Specified by Degree** means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

Components with square footprints (same number of pins on all four sides) can be rotated to any permitted orientation if you specify a horizontal or vertical rule. If you specify the permitted orientation rules by degrees, SPECCTRA follows the rules exactly for square components.

Permitted component orientation rules take precedence over image, image set, and PCB rules. Rules at other levels such as room or room image set override conflicting component rules.

Component rules override rules assigned to the component's image. If you do not assign

rules for a component, SPECCTRA uses default rules or rules set at a lower precedence level.

## Rules - Component - Permitted Sides

### Sets permitted side rules for individual components

Permitted sides rules determine the sides of the PCB on which components can be placed. Use the Permitted Component Side Rules dialog box to assign permitted side rules for individual components. The permitted sides options are

**Both** means component can be placed on either side of the PCB.

**Front** means component can be placed only on the front side of the PCB.

**Back** means component can be placed only on the back side of the PCB.

Component permitted side rules are assigned to the active component. The component ID of the active component is displayed at the top of the Permitted Component Side Rules dialog box. You can use the Pick Active Component dialog box to change the active component. Enter the component ID or a wildcard in the [Filter](#) data entry box or click the component ID in the [Components list](#). Click OK in the Pick Active component dialog box.

### Notes

If you do not set permitted side rules, placement is permitted on both sides of the PCB by default.

Permitted component orientation rules take precedence over image, image set, and PCB rules. Rules at other levels such as room or room image set override conflicting component rules.

Component rules override rules assigned to the component's image. If you do not assign rules for a component, SPECCTRA uses default rules or rules set at a lower precedence level.

## Rules - Component - Opposite Sides

### Sets opposite side rules for individual components

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side.

By default, all opposite side placement is permitted. Use the Component Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed on the opposite side of other large components.

**Large\_Small** permits large components to be placed on the opposite side of small components and small components to be placed on the opposite side of large components.

**Small\_Small** permits small components to be placed on the opposite side of other small components.

Large\_Large is ignored when opposite side rules are set for a capacitor or discrete component. Small\_Small is ignored when opposite side rules are set for a large component.

Component opposite side rules are assigned to the active component. The reference designator of the active component is displayed at the top of the Component Opposite Side Rules dialog box. You can use the Pick Active Component dialog box to change the active component. Enter the component ID or a wildcard in the [Filter](#) data entry box or click the component ID in the [Components list](#). Click OK in the Pick Active Component dialog box.

### Notes

Component opposite side rules take precedence over image, image set, and PCB rules. Rules at other levels such as room or room image set override conflicting component rules.

Component rules override rules assigned to the component's image. If you do not assign rules for a component, SPECCTRA uses default rules or rules set at a lower precedence level.



## Rules - Room

**Sets contents and placement rules for components or image sets within rooms**

The commands on the Rules - Room menu are

[Contents](#)

[All Components](#)

[Large](#)

[Small](#)

[Capacitor](#)

[Discrete](#)

## Rules - Room - Contents

### Sets content rules that restrict component placement in rooms

A room is an area that you define to control in which SPECCTRA places components on the PCB. Room contents rules set conditions that help determine component room assignments. These conditions are

- Included components or clusters
- Excluded components or clusters
- Power dissipation limit (maximum)
- Height limits (minimum and maximum)
- Permitted power nets

Components and clusters are classified as hard-bound or soft-bound and as included or excluded.

**Hard-bound Incl Comp List:** assigns components and clusters to be placed completely within the room. No part of an assigned component can lie outside the room.

**Soft-bound Incl Comp List:** sets a preference for placing components and clusters in the room if space is available. Otherwise, the components or clusters can be placed outside the room.

**Hard-bound Excl Comp List:** prevents any part of a specified component, or of components in a specified cluster, from being placed inside the room.

**Soft-bound Excl Comp List:** sets a preference for excluding components and clusters from the room unless they can't be placed elsewhere.

Each classification can be turned on or turned off. To specify components, you can use the Components [list](#) or the [Filter](#) data entry box above the list. To specify clusters, you can use the Clusters [list](#) or the [Filter](#) data entry box above the list.

**Remain** specifies all remaining components.

**Room Height:** controls component placement in a room by specifying maximum or minimum component heights. All components must be assigned the maximum height property if you use this check box. You can specify a maximum height rule, a minimum height rule, or both. A value of -1 means the maximum or minimum height rule is unspecified.

**Max Power Dissipation:** controls component placement in a room based on the total power dissipation of all components in the room. All components must be assigned a power dissipation property if you use this check box. A value of -1 means the power dissipation rule is unspecified.

**Room Power Net List:** assigns components to be placed in the room based on their connection to specific power nets. To specify power nets, use the Power Nets [list](#) or the [Filter](#) data entry box above the list.

Room contents rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Contents Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Notes

You must define a room before you can assign contents rules to it.

If maximum height and power dissipation properties aren't defined in the design file, you can assign them using [Define - Component Properties](#) or [Define - Image Properties](#).

## Rules - Room - All Components

**Sets placement rules for all components in a room**

The commands on the Rules - Room - All Components menu are

[Spacing](#)

[Permitted Orientation](#)

[Permitted Sides](#)

[Opposite Sides](#)

## Rules - Room - All Components - Spacing

### Sets spacing rules for rooms

A room is an area that you define to control in which SPECCTRA places components on the PCB. Spacing rules assigned to a room take precedence over all image set, image, and component spacing rules assigned elsewhere in the PCB.

You can set a single spacing rule for a room, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All room object-to-object spacing rules can be set with the Room Spacing Rules dialog box. The dialog box contains two matrixes of data entry boxes, one for the front side of the PCB and the other for the back side of the PCB. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

Room spacing rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Spacing Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Images list](#). Click OK in the Pick Active Room dialog box.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Notes

Spacing rules assigned to room image sets override conflicting room spacing rules.

If you do not assign spacing rules for a room, lower precedence rules apply within the room.

## Rules - Room - All Components - Permitted Orientations

### Sets component orientation rules for rooms

A room is an area that you define to control in which SPECCTRA places components on the PCB. Permitted orientation rules assigned to a room take precedence over all image set, image, and component permitted orientation rules assigned elsewhere in the PCB.

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees or as horizontal or vertical. You can also permit different orientations for the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

If the largest horizontal and vertical arrays have the same number of pins, an image's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the image's orientation is unspecified.

All permitted orientation rules can be set with the Room Permitted Orientation Rules dialog box. Room permitted orientation rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Permitted Orientation Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

The orientation options for the FRONT and BACK sides of the PCB are

**No rule** means the rule is unspecified.

**Horizontal** means components can be aligned with the X axis.

**Vertical** means components can be aligned with the Y axis.

**Specified by Degree** means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

Components with square footprints (same number of pins on all four sides) can be rotated to any permitted orientation if you specify a horizontal or vertical rule. If specify the permitted orientation rules by degrees, SPECCTRA follows the rules exactly for square components.

Permitted orientation rules assigned to room image sets override conflicting room permitted orientation rules.

If you do not assign permitted orientation rules for a room, lower precedence rules apply within the room.

## Rules - Room - All Components - Permitted Sides

### Sets permitted side rules for rooms

A room is an area that you define to control in which SPECCTRA places components on the PCB. Permitted side rules assigned to a room take precedence over all image set, image, and component permitted side rules assigned elsewhere in the PCB.

Permitted side rules determine the sides of the PCB on which components can be placed. Use the Permitted Component Side Rules dialog box to assign permitted side rules for all components in the room. The side options are

**Both** means components in the room can be placed on either side of the PCB.

**Front** means components in the room can be placed only on the front side of the PCB.

**Back** means components in the room can be placed only on the back side of the PCB.

Room permitted side rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Permitted Side Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Notes

If you do not set permitted side rules, placement is permitted on both sides of the PCB by default.

Permitted side rules assigned to room image sets override conflicting room permitted side rules.

If you do not assign permitted side rules for a room, lower precedence rules apply within the room.

## Rules - Room - All Components - Opposite Sides

### Sets opposite side rules for rooms

A room is an area that you define to control in which SPECCTRA places components on the PCB. Opposite side rules assigned to a room take precedence over all image set, image, and component permitted side rules assigned elsewhere in the PCB.

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side.

By default, all opposite side placement is permitted. Use the Room Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed beneath other large components.

**Large\_Small** permits large components to be placed beneath small components and small components to be placed beneath large components.

**Small\_Small** permits small components to be placed beneath other small components.

Room opposite side rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Opposite Side Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Images list](#). Click OK in the Pick Active room dialog box.

### Notes

Opposite side rules assigned to room image sets override conflicting room opposite side rules.

If you do not assign opposite side rules for a room, lower precedence rules apply within the room.



## Rules - Room - Large

**Sets placement rules for all large components in a room**

The commands on the Rules - Room - Large menu are

[Spacing](#)

[Permitted Orientations](#)

[Permitted Sides](#)

[Opposite Sides](#)

## Rules - Room - Large - Spacing

### Sets spacing rules for large images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Large images have more than three pins. A room is an area that you define to control in which SPECCTRA places components on the PCB.

You can set the same spacing rule for all large images in the room, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All object-to-object spacing rules can be set with the Room Image Set Large Spacing Rules dialog box. The dialog box contains two tables of data entry boxes, one for SMD spacing and the other for PTH spacing. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

Room image set spacing rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Large Spacing Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Images list](#). Click OK in the Pick Active Room dialog box.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Note

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB. Image-to-image spacing rules that assign separate pad edge and body edge spacings override room image set spacing rules.

## Rules - Room - Large - Permitted Orientations

### Sets component orientation rules for large images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Large images have more than three pins. A room is an area that you define to control in which SPECCTRA places components on the PCB.

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees, or as horizontal or vertical. You can also permit different orientations for SMD and through-pin components, or on the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

If the largest horizontal and vertical arrays have the same number of pins, an image's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the image's orientation is unspecified.

All permitted orientation rules can be set with the Room Image Set Large Permitted Orientation Rules dialog box. Room permitted orientation rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Large Permitted Orientation Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

The orientation options are

**No rule** means the rule is unspecified.

**Horizontal** means components can be aligned with the X axis.

**Vertical** means components can be aligned with the Y axis.

**Specified by Degree** means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

Components with square footprints (same number of pins on all four sides) can be rotated to any permitted orientation if you specify a horizontal or vertical rule. If you specify the permitted orientation rules by degrees, SPECCTRA follows the rules exactly for square components.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.

## Rules - Room - Large - Permitted Sides

### Sets permitted side rules for large images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Large images have more than three pins. A room is an area that you define to control in which SPECCTRA places components on the PCB.

Permitted side rules determine the sides of the PCB on which components can be placed. Use the Room Image Set Large Permitted Side Rules dialog box to assign permitted side rules for all large components in a room. You can permit different sides for SMD and through-pin component packages. The permitted side options are

**Both** means the image instances can be placed on either side of the PCB.

**Front** means the image instances can be placed only on the front side of the PCB.

**Back** means the image instances can be placed only on the back side of the PCB.

Permitted side rules for large images in a room are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Large Permitted Side Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Notes

If you do not set permitted side rules for a component package, placement is permitted on both sides of the PCB by default.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.

## Rules - Room - Large - Opposite Sides

### Sets opposite side rules for large images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Large images have more than three pins. A room is an area that you define to control in which SPECCTRA places components on the PCB.

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side. You can set the same opposite side rule for all component packages, or you can set separate rules for SMD and PTH components

By default, opposite side placement is permitted. Use the Room Image Set Large Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed beneath other large components.

**Large\_Small** permits large components to be placed beneath small components and small components to be placed beneath large components.

**Small\_Small** permits small components to be placed beneath other small components.

Small\_Small is ignored when opposite side rules are set for large images.

Opposite side rules for large images in a room are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Large Opposite Side Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Notes

If you do not set opposite side rules for a component package, all opposite placements of those components are permitted by default.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.

## Rules - Room - Small

**Sets placement rules for all small components in a room**

The commands on the Rules - Room - Small menu are

[Spacing](#)

[Permitted Orientations](#)

[Permitted Sides](#)

[Opposite Sides](#)

## Rules - Room - Small - Spacing

### Sets spacing rules for small images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. A room is an area that you define to control in which SPECCTRA places components on the PCB.

You can set the same spacing rule for all small image instances in the room, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All object-to-object spacing rules can be set with the Room Image Set Small Spacing Rules dialog box. The dialog box contains two tables of data entry boxes, one for SMD spacing and the other for PTH spacing. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

Room image set small spacing rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Small Spacing Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Note

Room image set small spacing rules apply to all small images in the room, including those assigned the capacitor or discrete property. However, capacitor and discrete room image set spacing rules override conflicting small image rules.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB. Image-to-image spacing rules that assign separate pad edge and body edge spacings override room image set spacing rules.

## Rules - Room - Small - Permitted Orientations

### Sets component orientation rules for small images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. A room is an area that you define to control in which SPECCTRA places components on the PCB.

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees, or as horizontal or vertical. You can also permit different orientations for SMD and through-pin components, or on the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

If the largest horizontal and vertical arrays have the same number of pins, an image's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the image's orientation is unspecified.

All permitted orientation rules can be set with the Room Image Set Small Permitted Orientation Rules dialog box. Room permitted orientation rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Small Permitted Orientation Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

The orientation options are

**No rule**, which means the rule is unspecified.

**Horizontal**, which means components can be aligned with the X axis.

**Vertical**, which means components can be aligned with the Y axis.

**Specified by Degree**, which means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

Room image set small permitted orientation rules apply to all small images in the room, including those assigned the capacitor or discrete property. However, capacitor and discrete room image set permitted orientation rules override conflicting small image rules.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.



## Rules - Room - Small - Permitted Sides

### Sets permitted side rules for small images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. A room is an area that you define to control in which SPECCTRA places components on the PCB.

Permitted side rules determine the sides of the PCB on which components can be placed. Use the Room Image Set Small Permitted Side Rules dialog box to assign permitted side rules for all small components in a room. You can permit different sides for SMD and through-pin component packages. The permitted side options are

**Both** means the image instances can be placed on either side of the PCB.

**Front** means the image instances can be placed only on the front side of the PCB.

**Back** means the image instances can be placed only on the back side of the PCB.

Permitted side rules for small components in a room are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Small Permitted Sides Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Notes

If you do not set permitted side rules for a component package, placement is permitted on both sides of the PCB by default.

Room image set small permitted side rules apply to all small images in the room, including those assigned the capacitor or discrete property. However, capacitor and discrete room image set permitted side rules override conflicting small image rules.

Room image set rules take precedence over room rules and over all image set, image, and component rules.

## Rules - Room - Small - Opposite Sides

### Sets opposite side rules for small images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. A room is an area that you define to control in which SPECCTRA places components on the PCB.

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side. You can set the same opposite side rule for all component packages, or you can set separate rules for SMD and PTH components

By default, opposite side placement is permitted. Use the Room Image Set Small Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed beneath other large components.

**Large\_Small** permits large components to be placed beneath small components and small components to be placed beneath large components.

**Small\_Small** permits small components to be placed beneath other small components.

Large\_Large is ignored when opposite side rules are set for small images.

Opposite side rules for small images in a room are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Small Opposite Side Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Notes

If you do not set opposite side rules for a component package, all opposite placements of those components are permitted by default.

Room image set small opposite side rules apply to all small images in the room, including those assigned the capacitor or discrete property. However, capacitor and discrete room image set permitted side rules override conflicting small image rules.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.

## Rules - Room - Capacitor

**Sets placement rules for all capacitors in a room**

The commands on the Rules - Room - Capacitor menu are

[Spacing](#)

[Permitted Orientations](#)

[Permitted Sides](#)

[Opposite Sides](#)

## Rules - Room - Capacitor - Spacing

### Sets spacing rules for capacitors in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Capacitor images are small images assigned the capacitor property either in the design file or in SPECCTRA. A room is an area that you define to control in which SPECCTRA places components on the PCB.

You can set the same spacing rule for all capacitors in the room, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All room capacitor image object-to-object spacing rules can be set with the Room Image Set Capacitor Spacing Rules dialog box. The dialog box contains two tables of data entry boxes, one for SMD spacing and the other for PTH spacing. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

Room image set spacing rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Capacitor Spacing Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Note

SPECCTRA treats small components with pins connected only to power nets as decoupling capacitors. If these components are not assigned the capacitor property in the design file, SPECCTRA assigns it automatically. You can override the automatic assignment and assign the small or discrete property. Rules assigned to small images apply to capacitor images when the capacitor image rules are not specified.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB. Image-to-image spacing rules that assign separate pad edge and body edge spacings override room image set spacing rules.

## Rules - Room - Capacitor - Permitted Orientations

### Sets component orientation rules for capacitors in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Capacitors are small images assigned the capacitor property either in the design file or in SPECCTRA. A room is an area that you define to control in which SPECCTRA places components on the PCB.

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees or as horizontal or vertical. You can also permit different orientations for SMD and through-pin components or on the front and back sides of the PCB.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

If the largest horizontal and vertical arrays have the same number of pins, an image's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the image's orientation is unspecified.

All permitted orientation rules can be set with the Room Image Set Capacitor Permitted Orientation Rules dialog box. Room permitted orientation rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Capacitor Permitted Orientation Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

The orientation options are

**No rule** means the rule is unspecified.

**Horizontal** means components can be aligned with the X axis.

**Vertical** means components can be aligned with the Y axis.

**Specified by Degree** means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

SPECCTRA treats small components with pins connected only to power nets as decoupling capacitors. If these components are not assigned the capacitor property in the design file, SPECCTRA assigns it automatically. You can override the automatic assignment and assign the small or discrete property. Rules assigned to small images apply to capacitor images when capacitor image rules are not specified.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.

## Rules - Room - Capacitor - Permitted Sides

### Sets permitted side rules for capacitors in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Capacitor images are small images assigned the capacitor property either in the design file or in SPECCTRA. A room is an area that you define to control in which SPECCTRA places components on the PCB.

Permitted side rules determine the sides of the PCB on which components can be placed. Use the Room Image Set Capacitor Permitted Side Rules dialog box to assign permitted side rules for all capacitors in a room. You can permit different sides for SMD and through-pin component packages. The permitted side options are

**Both** means the image instances can be placed on either side of the PCB.

**Front** means the image instances can be placed only on the front side of the PCB.

**Back** means the image instances can be placed only on the back side of the PCB.

Permitted side rules for capacitor image instances in a room are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Capacitor Permitted Side Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Notes

If you do not set permitted side rules for a component package, placement is permitted on both sides of the PCB by default.

SPECCTRA treats small components with pins connected only to power nets as decoupling capacitors. If these components are not assigned the capacitor property in the design file, SPECCTRA assigns it automatically. Rules assigned to small images apply to capacitor images when capacitor image rules are not specified.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.

## Rules - Room - Capacitor - Opposite Sides

### Sets opposite side rules for capacitors in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Capacitor images are small images assigned the capacitor property either in the design file or in SPECCTRA. A room is an area that you define to control in which SPECCTRA places components on the PCB.

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side. You can set the same opposite side rule for all component packages, or you can set separate rules for SMD and PTH components

By default, opposite side placement is permitted. Use the Room Image Set Capacitor Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed beneath other large components.

**Large\_Small** permits large components to be placed beneath small components and small components to be placed beneath large components.

**Small\_Small** permits small components to be placed beneath other small components.

Large\_Large is ignored when opposite side rules are set for capacitors.

Opposite side rules for capacitors in a room are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Capacitor Opposite Side Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Notes

If you do not set opposite side rules for a component package, all opposite placements of those components are permitted by default.

SPECCTRA treats small components with pins connected only to power nets as decoupling capacitors. If these components are not assigned the capacitor property in the design file, SPECCTRA assigns it automatically. You can override the automatic assignment and assign the small or discrete property. Rules assigned to small images apply to capacitor images when capacitor image rules are not specified.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.

## Rules - Room - Discrete

**Sets placement rules for all discrete components in a room**

The commands on the Rules - Room - Discrete menu are

[Spacing](#)

[Permitted Orientations](#)

[Permitted Sides](#)

[Opposite Sides](#)



## Rules - Room - Discrete - Spacing

### Sets spacing rules for discrete images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Discrete images are small images assigned the discrete property either in the design file or in SPECCTRA. A room is an area that you define to control in which SPECCTRA places components on the PCB.

You can set the same spacing rule for all discrete image instances in the room, or you can set separate rules for each object type with respect to each of the other object types. For example, you can set separate SMD-to-SMD, SMD-to-PTH, and PTH-to-PTH rules. You can also set different spacing rules for the front and back sides of the PCB. The object types are

- PTH, which is a through-pin component package
- SMD, which is a surface-mounted device package
- Area, which is a keepout region, a placement keepout, or the PCB boundary

All room discrete image object-to-object spacing rules can be set with the Room Image Set Discrete Spacing Rules dialog box. The dialog box contains two tables of data entry boxes, one for SMD spacing and the other for PTH spacing. Each data entry box represents one object-to-object spacing rule. A value of -1 means a rule is unspecified.

Room image set spacing rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Discrete Spacing Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

You can use the All data entry box to assign a single value for all object-to-object spacing rules. If you set individual spacing rule values, these values are overridden by the value in the All data entry box when you click Apply or OK.

### Note

The discrete property is used to differentiate certain small images that are not decoupling capacitors but that you want to place separately from other small components. Rules assigned to small images apply to discrete images when discrete image rules are not specified.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB. Image-to-image spacing rules that assign separate pad edge and body edge spacings override room image set spacing rules.

## Rules - Room - Discrete - Permitted Orientations

### Sets component orientation rules for discrete images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Discrete images are small images assigned the discrete property either in the design file or in SPECCTRA. A room is an area that you define to control in which SPECCTRA places components on the PCB.

Orientation rules determine the component rotations that are permitted. You can specify orientation by degrees, or as horizontal or vertical. You can also permit different orientations for SMD and through-pin components, or on the front and back sides of the PCB. The orientation options are

**No rule** means the rule is unspecified.

**Horizontal** means components can be aligned with the X axis.

**Vertical** means components can be aligned with the Y axis.

**Specified by Degree** means components can be rotated to one or more permitted angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

SPECCTRA uses the orientation defined for a component in the design file as the base, zero-degree reference. The image footprints are analyzed during automatic placement to determine the correct orientations:

- If an image has more pins in a horizontal array than in any vertical array, the image is horizontal.
- If an image has more pins in a vertical array than in any horizontal array, the image is vertical.

If the largest horizontal and vertical arrays have the same number of pins, an image's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the image's orientation is unspecified.

All permitted orientation rules can be set with the Room Image Set Discrete Permitted Orientation Rules dialog box. Room permitted orientation rules are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Discrete Permitted Orientation Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Tip

Use the horizontal or vertical orientation if the images in your design file are defined inconsistently (zero-degree rotation is horizontal for some images and vertical for others).

### Notes

The discrete property is used to differentiate certain small images that are not decoupling capacitors but that you want to place separately from other small components. Rules assigned to small images apply to discrete images when discrete image rules are not specified.

Rules image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.

## Rules - Room - Discrete - Permitted Sides

### Sets permitted side rules for discrete images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Discrete images are small images assigned the discrete property either in the design file or in SPECCTRA room is an area that you define to control in which SPECCTRA places components on the PCB.

Permitted side rules determine the sides of the PCB on which components can be placed. Use the Room Image Set Discrete Permitted Side Rules dialog box to assign permitted side rules for all discrete image instances in a room. You can permit different sides for SMD and through-pin component packages. The permitted side options are

**Both** means the image instances can be placed on either side of the PCB.

**Front** means the image instances can be placed only on the front side of the PCB.

**Back** means the image instances can be placed only on the back side of the PCB.

Permitted side rules for discrete image instances in a room are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Discrete Permitted Sides Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Notes

If you do not set permitted side rules for a component package, placement is permitted on both sides of the PCB by default.

The discrete property is used to differentiate certain small images that are not decoupling capacitors but that you want to place separately from other small components. Rules assigned to small images apply to discrete images when discrete image rules are not specified.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.

## Rules - Room - Discrete - Opposite Sides

### Sets opposite side rules for discrete images in a room

SPECCTRA uses the number of component pins to differentiate large and small images. Small images have three pins or less. Discrete images are small images assigned the discrete property either in the design file or in SPECCTRA room is an area that you define to control in which SPECCTRA places components on the PCB.

Opposite side rules permit or constrain opposite side placement of components on one side of the PCB beneath components on the other side. You can set the same opposite side rule for all component packages, or you can set separate rules for SMD and PTH components

By default, opposite side placement is permitted. Use the Room Image Set Discrete Opposite Side Rules dialog box to constrain opposite side placement based on image size. The choices are

**Large\_Large** permits large components to be placed beneath other large components.

**Large\_Small** permits large components to be placed beneath small components and small components to be placed beneath large components.

**Small\_Small** permits small components to be placed beneath other small components.

Large\_Large is ignored when opposite side rules are set for discrete images.

Opposite side rules for discrete images in a room are assigned to the active room. The room ID of the active room is displayed at the top of the Room Image Set Discrete Opposite Side Rules dialog box. You can use the Pick Active Room dialog box to change the active room. Enter the room ID or a wildcard in the [Filter](#) data entry box or click the room ID in the [Rooms list](#). Click OK in the Pick Active Room dialog box.

### Notes

If you do not set opposite side rules for a component package, all opposite placements of those components are permitted by default.

The discrete property is used to differentiate certain small images that are not decoupling capacitors but that you want to place separately from other small components. Rules assigned to small images apply to discrete images when discrete image rules are not specified.

Room image set rules take precedence over room rules and over all image set, image, and component rules assigned elsewhere in the PCB.

## Rules - Check Rules

### Checks design for any current rule conflicts or violations

You can check for placement violations, or you can check for both routing conflicts and placement violations. The Check Rule menu commands are

**All** checks both routing rule conflicts and placement rule violations.

**Placement** checks only placement rule violations.

When you start a rules check for placement, the current component positions and orientations are examined against current placement rules. Components that violate current rules are indicated by a thick-lined bounding box with diamond-shaped markers at each corner of the component's bounding box.

A common use of Check Rules is to determine the impact of a rule change on current component placements and finished routes. To do this apply the rule changes you want to check and click **Rules - Check Rules - Placement**. Examine violations caused by the rule changes and determine whether to keep the rule changes or reset one or more to their previous values.

When you start a rules check for both placement and routing, the current wiring is examined against current routing rules.

- Crossing conflicts are marked graphically with a diamond shape.
- Clearance conflicts are marked graphically with a bounding rectangle.
- Length rule violations are marked graphically with a yellow dashed line.
- Crosstalk violations are marked graphically with a white rectangle.

The following topics are pop-ups that describe fields in the Rules dialog boxes:

## T-Junction

### Controls whether tjunctions are permitted on starburst nets

The **T-Junctions** check box controls whether tjunctions are allowed when the [Net Ordering](#) selector is set to Starburst.

- When T-Junctions is turned on, the [Junction Type](#) selector controls in which tjunctions can occur on starburst nets.
- When T-Junctions is turned off, tjunctions are not permitted on starburst nets.

When Net Ordering is set to Daisy, Mid-Driven Daisy, or Balanced Daisy, the T-Junctions check box is ignored, and tjunctions are permitted only if [Stub Length](#) is set to a positive value.

## Junction Type

### Controls in which tjunctions can occur on nets

The **Junction Type** selector controls whether tjunctions can occur on wire segments or only at pins, vias, and SMD pads. The choices are

**All**, which means tjunctions can occur at pins, vias, and SMD pads, and along wire segments.

**Term\_Only**, which means that tjunctions can occur only at pins, vias, and SMD pads.

**Junction Type** is used only when

- Net Ordering is set to starburst and the T-Junction check box is checked.
- Net Ordering is set to Daisy, Mid-Driven Daisy, or Balanced Daisy, and Stub Length is set to a positive value.



## Via at SMD

The Via at SMD check box controls whether SMD escape vias can be added under SMD pads. When Via at SMD is checked, vias can be placed under SMD pads during autorouting. You can control in which vias are added by using

[Via at SMD Grid](#)

[Via at SMD Fit](#)

### Note

Via at SMD rules are followed only when the [HYB](#) option is installed.

## Via at SMD Grid

The Via at SMD Grid check box controls whether SMD escape vias must be placed on grid or at the pad origin.

When Via at SMD Grid is checked, vias placed under SMD pads are added at the via grid point that is closest to the pad origin. When Via at SMD Grid is not checked (default), escape vias are added under SMD pads at the pad origin.

Via at SMD Grid is ignored if [Via at SMD](#) is not checked, and the check is removed from this check box when you apply the dialog box.

### Note

The [HYB](#) option is required for Via at SMD Grid.

## Via at SMD Fit

The Via at SMD Fit check box controls whether vias added under SMD pads must fit entirely within the pad boundary. When Via at SMD Fit is checked, vias must completely fit within an SMD pad boundary in order to be placed under the pad.

Via at SMD Fit is ignored if [Via at SMD](#) is not checked, and the check is removed from this check box when you apply the dialog box.

### Note

The [HYB](#) option is required for Via at SMD Fit.

## Net Ordering

**Net Ordering** controls how nets are ordered for routing. The Net ordering choices are

**Starburst**, which uses a minimum spanning tree algorithm that permits multiple connections at pins and vias. Tjunctions are permitted if [T-Junction](#) is checked. The [Junction Type](#) selector controls in which junctions can occur. Starburst net ordering produces the most efficient wiring solution.

**Daisy**, which permits no more than two connections at each pin on a net. Tjunctions are permitted if [Stub Length](#) is set to a positive value. The [Junction Type](#) selector controls in which tjunctions can occur.

**Mid-Driven Daisy**, which places a terminator at each end of a net and the loads are added back to the source. There must be exactly two terminator pins, or the net is ordered as a simple daisy chain. If the net has more than one source pin, the sources are chained together first before load and terminator pins are ordered. Tjunctions are permitted if [Stub Length](#) is set to a positive value. The [Junction Type](#) selector controls in which tjunctions can occur.

**Balanced Daisy**, which evenly distributes loads between source and terminator pins. This ordering method requires that the net have at least one source pin and two or more terminator pins. If more than one source pin is defined, the terminator and load branches are chained back to the closest source pin, and the remaining sources are ordered as an optimal daisy chain. When you specify a net to be ordered as Balanced Daisy, but it doesn't satisfy the minimum source, load, and terminator pin requirements, the net is ordered as a simple optimized daisy chain. Tjunctions are permitted if [Stub Length](#) is set to a positive value. The [Junction Type](#) selector controls in which tjunctions can occur.

## Limit Cross

### **Limits the number of crossing conflicts permitted when routing a connection**

The crossing limit range is from 0 to 255. If you do not supply a Limit Cross value, the autorouter computes a value for each routing pass. You can restore the limit cross rule to unspecified and use the autorouter's built in rules by setting the value to -1.

## Limit Bends

**Limits the number of bend points (corners) that can be used to route a connection**

The bend limit range is from 0 to 255. If you do not supply a Limit Bends value, the autorouter computes a value for each routing pass. You can restore the Limit Bends rule to unspecified and use the autorouter's built in rules by entering a value of -1.

## Limit Vias

**Limits the number of vias that can be used to route a connection.**

The via limit range is from 0 to 255. If you do not supply a Limit Vias value, the autorouter computes a value for each routing pass. You can restore the Limit Vias rule to unspecified and use the autorouter's built in rules by entering a value of -1.

### Note

Limit vias limits the number of vias on a pin-to-pin connection. See also [Max Total Vias](#) for details about setting limits on the number of vias on a net.

## Limit Way

### **Limits the wrong way routing distance**

The wrong way direction is vertical on horizontal routing layers and horizontal on vertical routing layers. The wrong way limit value must be a positive dimension (includes 0) and must be correctly scaled for your current measurement units. If you do not supply a Limit Way value, the autorouter computes a value for each routing pass. You can restore the limit way rule to unspecified and use the autorouter's built in rules by entering a value of -1.



## Max Stagger

**Max Stagger** determines the maximum via-to-via connection length on a mixed layer. A mixed layer is a power layer that can also be used to route signal connections. The Max Stagger value must be entered for the current measurement units. A value of -1 indicates that Max Stagger is unspecified and, therefore, a connection can be routed without length restrictions on a mixed layer.

## Stub Length

**Stub Length** determines the maximum stub length permitted on daisy-chain connections. It also determines whether tjunctions are permitted on these connections. Stub length is usually used when [Net Ordering](#) is set to Daisy, Mid-Driven Daisy, or Balanced Daisy.

Stub length is the length along a wire between a pin or via and a tjunction. Stub length is measured from the edge of the pad to the center of the stub wire. A Stub Length value of 0 prohibits stubs. A value of -1 resets the stub length rule to unspecified.

A Stub Length value greater than 0 permits tjunctions on the connections.

## Min Shield

**Min Shield** sets the minimum wire length that can be shielded. Length is calculated from terminal origin to terminal origin. The default minimum shield length is 0.125 inches if you do not specify a Min Shield value. You restore the Min Shield rule to its default by entering a value of -1.

### Note

The Min Shield rule is followed only when the [FST](#) option is installed.

## Pick Active Class for Rules

### **Changes the active class for which rules are assigned**

Use the Pick Active Class for Rules dialog box when you want to change the class for which you assign class rules. Each class rules dialog box has a Pick Class... button. When you click this button, and choose a class in the Pick Active Class for Rules dialog box, the current (or default) rules for the class appear in the class rules dialog box.

[Filter data entry box](#)

[Items list](#)

## Pick Active Fromto for Rules

### **Changes the active fromto for which rules are assigned**

Use the Pick Active Fromto for Rules dialog box when you want to change the fromto for which you assign fromto rules. Each fromto rules dialog box has a Pick Fromto... button. When you click this button, and choose a fromto in the Pick Active Fromto for Rules dialog box, the current (or default) rules for the fromto appear in the fromto rules dialog box.

[Filter data entry box](#)

[Items list](#)

## Pick Active Group for Rules

### **Changes the active group for which rules are assigned**

Use the Pick Active Group for Rules dialog box when you want to change the group for which you assign group rules. Each group rules dialog box has a Pick Group... button. When you click this button, and choose a group in the Pick Active Group for Rules dialog box, the current (or default) rules for the group appear in the group rules dialog box.

[Filter data entry box](#)

[Items list](#)

## Pick Active Layer for Rules

### **Changes the active layer for which rules are assigned**

Use the Pick Active Layer for Rules dialog box when you want to change the layer for which you assign layer rules. Each layer rules dialog box has a Pick Layer... button. When you click this button, and select a layer in the Pick Active Layer for Rules dialog box, the current (or default) rules for the layer appear in the layer rules dialog box.

[Filter data entry box.](#)

[Items list](#)

## Pick Active Net for Rules

### **Changes the active net for which rules are assigned**

Use the Pick Active Net for Rules dialog box when you want to change the net for which you assign net rules. Each net rules dialog box has a Pick Net... button. When you click this button, and select a net in the Pick Active Net for Rules dialog box, the current (or default) rules for the net appear in the net rules dialog box.

[Filter data entry box.](#)

[Items list.](#)



## Pick Active Padstack for Rules

### **Changes the active padstack for which rules are assigned**

Use the Pick Active Padstack for Rules dialog box when you want to change the padstack for which you assign padstack rules. The padstack rules dialog box has a Pick Padstack... button. When you click this button, and select a padstack in the Pick Active Padstack for Rules dialog box, the current (or default) rules for the padstack appear in the padstack rules dialog box.

[Filter data entry box.](#)

[Items list.](#)

## Pick Active Region for Rules

### **Changes the active region for which rules are assigned**

Use the Pick Active Region for Rules dialog box when you want to change the region for which you assign region rules. The region rules dialog box has a Pick Region ... button. When you click this button, and select a region in the Pick Active Region for Rules dialog box, the current (or default) rules for the region appear in the region rules dialog box.

[Filter data entry box.](#)

[Items list.](#)

## Length Factor

### **Sets a layer factor used for calculating wire lengths**

The length factor adjusts wire length calculations by layer. Actual wire lengths are multiplied by a layer's length factor to calculate routed length. Enter a value of -1 to set length factor to unspecified.

#### **Note**

Length rules are followed only when the FST option is installed.

## Specify as Ratios

**Specify as Ratios** determines whether the Min Length and Max Length values are used as actual length values or as factors. When Specify as Ratios is checked, the Min Length and Max Length values are used as factors. The Manhattan length of the net is multiplied by the Min Length and Max Length factors to calculate minimum and maximum length rules.

### Notes

For example, suppose you specify a Min Length of 1.2 and a Max Length of 1.4. The minimum length of the net can be no less than 120% of the Manhattan length. The maximum length of the net can be no greater than 140% of the Manhattan length.

Length rules are followed only when the FST option is installed.

## Min Length

**Min Length** determines the minimum routed length of a net. Enter either an actual length value or a factor. Min Length is used as a factor when Specify as Ratios is checked.

### Notes

Remember to consider the current measurement unit when you enter a dimensional value.

Length rules are followed only when the FST option is installed.

## Max Length

**Max Length** determines the maximum routed length of a net. Enter either an actual length value or a factor. Max Length is used as a factor when Specify as Ratios is checked.

### Notes

Remember to consider the current measurement unit when you enter a dimensional value.

Length rules are followed only when the FST option is installed.

## Length Gap

**Length Gap** determines the edge-to-edge distance maintained between adjacent segments when the autorouter uses an accordion, trombone, or serpentine pattern to follow a minimum or matched length rule or a minimum or matched delay rule.

### Notes

Remember to consider the current measurement unit when you enter a dimensional value.

Length rules are followed only when the [FSI](#) option is installed.

## Length Amplitude

**Length Amplitude** determines the maximum height when the autorouter uses an accordion pattern to follow a minimum length rule. The value must be correctly scaled for the current measurement units.

When Length Amplitude is set to a small number (between 1 and 2 mils), the router is limited to the trombone or serpentine pattern. The accordion pattern is not allowed.

When Length Amplitude is set to 0, the router is limited to the serpentine pattern. The trombone and accordion patterns are not allowed.

### Notes

Remember to consider the current measurement unit when you enter a dimensional value.

Length rules are followed only when the [FST](#) option is installed.



## Tjunctions

The **T-Junctions** check box controls whether tjunctions are allowed when the [Net Ordering](#) selector is set to Starburst.

- When **T-Junctions** is turned on, the **Junction Type** selector controls in which tjunctions can occur on starburst nets.
- When **T-Junctions** is turned off, tjunctions are not permitted on starburst nets.

When Net Ordering is set to Daisy, Mid-Driven Daisy, or Balanced Daisy, the T-Junctions check box is ignored, and tjunctions are permitted only if [Stub Length](#) is set to a positive value.

The **Junction Type** selector controls whether tjunctions can occur on wire segments or only at pins, vias, and SMD pads. The choices are

**All**, which means tjunctions can occur at pins, vias, and SMD pads, and along wire segments.

**Term\_Only**, which means that tjunctions can occur only at pins, vias, and SMD pads.

**Junction Type** is used only when

- [Net Ordering](#) is set to starburst and the [T-Junction](#) check box is checked.
- [Net Ordering](#) is set to Daisy, Mid-Driven Daisy, or Balanced Daisy, and [Stub Length](#) is set to a positive value.

## Net Priority

**Net Priority** determines when a net is scheduled for routing with respect to other nets. It also means components on the net are placed sooner than other components with similar connectivity levels during automatic placement.

Enter a value between 0 and 255. Assign the highest priority by entering a value of 255. If you do not assign a priority, the default priority for all nets is 10. When you assign priorities to several nets, separate each entry by 10 or more, otherwise the autorouter may consider the nets to have the same priority due to other rules or internal priority.

## Fromto Priority

**Fromto Priority** determines when a fromto is scheduled for routing with respect to other fromtos on the same net.

Enter a value between 0 and 255. Assign the highest priority by entering a value of 255. If you do not assign a priority, the default priority for all fromtos is 10.

## Match Net Length

**Match Net** determines whether all the nets in a class are routed to the same length or delay, minus a tolerance value. The tolerance value used depends on the timing option you specify.

- When the LENGTH option is used and Match Net is checked, all the nets in the class are routed to the same length minus the specified [Length Tolerance](#) value. A value of -1 means tolerance is unspecified, and the default tolerance of 1 inch is used.
- When the TIME option is used and Match Net is checked, all the nets in the class are routed to the same delay minus the specified [Delay Tolerance](#) value. A value of -1 means tolerance is unspecified, and the default tolerance of 1 inch multiplied by the [Time/Length Factor](#) is used.

If Match Net is used without setting a cap value by using [Max Length](#) for the LENGTH option or [Max Delay](#) for the TIME option, the default maximum length of the matched nets is 1.5 times the longest Manhattan length in the class.

## Match Fromtos

**Match Fromtos** determines whether the fromtos in a net, class, or group are routed to the same length or delay, minus a tolerance value. The tolerance value used depends on the timing option you specify.

- When the LENGTH option is used and Match Fromto is checked, all the fromtos in the net, class, or group are routed to the same length minus the specified [Length Tolerance](#) value. A value of -1 means tolerance is unspecified, and the default tolerance of 1 inch is used.
- When the TIME option is used and Match Fromto is checked, all the fromtos in the net, class, or group are routed to the same delay minus the specified [Delay Tolerance](#) value. A value of -1 means tolerance is unspecified, and the default tolerance of 1 inch multiplied by the [Time/Length Factor](#) is used.

If Match Fromto is used without setting a cap value by using [Max Length](#) for the LENGTH option or [Max Delay](#) for the TIME option, the default maximum length of the matched fromtos is 1.5 times the longest fromto in the net, class, or group.

## Tolerance

The autorouter subtracts a specified tolerance value from the target length or delay for matched nets or fromtos, while maintaining a matched length or delay.

**Length Tolerance** is the amount the autorouter can subtract from the target length.

**Delay Tolerance** is the amount the autorouter can subtract from the target delay.

The tolerance value must be either a positive value or a value of -1, which indicates the tolerance is unspecified. The default length tolerance is 1 inch. The default delay tolerance is 1 inch multiplied by the [Time/Length Factor](#).

The Length Tolerance value is used only when the LENGTH option is used and [Match Fromto](#), [Match Net](#), or both are checked.

The Delay Tolerance value is used only when the TIME option is used and [Match Fromto](#), [Match Net](#), or both are checked.

## Use Vias

**Use Vias** determines whether the vias you mark in the Vias list are used to route the net. When the Use Vias check box is checked, all vias marked in the Vias list are assigned for routing the net.

You can mark a via in the Vias list by clicking on it, or you can hold down the [Shift] or [Ctrl] keys when you click, to mark more than one via in the list. You can also use Filter to mark a via by entering the via id from the keyboard.

### Note

Use via rules are followed only when the [ADV](#) option is installed. You can specify a use via rule for a net, group, or class.

## Max Total Vias

**Max Total Vias** sets the maximum number of vias that can be used to route the net. You can enter a value of 0 and prohibit the use of vias to route the net. Enter a value of -1 to set the maximum number of vias for the net to unspecified.

### Note

You can set Max Total Vias for a net, for each net in a group, or for each net in a class.



## Effective Via Length

**Effective Via Length** determines the amount added to wire length calculations by each through-via. A value of -1 resets the effective via length to unspecified.

### Note

Remember to consider the current measurement unit when you enter a dimensional value. For delay calculations, the Effective Via Length is divided by the [Time/Length Factor](#) to calculate the delay for each via. For length calculations, the Effective Via Length is used to calculate the total minimum, maximum, or matched length.

Effective Via Length rules are followed only when the [FST](#) option is installed.

## Use Layers

**Use Layers** determines whether layers marked in the Layers list are assigned as routing layers. When the Use Layers check box is checked, layers marked in the Layers list are assigned for routing the active net, class, or group.

You can mark a layer in the list by clicking on it, or you can hold down the [Shift] or [Ctrl] keys when you click, to mark more than one layer. You can also use Filter to mark a layer by entering the layer name from the keyboard.

### Note

Use layers wiring rules are followed only when the [ADV](#) option is installed. You can specify a Use layers wiring rule for a net, a class of nets, or a group of fromtos.

When a layer is specified in a Use layers wiring rule, the layer is routed even if it is unselected.

## Length Tolerance

**Length Tolerance** is the amount the autorouter can subtract from the target length of a fromto or net, while maintaining a matched length..

The tolerance value must be either a positive value or a value of -1, which indicates the tolerance is unspecified. The default length tolerance is 1 inch.

The Length Tolerance value is used only when the LENGTH option is used and Match Fromto, Match Net, or both are checked.

## Min Delay

**Min Delay** is the minimum routed delay time.

### Note

You must set a Time/Length Factor before the autorouter can use the minimum delay rules.

## Max Delay

**Max Delay** is the maximum routed delay time.

### Note

You must set a Time/Length Factor before the autorouter can use the maximum delay rules.

## Time/Length Factor

**Time/Length Factor** is a time conversion factor for wire lengths. It is the ratio of time per unit length used as a multiplier to calculate effective wire lengths from delay times. The length is measured in the current measurement units, such as inch or mil. The conversion factor must be consistent with the time units you are using in the design.

You must set a time conversion factor if you want the autorouter to follow timing delay rules.

## Delay Tolerance

**Delay Tolerance** is the amount the autorouter can subtract from the target delay time of a fromto or net, while maintaining a matched delay.

The tolerance value must be either a positive value or a value of -1, which indicates the tolerance is unspecified. The default delay tolerance is 1 inch multiplied by the [Time/Length Factor](#).

The Delay Tolerance value is used only when the TIME option is used and [Match Fromto](#), [Match Net](#), or both are checked.

## Min Total Length

**Min Total Length** is the minimum length of the total routed length of fromtos in the group. The sum of the lengths of routed fromtos in the group must be within the Min Total Length and the Max Total Length.



## Max Total Length

**Max Total Length** is the maximum length of the total routed length of fromtos in the group. The sum of the lengths of routed fromtos in the group must be within the Min Total Length and the Max Total Length.

## Min Total Delay

**Min Total Delay** is the minimum delay time of the total routed fromtos in the group. The sum of the delay times of routed fromtos in the group must be within the Min Total Delay and the Max Total Delay.

### Note

You must set a Time/Length Factor before the autorouter can use the minimum total delay rules.

## Max Total Delay

**Max Total Delay** is the maximum delay time of the total routed fromtos in the group. The sum of the delay times of routed fromtos in the group must be within the Min Total Delay and the Max Total Delay.

### Note

You must set a [Time/Length Factor](#) before the autorouter can use the maximum total delay rules.

## **Autoroute Menu**

**Performs prerouting, routing, and postrouting operations**

The Autoroute menu commands are

[Setup](#)

[Pre Route](#)

[Route](#)

[Clean](#)

[Post Route](#)

## Autoplace Menu

### **Performs initial and automatic placement operations**

The AutoPlace menu commands are

Setup

UnPlace Components

Cluster Components

InitPlace Large Components

Interchange Components

InitPlace Small Components

Auto Rotate Components

Automatic Swap

Small Comp Pattern

Crossing Histogram

Density Analysis

## Autoroute - Setup

### **Sets the wire and via grids, global clearance and wire width rules, and the fence type**

The Routing Setup dialog box contains the following:

**Wire Grid**, which sets a uniform X, Y grid used for routing. The dimension you enter in the Wire Grid box creates equidistant grid points in the X and Y dimensions. New and rerouted wires are placed on the specified grid, except when entering or exiting off-grid pins. Existing wires that don't require rerouting are not changed.

**Via Grid**, which sets a uniform X, Y grid used for placing vias. The dimension you enter in the Via Grid box creates equidistant grid points in the X and Y dimensions. New and rerouted vias are placed on the specified grid. Existing vias that are not involved in rerouting are not changed.

**PCB Clearance**, which sets routing clearance rules at the PCB level. This is the lowest [precedence](#) rule level. Rules at other levels override conflicting PCB rules.

**PCB Wire Width**, which sets wire width rules at the PCB level. This is the lowest [precedence](#) rule level. Rules at other levels override conflicting PCB rules.

**Set All Fences**, which sets the fence type to either soft or hard when you create a fence.

**Soft** causes the autorouter to do the following:

- All connections inside the soft fence are routed within the fence boundary.
- All connections outside the soft fence are routed outside the fence and cannot cross the fence.
- All connections that cross the soft fence ignore the fence.

**Hard** causes the autorouter to route only connections that are completely inside the fence.

### **Tip**

Use a soft fence to separate analog and digital signals.

### **Note**

For information on creating a fence, see [Define - Fence](#) and [Define - Draw Fence Mode](#).

## Autoroute - Pre Route

### **Performs prerouting operations**

Commands on the Autoroute - Pre Route menu are

Fanout

Seed Vias

Wirebonds

Bus Routing

## Autoroute - Pre Route - Fanout

### Routes short escape wires from SMD pads to vias

Routing short escape wires from SMD pads to vias allows subsequent routing of these connections on other layers.

The autorouter chooses the SMD escape vias from the available via set and places them on the current via grid. You can select the components you want to fanout and specify which pin types to escape.

If no components or nets are selected, all active SMD component pins are escaped. "Active" does not include single pin nets.

Before you use fanout, consider the following:

- Fanout can assist the autorouter on PCBs with four or more signal layers, but is usually not used with two-layer PCB designs.
- If you want to escape only some pins on a component, select just those pins. Only selected pins are escaped when you use **Autoroute - Pre Route - Fanout**.
- If you escape all pin types, all pins (including pins without nets assigned) are escaped.

The Fanout dialog box contains the following options:

**Direction** directs the autorouter to escape wires and vias inside the component footprint (In), outside the footprint (Out), or both (Both). The default is Both.

**Max length** restricts the routed length of the escape wires. The maximum length is measured from a pad's origin to the center of the via. The default is -1, which means there is no restriction on the routed length.

**Passes** specifies the number of rip-up and reroute fanout passes. Conflicts are allowed in the escape wires until the last fanout pass. Five fanout passes are suggested. The default is 1 fanout pass.

**Pin Sharing** controls whether the autorouter can escape to through-pins. If this is on, the autorouter escapes to a through-pin if the cost is lower than the cost to use a via.

**Via Sharing** allows the autorouter to share vias between SMD pads on the same net. If this is off, the autorouter uses unique vias for every surface mount pad.

**Within distance** sets the maximum distance that a via or pin can be from a through-pin or via if Pin Sharing or Via Sharing is on. Vias and pins farther away from these pins will not share a fanout via. The default is -1, which means pin sharing can occur with any pin or via within the default distance of 200 mils. If you enter a value of zero, a maximum distance is not set.

**Grid for Fanout** specifies the fanout grid, which is used only while this command is being executed. The fanout grid can be one of the following

**Current Via Grid**, which uses the current via grid. You can specify the via grid by using [Autoroute - Setup](#).

**1 Wire between Vias**, which allows one wire to be routed between vias.

**2 Wires between Vias**, which allows two wires to be routed between vias.

**Specify**, which sets a uniform X, Y grid used for placing fanout vias. The dimension that you enter in the Specify box creates equidistant grid points in the X and Y dimensions.



**Pin Types** specifies which types of pins are escaped. The pin types are

**All**, which are all pins on the component, including active and unused.

**Active**, which are all signal pins that interconnect with one or more pins, and all power pins.

**Power Nets**, which are all pins that have power nets assigned.

**Signal Nets**, which are all pins that have signal nets assigned and interconnect with one or more other pins.

**Single Pin Nets**, which are all single pin signal nets.

**Unused Pins**, which are (**All**) all pins, including SMD pads and through-pins, that have no net assigned or (**Except thru-pins**) only SMD pads. Unused pins are collected into a single net called \*UNUSED\_PINS\*.

**Blind/Buried Vias** controls the direction of the routing for blind and buried vias. The options are

**Top**, which sets fanout toward the front or top side.

**Bottom**, which sets fanout toward the back or bottom side.

**Opposite Side**, which sets fanout to the opposite side of the design. Pads on the top side fanout toward the bottom side and pads on the bottom side fanout toward the top side.

Embedded pins fanout to the opposite side from the side to which they are closest.

**Max layer span** controls the number of layers a blind or buried via will use during fanout. The default is -1, which does not limit the number of layers.

#### Tip

After you execute **Autoroute - Pre Route - Fanout** with a specified fanout via grid, the escape patterns can be protected to avoid retooling for bed-of-nails testing. See [Autoroute - Post Route - Testpoints](#), which is used to generate test points.

## Autoroute - Pre Route - Seed Vias

### **Breaks a single connection into two shorter connections by adding a via**

You must define at least one through-via that extends through all signal layers before you can use **Autoroute - Pre Route - Seed Vias**. This command adds a single via at a corner of the bounding rectangle for each connection that satisfies the length criteria.

The Seed Vias dialog box is used to break up two-pin connections that are longer in both X- and Y- directions than the dimension you specify. The options in the Seed Vias dialog box are

**Break up connections longer than**, which is both an X- and Y-direction dimension value. The autorouter breaks up two-pin connections longer than this value. The default is one inch.

**Place vias under SMD components**, which specifies whether the autorouter can add vias under SMD components on two-signal layer designs. The default is off.

### **Tip**

**Autoroute - Pre Route - Seed Vias** is used for large multilayer designs that contain many long, diagonal connections. Because the number of vias can increase dramatically, depending on the dimension value you select, a dimension of two inches or more is suggested.

## Autoroute - Pre Route - Wirebonds

**Places bond sites and routes discrete wires from each site to the pads of a chip mounted on the PCB**

**Autoroute - Pre Route - Wirebonds** routes a chip's bond sites. Bond sites are placed based on your selection of padstacks. The autorouter completes the interconnection required by the netlist.

The AutoRoute Wirebonds dialog box contains the following:

[Filter](#) and a [Component list](#) specifies the reference designator of the target component.

[Filter](#) and a [Pads list](#) specifies the bond site padstack name.

**Maximum Length** sets the maximum length for the distance between the component pad and the bond site.

### Note

The [HYB](#) option is required for **Autoroute - Preroute - Wirebonds**.

## Autoroute - Pre Route - Bus Routing

### Routes component pins that share the same X or Y coordinates

**Autoroute - Pre Route - Bus Routing** uses a special algorithm that routes regular arrays of pins, such as those that interconnect memory devices. The autorouter determines which nets are candidates for bus routing, then routes these connections. Clearance rules must permit sufficient space to allow bus routing without conflicts.

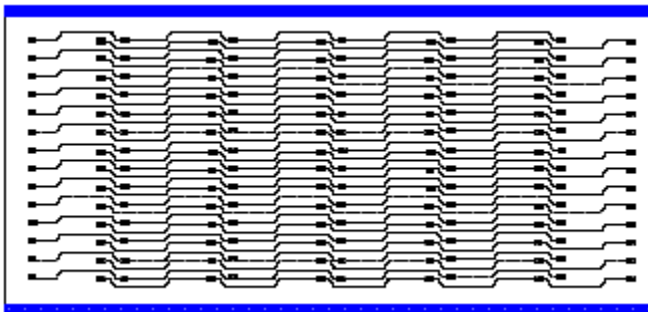
The AutoRoute Bus Routing dialog box contains the following:

**Diagonal routing** routes buses with a diagonal line. This option provides the highest routing density.

**Orthogonal routing** routes buses orthogonally.

**Protect bus routing when done** prevents the autorouter from ripping up and rerouting the bus routing.

The following is an example of bus routing with the **Diagonal routing** option.



## Autoroute - Route

### Routes the PCB design

Using **Autoroute - Route**, you can route in one of two ways. You can use Smart routing, which automatically routes and executes SPECCTRA commands based on evaluating your design, or you can use Basic routing, which simply runs routing passes. The default is Smart routing.

The AutoRoute dialog box contains the following options:

**Basic** runs routing passes. The options on the left side of the dialog box are used for this type of routing. They are not used if the Smart option is on. The options that apply to Basic routing are:

**Passes** sets the number of routing passes you want the autorouter to execute. The default is 25 routing passes.

**Start Pass** lets you set the pass number to where the autorouter left off in a previous session. If you do not supply a Start Pass number, the autorouter calculates a starting pass number based on the completion level of the routing. This influences the routing cost algorithm.

**Remove Mode** specifies that the autorouter create an unroutable rather than restore a wire to its original position if it tries to reroute the wire and cannot find a new path. This methodology is used only when the number of fails is greater than 100 and there are hundreds or thousands of conflicts over ten or more routing passes. This is executed automatically when the autorouter detects a poor completion rate and a high failure rate occurs over five passes.

**Smart** automatically routes your design and executes SPECCTRA commands based on evaluating your design. When you use the Smart option, SPECCTRA adjusts the autorouting based on the conflict reduction rate, the routing completion rate, the failure rate, and the number of layers. It applies bus routing, if necessary, and runs clean passes after the routing completes.

Smart routing is the default. The options on the right side of the dialog box are used for this type of routing. They are not used if the Basic option is on. The options that apply to Smart routing are:

**Minimum Via Grid** sets the minimum via grid. The default is the via grid set in the design file.

**Minimum Wire Grid** sets the minimum wire grid. The default is the wire grid set in the design file.

**Fanout if Appropriate** routes short escape wires from SMD pads to vias if there are more than two signal layers or if the top or bottom layer is not selected for routing. The default is on. The following options apply only if Fanout if Appropriate is on:

- **Via Sharing** controls whether the autorouter allows sharing vias between SMD pads on the same net. The default is on.
- **Pin Sharing** controls whether the autorouter can escape to through-pins. The autorouter will escape to a through-pin if the cost is lower than the cost to use a via. The default is on.

**Generate Testpoints** adds test points to routed signal nets. This option is executed when the routing is complete only if the **DFM** option is installed. The options you can specify

are:

**Side** specifies the probing layer where the testable via is exposed. The probing layer can be Front (TOP) , Back (BOTTOM), or Both sides. The default is Both.

**Use Grid** specifies the probing grid. The probing grid is the grid that matches your bed-of-nails tester.

**Miter After Route** changes 90 degree corners to 135 degree corners after all route, test point, and clean passes complete only if the **DFM** option is installed. If the routing does not converge, this option is not executed. The default is off.

## Notes

During the first five route passes, if you have not selected any connections, the autorouter tries to route all connections defined in the network, except those that are fixed or protected. After pass five, wires that are routed or rerouted are directly involved in conflicts, are close to wires involved in conflicts, or are connections that are not yet routed.

If you select any connections, the autorouter attempts only those connections.

In Basic routing, the autorouter performs route passes up to the number you specify unless the wiring completes with no crossing or clearance violations. If you have the FST license, the autorouter performs route passes up to the number you specify unless all wiring completes with no crossing, clearance, crosstalk, or maximum or minimum length rule violations.

## Autoroute - Clean

**Rips up and reroutes all connections to improve routing and manufacturability**

**Autoroute - Clean** removes unnecessary vias and bend points and improves SMD entries and exits. All connections are ripped up and rerouted with higher costs for via use, off-center SMD pad entry, and SMD pad side-exit.

Use **Autoroute - Clean** to get better quality routing and improve manufacturability.

The Clean dialog box contains the following:

**5** runs five clean passes. This is the default.

**Specify** runs the number of clean passes that you enter in the data entry box.

### Tip

Four clean passes are suggested after completing all routing passes.

### Note

When you use the Smart option in [Autoroute - Route](#), clean passes are performed automatically.

## Autoroute - Post Route

### **Performs postrouting operations**

The commands on the Autoroute - Post Route menu are

Critic

Filter Routing

Testpoints

Center Wires

Spread Wires

[Un]Miter Corners

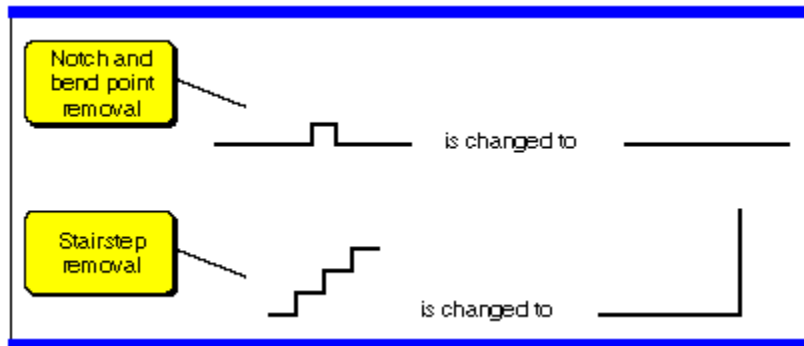


## Autoroute - Post Route - Critic

### Removes extra bends without performing rip-up and reroute operations

**Autoroute - Post Route - Critic** eliminates acute angles and removes extra bends. Critic is similar to **Autoroute - Clean** except that it does not rip up and reroute each wire and does not remove unnecessary vias. **Autoroute - Post Route - Critic** is faster than **Autoroute - Clean**, because it makes adjustments to the existing wires without ripping-up and rerouting. It can also improve pad and via entries and exits.

Below are examples of how **Autoroute - Post Route - Critic** can improve routing.



## Autoroute - Post Route - Filter Routing

### Removes routing conflicts

If a few conflicts remain after a large number of route and clean passes are completed, you might want to remove the conflicts and route the remaining connections in your layout system. You can use **Autoroute - Post Route - Filter Routing** to remove the conflicts and create unroutes.

When you specify more than one pass, each pass progressively increases the cost of routing conflicts. During the last filter pass, conflicts are prohibited and conflict-free routing is assured. The maximum (and default) number of filter passes is five.

The Filter Routing dialog box contains the following:

**5** runs five filter passes. This is the default.

**Specify** runs the number of filter passes that you enter in the data entry box. The maximum number that will run is five filter passes, even if you enter six or more in the data entry box.

### Note

See also [Edit - Delete Wires - Conflict Wires](#) and [Edit - Delete Wires - Conflict Wire Segments](#)

## Autoroute - Post Route - Testpoints

### Assigns test points to signal nets.

**Autoroute - Post Route - Testpoints** improves PCB testability by adding test points to routed signal nets. The perimeter of each component image is used as a boundary to restrict vias to locations outside the component bodies. Test points are through-pins, vias, or single layer shapes.

Testable vias are always exposed on the probing layer. Exposed means that the via is not covered by a component body. The probing layer can be front, back, or both.

The AutoRoute Testpoints dialog box contains the following:

**Side** specifies the probing layer where the testable via is exposed. The probing layer can be Front (TOP) , Back (BOTTOM), or Both Sides. The default is Both Sides.

**Grid** specifies the probing grid. The probing grid is the grid that matches your bed-of-nails tester.

**Center** controls the center-to-center distance between test points.

**Use Vias** specifies one or more via padstacks. If you do not specify a via, a via is selected from the current [via list](#). Single-layer padstacks can be used as test vias.

**Allow Pins** specifies the pins on particular components that can be used as test points. If you do not specify the components, all through-pins that satisfy the grid and center-to-center requirements can be used. When through-pins are allowed as test points, qualified pins are used to minimize the number of vias.

**By Component** specifies the components whose pins can be used as test points. You choose these components from the [Filter](#) or the [Components list](#).

**Component Outline Clearance** specifies how far test points are placed from components. This is the minimum required distance between the edge of the component outline and the edge of the test point.

### Tip

Use [Autoroute - Clean](#) after **Autoroute - Post Route - Testpoints** to remove unnecessary vias and eliminate improper tjunctions.

### Notes

**Autoroute - Post Route - Testpoints** is available only when the [DFM](#) option is installed.

Test points are not assigned to nets in a differential pair.

See also [Report - Testpoints](#).

## Autoroute - Post Route - Center Wires

**Moves single wire segments so that they are equidistant between adjacent pins of a component**

**Autoroute - Post Route - Center Wires** examines all wires that pass between adjacent pins of a component and positions these wire segments equidistant between the pins, if the following conditions are met.

- No new conflicts are introduced.
- Only a single wire segment lies between a pin pair (per layer).
- No new routing segments are required to achieve centering. Only a single segment move is permitted.
- No additional bends are added to wires.
- If a wiring grid is defined, wires are placed on the grid closest to the center line between the pins.

### Note

See also [Autoroute - Post Route - Spread Wires](#).

## Autoroute - Post Route - Spread Wires

### Adds extra space between wires, and between wires and pins

**Autoroute - Post Route - Spread Wires** adds extra wire-to-wire, wire-to-SMD pad, and wire-to-pin clearances to improve PCB manufacturability. Extra clearances are created by moving wires without moving or adding vias.

The Spread Wires dialog box uses two option buttons and several check boxes with accompanying data entry boxes to control where and how much extra clearance is attempted. The option buttons are

**General**, which indicates that all clearance types (wire-to-wire, wire-to-pin, wire-to-SMD) are attempted. Use the Starting and Ending data entry boxes to enter the extra clearance values you want the autorouter to attempt. See the following discussion for more information on how Starting and Ending clearance values are used.

**Specified**, which indicates that only the clearance types checked are attempted. The clearance types you can check are

**Wire to Wire**, which is the extra clearance between adjacent wires

**Wire to SMD**, which is the extra clearance between wires and SMD pads

**Wire to Pin**, which is the extra clearance between wires and through-pins

The General option, and each of the Specified clearance type check boxes, have corresponding Starting and Ending data entry boxes. The Starting data entry box is where you enter the initial extra clearance value that will be tried. If you do not enter a Starting extra clearance value, the default value is one-half the object-to-object clearance rules. If you do not enter a value in the Ending data entry box, only the Starting extra clearance value is attempted.

When you enter Starting and Ending values, the autorouter uses multiple passes and attempts to add extra clearances in progressively smaller increments. The Starting value is attempted in the first pass. Half the Starting value is attempted in the second pass, and in each subsequent pass, the previous value is halved and tried. When half of the previous value is equal to or less than the Ending value you entered, or when five passes are completed, the operation ends.

When you use Starting and Ending values, and you are using wiring grids, the grids should be smaller than the extra clearances you want to add. The **Autoroute - Post Route - Spread Wires** command does not change clearance rules. Extra clearance values apply only during the spread operation.

### Note

Use **Autoroute - Post Route - Spread Wires** after all route and clean passes and before you use **Autoroute - Post Route - Miter Corners**.

The **DFM** option is required for **Autoroute - Post Route - Spread Wires**.

## Autoroute - Post Route - [Un]Miter Corners

**Rounds or chamfers 90-degree wire corners, or removes 90-degree wire corners**

**Autoroute - Post Route - [Un]Miter Corners** chamfers 90-degree wire corners at 135 degrees or replaces them with arcs. When the miter style is set to diagonal, 90-degree corners are chamfered by using either specified setback values or the default setback values. This command is available only with the [DFM](#) option.

The [Un]Miter Corners dialog box contains the following:

**Miter** rounds or chamfers 90-degree corners with 135 degree corners or arcs, depending upon the Miter Options that you specify.

**UnMiter** changes 135-degree corners to 90-degree corners. Use this option if you want to make engineering changes to the design. The autorouter is more efficient when it is rerouting orthogonal wires. **UnMiter** does not remove round corners.

**Use layers** lets you pick the layers you want from the Layers [list](#). You pick a layer in the list by using the pointer, or by entering the layer name in the [Filter](#). Mitering or unmitering applies only to wires on the layers marked in the list.

### Miter Options

**Diagonal** chamfers 90-degree corners at 135-degrees. This is the default Miter Option.

**Rounded** fits an arc to 90-degree corners. (This requires that the [FST](#) option be installed.)

**Pin and Via Exits** permits chamfering of 90-degree corners at pin and via exits. The **Pin/Via Setback** is the distance from the pin and via exits corner to the point where the chamfer begins.

**Slant** permits a single chamfer to replace the two corners of a wrong-way segment. The **Slant Setback** is the distance from the corner to the point where the chamfer begins.

**T-Junctions** permits chamfering at tjunctions. The **T-junction Setback** is the distance from the corner to the point where the chamfer begins.

**Bend** permits chamfering at all 90-degree corners other than pin and via exits, slants, and tjunctions. The **Bend starting Setback** and **Bend ending Setback** set a range of values that are applied iteratively. When starting and ending setback values are used, the starting value is tried, and if at least one corner is chamfered, the same value is tried again iteratively until no additional corners are chamfered.

The Bend starting Setback value is then halved and chamfering is iteratively tried again until no corners are chamfered. The process of halving the previous setback value and iteratively trying to chamfer all remaining 90-degree corners continues, until either all corners are chamfered or the halved setback value is equal to or less than the Bend ending Setback value. When the halved setback value is less than Bend ending Setback, the actual ending value is used for the final iteration.

### Notes

This command is available if you have the [DFM](#) option.

The round miter feature can be used only when the [FST](#) option is installed.

## Autoplace - Setup

### Sets global placement rules and constraints

The Placement Setup dialog box defines PCB grid and spacing rules, sets the working origin and reference point for component alignments, and turns on or off the high speed and shove for move functions.

**PCB Placement Grid** sets a global placement grid for all components. The grid value you specify creates equidistant grid points in the X and Y directions. A grid value of 0 means the placement grid is undefined. You can override this grid spacing if you use [Rules - PCB - Placement Grids](#) to set separate placement grids for SMD and through-pin components.

**PCB Placement Spacing** sets a global spacing rule for all components. A spacing value of -1 means no global spacing rule is defined. You can override this spacing rule if you use [Rules - PCB - Spacing](#) to set separate spacing rules for SMD and through-pin components.

**Working Origin** determines the point on a component that the screen pointer points to during interactive operations. The default working origin is the component center. The options are

**Center**, which means the point at a component's center.

**Origin**, which means a component's origin defined in the design file.

**Align Reference** sets the reference point for component alignments. You can align components by component centers, by component origins, or by any one of four corner pin references. The default alignment reference is the upper left corner pin. The options are

**Upper Left Pin**

**Upper Right Pin**

**Lower Left Pin**

**Lower Right Pin**

**Center**

**Origin**

**High Speed** determines whether maximum and matched length routing rules are observed during automatic placement. If you have the SPECCTRA RouteFST license option and High Speed is turned on, SPECCTRA uses maximum or matched length routing rules to guide component placement. Components on nets assigned maximum or matched length rules are assigned high priorities to make sure wire length limits can be met during autorouting. High Speed is turned on by default.

**Shove for Move** determines whether SPECCTRA attempts to make space for a component you are relocating by shoving components out of the way. Shove for Move is turned off by default.

- When rule checking and Shove for Move are both on, you can move, pivot, or flip a component to a position that is already occupied by other components. SPECCTRA attempts to shove aside the components without causing a rule violation. If not enough space is available, the component you are trying to relocate is returned to its original position.
- When rule checking is turned off, Shove for Move has no effect.

## Autoplace - UnPlace Components

### Moves components outside the PCB boundary

Automatic placement applies only to components that are located completely outside the PCB boundary. If components you want to automatically place are located partially or completely within the boundary, you must first move them outside the boundary.

Before unplacing components, use [Lock Position mode](#) on the right button menu [Edit - \[Un\]Lock Components](#) to lock any components that you want to remain within the PCB boundary.

The commands on the AutoPlace - UnPlace Components menu are

[All](#)

[Small](#)

[Discrete](#)

[Capacitor](#)

[Selected](#)

[By List](#)



## Autoplace - UnPlace Components - All

### **Moves all components outside the PCB boundary**

**Autoplace - UnPlace Components - All** moves all unlocked components outside the PCB boundary. Components that are locked in position are not moved. Components that are located partially inside the PCB boundary are moved completely outside the boundary.

After you click **Autoplace - UnPlace Components - All** and if any of the components have attached wires, a message popup appears with the prompt

[Delete the Wires on the Picked Components and then Unplace?](#)

You can click Yes to delete the wires or click No to keep the wires. If you click No, SPECCTRA does not unplace the components.

### **Note**

Wires that have the fanout property need not be deleted. They can be unplaced or moved with the component.

## Autoplace - UnPlace Components - Small

### **Moves all small components outside the PCB boundary**

**Autoplace - UnPlace Components - Small** moves all unlocked small components outside the PCB boundary. Small components that are locked in position are not moved. Small components that are located partially inside the PCB boundary are moved completely outside the boundary.

SPECCTRA uses the number of component pins to differentiate large and small components. Small components have three pins or less. This command unplaces all small components including those assigned the capacitor property or the discrete property.

After you click **Autoplace - UnPlace Components - Small** and if any of the components have attached wires, a message popup appears with the prompt

[Delete the Wires on the Picked Components and then Unplace?](#)

You can click Yes to delete the wires or click No to keep the wires. If you click No, SPECCTRA does not unplace the components.

## Autoplace - UnPlace Components - Discrete

### Moves all discrete components outside the PCB boundary

**Autoplace - UnPlace Components - Discrete** moves all unlocked discrete components outside the PCB boundary. Discrete components that are locked in position are not moved. Discrete components that are located partially inside the PCB boundary are moved completely outside the boundary.

SPECCTRA uses the number of component pins to differentiate large and small components. Small components have three pins or less. Discrete components are small components assigned the discrete property either in the design file or in SPECCTRA.

After you click **Autoplace - UnPlace Components - Discrete** and if any of the components have attached wires, a message popup appears with the prompt

[Delete the Wires on the Picked Components and then Unplace?](#)

You can click Yes to delete the wires or click No to keep the wires. If you click No, SPECCTRA does not unplace the components.

### Note

Wires that have the fanout property need not be deleted. They can be unplaced or moved with the component.

## Autoplace - UnPlace Components - Capacitor

### Moves all capacitors outside the PCB boundary

**Autoplace - UnPlace Components - Capacitor** moves all unlocked capacitors outside the PCB boundary. Capacitors that are locked in position are not moved. Capacitors that are located partially inside the PCB boundary are moved completely outside the boundary.

SPECCTRA uses the number of component pins to differentiate large and small components. Small components have three pins or less. Capacitors are small components assigned the capacitor property either in the design file or in SPECCTRA.

A small component that does not have an assigned property type is treated as a capacitor if all its pins are connected to power nets. You can use [Define - Component Properties](#) to assign a small component with both pins attached to power nets as a small or discrete component type.

After you click **Autoplace - UnPlace Components - Capacitor** and if any of the capacitors have attached wires, a message popup appears with the prompt

[Delete the Wires on the Picked Components and then Unplace?](#)

You can click Yes to delete the wires or click No to keep the wires. If you click No, SPECCTRA does not unplace the components.

### Note

Wires that have the fanout property need not be deleted. They can be unplaced or moved with the component.

## Autoplace - UnPlace Components - Selected

### Moves selected components outside the PCB boundary

**Autoplace - UnPlace Components - Selected** moves selected unlocked components outside the PCB boundary. Components that are locked in position are not moved. Selected components that are located partially inside the PCB boundary are moved completely outside the boundary.

After you click **Autoplace - UnPlace Components - Selected** and if any of the components have attached wires, a message popup appears with the prompt

[Delete the Wires on the Picked Components and then Unplace?](#)

You can click Yes to delete the wires or click No to keep the wires. If you click No, SPECCTRA does not unplace the components.

### Note

Wires that have the fanout property need not be deleted. They can be unplaced or moved with the component.

## Autoplace - UnPlace Components - By List

### Moves all large components outside the PCB boundary

**Autoplace - UnPlace Components - By List** moves specified unlocked components outside the PCB boundary. Components that are locked in position are not moved. Components that are located partially inside the PCB boundary are moved completely outside the boundary.

The [Un]Place Components dialog box contains a Filter data entry box and a Components list that you use to choose the components you want to unplace.

After you click OK or Apply in the [Un]Place Components dialog box and if any of the components have attached wires, a message popup appears with the prompt

**Delete the Wires on the Picked Components and then Unplace?**

You can click Yes to delete the wires or click No to keep the wires. If you click No, SPECCTRA does not unplace the components.

### Note

Wires that have the fanout property need not be deleted. They can be unplaced or moved with the component.

## Autoplace - Cluster Components

### Automatically groups components into clusters

**Autoplace - Cluster Components** automatically groups components into floor plan type [clusters](#). The Cluster Components dialog box allows you to group components into clusters by specifying signal nets or power nets. You can also let SPECCTRA group all large components into clusters based on component connectivity.

The Cluster Components dialog box contains the following

#### Cluster by

**Signal (All)**, which means group all components into one or more clusters based on their connectivity. This is the default Cluster by option.

**Signal (Specify)**, which means group all components connected to the specified signal nets into one or more clusters.

**Power (Specify)**, which means group all components connected to the specified power nets into one or more clusters.

[Filter](#) and [Signal Nets list](#), which specifies the net names of signal nets.

[Filter](#) and [Power Nets list](#), which specifies the net names of power nets.

SPECCTRA automatically assigns names to the clusters. You can use [Report - Clusters](#) to generate a report containing the assigned cluster names.

## Autoplace - InitPlace Large Components

### Automatically places large components

**Autoplace - InitPlace Large Components** automatically places large components. Large components with the highest connectivity are placed first. SPECCTRA considers a component to be large if it has more than three pins. Only components that are completely outside the PCB boundary are placed.

The InitPlace Large Components dialog box allows you to place all large components, all selected large components, or a specified number of the most highly connected large components. The InitPlace Large Components dialog box contains the following:

#### Components

**All** means place all large components that are outside the PCB boundary.

**Selected** means place only the selected components.

**# Most Highly Connected** means place the specified number of large components. SPECCTRA chooses the most highly connected components that are outside the PCB boundary.

**Preferences** sets preferences for spacing, alignments, grids, sides, and orientations. You can set separate grid, side, and orientation preferences for SMD and PTH (through-pin) components. You can also set separate orientation preferences for the front and back sides of the PCB.

**Placement Spacing** sets the preferred component spacing. The preferred spacing is ignored if it is smaller than the current permitted spacing rules.

**Align Components** controls whether SPECCTRA makes minor adjustments at the end of the initplace operation, including the alignment, spread, and rotation of adjacent components.

**Small Components on Same Side**, if on, leaves room for small components on the side of the PCB where large components are placed. The default is off.

**SMD Grid** and **PTH Grid** set the preferred placement grids for SMD and PTH components. The PTH grid must be a multiple of the SMD grid. The preferred grids are ignored if they are not multiples of the current SMD and PTH placement grid rules.

**Side** is the preferred side for component placement. The default side for SMD components is No Preference. The default preferred side for PTH components is Front Only. The preferred sides are ignored if they are not permitted by the current permitted side rules. The choices are

**Front Only**, which means place components only on the front side of the PCB.

**Back Only**, which means place components only on the back side of the PCB.

**Front First**, which means place components on the front side of the PCB if possible; otherwise, place them on the back side.

**Back First**, which means place components on the back side of the PCB if possible; otherwise, place them on the front side.

**No Preference**, which means place components on the front or back sides of the PCB without a priority for either side.

**Orientation** is the preferred orientation for component rotations during placement. The default orientation is 0 degrees for SMD and PTH components on the front and back sides of



the PCB. The preferred orientations are ignored if they are not permitted by the current permitted orientation rules.

SPECCTRA uses the orientation defined for a component in the design file as the reference. The component footprints are analyzed to determine the correct orientations:

- If a component has more pins in a horizontal array than in any vertical array, the component is horizontal.
- If a component has more pins in a vertical array than in any horizontal array, the component is vertical.

If the largest horizontal and vertical arrays have the same number of pins, a component's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the component's orientation is unspecified.

The Orientation choices are

**Horizontal**, which means align components horizontally.

**Vertical**, which means align components vertically.

**Degree**, which means rotate components to one or more preferred angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Notes

SPECCTRA places large components in order of connectivity, starting with the most highly connected component.

Automatic placement applies only to components that are located completely outside the PCB boundary. If components you want to automatically place are located partially within the boundary, you must first move them outside the boundary.

Placement preferences are not rules. Preferences are ignored if they conflict with any applicable placement rules defined in SPECCTRA or in the design file. For example, the preferred spacing might be ignored for some components because it is smaller than the permitted spacing rule assigned to those components or their images.

## Autoplace - Interchange Components

### Automatically interchanges component locations to improve routability

**Autoplace - Interchange Components** improves routability by reducing Manhattan lengths. SPECCTRA measures the weighted length of a component's connections, and begins exchanging it through an iterative process with each component that is not locked in position. The weighted length is re-measured after each exchange to find the minimum value. This operation results in an overall reduction of Manhattan lengths.

The Interchange Components dialog box allows you to interchange all components or just components with specified property types by turning on one or more of the following check boxes:

**All**, which means interchange all components.

**Large**, which means interchange components with more than three pins.

**Small**, which means interchange components with three pins or less, including components assigned the discrete or capacitor properties.

**Discrete**, which means interchange small components assigned the discrete property.

**Capacitor**, which means interchange small components assigned the capacitor property.

You can also specify the number of interchange passes, display exchanges, and align components.

**Passes** is the number of times you want SPECCTRA to perform the iterative process of exchanging each component with each other component.

**Display Exchange** repaints the work area after each component interchange. Turn off this check box to improve performance.

**Align Components** controls whether SPECCTRA makes minor adjustments at the end of the interchange operation, including the alignment, spread, and rotation of adjacent components.

**Align Components** controls whether SPECCTRA makes minor adjustments at the end of the initplace operation, including the alignment, spread, and rotation of adjacent components.

### Notes

SPECCTRA interchanges only those components that are inside the PCB boundary.

Component interchange is sometimes referred to as "pairwise interchange" because only two components are exchanged one at a time. The goal is to place interconnected components as close as possible to reduce weighted Manhattan lengths.

A reduction in weighted Manhattan lengths depends on how components are placed before the interchange. Multiple interchange passes usually produce the best results. Use eight or more passes. When a pass doesn't result in a reduction of weighted Manhattan lengths compared to the previous pass, SPECCTRA terminates the interchange.

## Autoplace - InitPlace Small Components

### **Automatically places small components**

The commands on the Autoplace - InitPlace Small Components menu are

All

Discretes

Capacitors

## Autoplace - InitPlace Small Components - All

### Automatically places small components

**Autoplace - InitPlace Small Components - All** automatically places all small components, including those assigned the capacitor or discrete property. SPECCTRA considers a component to be small if it has three pins or less. Only components that are completely outside the PCB boundary are placed.

The InitPlace All Small Components dialog box allows you to place all small components or all selected small components. This dialog box contains the following:

**Preferences** sets preferences for spacing, placement under SMD pads, component alignments, power net priorities, grids, sides, and orientations. You can set separate grid, side, and orientation preferences for SMD and PTH (through-pin) components. You can also set separate orientation preferences for the front and back sides of the PCB.

**Placement Spacing** sets the preferred component spacing. The preferred spacing is ignored if it is smaller than the current permitted spacing rules.

**Under SMD Pads** controls whether small components can be placed directly beneath the pins of SMD components on the opposite side of the PCB.

**Align Components** controls whether SPECCTRA makes minor adjustments at the end of the initplace operation, including the alignment, spread, and rotation of adjacent components.

**Higher Priority Nets** turns on or turns off a priority for placing components with connections to the specified power nets before placing other components. Use the [Filter](#) data entry box or the [Nets list](#) to choose the priority nets.

**SMD Grid** and **PTH Grid** set the preferred placement grids for SMD and PTH components. The PTH grid must be a multiple of the SMD grid. The preferred grids are ignored if they are not multiples of the current SMD and PTH placement and site grid rules.

**Side** is the preferred side for component placement. The default side for SMD components is No Preference. The default preferred side for PTH components is Front Only. The preferred sides are ignored if they are not permitted by the current permitted side rules. The choices are

**Front Only**, which means place components only on the front side of the PCB.

**Back Only**, which means place components only on the back side of the PCB.

**Front First**, which means place components on the front side of the PCB if possible; otherwise, place them on the back side.

**Back First**, which means place components on the back side of the PCB if possible; otherwise, place them on the front side.

**No Preference**, which means place components on the front or back sides of the PCB without a priority for either side.

**Orientation** is the preferred orientation for component rotations during placement. The default orientation is 0 degrees for SMD and PTH components on the front and back sides of the PCB. The preferred orientations are ignored if they are not permitted by the current permitted orientation rules.

SPECCTRA uses the orientation defined for a component in the design file as the reference. The component footprints are analyzed to determine the correct orientations:

- If a component has more pins in a horizontal array than in any vertical array, the component is horizontal.
- If a component has more pins in a vertical array than in any horizontal array, the component is vertical.

If the largest horizontal and vertical arrays have the same number of pins, a component's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the component's orientation is unspecified.

The Orientation choices are

**Horizontal**, which means align components horizontally.

**Vertical**, which means align components vertically.

**Degree**, which means rotate components to one or more preferred angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Notes

Automatic placement applies only to components that are located completely outside the PCB boundary. If components you want to automatically place are located partially within the boundary, you must first move them outside the boundary.

Placement preferences are not rules. Preferences are ignored if they conflict with any applicable placement rules defined in SPECCTRA or in the design file. For example, the preferred spacing might be ignored for some components because it is smaller than the permitted spacing rule assigned to those components or their images.

## Autoplace - InitPlace Small Components - Discretes

### Automatically places discrete components

**Autoplace - InitPlace Small Components - Discretes** automatically places components assigned the discrete property in the design file or in SPECCTRA. Only components that are completely outside the PCB boundary are placed.

The InitPlace Discrete Components dialog box allows you to place all discrete components or all selected discrete components. This dialog box contains the following:

**Preferences** sets preferences for spacing, placement under SMD pads, component alignments, power net priorities, grids, sides, and orientations. You can set separate grid, side, and orientation preferences for SMD and PTH (through-pin) components. You can also set separate orientation preferences for the front and back sides of the PCB.

**Placement Spacing** sets the preferred component spacing. The preferred spacing is ignored if it is smaller than the current permitted spacing rules.

**Under SMD Pads** controls whether discrete components can be placed directly beneath the pins of SMD components on the opposite of the PCB.

**Align Components** controls whether SPECCTRA makes minor adjustments at the end of the initplace operation, including the alignment, spread, and rotation of adjacent components.

**Higher Priority Nets** turns on or turns off a priority for placing components with connections to the specified power nets before placing other components. Use the [Filter](#) data entry box or the [Nets list](#) to choose the priority nets.

**SMD Grid** and **PTH Grid** set the preferred placement grids for SMD and PTH components. The PTH grid must be a multiple of the SMD grid. The preferred grids are ignored if they are not multiples of the current SMD and PTH placement and site grid rules.

**Side** is the preferred side for component placement. The default side for SMD components is No Preference. The default preferred side for PTH components is Front Only. The preferred sides are ignored if they are not permitted by the current permitted side rules. The choices are

**Front Only**, which means place components only on the front side of the PCB.

**Back Only**, which means place components only on the back side of the PCB.

**Front First**, which means place components on the front side of the PCB if possible; otherwise, place them on the back side.

**Back First**, which means place components on the back side of the PCB if possible; otherwise, place them on the front side.

**No Preference**, which means place components on the front or back sides of the PCB without a priority for either side.

**Orientation** is the preferred orientation for component rotations during placement. The default orientation is 0 degrees for SMD and PTH components on the front and back sides of the PCB. The preferred orientations are ignored if they are not permitted by the current permitted orientation rules.

SPECCTRA uses the orientation defined for a component in the design file as the reference. The component footprints are analyzed to determine the correct orientations:

- If a component has more pins in a horizontal array than in any vertical array, the

component is horizontal.

- If a component has more pins in a vertical array than in any horizontal array, the component is vertical.

If the largest horizontal and vertical arrays have the same number of pins, a component's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the component's orientation is unspecified.

The Orientation choices are

**Horizontal**, which means align components horizontally.

**Vertical**, which means align components vertically.

**Degree**, which means rotate components to one or more preferred angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Notes

Automatic placement applies only to components that are located completely outside the PCB boundary. If components you want to automatically place are located partially within the boundary, you must first move them outside the boundary.

Placement preferences are not rules. Preferences are ignored if they conflict with any applicable placement rules defined in SPECCTRA or in the design file. For example, the preferred spacing might be ignored for some components because it is smaller than the permitted spacing rule assigned to those components or their images.

## Autoplace - InitPlace Small Components - Capacitors

**Autoplace - InitPlace Small Components - Capacitors** automatically places components assigned the capacitor property in the design file or in SPECCTRA. A small component that does not have an assigned property type is treated as a capacitor if all its pins are connected to power nets. Only capacitors that are completely outside the PCB boundary are placed.

The InitPlace Capacitor Components dialog box allows you to place all capacitors or all selected capacitors. This dialog box contains the following:

**Preferences** sets preferences for spacing, placement under SMD pads, component alignments, power net priorities, grids, sides, and orientations. You can set separate grid, side, and orientation preferences for SMD and PTH (through-pin) components. You can also set separate orientation preferences for the front and back sides of the PCB.

**Placement Spacing** sets the preferred component spacing. The preferred spacing is ignored if it is smaller than the current permitted spacing rules.

**Under SMD Pads** places decoupling capacitors directly beneath the pins of SMD components on the opposite side of the PCB. A small component is treated as a decoupling capacitor if it is assigned the capacitor property or all pins are connected to a power net.

**Align Components** controls whether SPECCTRA makes minor adjustments at the end of the initplace operation, including the alignment, spread, and rotation of adjacent components.

**Higher Priority Nets** turns on or turns off a priority for placing components with connections to the specified power nets before placing other components. Use the [Filter](#) data entry box or the [Nets list](#) to choose the priority nets.

**SMD Grid** and **PTH Grid** set the preferred placement grids for SMD and PTH components. The PTH grid must be a multiple of the SMD grid. The preferred grids are ignored if they are not multiples of the current SMD and PTH placement grid rules.

**Side** is the preferred side for component placement. The default side for SMD components is No Preference. The default preferred side for PTH components is Front Only. The preferred sides are ignored if they are not permitted by the current permitted side rules. The choices are

**Front Only** places components only on the front side of the PCB.

**Back Only** places components only on the back side of the PCB.

**Front First** places components on the front side of the PCB if possible; otherwise, places them on the back side.

**Back First** places components on the back side of the PCB if possible; otherwise, places them on the front side.

**No Preference** places components on the front or back sides of the PCB without a priority for either side.

**Orientation** is the preferred orientation for component rotations during placement. The default orientation is 0 degrees for SMD and PTH components on the front and back sides of the PCB. The preferred orientations are ignored if they are not permitted by the current permitted orientation rules.

SPECCTRA uses the orientation defined for a component in the design file as the reference. The component footprints are analyzed to determine the correct orientations:



- If a component has more pins in a horizontal array than in any vertical array, the component is horizontal.
- If a component has more pins in a vertical array than in any horizontal array, the component is vertical.

If the largest horizontal and vertical arrays have the same number of pins, a component's orientation is determined by its horizontal and vertical lengths. If the lengths are equal, the component's orientation is unspecified.

The Orientation choices are

**Horizontal**, which means align components horizontally.

**Vertical**, which means align components vertically.

**Degree**, which means rotate components to one or more preferred angles: 0 degrees, 90 degrees, 180 degrees, or 270 degrees.

### Notes

Automatic placement applies only to components that are located completely outside the PCB boundary. If components you want to automatically place are located partially within the boundary, you must first move them outside the boundary.

Placement preferences are not rules. Preferences are ignored if they conflict with any applicable placement rules defined in SPECCTRA or in the design file. For example, the preferred spacing might be ignored for some components because it is smaller than the permitted spacing rule assigned to those components or their images.

## Autoplace - Auto Rotate Components

### Automatically rotates placed components

**Autoplace - Auto Rotate Components** rotates placed components to improve routability by reducing Manhattan lengths and minimizing guide crossings. Current component directions are maintained.

The Automatic Rotate dialog box controls the types of components that SPECCTRA rotates.

You can rotate all components or just components with specified property types by turning on one or more of the following check boxes:

**All** rotates all components.

**Large** rotates components with more than three pins.

**Small** rotates components with three pins or less, including components assigned the discrete or capacitor properties.

**Discrete** rotates components assigned the discrete property.

**Capacitor** rotates components assigned the capacitor property.

## Autoplace - Automatic Swap

### Automatically swaps gates, subgates, pins, and terminators

**Autoplace - Automatic Swap** exchanges nets between functionally equivalent gates, subgates, pins, and terminators to improve routability by reducing circuit congestion, Manhattan lengths, and the number of vias required for routing.

The Automatic Swap dialog box allows you to choose the object types you want to swap and to specify the number of passes for each type. The choices are

**Swap Terminators**, which means swap gates that contain [terminators](#) and have swap codes in the design file.

**Swap Pins**, which means swap pins within gates or subgates that have swap codes in the design file.

**Swap Subgates**, which means swap [subgates](#) that have swap codes in the design file.

**Swap Gates**, which means swap [gates](#) that have swap codes in the design file.

**Passes** is the number of times you want to repeat a swap operation and attempt to reduce Manhattan lengths. SPECCTRA continues swapping until it has performed the specified number of passes or until the Manhattan lengths cannot be reduced. The default number of passes for each object type is 1.

You can select the instances of the objects (gate, subgate, pin, or terminator) you want to swap. SPECCTRA swaps only the selected instances. If you select only two instances of an object, SPECCTRA performs a swap even if it increases the Manhattan lengths.

### Notes

The necessary package swap information must be translated from your layout system libraries and included with the component definitions in the SPECCTRA design file. Swap data generated by SPECCTRA is saved when you generate a session file. Swap data must be translated and returned to your layout system for back annotation of gate and pin swaps.

SPECCTRA swaps only unlocked gates, subgates, pins, or terminators of those components that are inside the PCB boundary. If only two swappable objects are selected when you initiate automatic swap, the two objects are immediately swapped without considering Manhattan length improvements.

For best results, specify multiple passes. Considering typical time versus improvement ratios, start with 2 to 4 passes.

Most components do not have subgates. If subgates are not defined, subgate swapping has no effect.

## Autoplace - Small Comp Pattern

### **Interactively places small components in patterns near large components**

First you use interactive placement tools to create a pattern of one or more small components, such as decoupling capacitors, about a single large component. Use **Autoplace - Small Comp Pattern - Learn** to define the pattern. Then, you select one or more other large components, and apply the pattern to them using **Autoplace - Small Comp Pattern - Apply to Selected**.

The commands on the **Autoplace - Small Comp Pattern** menu are

[Learn](#)

[Apply to Selected](#)

## Autoplace - Small Comp Pattern - Learn

### **Defines a small component pattern relative to a large component**

**Autoplace - Small Comp Pattern - Learn** creates a placement pattern of one large component and one or more small components. Use this command when you want to place many small components, such as decoupling capacitors, in identical patterns. Each pattern must include a single large component, such as an integrated circuit.

Before using this command, you must define the pattern by arranging small components about a large component. The large component does not have to be inside the PCB boundary.

Use [Autoplace - Small Comp Pattern - Apply to Selected](#) to place other small components in identical patterns about other selected large components. The large components must all have the same image ID and identical image and component properties.

### **To create a small component pattern for interactive placement**

1. Select a small component, and move it to a position next to or under a large component.
2. Repeat step 1 with other small components until the pattern is complete.
3. Select both the large component and the small components.
4. Click **Autoplace - Small Comp Pattern - Learn**.
5. Unselect all components.

## Autoplace - Small Comp Pattern - Apply to Selected

**Places small components in identical patterns about selected large components**

**Autoplace - Small Comp Pattern - Apply to Selected** places small components in a defined pattern about selected large components. Use this command when you want to place many components, such as decoupling capacitors, in identical patterns about many large components.

Before using this command, you must define the pattern using [Autoplace - Small Comp Pattern - Learn](#).

When you apply the pattern, SPECCTRA automatically chooses and places small components that have the same image ID and the same image and component properties as the corresponding small components used to define the pattern.

The large components you select must be located inside the PCB boundary, and they must have the same image ID and the same image and component properties as the large component used to define the pattern.

### **To apply a small component pattern to selected large components**

1. Select the large components with which you want to place small components in the defined pattern.
2. Click **Autoplace - Small Comp Pattern - Apply to Selected**.

## Autoplace - Crossing Histogram

### Turns on and off the crossing histogram

The crossing histogram uses a bar graph to represent relative crossing congestion across the PCB. The graphs along the bottom and right side edges of the PCB boundary indicate areas of crossing congestion by the lengths of the bars. Each bar represents an invisible cut-line that extends across the PCB.

The graph along the bottom of the PCB represents crossing cuts that intersect the vertical cut-lines. The graph along the right edge of the PCB represents crossing cuts that intersect the horizontal cut-lines.

Smooth histogram curves indicate an even distribution of connections across the PCB. Large peaks indicate extremely congested areas that you should correct if possible.

**Autoplace - Crossing Histogram** acts like a switch. You use it to display the crossing histogram, and you can use it again to remove the crossing histogram display from the screen.

## Autoplace - Density Analysis

### **Turns on and off the density map display for density analysis**

The density map graphically shows circuit congestion by overlaying the PCB with an array of colored cells. SPECCTRA computes and automatically sizes the cells based on component size and number.

SPECCTRA uses colors to represent the relative congestion of a cell. A color index displayed below the PCB shows the colors used to represent the highest and lowest degrees of congestion. The default cell colors are red, yellow, and green.

- Red indicates the cell is highly congested.
- Yellow indicates a cell is moderately congested.
- Green indicates a cell is lightly congested.

These colors might be different on your system if you have changed your color map file.

SPECCTRA determines congestion by calculating wire channel demand based on the Manhattan tree. Wire channel supply is based on the total number of signal layers and the projected number of required vias.

**Autoplace - Density Analysis** acts like a switch. You use it to display the density map, and you can use it again to remove the density map display from the screen.



## Report Menu

### **Creates text files (reports) about the PCB design**

You view reports about the PCB design in a report window. SPECCTRA creates a temporary file for the report in your temporary directory.

The commands on the Report menu are

[Classes](#)

[Component](#)

[Conflicts](#)

[Corners](#)

[Crosstalk](#)

[Design](#)

[File](#)

[Groups](#)

[Keepouts](#)

[Length](#)

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[Network](#)

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## Report Menu

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The commands on the Report menu are

[Associations](#)

[Clusters](#)

[Component](#)

[Conflicts](#)

[Design](#)

[Families](#)

[File](#)

[Interchanges](#)

[Images](#)

[Keepouts](#)

[Net](#)

[Network](#)

[Padstacks](#)

[Placement](#)

[Place Lengths](#)

[Place Status](#)

[Rooms](#)

[Route Status](#)

[Rules](#)

[Swaps](#)

### Note

You can save a report by using the **report** keyboard command. See the SPECCTRA Reference manual for information about the **report** command.

## Report - Classes

### **Creates a report on all defined classes**

The class report lists all defined [classes](#) and the nets contained in each class.

To see the rules that apply to each class, use [Report - Rules](#).

## Report - Component

### Creates a report on a single component in the design

The Report Component dialog box contains a [Filter](#) and [Component list](#), which you use to choose the component.

The component report lists placement data about the specified component, along with position and net information for each component pin. The report can also contain floor plan information. The items included in the report are described below.

Component information consists of the following:

**Placed on** reports the layer on which the component is placed.

**Component Rotation** reports the degrees of rotation (counterclockwise) from the working origin.

**Location (X,Y)** reports the location of the origin of the component.

**Part Image** reports the library image name that defines the component.

**Component Type** reports the type of component as large, small, capacitor, or discrete.

**Component Property** reports the physical and electrical properties assigned to the component.

**Placement Rule** reports the spacing, permitted orientation, permitted layers, and opposite side rules, if they are assigned.

Pin information consists of the following:

**Pin** reports the component's physical pin numbers.

**Padstack** reports the library padstack names that define each pin.

**X** reports the X-coordinates of each pin.

**Y** reports the Y-coordinates of each pin.

**Z** reports the layer numbers on which each pin has a pad or contact point.

**Rotate** reports the rotation of each padstack in degrees relative to the origin of the padstack.

**Wires** reports the number of two-pin connections in which each pin appears.

**Net** reports the name of the net connected to each pin.

## Report - Conflicts

### Creates a report about the current conflicts in the design

The autorouter checks all routed wires and displays a conflict shape in the graphics display area. A diamond shape represents a crossover conflict. A rectangular shape represents a clearance conflict.



The conflict report lists the coordinates of all current crossover and clearance conflicts. Clearance violations list the minimum clearance rule. The report also lists the aperture width for each shape.

Fixed and protected wires are treated as keepouts during the checking process.

#### Note

This report lists only routing conflicts and rule violations. For a report of placement rule violations, change to Placement Mode before clicking **Report - Conflicts**.

## Report - Corners

### **Creates a report on the number of corners and their angles**

The corners report summarizes the status of all routed corners in the design. This report lists corners that are 90 and 135 degree angles, arcs, and other angles.

After executing recorner or miter commands, this report identifies how many 90 degree corners remain.

## Report - Crosstalk

### **Creates a report on parallel and tandem crosstalk violations**

The crosstalk report lists the instances of parallel and tandem rule violations. The report contains a list of rules in effect, indicates rule violations, and lists the amount of overlap. The nets, the pin-to-pin connections, the signal layer, and the locations of the violations are also listed.

Crosstalk violations listed in the report are marked graphically by a white box between offending wire segments. The long side of the box runs the length of the rule violated.

#### **Note**

This command is available with the [FST](#) option.

## Report - Design

### **Displays the current design file**

The *Design Language Reference* manual describes the syntax used in the design file.



## Report - File

### Displays a text file in the report window

You can use **Report - File** to look at text files without exiting SPECCTRA. Some types of files you might want to view by using this command are:

- Design
- Do
- Wires
- Routes
- Placement
- Floor Plan
- Network
- Conflicts
- Padstacks
- Corners
- Session

### Note

Using **Report - File** you can look at any text file, even a file that is unrelated to SPECCTRA.

## Report - Groups

### **Creates a report on fromto groups in the design**

The group report lists all defined [groups](#) of fromtos. Data is listed by group and includes group names, net names, and pin-to-pin connections.

To see a list of the rules assigned to each group, use [Report - Rules](#).

## Report - Keepouts

### Creates a report about all defined keepout areas

A [keepout](#) is an area used to prevent routing or placement in specific areas of the PCB design. You can define a keepout by using the [Define - Keepout](#) command.

The keepouts report lists all keepouts and the following information about each keepout area:

- **Keepout Type**, which are listed in the table below
- **Shape Type**, which is Rectangle or Polygon
- **Layers**, which are the layer(s) that the keepout is on
- **Coordinate List**, which are the coordinates that define the keepout area
- **Keepout ID**, which is the name assigned to the keepout area

Keepout Type	Prohibits these objects
Keepout	wires, vias, and components
Wire Keepout	wires
Bend Keepout	wire bends
Via Keepout	vias
Place Keepout	components

## Report - Length

### Creates a report about nets that have length and delay rules assigned

The length and delay report lists rules and violations for the following:

- maximum lengths
- minimum lengths
- match lengths
- maximum delays
- minimum delays
- match delays

The report lists all nets that have length or delay rules, the current values of these rules, the actual routed length or timing delay of the net, the total violations, and an error message for each net or fromto violating the rules. Length and delay rules are assigned with the Timing commands on the Rules menu.

#### Note

This report command is available only with the [FST](#) license. When the FST license is available, the autorouter reroutes connections to eliminate length violations.

## Report - Net

### Creates a report about a specified net

The net report provides a detailed description of a net. The items included in the report are described below.

**Net name** reports whether the net is fixed or wires are protected. The report includes the classes the net is assigned to, the number of pins, vias, wires, and tjunctions, and data on Manhattan versus routed lengths.

**Rules In Effect** reports pcb, class, and net width and clearance rules; net ordering; tjunction rule status; bend, crossing, and via limits; and the net's routing priority.

**Layer Rules In Effect** reports the layer rules that override the net rules currently in effect for this net. They are listed by layer. The wire width and all object-to-object clearance rules are listed for each signal layer.

**Fromto Rules In Effect** lists fromtos in the following form and includes any corresponding fromto rules in effect:

<component\_id> - <pin\_id> <component\_id> - <pin\_id>

**Network** section consists of six columns:

- **Place** lists the reference designators of components in the net.
- **Pin** lists all pins and vias in the net.
- **Padstack** lists the padstack for each pin.
- **X** lists the X-coordinate of the pin.
- **Y** lists the Y-coordinate of the pin.
- **Layer** lists each layer on which the pin can be connected (the layers on which a pad has been defined for the pin).

**Connections** reports the routed length for the net and marks fixed or protected fromtos as \*PROTECTED\*.

**Routing** lists the routed wire paths and vias used for the net.

## Report - Network

### **Creates a report about the selected nets or all nets in the design**

**Report - Network** sorts the netlist by name, length, ratio, or extra and writes statistics about each net. The Report Network dialog box contains the following:

**Name** sorts the information about the nets alphabetically according to the net name.

**Length** sorts the information about the nets from the highest to lowest length rule.

**Ratio** sorts the information about the nets from the highest to the lowest ratio of the actual routed length divided by the Manhattan length.

**Extra** sorts the information about the nets from the highest to the lowest difference between the actual routed length and the Manhattan distance.

**Window** displays the report in a new window.

**File** places the report information in a file that you specify in the data entry box.

The type of sort is identified in the report by changing the Name, Length, Actual, Ratio, or Extra column heading to all uppercase letters. Single-pin nets are included in the report. The fields in the report are described below.

**Name** reports the net names in the network file.

**Pins** reports the number of component pins in the net.

**Vias** reports the number of vias used to route the net.

**Wires** reports the number of two-point connections in the net.

**TJ** reports the number of tjunctions used in the net.

**Length** reports the calculated Manhattan length required to route the net based on the number of two-point connections.

**Actual** reports the actual length of routed connections.

**Ratio** reports the actual routed length divided by the Manhattan length.

**Extra** reports the difference between the actual routed length and the Manhattan distance.

## Report - Padstacks

**Creates a report about all padstacks in the design.**

The padstack report lists the via, pin, and SMD padstacks from the library section of the design file. Definitions of padstack properties syntax are listed in the *Design Language Reference* manual.

To see a list of the rules assigned to a padstack, use [Report - Rules](#).

## Report - Pairs

### **Creates a report about all differential pairs**

The pairs report lists each net in the differential pairs and the [pair gap](#). If a pair gap is not specified for a differential pair, SPECCTRA uses the wire to wire clearance rule and the report states

[No Pair Gap Specified](#)

You can define a differential pair by using [Define - Net Pair](#).

### **Note**

Differential pair operations are available only when the [FST](#) option is installed.

## Report - Pins Without Fanout Vias

### **Creates a report of all pins without escape wires and vias**

You can use this report to determine whether pins failed the fanout operation. After you use [Autoroute - Pre Route - Fanout](#), use this report to determine whether pins are blocked or cannot escape due to rule settings.

The report lists the net name, X,Y location, and padstack id for each component pin that lacks a fanout wire and via. The report contains the following information:

**PIN REFERENCE** is a reference designator, pin number combination.

**NET NAME** is the net id used in the design file.

**X** is the X coordinate location of the pin.

**Y** is the Y coordinate location of the pin.

**PADSTACK** is the padstack id for the pin.

### **Note**

Through-pins are included in the report only if an expose property is attached to them. You assign the expose property by using [Define - Pin Attributes](#).



## Report - Place Status

### Creates a report that contains a placement summary and PCB statistics

The placement status report contains a summary of placement commands, placement conflicts (violations), number of components placed, Manhattan lengths, and CPU time. The fields in the place status report are described in the following example.

Report Field	Description
#SPECCTRA Version V6.0 made 95/09/16 at 14:41:57	Identifies the SPECCTRA version number, build date and time.
#Host <id_number>	The CPU hostid.
#PLACEMENT STATUS <<< design.dsn >>>	The design filename.
Start Time: Thu Sep 15 04:43:35 1995 Report Time: Thu Sep 15 04:45:15 1995	The start time indicates when the autorouter was started. The report time indicates when the report was generated.
#PLACEMENT HISTORY	
Action	
Command	Indicates the placement command that was executed.
Times	The number of command passes.
Conflicts	The number of placement violations that resulted from the command action.
Placed	The number of components placed or processed by the command action.
Manhattan (<unit>)	The total Manhattan lengths for all connections expressed in <unit>.
CPU Time	
Pass	The CPU time to complete the command action (hr:min:sec).
Total	The accumulative CPU time.
# Overall Placement Time: 0:4:16	The overall placement time for the session.
#PLACEMENT STATISTICS	

Components = <number>

The total number of components in the design.

Placed = <number>

The total number of components placed.

Not Placed = <number>

The total number of components that could not be placed.

Completion = <percentage>

The percentage of the total number of components placed.

Manhattan length = <number> <unit>

The total Manhattan lengths for all connections on the PCB, expressed in <unit>.

#### **Note**

The default report filename is plc\_stat.rpt.

## Report - Regions

### Creates a report about defined regions

A [region](#) is an area of the design where you can assign a specific width or clearance rule. You can define a region by using [Define - Region](#).

The regions report states the number of defined regions and contains the following information under each region ID.

**Shape** is the net id used in the design file.

**Layer ID** is the layer id used in the design file.

**X1** and **Y1** is the X,Y coordinate of one corner of the region.

**X2** and **Y2** is the X,Y coordinate of the opposite corner of the region.

To see a list of the rules assigned to a region, use [Report - Rules](#).

### Notes

Region operations are available only when the [FST](#) option is installed.

See also [Rules - Region](#).

## Report - Route Status

### Creates a report that contains a routing summary and PCB statistics

The routing status report contains a summary of routing pass statistics. The status report will vary according to the options you have available. Examples of the fields in the report are described below.

#### Report Field

#SPECCTRA Version V6.0 made  
95/09/20 at 16:38:39

#Host 54697

#ROUTING STATUS <<< design >>>

Start Time: Thu Sep 21 04:43:35 1995

Report Time: Thu Sep 21 04:45:15 1995

Nets = 28    Connections = 44

Current Wire = 46    Reroute wires  
= 64

Completion = 56.82%  
Unconnections = 0

#### #ROUTING HISTORY:

Pass

Name

No

#### Description

This identifies the SPECCTRA version number and the version date and time.

The CPU hostid.

This is the name of the design file.

The start time indicates when the autorouter was started. The report time indicates when the report was generated.

The number of nets and the number of two-pin connections in the entire design.

The current or last wire routed and the total number of wires to be routed is indicated. This information is relevant only for a particular routing pass.

The completion percentage is:

$$(1 - ((\text{unconnections} + \text{wires in conflicts}) / \text{connections})) \times 100$$

Unconnections are two-pin connections that are not routed.

Identifies the type of pass completed.

The number of the pass

completed. Note that miter, bus, seedvia, critic, and delete operations do not increase the pass counter.

## Conflicts

Cross

The number of crossing conflicts.

Clear

The number of clearance rule violations.

Fail

The number of connections the router could not rip-up and reroute with a new path during this routing pass. Ripped up wires are returned to their previous position unless the -remove switch is used with the route command.

Unrte

The number of unconnections at the end of the pass.

Vias

The number of vias used.

Xtalk

The number of crosstalk rule violations.

Len.

The number of maximum and minimum length rule violations.

Red%

The percentage of reduction in conflicts from the previous pass.

CPU Time

Pass

The CPU time for the pass (hr:min:sec).

Total

The accumulative CPU time.

# Overall Routing Time: 0:0:16

The overall routing time for the session.

## #WIRING STATISTICS

PCB Area = 1.620 EIC = 5  
Area/EIC = 0.324

PCB Area is the PCB routing area. EIC is Equivalent Integrated Circuits (14-pin devices). This number is computed by dividing the total number of pins by 14. Area/EIC is derived from the PCB area divided by the number of equivalent ICs.

Components = 4 SMDs = 4

The total number of components and the total number of surface-mounted devices.

Signal Layers = 2 Power Layers = 1

The number of signal layers and the number of power layers.

Wire Junctions = 1, at vias = 0 Total Vias = 36

Wire tjunctions are identified separately from tjunctions at vias. The total number of vias is also identified in this line.

Conflicts=18 Crossovers=18, Clearances=0, Xtalk=0, Length=0

This line breaks down the number of conflicts into crossovers, clearances, xtalk, and length.

Manhattan length = 23.400 Horizontal = 13.150 Vertical = 10.250

Total Manhattan length for the design is displayed and is further broken down into the horizontal and vertical components of the total Manhattan length. This information is valuable for determining the necessary layer directions.

Routed length = 30.651 Horizontal = 17.655 Vertical= 12.996

The total routed length is listed and broken down into its horizontal and vertical components.

Ratio Actual / Manhattan= 1.3099

The ratio of the actual wire length to the calculated Manhattan length.

Unconnected length = 0.000 Horizontal = 0.000 Vertical = 0.000

If there are any unroutes, the sum of their Manhattan lengths are listed.

The following is an example of the summary statistics.

Layer	Direct	Pins	Vias	TJs	Conflicts	Length	Horizontal	Vertical
s1	Horz	38	36	1	14	18.011	12.205	5.806
s2	Vert	32	36	0	4	12.640	5.450	7.190

Summary statistics are listed by layer in the following table.

Report Field	Description
Layer	Routing layer name
Direct	Layer biasing (direction)
Pins	Number of component pins on the layer

Vias	Number of vias on the layer
TJs	Number of tjunctions at wires on the layer
Conflicts	Number of conflicts on the layer
Length	Total routed length on the layer
Horizontal	Horizontal routed length on the layer
Vertical	Vertical routed length on the layer

## Report - Rules

### **Creates a report on the current routing design rules**

The rules report contains all the current rules (default) or specific types of rules, which you specify in the Report Rules dialog box. It also contains the name of the design file, the number of signal and power layers, and the size of the via and wire grids. The Report Rules dialog box contains the following:

**All** lists all current design rules.

**Specify** lists specific design rules according to what you choose below:

**PCB Rules**

**Layer Rules**

**Class Rules**

**Net Rules**

**Group Rules**

**Fromto Rules**

**Class-Class Rules**

**Padstack Rules**

**Region Rules**

These rules are listed according to their precedence in the [SPECCTRA rules hierarchy](#). PCB rules have the lowest precedence. Region rules have the highest.

### Notes

Clearance rules are listed separately for each object to object setting.

The [FST](#) option is required in order to apply class to class, padstack, and region rules.

## Report - Testpoints

### Creates a report on test vias and through-pins in the design

After you assign test points by using [Autoroute - Post Route - Testpoints](#), you can use **Report -Testpoints** to create a report that contains the test point status for each net in the design. Test points can be through-hole component pins and vias.

The test point report contains the measurement units used in the design and the following:

**Summary**, which states the number of nets that do not have test points, the number of test points on each side of the PCB (front and back), the size of the test point grid, and the current test point spacing and clearance rules.

**Nets With No Testpoints**, which lists the nets that are not assigned test points.

**Testpoints on the Back/Front Side**, which lists the following for each test point:

**X and Y**, which is the X,Y coordinate of the test point

**TYPE**, which is the test point type (pin or via)

**NET**, which is the name of the net that is assigned the test point

**LAYER**, which is the layer that the test point is on

**Padstack**, which is the padstack name

**PIN/VIA**, which is the pin or via name

### Note

This command is available only with the [DFM](#) option.



## Report - Unconnects

**Creates a report about the connections that are not wired in the design**

This report lists all unconnected fromtos by net name. It includes the reference designator, pin number, and coordinate location for each pin in the fromto.

## Report - Vias

### **Creates a report about vias defined in the design**

The via report lists all vias defined in your design file. It includes the following information for each via:

- The layers on which the via can reside
- Whether the via is selected for routing
- The bounding box dimension (outline) for the via
- The padstack shapes on each layer that define each via

## Report - Associations

### **Creates a report on all defined component associations**

The association report lists all defined component associations between one large component and one or more small components. Each row of the report lists a large component and the small components with which it is associated. Components are identified by their component labels (reference designators).

The default filename is assoc.rpt

See also [Define - Associate Components](#)

## Report - Clusters

### **Creates a report on all defined component clusters**

The placement cluster report contains the total number of defined clusters and lists the following information about each cluster:

**Cluster**, which is the name assigned to the cluster.

**Component members**, which are all the components that make up the cluster.

**Type**, which is the cluster type. It can be floor\_plan, super\_component, piggy\_back, or super\_component piggy\_back type of cluster.

Super and super piggyback cluster types also include

**Relative locations**, which are the X,Y distances of each component relative to the origin of the super cluster. The origin of the super cluster is determined by the names of the components. If you list the components in a super cluster in alphanumeric order, the origin of the first component on the list is the origin of the super cluster.

The default filename is cluster.rpt

See also [Define - Cluster](#)

## Report - Conflicts

### **Creates a report on the current placement rule violations**

The conflicts report lists components that violate placement rules. You can list all components that violate placement rules, or you can select certain components and list only those components that violate placement rules. The conflicts report also includes a summary of placement violations and warnings.

#### **Note**

This report lists only placement rule violations. For a report of routing conflicts and rule violations, change to Routing Mode before clicking [Report - Conflicts](#).

## Report - Families

### **Creates a report about all image families in the design.**

The families report lists the images and family-to-family spacing rules assigned to each selected image family (if families are selected) or to each image family in the design. The images in a family are assigned the family image property with the family ID assigned to that family.

The default filename is family.rpt

## Report - Interchanges

### **Creates a report on component interchanges**

The interchange report lists all components interchanged during the last interchange command. An interchange involves two components, which are listed with old and new X,Y locations and rotations. The Old (before interchange) and New (after interchange) listings consist of

**Origin**, which is the X,Y location of the component origin

**Side**, which is either the front or back surface of the PCB

**Rotation**, which is the counterclockwise rotation of the component with respect to the design file image.

The interchange report also includes a summary of total Manhattan lengths as a result of each series of interchange passes. See also [Autoplace - Interchange Components](#)

The default filename is interchg.rpt

## Report - Images

### Creates a report on images

The Report Image dialog box contains a [Filter](#) and [Image list](#), which you use to choose the image.

The images report lists the following information:

**Image Properties** reports the image type property. It also reports whether the image is an SMD or PTH, and the sides (front, back, or both) where the image is placed.

**Placement Rule** reports the current placement rules that apply to the image.

**Component are instantiated from the image** lists all component instances of the image.

**Image Outline** reports the coordinates of the image outline.

**Image Pins** lists the pin padstacks used in the images, and includes the X, Y coordinate of the padstack and the rotation angle.

The default filename is image.rpt



## Report - Placement

### **Creates a report on component locations and other component information**

The placement report lists X,Y locations and other information for all components, or if you select certain components, it lists information for only those components. The component placement information is organized in several columns that are labeled

**Ref Des**, which is the component reference designator.

**X,Y**, which is the X and Y coordinate location of the component's origin.

**Side**, which is the front or back surface of the PCB on which the component is mounted.

**Rotate**, which is the component's counter clockwise angle of rotation with respect to the design file image.

**Pins**, which is the total number of the component's pins.

**Wires**, which is the number of connections attached to the component.

**Length**, which is the total of the Manhattan lengths for all connections attached to the component.

**Avg. Length**, which is the Length value divided by the Wires value.

## Report - Place Lengths

### Creates a length and delay rules report

The place lengths report lists all maximum, minimum, and match length rules, with warnings, and all nets that have assigned length rules, with the evaluated total net lengths and warnings for potential violations.

This report lists the length and delay rules of placed components by net, class, and group. Each net, class, and group listing includes

**Fromto Name** or **Net Name**, which is either the reference designator and pin number ([fromto](#)), or net names for the net, class, or group.

**Target Len**, which is the target Manhattan length that is based on the current placement.

**Toler**, which is the length tolerance for the net, class, or group.

**Range**, which is two values computed from actual net or fromto lengths and the tolerance.

**LF**, which is the length factor that is set by layer. If the length\_factor routing rule is not set, this field indicates N for none.

**Status**, which indicates OK when the Manhattan length or delay of a net or fromto complies with applicable length or delay rules.

When the Status field indicates \*NOTICE\*, the Manhattan length or delay of a net or fromto might not comply with applicable length or delay rules.

When the Status field indicates "ERROR", the Manhattan length or delay of a net or fromto is longer than the current length or delay rule. SPECCTRA indicates the net or fromto with a dashed line.

Matched length and matched delay listings include

**Total Len** or **Total Delay**, which is the Manhattan lengths or delays of a net or fromto expressed in either length or time units.

**Pair Avg**, which indicates N/A if the net is not a member of a differential pair. When the net is a member of a differential pair, this field indicates the average length of the net pair.

Maximum and minimum length rule and maximum and minimum delay rule listings include

**Max Len** or **Max Delay**, which is the maximum length or delay of a net or fromto expressed in either length or time units.

**Min Len** or **Min Delay**, which is the minimum length or delay of a net or fromto expressed in either length or time units.

**Total Len** or **Total Delay**, which is the actual Manhattan lengths or delays of the net or fromto expressed in either length or time units.

The default filename is plc\_len.rpt

### Note

The [FST](#) option is required to apply length and delay rules.

## Report - Rooms

### **Creates a report on all rooms defined in the design**

The rooms report lists all contents, spacing, permitted orientation, permitted layer, and opposite side rules for each room defined in the design. Each room listing includes

**Layer**, which identifies the sides (front, back, or both) of the room.

Room spacing rules are listed for front and back sides of the PCB as

**Pin\_Pin**, which is the room spacing rule between through-pin components.

**Pin\_SMD**, which is the room spacing rule between through-pin and SMD components.

**Pin\_Area**, which is the room spacing rule between through-pin components and keepout areas and the PCB boundary.

**SMD\_SMD**, which is the room spacing rule between SMD components.

**SMD\_Area**, which is the room spacing rule between SMD components and keepout areas and the PCB boundary.

**Area\_Area**, which is the room spacing rule between keepout areas.

Each room listing also includes

**Permitted Orientations**, which lists permitted orientations for components placed within the room on the front and back sides of the PCB.

**Permitted Layers**, which lists whether components can be placed within the room on front, back, or both sides of the PCB.

**Opposite Side**, which lists whether components placed within the room on the front side can be above components placed on the back side of the PCB.

The default filename is room.rpt

See also [Define - Room](#), [Rules - Room - All Components](#), and [Rules - Room - Contents](#)

## Report - Rules

### **Creates a report on the current placement design rules**

The rules report lists all current PCB level (global) spacing, permitted orientation, permitted layer, and opposite side rules. The report includes the following:

**PCB Placement Rule**, which are the spacing rules listed for front and back sides of the PCB. The information includes the following:

**Pin\_Pin**, which is the room spacing rule between through-pin components.

**Pin\_SMD**, which is the room spacing rule between through-pin and SMD components.

**Pin\_Area**, which is the room spacing rule between through-pin components and keepout areas and the PCB boundary.

**SMD\_SMD**, which is the room spacing rule between SMD components.

**SMD\_Area**, which is the room spacing rule between SMD components and keepout areas and the PCB boundary.

**Area\_Area**, which is the room spacing rule between keepout areas.

**Permitted Orientations**, which lists permitted orientations for components placed on the front and back sides of the PCB.

**Permitted Layers**, which lists whether components can be placed on front, back, or both sides of the PCB.

**Opposite Side**, which lists whether components placed on the front side can be above components placed on the back side of the PCB.

## Report - Swaps

### **Creates a report of gate, subgate, pin, and terminator swaps**

The swap report lists a history of all gate, subgate, pin, and terminator swaps that are performed in the current session. The total Manhattan length improvement is recorded for each series of gate, subgate, pin, or terminator swap operations. Each individual swap is also recorded, which includes its contribution to total Manhattan length improvement.

You read across the report, by row, to determine which gates, subgates, and pins have been swapped and the resulting improvement.

The default filename is swap.rpt

## Help Menu

**Provides information about routing procedures, example do files, and menu commands**

The Help menu commands are

[General Information](#)

[Autorouting Overview](#)

[Automatic Routing](#)

[Interactive Routing](#)

[Do File Examples](#)

[Menu Commands](#)

[Glossary](#)

[Point & Click](#)

[License Usage](#)

[About SPECCTRA](#)

For help learning how to use SPECCTRA, click a subject in the Help menu. For help in the main SPECCTRA window, choose **Help - Point & Click**, and click on an icon, a button, or a text label in the window.

### Notes

You can also access menu command help by clicking the Help button in a dialog box or by using the [Help] key on your keyboard. (Use the [F1] key if your keyboard does not have a [Help] key.)

For help on menubar commands, you can also drag the pointer to a command in a menu, and press the [Help] or [F1] key. For help on icons, buttons, or text labels in the main SPECCTRA window, you can also use the [Tab] and arrow keys to move the keyboard focus to the area of interest, and press the [Help] or [F1] key.

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## Help - General Information

### **Explains how to do general SPECCTRA tasks**

This help file provides information on the SPECCTRA graphical user interface (GUI), and explains how to perform various viewing and basic operations, such as measuring, highlighting, selecting, and saving information.



## Help - Autorouting Overview

### **Explains basic routing commands and methods you use to autoroute a PCB design**

This help file explains how the autorouter works and how to use a basic command file or the **smart\_route** command to achieve the best autorouting results. It also provides a methodology that you can use to autoroute a variety of printed circuit board designs. This help file contains the following five sections, each of which explains important concepts that are needed to use the autorouter effectively:

- How the autorouter works
- Controlling the autorouter
- Monitoring routing progress
- Identifying problems and correcting them
- Finishing the routing

## Help - Automatic Routing

### **Explains how to use keyboard commands to route your design automatically**

This help file provides information on what commands to add to a do file in order to meet design, high-speed, and manufacturing requirements. It also contains information about setting up the routing environment and controlling routing methodology.

## Help - Interactive Routing

### **Explains how to use EditRoute to route your design interactively**

EditRoute is the Cooper & Chyan Technology Shape-Based tool for interactively routing printed circuit board connections. This help file provides information on how to interactively edit and route a PCB design.

## Help - Placement

### **Explains how to place components interactively and automatically**

This help file provides information on how to interactively and automatically place components in a PCB design. It explains how to set up the placement environment and set rules, how to perform basic placement procedures, how to design and use a floor plan, and how to meet electrical, thermal, mechanical, and manufacturing requirements.

## Help - Do File Examples

### **Provides examples of do files**

These do file examples illustrate how you can automate such tasks as setting rules, placing components, and controlling how the autorouter routes nets. The do file examples are

- Class rules
- Layer rules
- Manufacturing postprocessing
- Segment-to-segment crosstalk control
- Coupled-noise crosstalk control
- Differential pairs and ground shielding
- Minimum and maximum length control
- Rules for specific regions
- Component placement control

## Help - Menu Commands

### **Provides information about SPECCTRA menu commands and dialog boxes**

This help file describes each command in the menu bar menus and on the interactive right mouse button menus. It also describes each dialog box that appears when you click on a command.

If you click the Help button in a dialog box, this help file opens and information about the dialog box appears.

## Help - Glossary

### **Provides definitions of terms used in SPECCTRA**

This help file provides an alphabetical listing of terms and acronyms used in SPECCTRA.

## Help - Point & Click

### **Sets the left mouse button to point and click help mode**

When you click **Help - Point & Click**, the pointer changes to a finger (on UNIX systems) or an arrow with a question mark (on Windows and Windows NT systems).

Move the pointer to the work area, to a menu name in the menu bar, to an icon in the window frame, or to a button or text label in the status area below the work area, and click the left mouse button to view information describing that part of the window.



## Help - License Usage

### **Displays a list of the available SPECCTRA licenses**

All SPECCTRA products and options are licensed, and licensing is controlled through a password or license file. The Help - License Usage command provides the following information:

- The host ID of the machine where SPECCTRA is running
- The name of the password or license file
- The kinds of available licenses
- The number of licenses in use
- The current license users

## Help - About SPECCTRA

**Displays information about the SPECCTRA product and when the current session started**

The Product Information includes

- Version number
- The date and time this version of SPECCTRA was created
- Copyright information
- Date and time your SPECCTRA session started



*Window Point and Click section*

## **Title Bar**

Contains the SPECCTRA version number and the design file name. The complete path to the design file appears with the filename.

## menu bar

Contains commands in pull down menus. Each of these menus contains commands that perform an operation, pull down a cascade menu, or open a dialog box.

### **To choose a menu command**

1. Move the pointer to the menu bar and click on a menu name.
2. When the menu appears, click a command name.

If a cascade menu appears, repeat step 2 until you choose a command that performs an operation or opens a dialog box.

## scroll bars

Used to pan the work area view left, right, up, and down. The horizontal scroll bar pans left and right. The vertical scroll bar pans up and down. Each scroll bar consists of two arrow buttons, a slider, and a trough through which the slider moves.

Use the arrow buttons to pan in small increments. Click on an arrow to pan one step in the direction of the arrow, or press and hold [LB] on an arrow to continually pan in increments.

Use the sliders or troughs to quickly pan the work area view. When you drag a slider, the work area view pans in the same direction that you move the slider. Click in a trough to pan a screen at a time.

If the entire design is displayed in the work area, no troughs appear in the scroll bars and panning is disabled.

## tool bar

The tool bar contains icons that initiate frequently used commands. SPECCTRA provides different tool bars for routing and placement.

For information about a particular icon, click **Help - Point & Click** and click the icon.



## work area

The area where the printed circuit board is displayed and routed. The work area is where you can zoom in and zoom out, and can pan the design.

## To zoom in

### To zoom in

1. Move the pointer to the lower left corner of the region you want to magnify.
2. Drag the middle mouse button in an upward direction to enclose the region. A bounding rectangle shows the zoom region. Before you release the middle mouse button, you can move the pointer and adjust the rectangle to enclose the exact region you want to magnify.
3. Release the middle mouse button.

### See also

[To zoom out](#)

[To pan](#)

## To zoom out

### To zoom out

1. Move the pointer to any location in the work area.
2. Drag the middle mouse button diagonally, in an downward direction. You will see two rectangles. An inner rectangle represents the current view. It's surrounded by an outer rectangle that changes size as you drag the pointer.

The relative size of the outer rectangle to the inner rectangle indicates how far you zoom out when you release the middle mouse button. For example, if you adjust the size of the outer rectangle so that it is about twice the size of the inner rectangle, you zoom out by a factor of about two to one.

3. Release the middle mouse button.

### See also

[To zoom in](#)

[To pan](#)

## To pan

### **To pan the work area**

1. Move the pointer to any location where you want as the new view center.
2. Click the middle mouse button.

### **See also**

[To zoom in](#)

[To zoom out](#)

## status bar

The status bar contains the Checking check box and current status information. Checking indicates whether design rule checking is turned on or off. Click this check box button to turn on or turn off check mode.

The status information changes depends on which environment you are using.

### See also

[Autorouting status bar](#)

[Interactive routing status bar](#)

[Placement status bar](#)

## Check

Checking indicates whether design rule checking is turned on or off. Click this check box to turn on or turn off rule checking for interactive routing or placement.

## **Autorouting status**

Status bar information includes the number of passes completed, unroutes, and conflicts. It also displays the percent of routes completed.

### **See also**

[Interactive routing status bar](#)

[Placement status bar](#)

## Interactive routing status

In the interactive router, the current net name of the wire you are editing replaces the number of passes completed. In addition, the Conflicts count is dimmed if you move wires. Click **Rules - Check Rules** to update the number of conflicts.

### See also

[Autorouting status bar](#)

[Placement status bar](#)



## Placement status

In placement, the status bar displays information such as the ratio of placed components to all components, the number of selected components, the number of locked components, and the number of placement violations. In interactive modes, when you move, pivot, flip, or trade components, the status bar displays the component reference designator (Ref) and the change in Manhattan length. When you pivot a component, the status bar also displays the change in rotation (DR).

### See also

[Autorouting status bar](#)

[Interactive routing status bar](#)

## **command entry area**

The area where commands appear when you type them on the keyboard. A thick border appears around this area when it is active. If the command entry area is not active, you must click in the area before typing a command.

## control area

Used to monitor SPECCTRA operating status and to control or interrupt a command. The following messages and buttons appear in the control area.

What appears	What it mean
Idle	SPECCTRA is waiting for you to take some action, such as entering a command, clicking a menu item, or measuring
Busy	SPECCTRA is performing an operation that you cannot interrupt
Msg...	A message dialog box is waiting for your input
Pause	Click this button to pause an operation
Continue and Stop	When you pause an operation, you can click the Continue button to continue the operation or click the Stop button to stop the operation.

## mode status area

Displays the current left mouse button mode.

## **coordinate readout area**

Displays the X and Y coordinates as you move the pointer in the work area. In Measure mode, a point-to-point distance appears beside the delta symbol if you drag the pointer in the work area.

## **unit selector button**

Indicates the unit of measurement. You can click this button to display a popup menu, and choose a different measurement unit.

## **message area**

Displays warnings, error messages, prompts, and information about current operations.

## Placed

Shows the ratio of placed components to all components.

## **Selected**

Shows number of components that are currently selected.



## Locked

Shows number of components that are currently locked.

## Violation

Shows number of current placement violations.

*Tool Bar Icon section*

## Repaint

Refreshes the work area of the SPECCTRA window

## **View all**

Displays the entire design in the work area of the SPECCTRA window

## Layer panel

This tool bar icon displays the Layer panel, which controls layer visibility, selection for routing, and routing direction. The Layer panel can remain on the screen while you perform routing or placement operations.

## **Route status report**

Creates a report that contains a routing summary and PCB statistics

## Placement status report

Creates a report that contains a placement summary and PCB statistics



## Measure mode

Sets the left mouse button mode to measure mode. You can use the left mouse button to measure the distance between two points or extract information about routing objects and design rule violations. SPECCTRA displays the information in the output window.

*Highlighting section*

## Shielded wires

You can choose either wires with shields or wires missing shields

**Wires with shields** include GND shields and tie-in vias.

**Wires missing shields** are wires that are supposed to be shielded but the autorouter did not shield them because it could not find space for the shield.

You cannot assign a shield to a wire that is shorter than the **min\_shield** rule.

## Wire bends

Wires that have either 45 degree or 90 degree bends.

## SMD pads without fanouts

All SMD signal pads that the autorouter attempted and failed to fan out during the most recent **fanout** command.

## **Nets without testpoints**

All nets that do not have testpoints.

## Incomplete wires

Incomplete wiring includes

- Pin-to-pin connections that have a missing segment (the other segments are highlighted)
- Segments that tee into a pin-to-pin connection but that end in mid-air or at a guide wire
- Segments that start at a pin and end in mid-air (not including segments that end at vias, which are presumed to be fanouts or testpoints)
- Dangling wires left after use **delete conflicts -remove**.

## **Redundant wires**

Extra wire segments and vias on power nets.



## **Last loads of nets**

Component pins which were the last on a net to be assigned a load property.

## Off grid

Wires, vias, components, pin (not including unused pins), or all objects that are not aligned on the appropriate grid.

*Unroutes section*

## All

Displays the guides for all signal net connections in the design.

## Placed

Displays the guides for signal net connections to components placed inside the PCB boundary.

## Last

Displays the guides for signal net connections to the last automatically placed component.

## Front

Displays the guides for signal net connections to components placed on the front side of the PCB.

## **Back**

Displays the guides for signal net connections to components placed on the back side of the PCB.



## Between

Displays the guides for signal net connections between components placed on the front and back sides of the PCB.

## **Selected**

Displays the guides for signal net connections to all selected components.

## Highlighted

Displays the guides for signal net connections to all highlighted components.

*Placement Setup section*

## PCB placement grid

PCB Placement Grid sets a global minimum placement grid for all components. This grid applies to both SMD and through-pin components. A value of -1 means the grid is undefined.

## PCB placement spacing

PCB placement spacing sets a global minimum permitted spacing rule. This rule applies to all spacing combinations between SMD components, through-pin components, and keepout areas. A value of -1 means the rule is undefined.

## Shove for move

Shove for Move helps you interactively move, pivot, or flip components into densely packed areas of the design.

When Shove for Move and rule checking are turned on, SPECCTRA attempts to shove aside previously placed components to make room for the component you are trying to relocate. If space is available and no rules are violated, SPECCTRA relocates the component. Otherwise, SPECCTRA returns the component to its original position. If rule checking is turned off, Shove for Move has no effect. Shove for move is turned on by default.

When Shove for Move is turned off, SPECCTRA does not attempt to shove aside components.

## Align reference

Sets the reference point used for interactively aligning components. The options are the

- the component center
- the component origin
- one of the four component corner pins (upper left, upper right, lower left, or lower right)

The default align reference point is the pin at the upper left corner of the component.

### Note

Alignment by pin reference uses the origin of the specified pin. If different components have different locations for their pin origins, alignment by pin reference can produce unexpected results.



## Working origin

The working origin is the point on a component that the pointer attaches to during interactive operations. The default working origin is the center of the component. You can change the working origin to the component origin.

## High speed

When High Speed is turned on, SPECCTRA observes high speed routing rules during automatic placement operations. When High Speed is turned off, SPECCTRA does not observe high speed routing rules. By default, High Speed is turned on.

*Interactive modes section*

## Select component mode

### To set [LB] to select or unselect components

Do one of the following:

- Click **Select - Components - Sel Comp Mode**
- Click the Select Component mode icon in the tool bar
- Press [RB] and choose **Select - Comp Mode**

You can select or unselect individual components by clicking them. To select or unselect several adjacent components, drag the pointer to define a rectangular area. SPECCTRA selects or unselects components that are totally or partially within the area.

SPECCTRA highlights selected components with the select color (yellow in the default color map), and displays their component labels. All pins, wires, and guides attached to selected components are also selected.

## Select net mode

### To set [LB] to select or unselect nets

Do one of the following:

- Click **Select - Nets - Sel Net Mode**
- Click the Select Net mode icon in the tool bar
- Press [RB] and choose **Select - Net Mode**

You can select or unselect individual [nets](#) by clicking them. To select or unselect several adjacent nets, drag the pointer to define a rectangular area. SPECCTRA selects or unselects nets that are totally or partially within the area.

SPECCTRA highlights selected nets with the select color (yellow in the default color map). All pins, wires, and guides attached to selected nets are also selected.

## Select wire mode

### To set [LB] to select or unselect wires

Do one of the following:

- Click **Select - Wires - Sel Wire Mode**
- Click the Select Wire mode icon in the tool bar
- Press [RB] and choose **Select - Wire Mode**

You can select or unselect individual wires by clicking them. To select or unselect several adjacent wires, drag the pointer to define a rectangular area. SPECCTRA selects or unselects wires that are totally or partially within the area.

SPECCTRA highlights selected wires with the select color (yellow in the default color map). All pins, vias, and guides attached to selected wires are also selected.

## Select guide mode

### To set [LB] to select or unselect guides

Do one of the following:

- Click **Select - Guides - Sel Guide Mode**
- Click the Select Guide mode icon in the tool bar
- Press [RB] and choose **Select - Guide Mode**

You can select or unselect individual guides by clicking them. To select or unselect several adjacent guides, drag the pointer to define a rectangular area. SPECCTRA selects or unselects guides that are totally or partially within the area.

SPECCTRA highlights selected guides with the select color (yellow in the default color map).

## Select image mode

### To set [LB] to select or unselect images

- Click **Select - Images - Sel Image Mode**

You can select or unselect all instances of individual images by clicking them. To select or unselect several adjacent images, drag the pointer to define a rectangular area. SPECCTRA selects or unselects images that are totally or partially within the area.

SPECCTRA selects all instances of the images, highlights all instances of selected images with the select color (yellow in the default color map), and displays their component labels. All pins, wires, and guides attached to selected images are also selected.



## Select room mode

### To set [LB] to select or unselect rooms

- Click **Select - Rooms - Sel Room Mode**

You can select or unselect individual rooms by clicking anywhere within their boundaries. To select or unselect several adjacent rooms, drag the pointer to define a rectangular area. SPECCTRA selects or unselects rooms that are totally or partially within the area.

SPECCTRA highlights the boundaries of selected rooms with the select color (yellow in the default color map).

## Lock position mode

Sets the left mouse button to lock and unlock components at their current positions

### To set this mode, you can

- Click the Lock Position mode icon in the tool bar
- Click **Edit - [Un]Lock Components Mode**

### Note

This mode locks or unlocks only a component's position. Use **Edit [Un] Lock Components** if you want to lock or unlock gates, subgates, or pins.

## Select gate mode

### To set [LB] to select or unselect gates

Do one of the following:

- Click **Select - Gates - Sel Gate Mode**
- Press [RB] and choose **Select - Gate Mode**

You can select or unselect individual [gates](#) by clicking them. To select or unselect several adjacent gates, drag the pointer to define a rectangular area. SPECCTRA selects or unselects gates that are totally or partially within the area.

SPECCTRA highlights the pins of selected gates with the select color (yellow in the default color map). All wires and guides attached to selected gates are also selected.

## Select equivalent gate mode

### To set [LB] to select or unselect equivalent gates

- Click **Select - Gates - Eq Sel Gate Mode**

You can select or unselect individual [gates](#) and their equivalents by clicking them. To select or unselect several adjacent gates, drag the pointer to define a rectangular area. SPECCTRA selects or unselects gates that are totally or partially within the area, and their equivalents anywhere in the design.

SPECCTRA highlights the pins of selected equivalent gates with the select color (yellow in the default color map). All wires and guides attached to selected gates are also selected.

## Select subgate mode

### To set [LB] to select or unselect subgates

Do one of the following:

- Click **Select - Subgates - Sel Subgate Mode**
- Press [RB] and choose **Select - Subgate Mode**

You can select or unselect individual subgates by clicking them. To select or unselect several adjacent subgates, drag the pointer to define a rectangular area. SPECCTRA selects or unselects subgates that are totally or partially within the area.

SPECCTRA highlights the pins of selected subgates with the select color (yellow in the default color map). All wires and guides attached to selected subgates are also selected.

## Select equivalent subgate mode

### To set [LB] to select or unselect equivalent subgates

- Click **Select - Subgates - Eq - Sel Subgate Mode**

You can select or unselect individual [subgates](#) and their equivalents by clicking them. To select or unselect several adjacent subgates, drag the pointer to define a rectangular area. SPECCTRA selects or unselects subgates that are totally or partially within the area, and their equivalents anywhere in the design.

SPECCTRA highlights the pins of selected equivalent subgates with the select color (yellow in the default color map). All wires and guides attached to selected subgates are also selected.

## Select pin mode

### To set [LB] to select or unselect pins

Do one of the following:

- Click **Select - Pins - Sel Pin Mode**
- Press [RB] and choose **Select - Pin Mode**

You can select or unselect individual pins by clicking them. To select or unselect several adjacent pins, drag the pointer to define a rectangular area. SPECCTRA selects or unselects pins that are totally or partially within the area.

SPECCTRA highlights selected pins with the select color (yellow in the default color map). All wires and guides attached to selected pins are also selected.

## Select equivalent pin mode

### To set [LB] to select or unselect equivalent pins

- Click **Select - Pins - Sel Eq Pin Mode**

You can select or unselect individual pins and their equivalents by clicking them. To select or unselect several adjacent pins, drag the pointer to define a rectangular area. SPECCTRA selects or unselects pins that are totally or partially within the area, and their equivalents anywhere in the design.

SPECCTRA highlights selected equivalent pins with the select color (yellow in the default color map). All wires and guides attached to selected pins are also selected.



## Select terminator mode

### To set [LB] to select or unselect terminators

Do one of the following:

- Click **Select - Terminators - Sel Terminator Mode**
- Press [RB] and choose **Select - Terminator Mode**

### To set [LB] to select or unselect terminator pins

- Click **Select - Terminators - Sel Terminator Mode**

You can select or unselect individual [terminators](#) by clicking them. To select or unselect several adjacent terminators, drag the pointer to define a rectangular area. SPECCTRA selects or unselects terminators that are totally or partially within the area.

SPECCTRA highlights selected terminators with the select color (yellow in the default color map). All wires and guides attached to selected terminators are also selected.

You can select only those terminator pins that belong to gates defined in the design file.

## Select logical part mode

### To set [LB] to select or unselect logical parts

- Click **Select - Logical Parts - Sel Logical Part Mode**

You can select or unselect individual [logical parts](#) by clicking them. To select or unselect several adjacent logical parts, drag the pointer to define a rectangular area. SPECCTRA selects or unselects logical parts that are totally or partially within the area.

SPECCTRA highlights all instances of selected logical parts with the select color (yellow in the default color map), and displays their component labels. All pins, wires, and guides attached to selected logical parts are also selected.

## Select physical part mode

### To set [LB] to select or unselect physical parts

- Click **Select - Physical Parts - Sel Physical Part Mode**

You can select or unselect individual [physical parts](#) by clicking them. To select or unselect several adjacent physical parts, drag the pointer to define a rectangular area. SPECCTRA selects or unselects physical parts that are totally or partially within the area.

SPECCTRA highlights all instances of selected physical parts with the select color (yellow in the default color map), and displays their component labels. All pins, wires, and guides attached to selected physical parts are also selected.

## Draw fence mode

Sets the left mouse button to draw a fence for automatic routing

Use Draw Fence mode to define autorouting keepin areas. You can draw a [hard fence](#) or a [soft fence](#).

**To set this mode, you can**

- Click **Define - Draw Fence Mode**

## Draw room mode

Sets the left mouse button to draw rooms for component placement

You can draw rectangle or polygon shaped rooms. After drawing a room, you can control placement within the room area by including or excluding specific components and clusters, and by applying height or power dissipation constraints. You can also assign placement rules to rooms.

### To set this mode, you can

- Click **Define - Draw Room Mode**

## Draw keepout mode

Sets the left mouse button to draw keepout areas for routing or placement

You can draw new keepout areas or modify keepouts defined in the structure section of the design file.

**To set this mode, you**

- Click **Define - Draw Keepout Mode**

## Draw place boundary mode

Sets the left mouse button to draw the placement boundary

You can draw a placement boundary, if it is not defined in the design file, or modify the existing placement boundary. If no placement boundary is defined, the routing (signal) boundary is used for component placement.

**To set this mode, you**

- Click **Define - Draw Place Boundary Mode**

## Edit route mode

Sets the left mouse button to create new wire paths and add vias

If Push is checked in the Interactive Routing Setup dialog box, wires that are not protected or fixed are shoved aside to add the new path.

### To set this mode, you can

- Click the Edit Route mode icon in the tool bar
- Press [RB] and choose **Edit Route Mode**



## Move route mode

Sets the left mouse button to move single wires or vias

If Push is checked in the Interactive Routing Setup dialog box, all movable wires in the path of a wire or via you are moving are shoved aside.

### To set this mode, you can

- Click the Move Route mode icon in the tool bar
- Press [RB] and choose **Move Route Mode**

## Copy route mode

Sets the left mouse button to copy wires and vias

You can copy an existing wire to an unroute with a similar length and path. You can also copy fanout wires and vias, with their fanout attributes, from a component to another component with the same image IC.

### To set this mode, you can

- Click the Copy Route mode icon in the tool bar
- Press [RB] and choose **Copy Route Mode**

## Critic route mode

Sets the left mouse button to remove extra bend points in a single wire or in several wires if you draw a bounding box

### To set this mode, you can

- Click the Critic Route mode icon in the tool bar
- Press [RB] and choose **Critic Route Mode**

## Change via mode

Sets the left mouse button to replace a via with another type of via

### To change via types

1. Press [RB] and choose **Change Via Mode** to open the Change Via Setup dialog box.
2. Choose a via type in the Vias [list](#) or enter a via type in the [Filter](#) data entry box, and click Apply or OK.
5. Click on the vias you want to replace with the new type.

To set a different via type, press [RB] and choose Setup Via Parameters to reopen the Change Via Setup dialog box. To exit Change Via mode, press [RB] and choose Cancel.

## Change wire mode

Sets the left mouse button to change the width of individual segments of routed wires.

### To change the wire width of a wire segment

1. Press [RB] and choose **Change Wire Mode** to open the Change Wire Setup dialog box.
2. Enter a value in the Edit Wire Width data entry box, and click Apply or OK.
3. Click on the wire segments you want to change.

To set a different wire width, press [RB] choose Setup Wire Parameters to reopen the Change Wire Setup dialog box. To exit Change Wire mode, press [RB] and choose Cancel.

You cannot violate the minimum wire width rule, which is the layer wire width rule, if set, or the PCB wire width rule. You must protect the wire segments if you want to retain the new widths during rerouting.

## Cut segment mode

Sets the left mouse button to break a single segment into two

### To set this mode, you can

- Click the Cut Segment mode icon in the tool bar
- Press [RB] and choose **Cut Segment Mode**

## Delete segment mode

Sets the left mouse button to remove a single wire segment

### To set this mode, you can

- Click the Delete Segment mode icon in the tool bar
- Press [RB] and choose **Delete - Segment Mode**

## Delete wire mode

Use this mode to delete all segments between two terminal points. A terminal point is a pin, via, or tjunction.

### To set this mode

- Press [RB] and choose **Delete - Wire Mode**



## Delete net mode

Use this mode to delete all wires and vias on a net. The net is not deleted.

### To set this mode

- Press [RB] and choose **Delete - Net Mode**

## Repair net mode

Use this mode to delete wire segments that violate fromto order rules on a net. A fromto is a user-specified pin-to-pin connection.

### To set this mode

- Press [RB] and choose **Delete - Repair Net Mode**

## Place connect mode

Sets the left mouse button to place components by connectivity without guidance from SPECCTRA

### To set this mode, you can

- Press [RB] and choose **Place Components - Place Connect Mode**

Move the pointer into the work area. SPECCTRA attaches a ghost image of the most highly connected component to the pointer. You click on the location where you want to place the component.

This process is repeated for each component in the design that is currently located outside the placement boundary.

## Guided place overlap allowed mode

Sets the left mouse button to place components by connectivity, with guidance from SPECCTRA in suggesting a location, but without considering whether the location violates component spacing rules

### To set this mode, you can

- Press [RB] and choose **Place Components - Guided Place Overlap Allowed Mode**

Move the pointer into the work area. SPECCTRA attaches a ghost image of the most highly connected component to the pointer, and highlights a suggested location. You can accept this location or click on a different location.

This process is repeated for each component in the design that is currently located outside the placement boundary.

## Guided place connect mode

Sets the left mouse button to place components by connectivity, with guidance from SPECCTRA in suggesting a location

### To set this mode, you can

- Press [RB] and choose **Place Components - Guided Place Connect Mode**

Move the pointer into the work area. SPECCTRA attaches a ghost image of the most highly connected component to the pointer, and highlights a suggested location. You can accept this location or click on a different location.

This process is repeated for each component in the design that is currently located outside the placement boundary.

## Define - Associate Components Mode

Sets the left mouse button to associate a large component with one or more small components

**To set this mode, you can**

- Click **Define - Associate Components Mode**

## Move component mode

Sets the left mouse button to move components

### To set this mode, you can

- Click the Move Comp mode icon in the tool bar
- Press [RB] and choose **Move Comp Mode**

## Push component mode

Sets the left mouse button to push unlocked components out of the way as you slide a component from one position to another.

### To set this mode, you can

- Click the Push Comp mode icon in the tool bar
- Press [RB] and choose **Push Comp Mode**



## Pivot component mode

Sets the left mouse button to rotate components

### To set this mode, you can

- Click the Pivot Comp mode icon in the tool bar
- Press [RB] and choose **Pivot Comp Mode**

## Flip component mode

Sets the left mouse button to flip components between the front and back sides of the PCB

### To set this mode, you can

- Click the Flip Comp mode icon in the tool bar
- Press [RB] and choose **Flip Comp Mode**

## Trade component mode

Sets the left mouse button to trade like and unlike components

### To set this mode, you can

- Click the Trade Comp mode icon in the tool bar
- Press [RB] and choose **Trade Comp Mode**

## Align component mode

Sets the left mouse button to align components relative to a common reference point

### To set this mode, you can

- Click the Align Comp mode icon in the tool bar
- Press [RB] and choose **Align Comp Mode**

The default alignment reference point is the upper left corner pin. To use a different alignment reference point, click **Autoplace - Setup** and choose a different Align Reference option in the Setup dialog box.

## Swap gate mode

Sets [LB] to swap net connections on gates

### To set this mode, you can

- Press [RB] and choose **Swap - Gate Mode**

You can swap two or more gates by dragging the pointer to define a rectangular area. SPECCTRA swaps net connections on all swappable gates within the area.

## Swap subgate mode

Sets [LB] to swap net connections on subgates

### To set this mode, you can

- Press [RB] and choose **Swap - Sub-Gate Mode**

You can swap two or more subgates by dragging the pointer to define a rectangular area. SPECCTRA swaps net connections on all swappable subgates within the area.

## Swap pin mode

Sets [LB] to swap net connections on pins

### To set this mode, you can

- Press [RB] and choose **Swap - Pin Mode**

You can swap two or more pins by dragging the pointer to define a rectangular area. SPECCTRA swaps net connections on all swappable pins within the area.

## Swap terminator mode

Sets [LB] to swap net connections on terminators

### To set this mode, you can

- Press [RB] and choose **Swap - Terminator Mode**

You can swap two or more terminators by dragging the pointer to define a rectangular area. SPECCTRA swaps net connections on all swappable terminator pins within the area.



*Misc. popup section*

## Filter data entry box

The Filter data entry box is used to mark one or more items in a list. You use the Filter to enter the actual name of the item you want to mark, or to mark a range of items by entering a filter pattern that includes the ? or \* wildcards. Press [Enter] to mark the item or items. You can repeat this procedure, entering a different name or filter pattern, to mark additional items.

### To search and mark a specific name

1. Click in the Filter box.

If there's a default filter, move the cursor to the portion of text you want to change and use [Backspace] to erase characters.

2. Type the name in the Filter data entry box.
3. Press [Enter] to apply the Filter.
4. Repeat steps 1 through 3 if you want to mark another name.

In some lists you mark only one active item. For instance, to assign layer wiring rules, you pick only one active layer.

### To search and mark one or more items that match the filter pattern

1. Click in the Filter box.

If there's a default filter, move the cursor to the portion of text you want to change and use [Backspace] to erase characters.

2. Type the name including the ? and \* wildcard characters in the Filter data entry box.
3. Press [Enter] to apply the Filter.
4. Repeat steps 1 through 3 if you want to mark additional names.

## List

A list contains a series of items.

### To mark an item in a list

- Click on the item. Items that were marked previously are no longer marked.

In some lists you mark only one active item. For instance, to assign layer wiring rules, you pick only one active layer.

### To mark adjacent items in a list

1. Click and hold the left mouse button
2. Drag the pointer over several consecutive items and mark them.

or

1. Click the first item in the sequence.
2. Press [Shift]-click on the last item in the sequence.

### To mark items that are not adjacent in a list

1. Click the first item.
2. Press [Ctrl] and click on the additional items you want to mark.

### To unmark some items in a list

1. Press [Ctrl].
2. Click on each item you want to unmark.

## Directories List

A Directories list contains a list of directories, including the current directory (represented by a period) and the directory above the current directory (represented by two periods).

You can choose only one directory in a Directories list. The default directory is the current directory.

### **To choose a directory**

- Double-click on the directory name.

## Files List

A Files list contains a list of files. You can choose only one file in the Files list.

### To choose a file

- Double-click on the file name.

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## accordion



A wiring pattern that looks like a rectangular wave. This pattern increases the wire length between pins in a connection.

## ADV

Advanced Rules option includes the following features:

- layer assignment of signals
- via assignment by net and net class
- width and clearance by layer
- net and net class rules by layer

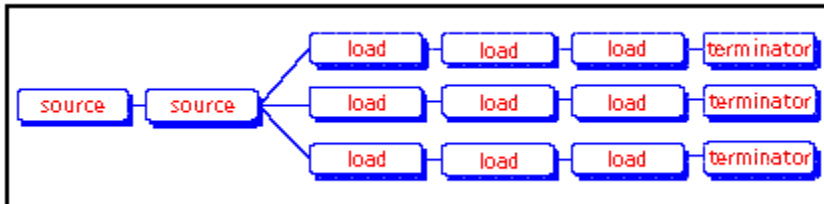


## **antipads**

Shapes defined on power layers in pin and via padstacks. These shapes are used to check clearances on the power layers if an antipad\_gap clearance is specified.

## balanced daisy-chain topology

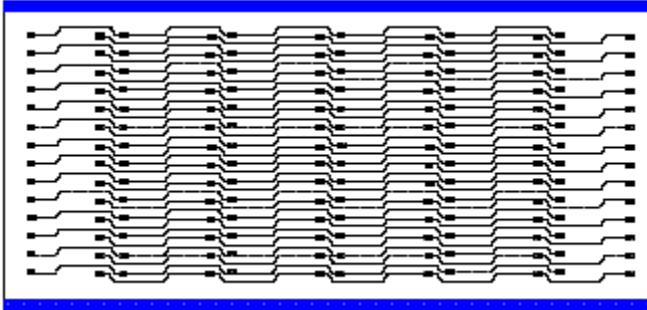
A type of daisy-chain routing in which the net must have at least one source pin and two or more terminator pins. Loads are evenly distributed between source and terminator pins. If more than one source pin is defined, the terminator and load branches are chained back to the closest source pin and the remaining source pins are ordered as an optimal daisy chain. If a net is ordered as daisy (type balanced) and it does not meet the minimum requirements, the net is ordered as a simple optimized daisy chain.



## bus diagonal routing

Bus diagonal routing connects arrays of pins with a diagonal wire segments, as opposed to orthogonal routing. This allows for high density routing.

This is an example of bus diagonal routing.



## capacitors

A capacitor in SPECCTRA is defined as a decoupling capacitor. SPECCTRA automatically treats a small component as a capacitor if its pins are connected only to power or ground. You can assign the Capacitor property type to any image or component that has three pins or less.

## **circuit**

A net or fromto for which electrical constraints are specified.

## class

A user-defined set of nets. You define classes in the design file or by using the **define class** command. A net can appear in more than one class.

## **clearance**

The distance between adjacent shapes placed within the PCB boundary.

## cluster

A collection of components grouped together based on criteria you define.

You can define a cluster by specifying its type and the components you want to include in the cluster. Valid cluster types are [floor plan](#), [super](#), [piggyback](#), and [super piggyback](#).

You can also form floor plan clusters by specifying power or signal net connections and letting SPECCTRA choose the components.



## **color map file**

Overrides the default colors. The color map file determines the colors and fill patterns of all routing objects, the background, and the PCB boundary.

## commands

Commands control the routing and placement tools. There are three ways you can enter commands:

- Choosing commands from menus (menu commands)
- Typing commands on the command line (keyboard commands)
- Running a batch file, called a do file, that contains a series of keyboard commands

## component

An electronic package such as a dual-inline package, surface mount device, pin grid array, and capacitor. A component consists of

- a unique reference designator or component ID
- an image name that identifies the component footprint
- an X,Y location
- a rotation in degrees, including zero
- a side that defines the component mounting, such as front or back

## conflicts

Conflicts are crossover and clearance violations.



Conflicts are marked graphically with a diamond or conflict box.

Other violations include the following:

- Length rule violation is marked as a yellow dashed line
- Crosstalk violation is marked as a white rectangle
- Placement violation is marked as a thick white rectangle with diamond symbols on each corner

## converge phase

The converge autorouting phase consists of the sixth and subsequent routing passes. The goal of the converge phase is to route the PCB completely.

Only connections that are involved with conflicts are ripped up and rerouted. You should not see unroutes during this stage. If unroutes exist, they probably cannot be completed in subsequent passes.

In the converge phase, conflict reduction proceeds at a slower pace. You typically see small percentage reductions of conflicts (less than 30%) during each of the converge passes. The overall trend during converge passes should be downward for any ten passes.

## daisy

A net ordering method that permits only a single entry and single exit in the net on each pin and does not allow tjunctions, unless a max\_stub rule is specified.

## **design file**

A text file used as input to the autorouter. This file is created from your host CAD system database by a translator that extracts the net list, component data, and rules information. The design file defines the PCB's size, components, netlist, design rules, preroutes, and pin and via definitions.

## DFM

The Design for Manufacturing option includes the following features

- automatic test point generation
- mitering
- spreading



## discretes

A discrete component can be any component that you want SPECCTRA to handle separately from other small components during automatic placement operations. You can assign the Discrete property type to any component that has three pins or less.

## did file

Contains the commands that were executed during an routing or placement session. The default filename is the month, day, and time with a .did extension. For example, if you started an session on July 28, 1995 at 9:00 am., the default did file name would be 0728940900.did.

You can specify the name of the did file when you start the autorouter or by using the **did\_file** command.

By default, the did file is placed in the design directory. You can change the location of the did file by using the -did switch on the command line or by specifying the path of the did file in the Startup dialog box.

## do file

A text file that contains a sequence of autorouter commands. Think of the do file as a script that controls the autorouter. An example of a do file follows.

```
# Lines beginning with '#' are comments
# General purpose do file
# Initial Commands
bestsave on bestsave.wre
status_file route.sts
unit mil
grid smart (wire 1) (via 1)
# Standard Routing Commands
smart_route
```

The order of commands in a do file is very important because the autorouter executes each command in sequence. For example, you would not want to route the design before you set rules, such as clearance and width rules, that you want the autorouter to follow.

## fanout

An autorouter command that generates short, breakout wires and vias for SMD pads.

## fix

Fixing allows you to isolate nets so the autorouter can't move any part of the net (same as protect) and can't route to any point on the net. If part of the net was routed before it was fixed, that part is treated as a keepout.

## **floor plan cluster**

A group of components, all of which you want to place either inside or outside a room.

## fromto

A single pin to pin connection on a net. A net consists of one or more fromtos (except single pin nets). A fromto is not changed when the autorouter breaks up nets.

## FST

Fast Circuit option includes the following features:

- crosstalk controls
- routed length controls
- differential pair routing
- rules by area
- shielding
- rounded cornering
- virtual pin topology control



## gap

The edge to edge distance between parallel or tandem (parallel on adjacent layers) wires.

## **gap (differential pair)**

The edge-to-edge distance between the wire pair. The autorouter maintains the differential pair gap unless the wire pair must diverge because of an obstacle in the routing path.

## gate

A set of pins that can be swapped within a component or between components. A gate consists of all the input and output pins of a functional block.

## group

Fromtos of the same net or different nets that you define as a group. The same fromto can exist in multiple groups.

## GUI

An acronym for Graphic User Interface. The GUI consists of menus, icons, dialog boxes, and window elements that you use to control the software program.

## guide

An implied connection between two points on a PCB. The connection points can be a combination of pins, SMD pads, vias, and polygons. A guide can connect to endpoints of wire segments, such as those created with **Edit - Delete Wires - Conflict Wire Segment**.

## **hard fence**

A hard (default) fence causes the autorouter to route only connections that are completely inside the fence. If only one pin of a connection is within the fence, the connection is not routed. Connections outside the fence are not routed.

## **HYB**

The Hybrid Design option includes the following features

- blind and buried via support
- vias under SMDs
- wirebond support



## image

A geometric representation of a component. The component shapes, a set of pins, and any associated keepouts are defined with an image. An image is defined by

- A unique image ID
- An outline description that defines the shape and dimensions of the component footprint
- A side that defines the component mounting, such as front or back

Each pin is defined by

- A unique pin ID
- A padstack name
- An X,Y location relative to the component origin
- A rotation angle in degrees

## **initial phase**

The initial autorouting phase consists of the first five routing passes. The objective during the initial phase is to create a path for all connections by allowing conflicts and to develop the overall routing flow. The key status file indications to watch during the initial phase are fails, unroutes, and conflicts.

## initial via grid

The autorouter computes an initial via grid, which might be the same as the minimum via grid if the minimum via grid is very large. The initial via grid is a multiple of the wire and via grids, and is designed to preserve routing channels by allowing two wires between vias, depending on the design rules. The initial via grid is used until the autorouter completes three routing passes or completes 50% of the routing.

Once the third routing pass or a completion rate of 50% is reached, the autorouter uses the via grid that was set in the **grid smart** command.

## **jumper layer**

An imaginary layer to which you assign jumper wires. This layer is included in the normal layer stack in the design file. You can apply width and clearance rules to a jumper layer.

## keepouts

Shapes added to a design to prevent routing in specific areas of the design. A keepout prohibits both wires and vias in an area. In addition, `place_keepouts`, `wire_keepouts`, `bend_keepouts`, and `via_keepouts` are supported. `Place_keepouts` prohibit components in an area. `Wire_keepouts` prohibit wires, but allow vias in an area. `Bend_keepouts` prohibit bends in wires in an area. `Via_keepouts` prohibit vias in an area.

## **large components**

Large components are defined as components with more than three pins. SPECCTRA automatically assigns the Large property type to images and components that have more than three pins.

## layer

The autorouter uses the following layer types.

Layer type	Description
Signal	Used for routing wires
Power	Used for power distribution
Mixed	Power (plane) layer that you can use for signal routing
Jumper	Used for jumper wires
System	For internal autorouter use and to display graphics (PCB, Unroutes, and Grid are system layers)

## layer panel

The layer panel controls layer selection, layer routing direction, and layer visibility.



## logical part

A logical part is a image in your design that includes logical [gate](#) and [subgate](#) definitions. Logical parts are defined in the part library section of the SPECCTRA design file. A logical part can have one or more instances in the design.



## Manhattan length

The sum of the X and Y distances between a pin pair. The Manhattan length is the minimum wire length if a pin pair is routed orthogonally. After recornering (mitering) is done, the actual length can be less than the Manhattan length.

## **max\_noise**

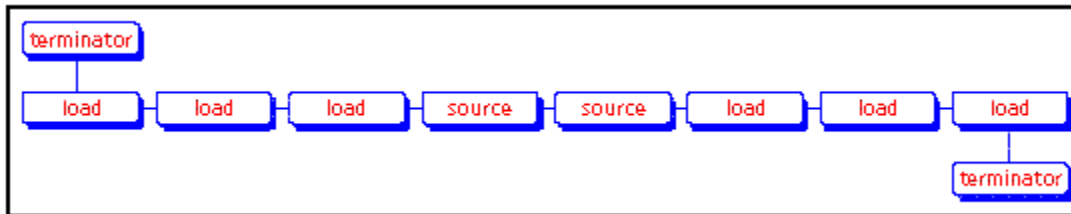
The maximum noise that can accumulate on a net before a coupled noise violation occurs.

## **max\_stub**

The maximum distance between a terminal point and a wire tjunction. The stub length is measured from the edge of a pad to the center of the tjunction.

## mid-driven daisy-chain topology

A type of daisy-chain routing in which a terminator is placed at each end of the net, and the loads are added back to a source. There must be exactly two terminators, or the net is ordered as a simple optimized daisy chain. If there is more than one source, the sources are chained together first before the rest of the net is processed.



## monitor.sts

The default routing status file. During autorouting, the autorouter writes status information to the file monitor.sts in the same directory as the design file. If you want to rename this file and write it to a different directory, use the **status\_file** command or the Status File option when you start the autorouter.

## net

A set of pins with the same signal or voltage name. The autorouter must connect these pins with wires. Voltage can be assigned to a "power" layer. Each net is defined in the network section of the design file. Every pin of a net is identified by a component reference designator and a physical pin name.

## orphan shapes

Copper shapes without net assignments.

## **padstack**

A set of user-defined shapes that define a pin, pad, or via. These shapes can span multiple layers.



## parallel

A condition where the gap between wires on the same layer is constant over some length.

## PCB

An acronym for Printed Circuit Board. A PCB consists of a set of physical layers. A two-layer PCB consists of top and bottom or front and back sides. A multilayer PCB consists of four or more layers.

## physical part

An alternate image that lacks logical [gate](#) and [subgate](#) definitions. Physical parts map to [logical parts](#) that do include gates and subgates in their library definitions, so that a single logic definition of gates and subgates can be maintained for several equivalent library images.

Physical parts are defined in the part library section of the SPECCTRA design file. A physical part can have one or more instances in the design.

## **piggyback cluster**

A group of components that can overlap without violating placement rules. You must preplace and lock piggyback clusters before performing automatic placement.

## priority values

Priority values are assigned to nets in the range of 0 to 255. If no priority is assigned, all nets have the same default priority value of 10.

When you assign priority to multiple nets, separate each priority assignment by at least 10. If priority values are too close, the autorouter can override the priority due to other factors that determine the routing schedule.

## protect wire

Protecting allows you to isolate nets so the autorouter can't change any part of the net. However, the autorouter can route to a protected wire at its terminal or to a segment if tjunctions are allowed. For example, you can fanout a component, protect the fanout wires and vias, and route the PCB. Wires route to fanout vias when they are protected.

## PTH

An acronym for Plated Through Hole, a plated hole that extends all the way through the PCB.

## region

A rectangular area of the PCB where you can apply rules. You can define a region on single or multiple signal layers.



## room

A rectangular or polygon-shaped area of the PCB that you define. You specify room contents and room rules to control how SPECCTRA places components inside a room.

## routes file

An output file generated when you use the **File - Write - Routes** menu command or the **write routes** keyboard command. The routes file contains the routing produced by the autorouter. Use this file to return the routing to your layout system or to restart the autorouter.

## rule precedence

### Routing rules

SPECCTRA applies routing rules according to the following hierarchy:

pcb < layer < class < class\_layer < group\_set < group\_set layer < net < net\_layer < group < group\_layer < fromto < fromto\_layer < class\_class < class\_class\_layer < padstack < region

A pcb rule (global rule for the PCB design) has the lowest precedence in the hierarchy. A region rule has the highest precedence. Rules set at one level of the hierarchy override conflicting rules set at lower levels.

### Placement rules

SPECCTRA applies placement rules according to the following hierarchy:

pcb < image\_set < image < component < super cluster < room < room\_image\_set < family\_family < image\_image

A pcb rule (global rule for the PCB design) has the lowest precedence in the hierarchy. An image to image spacing rule has the highest precedence. Rules set at one level of the hierarchy override conflicting rules set at lower levels.

## rules

Geometric constraints that you assign to a net or to connections in a net. The rules are hierarchical, meaning that certain rules have precedence over others.

## seedvia

A via assigned by the autorouter before routing begins if you use the **seedvia** command. The via is placed so that it reduces a long diagonal connection to two orthogonal connections joined by the seedvia.

## **select**

SPECCTRA mechanism that lets you identify individual objects, such as wires, nets, or components, for exclusive processing by automatic routing or placement commands. When you select wires, nets, components, or other objects before running a command, SPECCTRA operates only on the objects that you have selected.

## **serpentine**

A wiring topology that follows no regularly defined pattern.

## **session file**

Contains the design filename and a history of previous session files. This file can contain optional component placement, floor plan, and route data.



## shape

The basic data element. A shape is an object type: through-hole pin, SMD pad, via, wire, or a keepout area. These object types can be made up of the following graphic elements: rectangle, circle, polygon, path, and arc.

## **small components**

Small components are defined as components that have three or fewer pins. SPECCTRA automatically assigns the Small property type to images and components that have three pins or less. You can assign the Capacitor or Discrete property type to any small component.

## **SMD**

An acronym for a surface-mount device, which is a component that attaches directly to an exterior surface of the PCB.

## soft fence

A soft fence is useful in separating analog and digital signals. A soft fence causes the autorouter to do the following:

- All connections inside the soft fence are routed within the fence boundary.
- All connections outside the soft fence are routed outside the fence and do not cross the fence.
- All connections that cross the soft fence ignore the fence and are routed.

## **starburst**

A net ordering method that uses a minimum spanning tree algorithm and permits multiple entries and exits on pins.

## status file

A file that contains autorouting status information. It is updated after every 100 wires are routed or at the end of a pass, whichever occurs first. The default status file is monitor.sts. You can specify the name of the status file when you start the autorouter.

The following is an example of a status file

```
#Model 50 Version 6.0 made on DATE:95/07/26 TIME:15:27:08
#Host 5540a2fb Estimated Mips = 25.5
#ROUTING STATUS <<< design1.dsn >>>
Start Time: Wed July 26 14:48:50 1995
Report Time: Thu July 27 02:41:42 1995

Nets = 352 Connections = 2884
Current Wire = 6444 Reroute wires = 6444
Completion = 77.5% Unconnections = 0
| ROUTING HISTORY =====
| Pass | Conflicts | | | | | | | | | | CPU Time |
| Name | No. | Cross | Clear | Fail | Unrte | Vias | XTalk | Len | % | | Pass | Total |
|-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+
| Bus | 0 | 0 | 0 | 45 | 2884 | 0 | 0 | 0 | 0 | 0:00:03 | 0:00:03 |
| Route | 1 | 6803 | 1041 | 41 | 41 | 2786 | 0 | 0 | 0 | 0:45:57 | 0:46:00 |
| Route | 2 | 3745 | 716 | 32 | 17 | 3201 | 0 | 0 | 43 | 1:08:49 | 1:54:49 |
| Route | 3 | 2016 | 518 | 17 | 0 | 3626 | 0 | 0 | 43 | 1:05:28 | 3:00:17 |
| Route | 4 | 1171 | 374 | 5 | 0 | 3994 | 0 | 0 | 39 | 1:04:24 | 4:04:41 |
| Route | 5 | 742 | 317 | 9 | 0 | 4238 | 0 | 0 | 31 | 0:56:23 | 5:01:04 |
```

## status report file

The status report file contains the same routing status information as the [status file](#) plus additional information about the PCB, shown below.

### #WIRING STATISTICS

```
=====
PCB Area = 135954000.000      EIC = 315      Area/EIC = 431600.000
Components = 881              SMDs = 735
Signal Layers = 2             Power Layers = 2
Wire Junctions = 610,         at vias = 435      Total Vias = 4401
Conflicts = 0                 Crossovers = 0      Clearances = 0
Manhattan length = 4021497.000 Horizontal = 2325810.000 Vertical = 1695687.000
Routed length = 4670067.186   Horizontal = 2652766.020 Vertical = 2018454.580
Ratio Actual / Manhattan = 1.1613
Unconnected length = 2287.000 Horizontal = 2077.000 Vertical = 210.000
=====
```

Layer	Direct	Pins	Vias	TJs	Conflicts	Length	Horizontal	Vertical
COMP	Horz	2905	4401	80	0	2175312.418	512026.190	1663477.780
SOLDER	Vert	2196	4401	95	0	2494754.768	2140739.830	354976.800

## subgate

A set of pins that can be swapped only within a [gate](#). A subgate usually consists of only a subset of the input pins in a functional block.



## **super cluster**

A group of components whose positions and rotations are fixed with respect to each other, forming in effect a single *super component*.

## super piggyback cluster

A group of components, with fixed positions and rotations, that can overlap without violating placement rules. A super piggyback cluster is in effect a single *super component*.

## tandem

A condition where the gap between wires on adjacent layers (instead of the same layer) is constant over some length. Tandem conditions are not calculated on mixed layers nor are they calculated between two signal layers that are separated by a power (plane) layer.

## terminal

A shape on one layer or a set of shapes at the same vertex on multiple layers. The geometry of each terminal, except pseudo-pin and area, is defined by a padstack. A terminal can be one of the following.

Terminal	Description
Pin	A fixed shape resulting from placing a component pin. A pin extends through all the layers in the PCB design.
SMD pad	A fixed, single-layer shape resulting from placing a surface-mount component lead.
Tjunction	A via that connects three or more wires.
Via	A shape that interconnects two or more layers.
Pseudo-pin	A vertex where three or more paths are connected on the same layer. The vertex at which pseudo-pins occur is called a tjunction.
Area	A stationary shape that can be defined as a keepout, wire_keepout, via_keepout, signal boundary, fence, or wire (split power plane).

## terminator

A pin that is assigned the terminator property in the design file or in SPECCTRA. In Routing mode, you can assign the terminator property by using **Define - Assign Pin** or by using the **assign\_pin** command.

## **testpoint**

A pin or via assigned to each net. The testpoint is used for manufacturing tests of the PCB. Testpoints must not be covered by any components and can be on a specified test grid.

## **threshold**

The maximum parallel or tandem length that can be ignored for coupled noise calculations.

## **time\_length\_factor**

The factor that converts time units used in delay rules to units of length. The time\_length\_factor is the amount of time per unit of wire length.

If the time\_length\_factor is not set, delay rules are ignored.

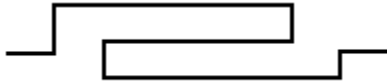
## tjunction

An intersection of three paths at a terminal created by the autorouter. These paths belong to the same net.



## trombone

A wiring pattern that looks like the folded length of a trombone.

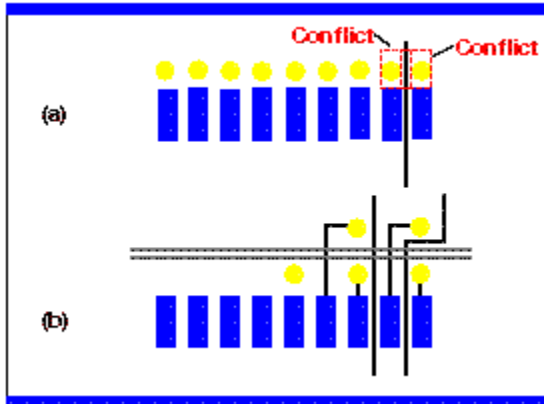


## via

A shape that interconnects two or more layers. Blind and buried vias are supported.

## via barrier

A via barrier occurs when vias are placed so that wires cannot pass between them. If the via grid is too fine, the autorouter can create a via barrier of fanout vias shown in (a). (b) shows how you can allow routing between pads without producing conflicts by having a small wire grid and a larger via grid.



## via grid

User-defined, equidistant points on which vias are allowed.

## virtual pin

A pseudo pin or via that allows you to specify a from-to tree or other topology. You can use virtual pins to control delays by matching routing lengths (such as minimizing clock skew) without adding excessive wiring on each branch of a net. Also, you can use virtual pins to control impedance so that the common path can have a different width rule.

## weight

A value equal to the amount of noise (usually in millivolts) per unit of parallel or tandem wire length that is coupled from a transmitting net onto a receiving net. The weight value is transmitted when the distance between parallel and tandem wires is less than the associated gap value.

## wire

A physical connection between two terminals.

## wire grid

User-defined, equidistant points on which center lines of a path must route. If you define a grid of zero, the autorouter routes gridless.



## wires file

An output file generated when you use the **File - Write - Wires** menu command or the **write wires** keyboard command. It contains routing information. The wires file is used when you restart the autorouter and you want to use the routing information from a previous autorouting session.

