NOTE: This Technical Note has been retired. Please see the Technical Notes page for current documentation.

Technical Note HW25

Macintosh Memory Configurations

CONTENTS

Developer Technical Support receives numerous questions about the many different possible configurations of RAM on the different Macintosh models, so we'll attempt to answer these questions in this Technical Note, as well as to provide a showcase for some outstanding Macintosh Plus and SE artwork by Apple engineer Brian Howard. Interested readers should refer to the *Guide to the Macintosh Family Hardware* , Second Edition, which contains much more detail on the memory configurations and specifications for all Macintosh models released to date. For information on the newer Macintosh models not mentioned in the *Guide to the Macintosh Family Hardware,* please refer to the companion developer notes for those particular products.

[Nov 01 1987]

Macintosh Quadra 900

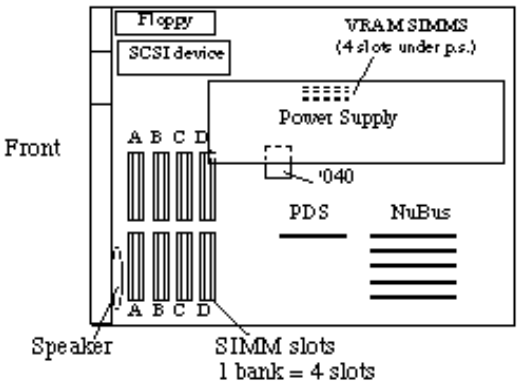


Figure 8 - View of the Macintosh Quadra 900 With Case Open

The memory control unit (MCU) controls four banks of dynamic RAM, for a total of 16 SIMM slots. Each bank accepts standard 80 ns SIMMs containing 1 MB, 4 MB, and perhaps 16 MB SIMMs (256K and 2 MB are not supported), giving total memory sizes from 4 MB to 16 MB for each bank (64 MB if 16 MB SIMMs work). Therefore, the Macintosh Quadra

900 could have a total of 64 MB when using currently available 4 MB SIMMs. 16 MB SIMMs have not been thoroughly tested on the Quadra 900 and therefore cannot be listed as a possible configuration. The Macintosh Quadra 900 can also use 60 ns SIMMs, but the MCU is programmed for 80 ns DRAM, so a 60 ns SIMM wouldn't improve the speed.

If one slot in a given bank is filled, then all slots in that particular bank must be populated with the same size SIMM. It is not possible to mix the speed of RAM, even between banks. The order that the banks are populated does not matter (for example, it is acceptable to have four 1 MB SIMMs in Bank B, and four 4 MB SIMMs in Bank D).

Note:
When large amounts of DRAM are installed, the memory check upon startup is lengthy and can cause users to think that the machine isn't functioning. There is no software indication that the machine is running memory checks.

Macintosh Quadra 700

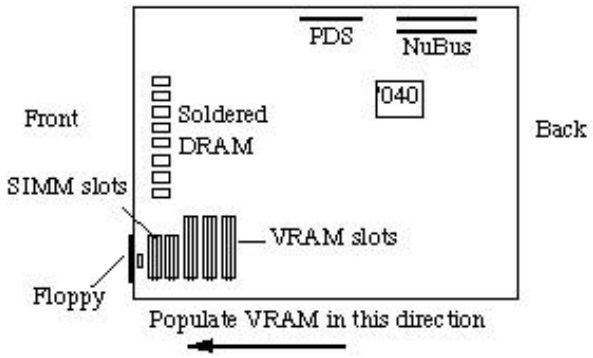


Figure 9 - View of the Macintosh Quadra 700 With Case Open

The memory control unit (MCU) IC controls two banks of dynamic RAM on the Macintosh Quadra 700. The first bank is soldered down at the factory, and fixed at 4 MB. The additional bank accepts standard 80 ns SIMMs containing 1 MB, 4 MB, and perhaps 16 MB (256K and 2 MB are not supported), giving total memory sizes from 4 MB to 16 MB for each bank. Therefore the Macintosh Quadra 700 could have a total of 20 MB when using SIMMs that are currently available. 16 MB SIMMs have not been tested on the Quadra 700 and therefore cannot be listed as a possible configuration. The Macintosh Quadra 700 can also use 60 ns SIMMs, but the MCU is programmed for 80 ns DRAM, so a 60 ns SIMM wouldn't improve the speed. If one slot in a given bank is filled, then all slots in the bank must be populated. It is not possible to mix the speed of RAM SIMMs on the Quadra 700.

Note:
Due to the location of the SIMM slots on the Macintosh Quadra 700, it is unlikely that third- party vendors will be able to develop 16 MB SIMMs that work on this machine. The placement of the SIMM slots (under the hard drive) is unfortunate, but necessary due to the logic board real estate.

Macintosh Classic II

The Macintosh Classic II can support up to 10 MB of system RAM. The logic board includes 2 MB soldered and 2 SIMM sockets that can accommodate 1, 2, or 4 MB SIMMS for possible system configurations of 2, 4, 6, or 10 MB. The Classic II requires 100 ns or faster access time for SIMMs to be compatible.

Possible memory configurations:

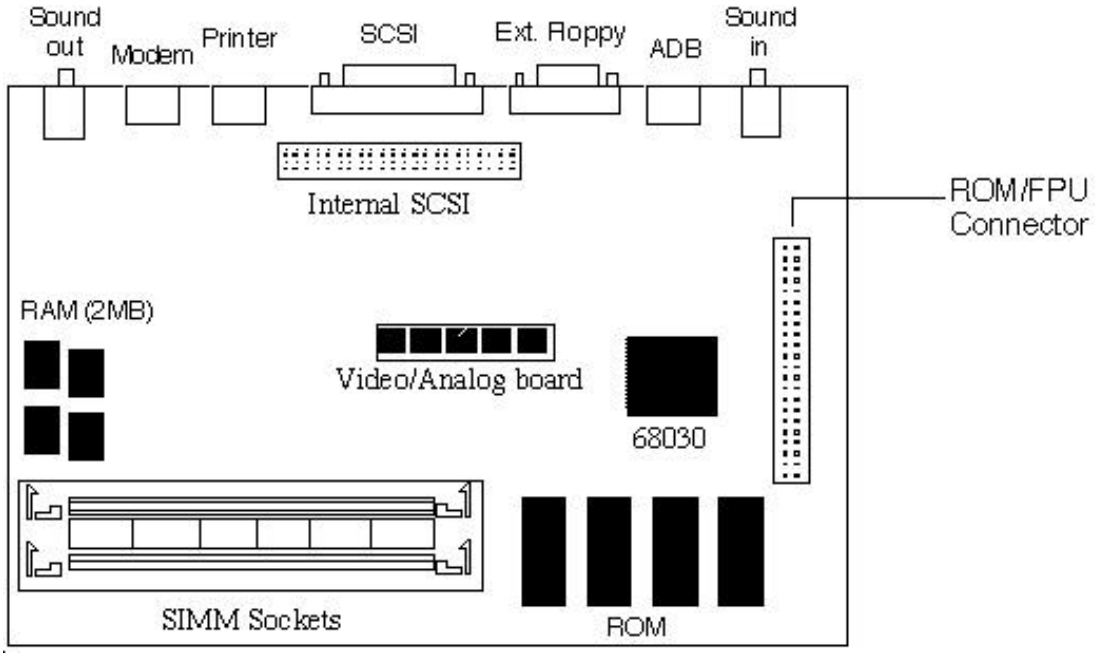
Built-in + SIMM size x2 = Total RAM (MB)

2 0 2

2 1 4

2 2 6

2 4 10



Macintosh Classic II

(SIMMs must be 100 ns RAS-access time or faster.)

Macintosh PowerBook 140 and Macintosh PowerBook 170

The Macintosh PowerBook 140 and 170 ship with 2 MB of PSRAM (pseudo-static) on the daughter board. The RAM is arranged physically as four 4 Mbit chips of 512K x 8-bits each. Additionally, an expansion slot allows RAM to be expanded to a total of 8 MB. Both notebook systems use 100 ns PSRAM. The Macintosh PowerBook 140 has one wait state (four clock cycles). The Macintosh PowerBook 170 has two wait states (five clock cycles). PSRAM needs to be refreshed, and the refresh is accomplished by circuitry in the CPU Glue Logic ASIC. The refresh requirement causes a 2% reduction in performance over SRAM. However, PSRAM uses less current in sleep mode and costs less than SRAM.

The PowerBook computers contain a 70-pin RAM expansion connector (slot) that supports RAM expansion card sizes of 2, 4, and 6 MB. Apple offers a 2 MB and 4 MB memory card.

Note:
If a RAM expansion card is designed correctly, it will work in all of the PowerBook computers. The 68030-based PowerBooks have a 32-bit data bus whereas the 68HC000-based machine (the PowerBook 100) has only a 16-bit data bus. If the expansion card is designed as a 32-bit device it will only work in the PowerBook 140 and 170, but if the data lines and chip select lines are in the correct location on the card, users can use the same card in either machine without loss of performance. The separated chip select lines are necessary for the 68HC000-based machine because it can get access to only 16 bits at a time. The Macintosh PowerBook 140 and 170 do not require separated chip select lines because both have a 32-bit data bus; therefore the lines are tied back together on the computer's main logic board.

The Apple PowerBook RAM cards will work in all three PowerBook systems. If purchasing RAM from third-party vendors, make sure it will work in the 68HC000-based portable as well.

RAM is always contiguous because only one size of RAM chip (4 Mbits) is used. As a result, the amount of memory the computer has doesn't have to be determined by the software. The RAM array is nominally located in the system memory map between addresses $0000 0000 and $0020 0000 (up to $0080 0000 in an 8 MB system), except following a system reset or sleep cycle, at which time it is overlaid by system ROM. However, the overlay is removed following access to normal ROM space, and the RAM space is then accessible. Both RAM and ROM memory spaces provide DSACK signals to the processor even if memory is not actually installed.

RAM wait states: access to the RAM from the main processor requires 100 ns PSRAM and two processor wait states (five clock cycles per RAM access). The CPU Glue Logic custom chip includes special circuitry that performs the refresh function.

Battery backup: both main and expansion RAM memories are backed up when the computer is in the sleep mode. This means that when the computer is not in use, the contents of the memory array are retained as long as the battery remains charged.

Note:
When the battery is removed RAM contents are lost. Unlike the Macintosh PowerBook 100 and Macintosh Portable, when the battery is removed, the contents of RAM are lost. The user must shut down the unit before replacing the battery. The backup battery in the Macintosh PowerBook 140 and 170 computers supply power only to the RTC chip (the clock).

Macintosh PowerBook 100

The system comes with 2 MB of PSRAM (pseudo-static RAM) . The RAM is arranged as four 4 Mbit chips of 512 by 8 bits each. The memory chips have an access and cycle time of 100 ns. There are no processor wait states to RAM unless the requested location in the pseudo-static RAM is being refreshed.

The system RAM can be expanded via a new 70-pin RAM expansion connector. The expansion slot can be filled with card sizes of 2 MB, 4 MB, or 6 MB. The system will automatically determine the card's memory size. These memory expansion cards can be used with the Macintosh PowerBook 140 and 170 computers.

System RAM is always powered; therefore RAM disks will be saved even after shutdown (similar to the Macintosh Portable). RAM will be maintained by three lithium batteries during a main battery exchange.

4 Mbit DRAMs in Revolt

When the Macintosh II was originally designed, Apple engineers intended for it to accept large amounts of memory in the form of 4 MB and 16 MB DRAM SIMMs. That was in 1986, when 1 Mbit DRAM was difficult to find and the higher-density chips did not yet exist. The engineers anticipated the pinouts of the yet to be introduced 4 MB SIMMs and provided all the necessary hardware and address multiplexing to allow installation of these parts when they became available.

Woe that Cupertino is not Camelot, James Brown is still on probation, and 4 MB SIMMs do not work as advertised in most cases. This is the story of the Revolt of the 4 MB DRAM SIMMs.

Preliminary Notes

Before diving into the problem with 4 Mbit DRAMs, there is some preliminary ground that must be covered.

First, there are a couple ways to construct a 4 MB SIMM. Using old technology, it is possible to cram together 32 DRAM ICs of 1M x 1 density. Using new technology, it only takes eight 4M x 1 ICs, resulting in a much smaller, lower-power module. If a 4 MB SIMM is of the large, so-called composite type (that is, it is constructed of 32 1 Mbit ICs), then everything is fine except on the original Macintosh II. Please refer to page 7 of this Technote for more information on Macintosh II RAM.

With the FDHD SuperDrive upgrade kit installed, the Macintosh II is on equal footing with the Macintosh IIx. That is, SIMMs made exclusively of the new 4 Mbit ICs still won't work, regardless of whether you are using a Macintosh II or IIx; therefore, for the remainder of this discussion, *Macintosh II* is used to refer to not only the original Macintosh II, but also the IIx.

Subsequent Macintosh models have revised ROMs that recognize 4 MB SIMMs.

The 4 Mbit Problem

DRAM ICs are now available in 4 Mbit density, but they come with a very nasty surprise. JEDEC, the committee overseeing the standardization of new solid-state devices, has added an additional built-in test mode to high-density DRAMs. The test mode is invoked by a sequence of electrical signals that was ignored by earlier-generation DRAM. The crux of the situation is this: under certain conditions, the Macintosh II unwittingly activates this new test mode and large amounts of memory become very forgetful.

More Specifically . . .

Those who are interested in the specific phenomenon occurring within the memory ICs should consult the detailed technical data supplied by the DRAM manufacturers. This Note only explains how the Macintosh II offends this new feature of the 4 Mbit DRAM, and hence, what might be done to work around the problem.

The Macintosh II uses /CAS-before-/RAS refresh cycles to keep RAM up to date on its contents. For 1 Mbit DRAM, the state of the /W control line is ignored during this type of refresh cycle. No longer. DRAM of the 4 Mbit variety goes off into test mode if /W is asserted (low, so that the RAM thinks it is write-enabled) during a /CAS-before-/RAS refresh cycle. The problem with the Macintosh II is that /W is the same signal as the MPU R/W line, and if the MPU is writing to an I/O address or a NuBus(TM) card concurrently with a refresh cycle, all the conditions are right for a waltz into test mode. Unfortunately, this condition is not all that unusual, since video card accesses qualify.

Consolation for SIMM manufacturers: SIMMs constructed with an on-board PAL are not necessarily Macintosh II-specific. SIMMs constructed in this manner should work without modification in any usage calling for 4 MB SIMMs (except in the unlikely event that the new test mode is required).

The Salvage Process

All is not necessarily lost, and although the situation is ugly, there is still a way to use 4 Mbit DRAM ICs to construct 4 MB SIMMs that work in the Macintosh II. A solution lies in the addition of a ninth IC to the SIMM. Programmed with suitable logic, a high-speed (-D or -E suffix) PAL on the SIMM itself can recognize and intercept /CAS-before-/RAS refresh cycles and set /W appropriately before any damage is done. More or less, the PAL becomes an intelligent buffer between the MPU read/write line and the DRAM write-enable lines. When the PAL senses a refresh cycle commencing, it holds /W high, ensuring that the ICs are not corrupted by the potentially dangerous processor-generated R/W signal.

What's the Point?

You have overcome all the problems discussed in this section and have working 4 Mbit SIMMs installed in your Macintosh. You probably have at least 20 MB of RAM. What can you do with all of it? Create lots of huge 32-bit PICTs and edit them all simultaneously? Model and animate Bay Area weather patterns in Mathematica? Yes! But, you have to use the appropriate system software to address this memory. Also, if you're running in 32-bit addressing mode, the applications that you desire to use need to be 32-bit clean. For more information on 32-bit cleanliness and addressing, please see Technical Notes #212 and #213.

Under System 7.0, applications can finally access additional physical memory over and above 8 MB. As mentioned previously in this Technote, the 32-bit addressing mode of System 7 requires either a Macintosh with 32-bit clean ROMs (listing is on page 2), or else the 32-bit software solution provided by the MODE32 system extension. A/UX is an alternative that can use up to 256K of RAM on Macintosh computers that support A/UX. Many manufacturers of large SIMMs also offer RAM disks. This is a volatile form of storage, but can certainly be useful for I/O intensive operations.

Other Permutations

The problem with 4 Mbit DRAM is not limited to 4 MB SIMMs. It is the 4 Mbit density of the individual RAM ICs that causes problems with certain machines. There exist 1 MB SIMMs constructed of only two 1M x 4 (4 Mbit) ICs. These do not work in a Macintosh II or IIx, any more than 4 MB SIMMs constructed of eight 4M x 1 ICs.

A few machines, namely the Macintosh Plus, Macintosh SE, and Macintosh Classic, depend on video accesses to refresh all of their DRAM. As the video circuitry accesses sequential locations through the video frame buffer, it simultaneously refreshes row after row of memory, eventually refreshing all 512 rows. Memory at the 4 Mbit density, however, is arranged as 1024 rows and there are not sufficient video accesses to refresh all 1024 rows. Chunks of memory simply go blank. Thus for a different reason, 4 Mbit DRAM parts are also not compatible with these older Macintosh hardware designs.

Summary

Owners of the Macintosh Plus, SE, Classic, II, or IIx are all likely to have problems with any 1 MB SIMM carrying only two ICs, or any 4 MB SIMM carrying only 8 ICs. Any SIMM constructed in one of these ways likely uses 4 Mbit density DRAM ICs and does not account for problems with the 4 Mbit test mode nor the video refresh strategy of older Macintosh designs.

References

Inside Macintosh , Volume V-1, Compatibility Guidelines

Guide to the Macintosh Family Hardware , Second Edition

Macintosh IIsi, LC, and Classic Developer Notes

Macintosh Classic II, Macintosh PowerBook Family, and Macintosh Quadra Family

Developer Notes

Macintosh Technical Notes #212 and #213

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