

Hardware_Manual

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Chapter 1

Hardware_Manual

1.1 Amiga® Hardware Reference Manual: E I/O Connectors And Interfaces

This appendix consists of four distinct parts, related to the way in which the Amiga talks to the outside world.

The first part specifies the pinouts of the externally accessible connectors and the power available at each connector. It does not, however, provide timing or loading information.

The second part briefly describes the functions of those pins whose purpose may not be evident.

The third part contains a list of the connections for certain internal connectors, notably the disk.

The fourth part specifies how various signals relate to the available ports of the 8520. This information enables the programmer to relate the port addresses to the outside-world items (or internal control signals) that are to be affected.

The third and fourth parts are primarily for the use of the systems programmer and should generally not be utilized by applications programmers.

Systems software normally is configured to handle the setting of particular signals, no matter how the physical connections may change. In other words, if you have a version of the system software that matches the revision level of the machine (normally a true condition), when you ask that a particular bit be set, you don't care which port that bit is connected to. Thus, applications programmers should rely on system documentation rather than going directly to the ports.

Warning:

In a multitasking operating system, many different tasks may be competing for the use of the system resources. Application programmers should follow the established rules for resource access in order to assure compatibility of their software with the system. Don't just hit the hardware registers directly, ask the system for exclusive control first.

Part 1 - Amiga I/O Connector Pins
 Part 2 - Explanation of Amiga I/O Connectors
 Part 3 - Internal Connectors
 Part 4 - Port Signal Assignments for 8520 CIAS

1.2 E I/O Connectors And Interfaces / Part 1 - Amiga I/O Connector Pins

This is a list of the I/O connections to the outside world on the Amiga.

RS232 and MIDI Port	External Disk
Parallel Port	External SCSI Disk
Keyboard	RAMEX
Video	Expansion
Video Display Enhancer	Joy Sticks
RF Monitor	

1.3 E / Amiga I/O Connector Pins / RS232 and MIDI Port

RS232 and MIDI Port

PIN	RS232	A1000	A500/ A2000/	CBM	PCs	HAYES	DESCRIPTION
			A3000				
1	GND	GND	GND	GND	GND	GND	FRAME GROUND
2	TXD	RXD	RXD	RXD	RXD	RXD	TRANSMIT DATA
3	RXD	RXD	RXD	RXD	RXD	RXD	RECEIVE DATA
4	RTS	RTS	RTS	RTS	-	-	REQUEST TO SEND
5	CTS	CTS	CTS	CTS	CTS	CTS	CLEAR TO SEND
6	DSR	DSR	DSR	DSR	DSR	DSR	DATA SET READY
7	GND	GND	GND	GND	GND	GND	SYSTEM GROUND
8	CD	CD	CD	DCD	DCD	DCD	CARRIER DETECT
9	-	-	+12v	+12v	-	-	+ 12 VOLT POWER
10	-	-	-12v	-12v	-	-	- 12 VOLT POWER
11	-	-	AUDO	-	-	-	AUDIO OUTPUT (A500, A2000, A3000)
12	S.SD	-	-	-	SI	-	SPEED INDICATE
13	S.CTS	-	-	-	-	-	
14	S.TXD	-5Vdc	-	-	-	-	- 5 VOLT POWER
15	TXC	AUDO	-	-	-	-	AUDIO OUTPUT (A1000)
16	S.RXD	AUDI	-	-	-	-	AUDIO INPUT (A1000)
17	RXC	EB	-	-	-	-	BUFFERED PORT CLOCK 716kHz
18	-	INT2*	AUDI	-	-	-	INTERRUPT LINE A1000/AUDIO INPUT (A500, 2000, 3000)
19	S.RTS	-	-	-	-	-	
20	DTR	DTR	DTR	DTR	DTR	DTR	DATA TERMINAL READY
21	SQD	+5	-	-	-	-	+ 5 VOLT POWER
22	RI	-	RI	RI	RI	RI	RING INDICATOR
23	SS	+12Vdc	-	-	-	-	+12 VOLT POWER
24	TXC1	C2*	-	-	-	-	3.58 MHZ CLOCK
25	-	RESB*	-	-	-	-	BUFFERED SYSTEM RESET

1.4 E / Amiga I/O Connector Pins / Parallel Port

Parallel (Centronics) Port

PIN	A1000	A500/A2000/A3000	Commodore PCs
---	-----	-----	-----
1	DRDY*	STROBE*	STROBE*
2	Data 0	Data 0	Data 0
3	Data 1	Data 1	Data 1
4	Data 2	Data 2	Data 2
5	Data 3	Data 3	Data 3
6	Data 4	Data 4	Data 4
7	Data 5	Data 5	Data 5
8	Data 6	Data 6	Data 6
9	Data 7	Data 7	Data 7
10	ACK*	ACK*	ACK*
11	BUSY (data)	BUSY	BUSY
12	POUT (clk)	POUT	POUT
13	SEL	SEL	SEL
14	GND	+5v pullup	AUTOFDXT
15	GND	NC	ERROR*
16	GND	RESET*	INIT*
17	GND	GND	SLCT IN*
18-22	GND	GND	GND
23	+ 5	GND	GND
24	NC	GND	GND
25	Reset*	GND	GND

1.5 E / Amiga I/O Connector Pins / Keyboard

KEYBOARD ...RJ11 (Not Applicable to the A500)

	A1000	A2000/A3000
	-----	-----
1	+5 Volts	KCLK
2	CLOCK	KDAT
3	DATA	NC
4	GND	GND
5		+5 Volts

1.6 E / Amiga I/O Connector Pins / Video

Video ...DB23 MALE

For A500, A1000, A2000 and A3000 unless otherwise stated

1	XCLK*	13	GNDRTN (Return for XCLKEN*)
2	XCLKEN*	14	ZD*
3	RED	15	C1*
4	GREEN	16	GND

5	BLUE	17	GND
6	DI	18	GND
7	DB	19	GND
8	DG	20	GND
9	DR	21	-5 VOLT POWER (A1000,A2000,A3000)
10	CSYNC*		-12 VOLT POWER (A500)
11	HSYNC*	22	+12 VOLT POWER
12	VSNC*	23	+5 VOLT POWER

1.7 E / Amiga I/O Connector Pins / Video Display Enhancer

Video Display Enhancer - DB 15 Female (A3000 ONLY)

1	RED VIDEO
2	GREEN VIDEO
3	BLUE VIDEO
4	MONITOR ID BIT 2 (NOT USED)
5	GROUND
6	RED RETURN (GROUND)
7	GREEN RETURN (GROUND)
8	BLUE RETURN (GROUND)
9	KEY (NO PIN)
10	SYNC RETURN (GROUND)
11	MONITOR ID BIT 0 (NOT USED)
12	MONITOR ID BIT 1 (NOT USED)
13	HORIZONTAL SYNC
14	VERTICAL SYNC
15	NOT USED

1.8 E / Amiga I/O Connector Pins / RF Monitor

RF Monitor ...8 PIN DIN (J2) (A1000 Only)

1	N.C.
2	GND
3	AUDIO LEFT
4	COMP VIDEO
5	GND
6	N.C.
7	+12 VOLT POWER
8	AUDIO RIGHT

1.9 E / Amiga I/O Connector Pins / External Disk

EXTERNAL DISK ...DB23 FEMALE

For A1000, A500, A2000 and A3000 with A2000 and A3000 differences noted.

1	RDY*	13	SIDEB*
2	DKRD*	14	WPRO*
3	GND	15	TK0*
4	GND	16	DKWEB*
5	GND	17	DKWDB*
6	GND	18	STEPB*
7	GND	19	DIRB
8	MTRXD*	20	SEL3B* (A2000/A3000 not used (1))
9	SEL2B* (A2000/A3000 SEL3B* (1))	21	SEL1B* (A2000/A3000 SEL2B* (1))
10	DRESB*	22	INDEX*
11	CHNG*	23	+12
12	+5		

(1) SEL1B* is not drive 1, but rather the first external drive. Not all select lines may be implemented.

1.10 E / Amiga I/O Connector Pins / External SCSI Disk

EXTERNAL SCSI DISK DB25 FEMALE (A3000 ONLY)

1	REQ	14	GROUND
2	MSG*	15	C/D
3	I/O	16	GROUND
4	RST*	17	ATN*
5	ACK*	18	GROUND
6	BSY*	19	SEL*
7	GROUND	20	PARITY
8	DATA0	21	DATA1
9	GROUND	22	DATA2
10	DATA3	23	DATA4
11	DATA5	24	GROUND
12	DATA6	25	TERMINATION POWER
13	DATA7		

See the ANSI (American National Standard Institute) standard SCSI (Small Computer Standard Interface) Specification for more information.

1.11 E / Amiga I/O Connector Pins / RAMEX

RAMEX ...60 PIN EDGE (.156) (P1) (A1000 only)

1	gnd	A	gnd
2	D15	B	D14
3	+5	C	+5
4	D12	D	D13
5	gnd	E	gnd
6	D11	F	D10
7	+5	H	+5
8	D8	J	D9

9	gnd	K	gnd
10	D7	L	D6
11	+5	M	+5
12	D4	N	D5
13	gnd	P	gnd
14	D3	R	D2
15	+5	S	+5
16	D0	T	D1
17	gnd	U	gnd
18	DRA4	V	DRA3
19	DRA5	W	DRA2
20	DRA6	X	DRA1
21	DRA7	Y	DRA0
22	gnd	Z	gnd
23	RAS*	AA	RRW*
24	gnd	BB	gnd
25	gnd	CC	gnd
26	CASU0*	DD	CASU1*
27	gnd	EE	gnd
28	CASL0*	FF	CASL1*
29	+5	HH	+5
30	+5	JJ	+5

1.12 E / Amiga I/O Connector Pins / Expansion

EXPANSION ...86 PIN EDGE (.1) (P2)

See Appendix K for the 100 pin Zorro II and Zorro III bus connector

PIN	A500	A1000	A2000	A2000b	FUNCTION
---	----	-----	-----	-----	-----
1	x	x	x	x	ground
2	x	x	x	x	ground
3	x	x	x	x	ground
4	x	x	x	x	ground
5	x	x	x	x	+5VDC
6	x	x	x	x	+5VDC
7	x	x	x	x	No Connect
8	x	x	x	x	-5VDC
9	x	x			No Connect
			x	x	28MHz Clock
10	x	x	x	x	+12VDC
11	x	x	x		No Connect
				x	/COPCFG (Configuration Out)
12	x	x	x	x	CONFIG IN, Grounded
13	x	x	x	x	Ground
14	x	x	x	x	/C3 Clock
15	x	x	x	x	CDAC Clock
16	x	x	x	x	/C1 Clock
17	x	x	x	x	/OVR
18	x	x	x	x	RDY
19	x	x	x	x	/INT2
20		x			/PALOPE
	x		x		No Connect

				x	/BOSS
21	x	x	x	x	A5
22	x	x	x	x	/INT6
23	x	x	x	x	A6
24	x	x	x	x	A4
25	x	x	x	x	ground
26	x	x	x	x	A3
27	x	x	x	x	A2
28	x	x	x	x	A7
29	x	x	x	x	A1
30	x	x	x	x	A8
31	x	x	x	x	FC0
32	x	x	x	x	A9
33	x	x	x	x	FC1
34	x	x	x	x	A10
35	x	x	x	x	FC2
36	x	x	x	x	A11
37	x	x	x	x	Ground
38	x	x	x	x	A12
39	x	x	x	x	A13
40	x	x	x	x	/IPL0
41	x	x	x	x	A14
42	x	x	x	x	/IPL1
43	x	x	x	x	A15
44	x	x	x	x	/IPL2
45	x	x	x	x	A16
46	x	x	x	x	BEER*
47	x	x	x	x	A17
48	x	x	x	x	/VPA
49	x	x	x	x	Ground
50	x	x	x	x	E Clock
51	x	x	x	x	/VMA
52	x	x	x	x	A18
53	x	x	x	x	RST
54	x	x	x	x	A19
55	x	x	x	x	/HLT
56	x	x	x	x	A20
57	x	x	x	x	A22
58	x	x	x	x	A21
59	x	x	x	x	A23
60	x	x	x	x	/BR
				x	/CBR
61	x	x	x	x	Ground
62	x	x	x	x	/BGACK
63	x	x	x	x	D15
64	x	x	x	x	/BG
				x	/CBG
65	x	x	x	x	D14
66	x	x	x	x	/DTACK
67	x	x	x	x	D13
68	x	x	x	x	R/W
69	x	x	x	x	D12
70	x	x	x	x	/LDS
71	x	x	x	x	D11
72	x	x	x	x	/UDS
73	x	x	x	x	Ground
74	x	x	x	x	/AS

75	x	x	x	x	D0
76	x	x	x	x	D10
77	x	x	x	x	D1
78	x	x	x	x	D9
79	x	x	x	x	D2
80	x	x	x	x	D8
81	x	x	x	x	D3
82	x	x	x	x	D7
83	x	x	x	x	D4
84	x	x	x	x	D6
85	x	x	x	x	Ground
86	x	x	x	x	D5

1.13 E / Amiga I/O Connector Pins / Joy Sticks

JOY STICKS ...DB9 male

USAGE	JOYSTICK	MOUSE
-----	-----	-----
1	FORWARD*	(MOUSE V)
2	BACK*	(MOUSE H)
3	LEFT*	(MOUSE VQ)
4	RIGHT*	(MOUSE HQ)
5	POT X	(or button 3 ... if used)
6	FIRE*	(or button 1)
7	+5	
8	GND	
9	POT Y	(or button 2)

1.14 E I/O Connectors And Interfaces / Explanation of Amiga I/O Connectors

Parallel Connector Interface Specification

Serial Interface Connector Specification

Game Controller Connector Interface Specification

External Disk Interface Connector Specification

1.15 E / Explanation of I/O Connectors / Parallel Interface Specification

The 25-pin D-type connector with pins (DB25P=male for the A1000, female for A500/A2000 and IBM compatibles) at the rear of the Amiga is nominally used to interface to parallel printers. In this capacity, data flows from the Amiga to the printer. This interface may also be used for input or bidirectional data transfers. The implementation is similar to Centronics, but the pin assignment and drive characteristics vary significantly from that specification (see Pin Assignment). Signal names correspond to those used in the other places in this appendix, when possible.

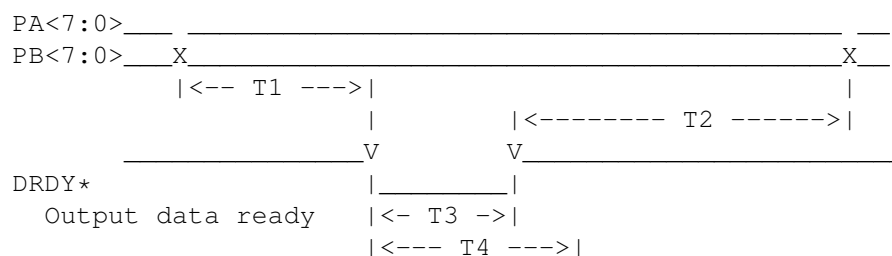
Pin Assignment (J8)

Interface Timing, Output Cycle
Interface Timing, Input Cycle

1.16 E // Parallel Interface Specification / Pin Assignment (J8)

NAME	DIR	NOTES
-----	----	-----
DRDY*	O	Output-data-ready signal to parallel device in output mode, used in conjunction with ACK* (pin 10) for a two-line asynchronous handshake. Functions as input data accepted from Amiga in input mode (similar to ACK* in output mode). See timing diagrams in the following section.
D0	I/O	+
D1	I/O	
D2	I/O	
D3	I/O	D0-D7 comprise an eight-bit bidirectional bus
D4	I/O	for communication with parallel devices,
D5	I/O	nominally, a printer.
D6	I/O	
D7	I/O	+
ACK*	I	Output-data-acknowledge from parallel device in output mode, used in conjunction with DRDY* (pin 1) for a two-line asynchronous handshake. Functions as input-data-ready from parallel device in input mode (similar to DRDY* in output mode). See timing diagrams . The 8520 can be programmed to conditionally generate a level 2 interrupt to the 680x0 whenever the ACK* input goes active.
BUSY	I/O	This is a general purpose I/O pin also connected to a serial data I/O pin (serial clock on pin 12). Note: Nominally used to indicate printer buffer full.
POUT	I/O	This is a general purpose I/O pin to a serial clock I/O pin (serial data on pin 11). Note: Nominally used to indicate printer paper out.
SEL	I/O	This is a general purpose I/O pin. Note: nominally a select output from the parallel device to the Amiga. On the A500/A2000 also shared with RS232 "ring indicator" signal.
RESET*	O	Amiga system reset

1.17 E // Parallel Interface Specification / Interface Timing Output Cycle



Pins on the RS232 connector other than these standard ones described below may be connected to power or other non-RS232 standard signals. When making up RS232 cables, connect only those pins actually used for a particular application. Avoid generic 25-connector "straight-thru" cables.

Pin Assignment (J6)

Timing

Electrical Characteristics

1.20 E // Serial Interface Specification / Pin Assignment (J6)

RS-232-C

NAME	DIR	STD	NOTES
----	---	---	-----
FGND		y	Frame ground -- do not tie to signal ground
TXD	O	y	Transmit data
RXD	I	y	Receive data
RTS	O	y	Request to send
CTS	I	y	Clear to send
DSR	I	y	Data set ready
GND		y	Signal ground -- do not tie to frame ground
CD	I	y	Carrier detect
-5V		n*	50 ma maximum *** WARNING -5V ***
AUDO	O	n*	Audio output from left (channels 0, 3) port, intended to send audio to the modem.
AUDI	I	n*	Audio input to right (channels 1, 2) port, intended to receive audio from the modem; this input is mixed with the analog output of the right (channels 1, 2). It is not digitized or used by the computer in any way.
DTR	O	y	Data terminal ready.
RI	I	y	Ring Indicator (A500/A2000 only) shared with printer "select" signal.
RESB*	O	n*	Amiga system reset.

NOTES:

n*: See warning above

See part 1 of this appendix for pin numbers .

1.21 E // Serial Interface Specification / Timing

Maximum operating frequency is 19.2 KHz. Refer to EIA standard RS-232-C for operating and installation specifications. A rate of 31.25 KHz will be supported through the use of a MIDI adapter.

Modem control signals (CTS, RTS, DTR, DSR, CD) are completely under software control. The modem control lines have no hardware affect on and are completely asynchronous to TXD and RXD .

1.22 E // Serial Interface Specification / Electrical Characteristics

OUTPUTS	MIN	TYP	MAX		
-----	---	---	---		
Vo (-):	-13.2	-x-	-2.5	V	Negative output voltage range
Vo (+):	8.0	-x-	13.2	V	Positive output voltage range
Io:	-x-	-x-	10.0	ma	Output current
INPUTS	MIN	TYP	MAX		
-----	---	---	---		
Vi (+):	3.0	-x-	25.0	V	Positive input voltage range
Vi (-):	-25.0	-x-	0.5	V	Negative input voltage range
Vhys:	-x-	1.0	-x-	V	Input hysteresis voltage
Ii:	0.3	-x-	10.0	ma	Input current

Unconnected inputs are interpreted the same as positive input voltages.

1.23 E / Explanation of I/O Connectors / Game Controller Interface Spec

The two 9-pin D-type connectors with pins (male) are used to interface to four types of devices:

1. Mouse or trackball, 3 buttons max.
2. Digital joystick, 2 buttons max.
3. Proportional (pot or proportional joystick), 2 buttons max.
4. Light pen, including pen-pressed-to-screen button.

The connector pin assignments are discussed in sections organized by similar hardware and/or software operating requirements as shown in the previous list. Signal names follow those used elsewhere in this appendix, when possible.

J11 is the right controller port connector (JOY1DAT , POT1DAT).
J12 is the left controller port connector (JOY0DAT , POT0DAT).

NOTE:

While most of the hardware discussed below is directly accessible, hardware should be accessed through ROM kernel software. This will keep future hardware changes transparent to the user.

Mouse/Trackball	Proportional Controllers
Digital Joysticks	Light Pen
Fire Buttons	

1.24 E // Game Controller Interface Specification / Mouse/Trackball

A mouse or trackball is a device that translates planar motion into pulse trains. Quadrature techniques are employed to preserve the direction as well as magnitude of displacement. The registers JOY0DAT and JOY1DAT become counter registers, with y displacement in the high byte and x in the low byte. Movement causes the following action:

Up: y decrements
 Down: y increments
 Right: x increments
 Left: x decrements

To determine displacement, JOYxDAT is read twice with corresponding x and y values subtracted (careful, modulo 128 arithmetic). Note that if either count changes by more than 127, both distance and direction become ambiguous. There is a relationship between the sampling interval and the maximum speed (that is, change in distance) that can be resolved as follows:

$$\text{Velocity} < \text{Distance(max)} / \text{SampleTime}$$

$$\text{Velocity} < \text{SQRT}(\text{DeltaX}^2 + \text{DeltaY}^2) / \text{SampleTime}$$

For an Amiga with a 200 count-per-inch mouse sampling during each vertical blanking interval, the maximum velocity in either the X or Y direction becomes:

$$\text{Velocity} < (128 \text{ Counts} * 1 \text{ inch}/200 \text{ Counts}) / .017 \text{ sec} = 38 \text{ in/sec}$$

which should be sufficient for most users.

NOTE:

The Amiga software is designed to do mouse update cycles during vertical blanking. The horizontal and vertical counters are always valid and may be read at any time.

CONNECTOR PIN USAGE FOR MOUSE/TRACKBALL QUADRATURE INPUTS

PIN	MNEMONIC	DESCRIPTION	HARDWARE REGISTER/NOTES
1	V	Vertical pulses	JOY[0/1]DAT<15:8>
2	H	Horizontal pulses	JOY[0/1]DAT<7:0>
3	VQ	Vertical quadrature pulses	JOY[0/1]DAT<15:8>
4	HQ	Horizontal quadrature pulses	JOY[0/1]DAT<7:0>
5	UBUT*	Unused mouse button	See Proportional Inputs .
6	LBUT*	Left mouse button	See Fire Button .
7	+5V	+5V, current limited	
8	Ground		
9	RBUT*	Right mouse button	See Proportional Inputs .

1.25 E // Game Controller Interface Specification / Digital Joysticks

A joystick is a device with four normally opened switches arranged 90 degrees apart. The JOY[0/1]DAT registers become encoded switch input ports as follows:

Forward: bit#9 xor bit#8
 Left: bit#9

Back: bit#1 xor bit#0
 Right: bit#1

Data is encoded to facilitate the mouse/trackball operating mode.

NOTE:

The right and left direction inputs are also designed to be right and left buttons, respectively, for use with proportional inputs. In this case, the forward and back inputs are not used, while right and left become button inputs rather than joystick inputs.

The JOY[0/1]DAT registers are always valid and may be read at any time.

CONNECTOR PIN USAGE FOR DIGITAL JOYSTICK INPUTS

PIN	MNEMONIC	DESCRIPTION	HARDWARE REGISTER/NOTES
---	-----	-----	-----
1	FORWARD*	Forward joystick switch	JOY[0/1]DAT<9 xor 8>
2	BACK*	Back joystick switch	JOY[0/1]DAT(1 xor 0>
3	LEFT*	Left joystick switch	JOY[0/1]DAT<9>
4	RIGHT*	Right joystick switch	JOY[0/1]DAT<1>
5	Unused		
6	FIRE*	Left mouse button	See Fire Button .
7	+5V	125ma max, 200ma surge	Total both ports.
8	Ground		
9	Unused		

1.26 E // Game Controller Interface Specification / Fire Buttons

The fire buttons are normally opened switches routed to the 8520 adapter PRA0 as follows:

PRA0 bit 7 = Fire* left controller port
 PRA0 bit 6 = Fire* right controller port

Before reading this register, the corresponding bits of the data direction register must be cleared to define input mode:

DDRA0<7:6> cleared as appropriate

NOTE:

Do not disturb the settings of other bits in DDRA0 (Use of ROM kernel calls is recommended).

Fire buttons are always valid and may be read at any time.

CONNECTOR PIN USAGE FOR FIRE BUTTON INPUTS

PIN	MNEMONIC	DESCRIPTION
-----	----------	-------------

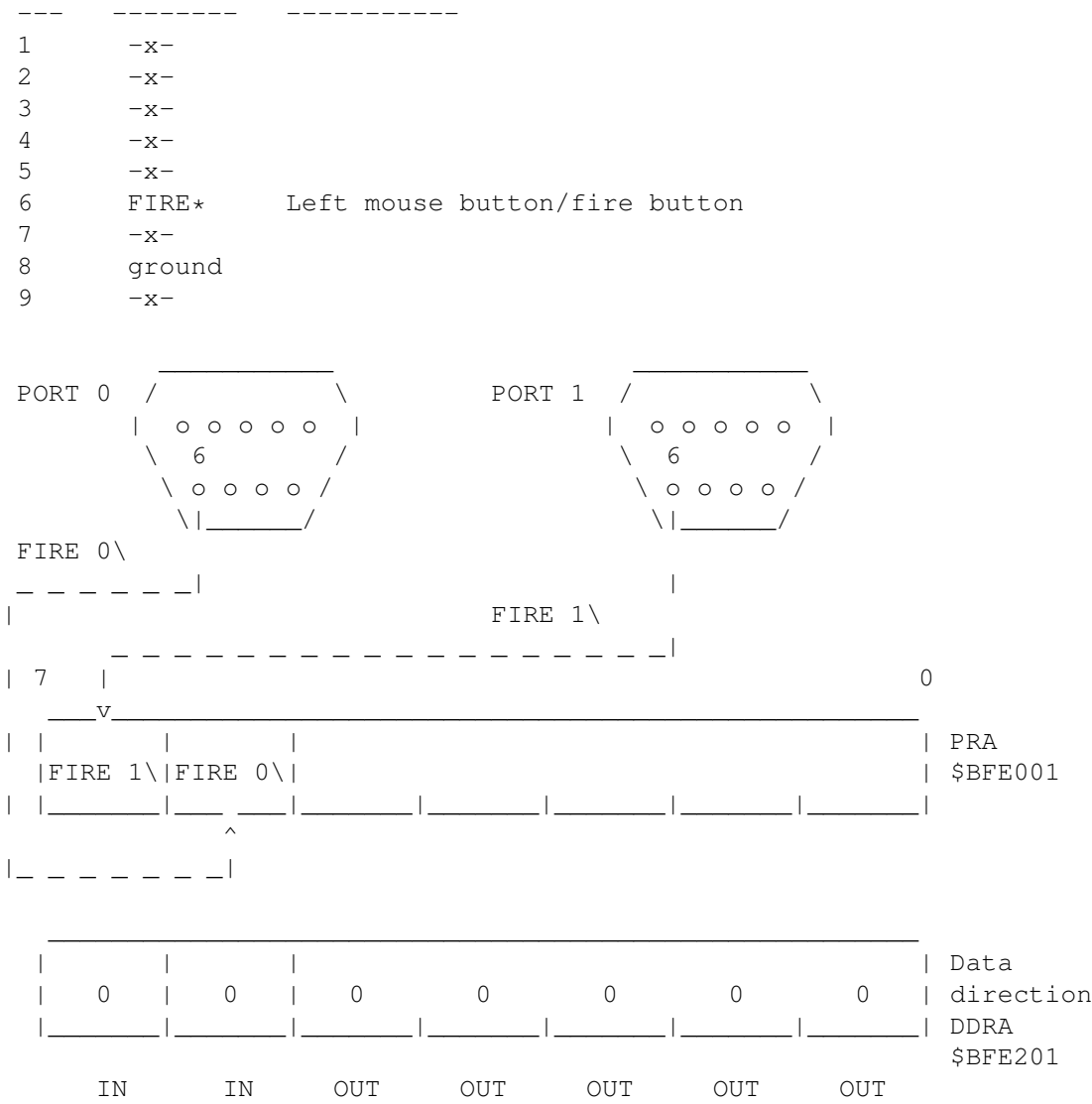


Figure E-1: Reading Fire Buttons

1.27 E // Game Controller Interface Spec / Proportional Controllers

Resistive (potentiometer) element linear taper proportional controllers are supported up to 528k Ohms max (470k +/- 10% recommended). The JOY[0/1]DAT registers contain digital translation values for y in the high byte and x in the low byte. A higher count value indicates a higher external resistance. The Amiga performs an integrating analog-to-digital conversion as follows:

- 1. For the first 7 (NTSC) or 8 (PAL) horizontal display lines, the analog input capacitors are discharged and the positions counters reflected in the POT[0/1]DAT registers are held reset.

For the remainder of the display field, the input capacitors are allowed to recharge through the resistive element in the external control device.

- 2. The gradually increasing voltage is continuously compared to an internal reference level while counter keeps track of the number of lines since the end of the reset interval.
- 3. When the input voltage finally exceeds the internal threshold for a given input channel, the current counter value is latched into the POT[0/1]DAT register corresponding to that channel.
- 4. During the vertical blanking interval, the software examines the resulting POT[0/1]DAT register values and interprets the counts in terms of joystick position.

NOTE:

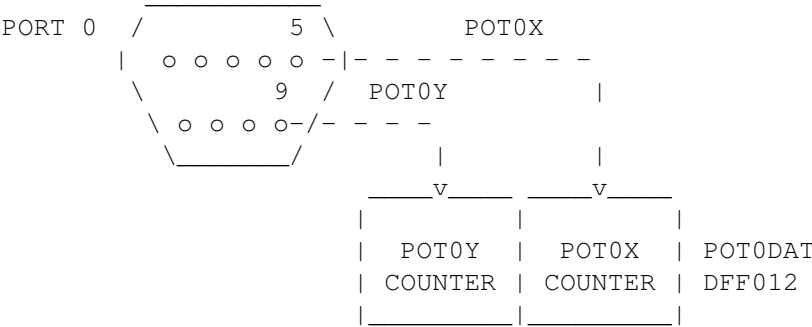
The POTY and POTX inputs are designated as "right mouse button" and "unused mouse button" respectively. An opened switch corresponds to high resistance, a closed switch to a low resistance. The buttons are also available in POTGO and POTGOR registers. It is recommended that ROM kernel calls be used for future hardware compatibility.

It is important to realize that the proportional controller is more of a "pointing" device than an absolute position input. It is up to the software to provide the calibration, range limiting and averaging functions needed to support the application's control requirements.

The POT[0/1]DAT registers are typically read during video blanking, but MAY be available prior to that.

CONNECTOR PIN USAGE FOR PROPORTIONAL INPUTS

PIN	MNEMONIC	DESCRIPTION	HARDWARE REGISTER/NOTES
1	XBUT	Extra Button	
2	Unused		
3	LBUT*	Left button	See Digital Joystick
4	RBUT*	Right button	See Digital Joystick
5	POTX	X analog in	POT[0/1]DAT<7:0>, POTGO, POTGOR
6	Unused		
7	+5V	125ma max, 200 ma surge	
8	Ground		
9	POTY	Y analog in	POT[0,1]DAT<15:8>, POTGO, POTGOR



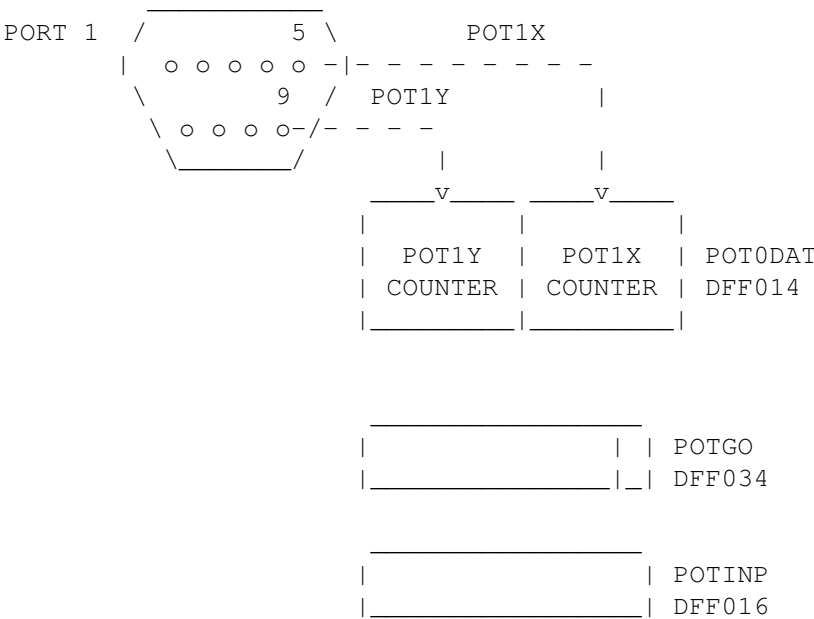


Figure E-2: Pot Counters

1.28 E // Game Controller Interface Specification / Light Pen

A light pen is an optoelectronic device whose light-sensitive portion is placed in proximity to a CRT. As the electron beam sweeps past the light pen, a trigger pulse is generated which can be enabled to latch the horizontal and vertical beam positions. There is no hardware bit to indicate this trigger, but this can be determined in the two ways as shown in chapter 8, "Interface Hardware."

Light pen position is usually read during blanking, but MAY be available prior to that.

CONNECTOR PIN USAGE FOR LIGHT PEN INPUTS

PIN	MNEMONIC	DESCRIPTION	HARDWARE REGISTER/NOTES
---	-----	-----	-----
1	Unused		
2	Unused		
3	Unused		
4	Unused		
5	LPENPR*	Light pen pressed	See Proportional Inputs
6	LPENTG*	Light pen trigger	VPOSR, VHPOSR
7	+5V	125ma max, 200 ma surge	Both ports
8	Ground		
9	Unused		

* Note: depending on the maker, the light pen input may be either.

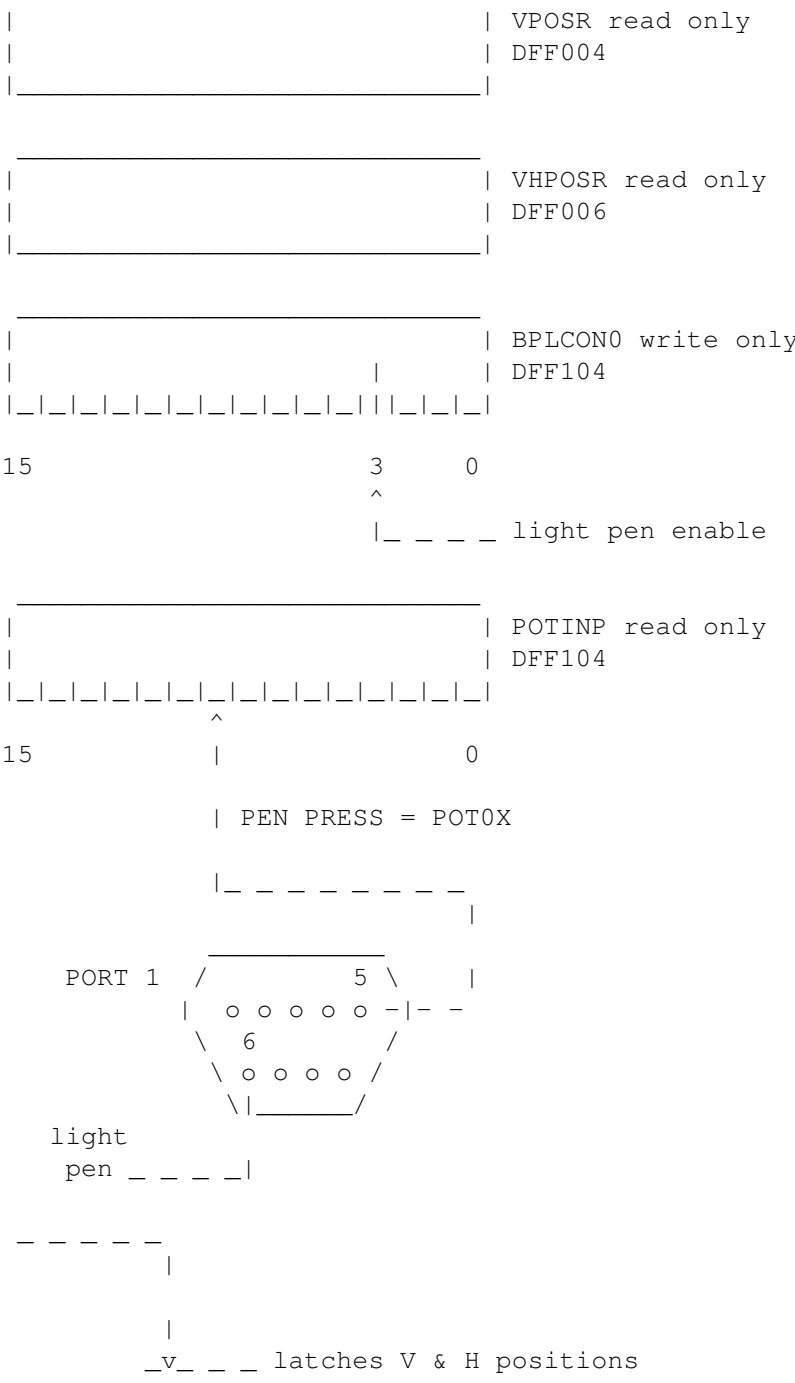


Figure E-3: Light Pen

1.29 E / Explanation of Connectors / External Disk Interface Specification

The 23-pin D-type connector with sockets (DB23S) at the rear of the Amiga is nominally used to interface to MFM devices.

Pin Assignment (J7)
Identification Mode

Limitations

1.30 E // External Disk Interface Specification / Pin Assignment (J7)

PIN	NAME	DIR	NOTES
----	-----	----	-----
1	RDY*	I/O	If motor on, indicates disk installed and up to speed. If motor not on, identification mode. See below.
2	DKRD*	I	MFM input data to Amiga.
3	GND		
4	GND		
5	GND		
6	GND		
7	GND		
8	MTRXD*	OC	Motor on data, clocked into drive's motor-on flip-flop by the active transition of SELxB*. Guaranteed setup time is 1.4 usec. Guaranteed hold time is 1.4 usec.
9	SEL2B*	OC	Select drive 2.*
10	DRESB*	OC	Amiga system reset. Drives should reset their motor-on flip-flops and set their write-protect flip-flops.
11	CHNG*	I/O	Note: Nominally used as an open collector input. Drive's change flop is set at power up or when no disk is not installed. Flop is reset when drive is selected and the head stepped, but only if a disk is installed.
12	+5V		270 ma maximum; 410 ma surge When below 3.75V, drives are required to reset their motor-on flops, and set their write-protect flops.
13	SIDEB*	O	Side 1 if active, side 0 if inactive
14	WPRO*	I/O	Asserted by selected, write-protected disk.
15	TK0*	I/O	Asserted by selected drive when read/write head is positioned over track 0.
16	DKWEB*	OC	Write gate (enable) to drive.
17	DKWDB*	OC	MFM output data from Amiga.
18	STEPB*	OC	Selected drive steps one cylinder in the direction indicated by DIRB.
19	DIRB	OC	Direction to step the head. Inactive to step towards center of disk (higher-numbered tracks).
20	SEL3B*	OC	Select drive 3. *
21	SEL1B*	OC	Select drive 1. *
22	INDEX*	I/O	Index is a pulse generated once per disk revolution, between the end and beginning of cylinders. The 8520 can be programmed to conditionally generate a level 6 interrupt to the 680x0 whenever the INDEX* input goes active.
23	+12V		160 ma maximum; 540 ma surge.

* Note: the drive select lines are shifted as they pass through a string of daisy chained devices. Thus the signal that appears as drive 2 select at the first drive shows up as drive 1 select

at the second drive and so on...

1.31 E // External Disk Interface Specification / Identification Mode

An identification mode is provided for reading a 32-bit serial identification data stream from an external device. To initialize this mode, the motor must be turned on, then off. See pin 8, MTRXD* for a discussion of how to turn the motor on and off. The transition from motor on to motor off reinitializes the serial shift register. After initialization, the SELxB* signal should be left in the inactive state. Now enter a loop where SELxB* is driven active, read serial input data on RDY* (pin 1), and drive SELxB* inactive. Repeat this loop a total of 32 times to read in 32 bits of data. The most significant bit is received first.

DEFINED IDENTIFICATIONS

\$0000 0000 - no drive present.
\$FFFF FFFF - Amiga standard 3.25 diskette.
\$5555 5555 - 48 TPI double-density, double-sided.

As with other peripheral ID's, users should contact Amiga, Inc. for ID assignment.

The serial input data is active low and must therefore be inverted to be consistent with the above table.

1.32 E // External Disk Interface Specification / Limitations

1. The total cable length, including daisy chaining, must not exceed 1 meter.
2. A maximum of 3 external devices may reside on this interface, but specific implementations may support fewer external devices.
3. Each device must provide a 1000-Ohm pull-up resistor on those outputs driven by an open-collector device on the Amiga (pins 8-10, 16-21).
4. The system provides power for only the first external device in the daisy chains.

1.33 E I/O Connectors And Interfaces / Part 3 - Internal Connectors

Internal Disk
Internal Disk Power
Internal SCSI Disk

1.34 E / Internal Connectors / Internal Disk

INTERNAL DISK ...34 PIN RIBBON (J10)

1	GND	18	DIRB
2	CHNG*	19	GND
3	GND	20	STEPB*
4	MTR0D*(led)	21	GND
5	GND	22	DKWDB*
6	N.C.	23	GND
7	GND	24	DKWEB*
8	INDEX*	25	GND
9	GND	26	TK0*
10	SEL0B*	27	GND
11	GND	28	WPRO*
12	N.C.	29	GND
13	GND	30	DKRD*
14	N.C.	31	GND
15	GND	32	SIDEB*
16	MTR0D*	33	GND
17	GND	34	RDY*

1.35 E / Internal Connectors / Internal Disk Power

INTERNAL DISK POWER ...4 PIN STRAIGHT (J13)

1	+12 (some drives are +5 only)
2	GND
3	GND
4	+5

1.36 E / Internal Connectors / Internal SCSI Disk

INTERNAL SCSI DISK ...50 PIN CONNECTOR (A3000 MOTHERBOARD)

2	DATA 0	26	TERMINATION POWER
4	DATA 1	28	GROUND
6	DATA 2	30	GROUND
8	DATA 3	32	ATN*
10	DATA 4	34	N.C.
12	DATA 5	36	BSY
14	DATA 6	38	ACK*
16	DATA 7	40	RST*
18	PARITY	42	MSG*
20	GROUND	44	SEL*
22	GROUND	46	C/D
24	GROUND	48	REQ*
		50	I/O

(ALL ODD-NUMBERED PINS, EXCEPT PIN 25, ARE CONNECTED TO GROUND. PIN 25 IS OPEN)

See the ANSI standard SCSI (Small Computer Standard Interface) Specification for more information.

1.37 E Connectors And Interfaces / Port Signal Assignments for 8520 CIAS

CIA-A Address BFE_x01 data bits 7-0 (A12*) (int2)

```

PA7..game port 1, pin 6 (fire button*)
PA6..game port 0, pin 6 (fire button*)
PA5.. RDY*      disk ready*
PA4.. TK0*      disk track 00*
PA3.. WPRO*     write protect*
PA2.. CHNG*     disk change*
PA1..LED*       led light (0=bright)/audio filter control (A500 & A2000)
PA0..OVL        ROM/RAM overlay bit

SP... KDAT      keyboard data
CNT.. KCLK      keyboard clock
PB7..P7         data 7
PB6..P6         data 6
PB5..P5         data 5      Centronics parallel interface
PB4..P4         data 4      data
PB3..P3         data 3
PB2..P2         data 2
PB1..P1         data 1
PB0..P0 data 0

PC... drdy*          Centronics control
F.... ack*
```

CIA-B Address BFD_x00 data bits 15-8 (A13*) (int6)

```

PA7..com line DTR* , driven output
PA6..com line RTS* , driven output
PA5..com line carrier detect*
PA4..com line CTS*
PA3..com line DSR*
PA2.. SEL      Centronics control
PA1.. POUT +--- paper out -----+
PA0.. BUSY | +--busy -----+ |
           | |               | |
SP... BUSY | +- commodore serial bus + |
CNT.. POUT +----commodore serial bus --+

PB7.. MTR*      motor
PB6.. SEL3*     select external 3rd drive
PB5.. SEL2*     select external 2nd drive
PB4.. SEL1*     select external 1st drive
PB3.. SEL0*     select internal drive
```

PB2.. SIDE* side select*
PB1.. DIR direction
PB0.. STEP* step*

PC...not used
F.... INDEX* disk index pulse*