Hardware_Manual

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Chapter 1

Hardware_Manual

1.1 Amiga® Hardware Reference Manual: J Custom Chip Pin Allocation List

This section gives the pin assignments used by the Amiga's custom chip set.

NOTE: * Means an active low signal.

Original Agnus Pin Assignment
Paula Pin Assignment
Denise Pin Assignment
Fat Agnus Pin Assignment

1.2 J Custom Chip Pin Allocation List / Original Agnus Pin Assignment

PIN #	DESIGNATION	FUNCTION	DEFINITION
01-09	D8-D0	Data bus lines 8 to 0	I/O
10	VCC	+5 Volt	I
11	RES*	System reset	I
12	INT3*	Interrupt level 3	O
13	DMAL	DMA request line	I
14	BLS*	Blitter slowdown	I
15	DBR*	Data bus request	O
16	ARW*	Agnus RAM write	O
17-24	RGA8-RGA1	Register address bus 8-1	I/O
25	CCK	Color clock	I
26	CCKQ	Color clock delay	I
27	VSS	Ground	I
28-36	DRA0-DRA8	DRAM address bus 0 to 8	O
37	LP*	Light pen input	I
38	VSY*	Vertical sync	I/O
39	CSY*	Composite sync	O
40	HSY*	Horizontal sync	I/O
41	VSS	Ground	I
42-48	D15-D9	Data bus lines 15 to 9	I/O

1.3 J Custom Chip Pin Allocation List / Denise Pin Assignment

PIN #	DESIGNATION	FUNCTION	DEFINITION
01-07	D6-D0	Data bus lines 6 to 0	I/O
08	M1H	Mouse 1 horizontal	I
09	M0H	Mouse 0 horizontal	I
10-17	RGA8-RGA1	Register address bus 8-1	I
18	BURST*	Color burst	O
19	VCC	+5 Volt	I
20-23	R0-R3	Video red bits 0-3	O
24-27	B0-B3	Video blue bits 0-3	O
28-31	G0-G3	Video green bits 0-3	O
32	/CSYNC	Composite sync	I
33	ZD*	Background indicator	O
34	N/C	Not connected	N/C (old Denise)
	CDAC	CDAC clock	I (ECS Denise)
35	7M	7.15909 MHZ	I
36	CCK	Color clock	I
37	VSS	Ground	I
38	M0V	Mouse 0 vertical	I
39	M1V	Mouse 1 vertical	I
40-48	D15-D7	Data bus lines 15 to 7	I/O

1.4 J Custom Chip Pin Allocation List / Paula Pin Assignment

PIN #	DESIGNATION	FUNCTION	DEFINITION
01-07	D8-D2	Data bus lines 8 to 2	I/O
08	VSS	Ground	I
09-10	D1-D0	Data bus lines 1 and 0	I/O
11	RES*	System reset	I
12	DMAL	DMA request line	O
13-15	IPL0*-IPL2	Interrupt lines 0-2	O
16	INT2*	Interrupt level 2	I
17	INT3*	Interrupt level 3	I
18	INT6*	Interrupt level 6	I
19-26	RGA8-RGA1	Register address bus 8-1	I
27	VCC	+5 Volt	I
28	CCK	Color clock	I
29	CCKQ	Color clock delay	I
30	AUDB	Right audio	O
31	AUDA	Left audio	O
32	POT0X	Pot 0X	I/O
33	POT0Y	Pot 0Y	I/O
34	VSSANA	Analog ground	I
35	POT1X	Pot 1X	I/O
36	POT1Y	Pot 1Y	I/O
37	DKRD*	Disk read data	I
38	DKWD*	Disk write data	O
39	DKWE	Disk write enable	O
40	TXD	Serial transmit data	O
41	RXD	Serial receive data	I
42-48	D15-D9	Data bus lines 15 to 9	I/O

1.5 J Custom Chip Pin Allocation List / Fat Agnus Pin Assignment

PIN #	DESIGNATION	FUNCTION	DEFINITION	
01-14	RD15-RD2	Register bus lines 15 to 2	I/O	
17	INT3*	Blitter ready interrupt	O	
18	DMAL	Request audio/disk DMA	I	
18	RD1	Register bus line 1	I/O	
18	RST*	Reset	I	
19	BLS*	Blitter slowdown	I	
20	DBR*	Data bus request	O	
21	RRW	DRAM Write/Read	O	
22	PRW	Processor Write/Read	I	
23	RGEN*	RG Enable	I	
24	AS*	Address Strobe	I	
25	RAMEN*	RAM Enable	I	
26-33	RGA8-RGA1	Register address bus 8-1	O	
34	28MHZ	Master clock	I	
35	XCLK	Alternate master clock	I	
36	XCLKEN*	Master clock enable	I	
37	CDAC*	Inverted shifted 7MHZ clk	O	
38	7MHZ	28MHZ clk divided by four	O	
39	CCKQ	Color clock delay	O	
40	CCK	Color clock	O	
41	TEST	Test - access registers	I	(old Fat Agnus)
	NTSC/PAL	Select video environment	I	(ECS Fat Agnus)
43-51	MA0-MA8	Output bus lines 0 to 8	O	
52	LDS*	Lower data strobe	I	
53	UDS*	Upper data strobe	I	
54	CASL*	Column addr strobe lower	O	
55	CASU*	Column addr strobe upper	O	
56	RAS1*	Row address strobe one	O	
57	RAS0*	Row address strobe zero	O	
59-77	A19-A1	Address bus lines 19 to 1	I	
78	LP*	Light pen	O	
79	VSY*	Vertical synch	I/O	
80	CSY*	Composite video synch	O	
81	HSY*	Horizontal synch	I/O	
84	RD0	Register bus line 0	I/O	