LH28F008SA-K/SAH-K

8 M-bit (1 MB x 8) Dual 5 V/12 V Power Supply Flash Memories

DESCRIPTION

The LH28F008SA-K/SAH-K dual 5 V/12 V power supply flash memories are the high-density, nonvolatile, read/write solution for solid state storage. The LH28F008SA-K/SAH-K's enhanced cycling capability, symmetrically blocked architecture, fast access time, write automation and low power consumption provide a more reliable, lower power, lighter weight and higher performance alternative to traditional rotating disk technology. The LH28F008SA-K/SAH-K bring new capabilities to portable computing. Application and operating system software stored in resident flash memory arrays provide instant-on rapid execute-in-place and protection from obsolescence through in-system software updates. Resident software also extends system battery life and increases reliability by reducing disk drive accesses.

For high density data acquisition applications, the LH28F008SA-K/SAH-K offer a more cost-effective and reliable alternative to SRAM and battery. Traditional high density embedded applications, such as telecommunications, can take advantage of the LH28F008SA-K/SAH-K's nonvolatility, blocking and minimal system code requirements for flexible firmware and modular software designs.

The LH28F008SA-K/SAH-K employ advanced CMOS circuitry for systems requiring low power consumption and noise immunity. Their high speed read access time provides superior performance when compared with magnetic storage media. A deep power-down mode lowers power consumption, crucial in portable computing, handheld instrumentation and other low-power applications. The RP# power control input also provides absolute data protection during system power-up/down.

FEATURES

- Supply voltage
  - 5 V V_{CC}
  - 12 V V_{PP}
- High performance read access time
  LH28F008SA-K85/SAH-K85
  - 85 ns (5.0±0.25 V)/90 ns (5.0±0.5 V)
  LH28F008SA-K12/SAH-K12
  - 120 ns (5.0±0.5 V)
- System performance enhancements
  - RY/BY# status output
  - Erase suspend capability
- Enhanced data protection features
  - Absolute protection with V_{PP} = GND
  - Block erase/byte write lockout during power transitions
- SRAM-compatible write interface
- High-density symmetrically-blocked architecture
  - Sixteen 64 k-byte erasable blocks
- Enhanced cycling capability
  - 100 000 block erase cycles
  - 1.6 million block erase cycles/chip
- Low power management
  - Deep power-down mode :
    10 µA I_{CC} (MAX.) [0 to +70°C]
    20 µA I_{CC} (MAX.) [–25 to +85°C]
- Automated byte write and block erase
  - Command user interface
  - Status register
- ETOX™* V nonvolatile flash technology
- Package
  - 40-pin TSOP Type I (TSOP040-P-1020)
    Normal bend/Reverse bend

* ETOX is a trademark of Intel Corporation.

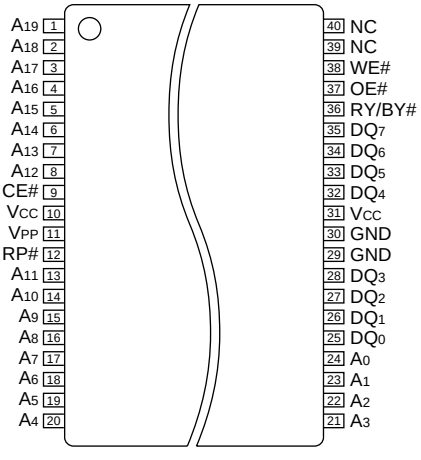
COMPARISON TABLE

VERSIONS	OPERATING TEMPERATURE	DC CHARACTERISTICS V_{CC} deep power-down current (MAX.)
LH28F008SA-K	0 to +70°C	10 µA
LH28F008SAH-K	–25 to +85°C	20 µA

PIN CONNECTIONS

40-PIN TSOP (Type I)

TOP VIEW

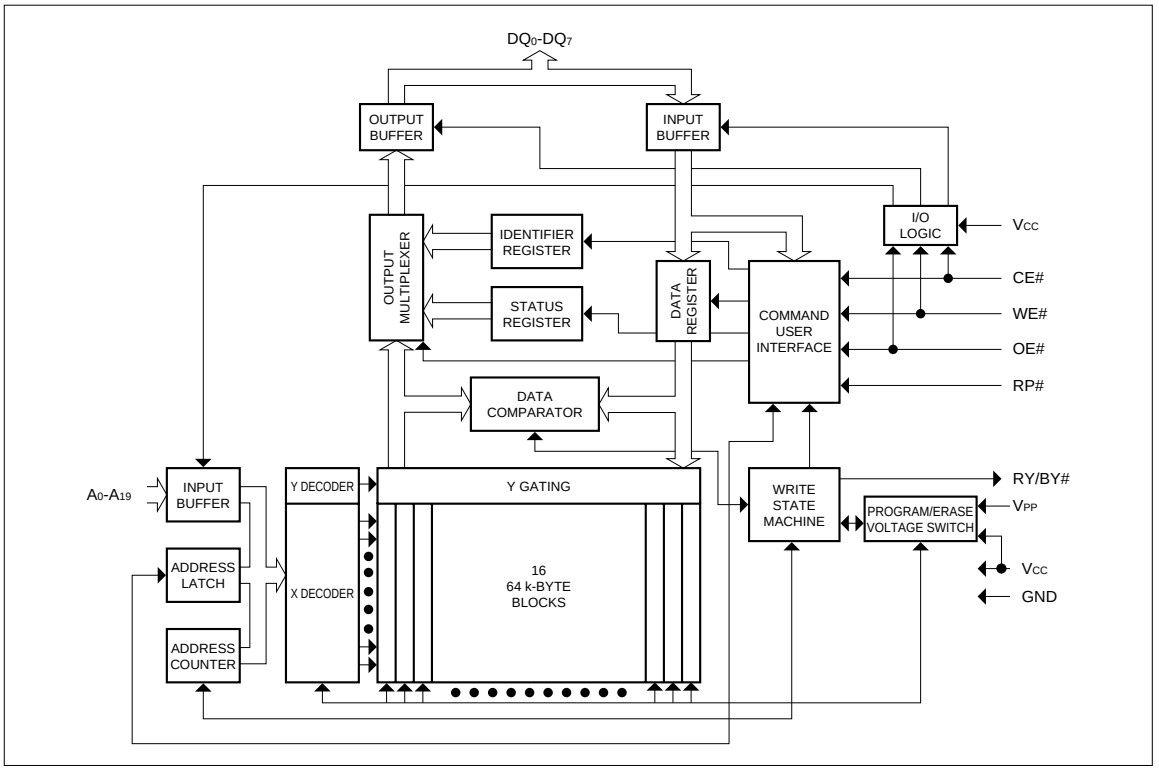


(TSOP040-P-1020)

NOTE :

Reverse bend available on request.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
A_0-A_{19}	INPUT	**ADDRESS INPUTS :** For memory addresses. Addresses are internally latched during a write cycle.
DQ_0-DQ_7	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS :** Inputs data and commands during Command User interface write cycles; outputs data during memory array, status register and identifier read cycles. The data pins are active high and float to tri-state off when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
CE#	INPUT	**CHIP ENABLE :** Activates the device's control logic input buffers decoders, and sense amplifiers. CE# is active low; CE#-high deselects the memory device and reduces power consumption to standby levels.
RP#	INPUT	**RESET/POWER-DOWN :** Puts the device in deep power-down mode and resets internal automation. RP# is active low; RP#-high gates normal operation. RP# also locks out block erase or byte write operations when active low, providing data protection during power transitions. Exit from deep power-down sets device to read array mode.
OE#	INPUT	**OUTPUT ENABLE :** Gates the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	**WRITE ENABLE :** Controls writes to the CUI and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
RY/BY#	OUTPUT	**READY/BUSY :** Indicates the status of the internal WSM. When low, it indicates that the WSM is performing a block erase or byte write operation. RY/BY#-high indicates that the WSM is ready for new commands, block erase is suspended or the device is in deep power-down mode. RY/BY# is always active and does not float to tri-state off when the chip is deselected or data outputs are disabled.
V_{PP}	SUPPLY	**BLOCK ERASE/BYTE WRITE POWER SUPPLY :** For erasing blocks of the array or writing bytes of each block. **NOTE :** With $V_{PP} < V_{PPLMAX}$, memory contents cannot be altered.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (5.0±0.5 V, 5.0±0.25 V)**
GND	SUPPLY	**GROUND**
NC		**NO CONNECT :** Lead is not internal connected; recommend to be floated.

1 INTRODUCTION

This datasheet contains LH28F008SA-K/SAH-K specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, 5, 6, 7 and 8 describe the memory organization and functionality. Section 9 covers electrical specifications. LH28F008SA-K/SAH-K flash memory documentation also includes ordering information which is referenced in Section 10.

1.1 Product Overview

The LH28F008SA-K/SAH-K is a high-performance 8 M-bit dual 5 V/12 V power supply flash memories organized as 1 M-byte of 8 bits. Sixteen 64 k-byte blocks are included on the LH28F008SA-K/SAH-K. A memory map is shown in **Fig. 1** of this specification. A block erase operation erases one of the sixteen blocks of memory in typically 1.6 seconds, independent of the remaining blocks. Each block can be independently erased and written 100 000 cycles. Erase suspend mode allows system software to suspend block erase to read data or execute code from any other block of the LH28F008SA-K/SAH-K.

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the LH28F008SA-K/SAH-K.

Byte write and block erase automation allow byte write and block erase operations to be executed using a two-write command sequence to the Command User Interface. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for byte write and block erase operations, including verifications, thereby unburdening the microprocessor or microcontroller. Writing of memory data is performed in byte increments typically within 8 µs. I_{PP} byte write and block erase currents are 10 mA typical, 30 mA maximum. V_{PP} byte write and block erase voltage is 11.4 to 12.6 V.

The status register indicates the status of the WSM and when the WSM successfully completes the desired byte write or block erase operation.

The RY/BY# output gives an additional indicator of WSM activity, providing capability for both hardware signal of status (versus software polling) and status masking (interrupt masking for background erase, for example). Status polling using RY/BY# minimizes both CPU overhead and system power consumption. When low, RY/BY# indicates that the WSM is performing a block erase or byte write operation. RY/BY#-high indicates that the WSM is ready for new commands, block erase is suspended or the device is in deep power-down mode.

The access time is 85 ns (t_{AVQV}) at the V_{CC} supply voltage range of 4.75 to 5.25 V over the temperature range, 0 to +70°C (LH28F008SA-K)/ −25 to +85°C (LH28F008SAH-K). At 4.5 to 5.5 V V_{CC}, the access time is 90 ns or 120 ns. I_{CC} active current (CMOS Read) is 20 mA typical, 35 mA maximum at 8 MHz.

When the CE# and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled.

A deep power-down mode is enabled when the RP# pin is at GND, minimizing power consumption and providing write protection. I_{CC} current in deep power-down is 10 µA (LH28F008SA-K)/20 µA (LH28F008SAH-K) maximum. Reset time of 400 ns is required from RP# switching high until outputs are valid to read attempts. Equivalently, the device has a wake time of 1 µs from RP#-high until writes to the CUI are recognized by the LH28F008SA-K/SAH-K. With RP# at GND, the WSM is reset and the status register is cleared.

Do not execute reprogramming "0" for the bit which has already been programmed "0". Overwrite operation may generate unerasable bit. In case of reprogramming "0" to the data which has been programmed "1".

- Program "0" for the bit when changing data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "10111101" to "10111100" requires "11111110" programming.

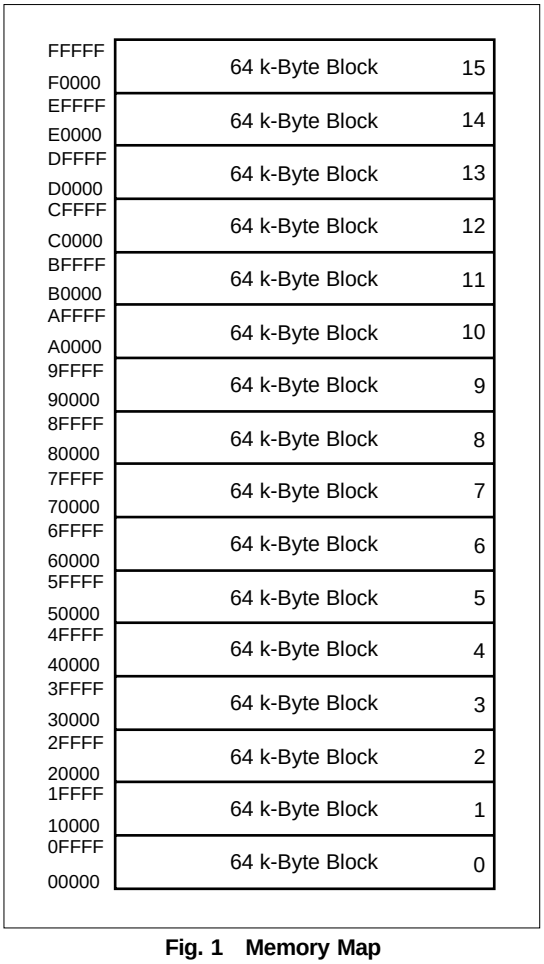


Fig. 1 Memory Map

2. PRINCIPLES OF OPERATION

The LH28F008SA-K/SAH-K include on-chip write automation to manage write and erase functions. The WSM allows for : 100% TTL-level control inputs; fixed power supplies during block erasure and byte write; and minimal processor overhead with RAM-like interface timings.

After initial device power-up, or after return from deep power-down mode (see **Table 1 "Bus Operations"**), the LH28F008SA-K/SAH-K function as a read-only memory. Manipulation of external memory-control pins allow array read, standby and output disable operations. Both status register and intelligent identifiers can also be accessed through the CUI when $V_{PP} = V_{PPL}$.

This same subset of operations is also available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables successful block erasure and byte writing of the device. All functions associated with altering memory contents—byte write, block erase, status and intelligent identifier—are accessed via the CUI and verified thru the status register.

Commands are written using standard micro-processor write timings. CUI contents serve as input to the WSM, which controls the block erase and byte write circuitry. Write cycles also internally latch addresses and data needed for byte write or block erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the intelligent identifier codes, or output byte write and block erase status for verification.

Interface software to initiate and poll progress of internal byte write and block erase can be stored in any of the LH28F008SA-K/SAH-K blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of byte write and/or block erase,

code/data reads from the LH28F008SA-K/SAH-K are again possible via the Read Array command. Erase suspend/resume capability allows system software to suspend block erase to read data and execute code from any other block.

2.1 Command User Interface and Write Automation

An on-chip state machine controls block erase and byte write, freeing the system processor for other tasks. After receiving the Erase Setup and Erase Confirm commands, the state machine controls block pre-conditioning and erase, returning progress via the status register and RY/BY# output. Byte write is similarly controlled, after destination address and expected data are supplied. The program and erase algorithms of past standard flash memories are now regulated by the state machine, including pulse repetition where required and internal verification and margining of data.

2.2 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory byte writes/block erases are required) or hardwired to V_{PPH}. When $V_{PP} = V_{PPL}$, memory contents cannot be altered. The LH28F008SA-K/SAH-K CUI architecture provides protection from unwanted byte write or block erase operations even when high voltage is applied to V_{PP}. Additionally, all functions are disabled whenever V_{CC} is below the write lockout voltage V_{LKO}, or when RP# is at V_{IL}. The LH28F008SA-K/SAH-K accommodate either design practice and encourages optimization of the processor-memory interface.

The two-step byte write/block erase CUI write sequence provides additional software write protection.

3. BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

The LH28F008SA-K/SAH-K have three read modes. The memory can be read from any of its blocks, and information can be read from the intelligent identifier or status register. V_{PP} can be at either V_{PPL} or V_{PPH}.

The first task is to write the appropriate read mode command (Read Array, Read Intelligent Identifier, or Read Status Register) to the CUI. The LH28F008SA-K/SAH-K automatically reset to read array mode upon initial device power-up or after exit from deep power-down. The LH28F008SA-K/SAH-K have four control pins, two of which must be logically active to obtain data at the outputs. Chip Enable (CE#) is the device selection control, and when active enables the selected memory device. Output Enable (OE#) is the data input/output (DQ_0-DQ_7) direction control, and when active drives data from the selected memory onto the I/O bus. RP# and WE# must also be at V_{IH}. **Fig. 8** illustrates read bus cycle waveforms.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ_0-DQ_7) are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the LH28F008SA-K/SAH-K in standby mode. Standby operation disables much of the LH28F008SA-K/SAH-K's circuitry and substantially reduces device power consumption. The outputs (DQ_0-DQ_7) are placed in a high-impedance state independent of the status of OE#. If the LH28F008SA-K/SAH-K are

deselected during block erase or byte write, the device will continue functioning and consuming normal active power until the operation completes.

3.4 Deep Power-Down

The LH28F008SA-K/SAH-K offer a deep power-down feature, entered when RP# is at V_{IL}. Current draw thru V_{CC} is 10 µA (0 to +70°C)/20 µA (–25 to +85°C) maximum in deep power-down mode, with current draw through V_{PP} maximal 5 µA. During read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. The LH28F008SA-K/SAH-K require time t_{PHQV} (see **Section 9.2.4 "AC CHARACTERISTICS - READ-ONLY OPERATIONS"**) after return from deep power-down until initial memory access outputs are valid. After this wakeup interval, normal operation is restored. The CUI is reset to read array, and the upper 5 bits of the status register are cleared to value 10000, upon return to normal operation.

During block erase or byte write modes, RP#-low will abort either operation. Memory contents of the block being altered are no longer valid as the data will be partially written or erased. Time t_{PHWL} after RP# goes to logic-high (V_{IH}) is required before another command can be written.

3.5 Intelligent Identifier Operation

The intelligent identifier operation outputs the manufacture code, 89H; and the device code, A2H for the LH28F008SA-K/SAH-K. The system CPU can then automatically match the device with its proper block erase and byte write algorithms.

The manufacture and device codes are read via the CUI. Following a write of 90H to the CUI, a read from address location 00000H outputs the manufacture code (89H). A read from address 00001H outputs the device code (A2H). It is not necessary to have high voltage applied to V_{PP} to read the intelligent identifiers from the CUI.

3.6 Write

Writes to the CUI enable reading of device data and intelligent identifiers. They also control inspection and clearing of the status register. Additionally, when $V_{PP} = V_{PPH}$, the CUI controls block erasure and byte write. The contents of the interface register serve as input to the internal state machine.

The CUI itself does not occupy an addressable memory location. The interface register is a latch used to store the command and address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Byte Write Setup command requires both appropriate command data and the address of the location to be written, while the Byte Write command consists of the data to be written and the address of the location to be written.

The CUI is written by bringing WE# to a logic-low level (V_{IL}) while CE# is low. Addresses and data are latched on the rising edge of WE#. Standard microprocessor write timings are used.

Refer to "AC Write Characteristics" (**Section 9.2.5 and 9.2.6**) and the AC waveforms for write operations" (**Fig. 9** and **Fig. 10**).

4. COMMAND DEFINITIONS

When V_{PPL} is applied to the V_{PP} pin, read operations from the status register, intelligent identifiers, or array blocks are enabled. Placing V_{PPH} on V_{PP} enables successful byte write and block erase operations as well.

Device operations are selected by writing specific commands into the CUI. **Table 2** defines the LH28F008SA-K/SAH-K commands.

Table 1 Bus Operations

MODE	NOTE	RP#	CE#	OE#	WE#	A_0	V_{PP}	DQ_{0-7}	RY/BY#
Read	1, 2, 3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable	3	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	3	V_{IH}	V_{IH}	X	X	X	X	High Z	X
Deep Power-Down		V_{IL}	X	X	X	X	X	High Z	V_{OH}
Intelligent Identifier (Mfr)		V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	89H	V_{OH}
Intelligent Identifier (Device)		V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	A2H	V_{OH}
Write	3, 4, 5	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES :

1. Refer to **Section 9.2.3 "DC CHARACTERISTICS"**. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPL} or V_{PPH} for V_{PP}. See **Section 9.2.3 "DC CHARACTERISTICS"** for V_{PPL} and V_{PPH} voltages.
3. RY/BY# is V_{OL} when the WSM is executing internal block erase or byte write algorithms. It is V_{OH} when the WSM is not busy, in erase suspend mode or deep power-down mode.
4. Command writes involving block erase or byte write are only successfully executed when $V_{PP} = V_{PPH}$.
5. Refer to **Table 2** for valid D_{IN} during a write operation.

Table 2 Command Definitions (NOTE 6)

COMMAND	BUS CYCLES REQ'D.	NOTE	FIRST BUS CYCLE			SECOND BUS CYCLE		
			Oper (NOTE 1)	Addr (NOTE 2)	Data (NOTE 3)	Oper (NOTE 1)	Addr (NOTE 2)	Data (NOTE 3)
Read Array/Reset	1		Write	X	FFH			
Intelligent Identifier	3	4	Write	X	90H	Read	IA	IID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Erase Setup/Erase Confirm	2		Write	BA	20H	Write	BA	D0H
Erase Suspend/Erase Resume	2		Write	X	B0H	Write	X	D0H
Byte Write Setup/Write	2	5	Write	WA	40H	Write	WA	WD
Alternate Byte Write Setup/Write	2	5	Write	WA	10H	Write	WA	WD

NOTES :

1. BUS operations are defined in **Table 1**.
2. X = Any valid address within the device.
   IA = Identifier code address : 00H for manufacture code, 01H for device code.
   BA = Address within the block being erased.
   WA = Address of memory location to be written.
3. SRD = Data read from status register. See **Table 3** for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of WE#.
   IID = Data read from intelligent identifiers.
4. Following the intelligent identifier command, two read operations access manufacture and device codes.
5. Either 40H or 10H is recognized by the WSM as the Byte Write Setup command.
6. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the LH28F008SA-K/SAH-K default to read array mode. This operation is also initiated by writing FFH into the CUI. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the CUI contents are altered. Once the internal WSM has started a block erase or byte write operation, the device will not recognize the Read Array command, until the WSM has completed its operation. The Read Array command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

4.2 Intelligent Identifier Command

The LH28F008SA-K/SAH-K contain an intelligent identifier operation, initiated by writing 90H into the CUI. Following the command write, a read cycle from address 00000H retrieves the manufacture code of 89H. A read cycle from address 00001H returns the device code of A2H. To terminate the operation, it is necessary to write another valid command into the register. Like the Read Array command, the Intelligent Identifier command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

4.3 Read Status Register Command

The LH28F008SA-K/SAH-K contain a status register which may be read to determine when a byte write or block erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the Read Status Register command (70H) to the CUI. After writing this command, all subsequent read operations output data from the status register, until another valid command is written to the CUI. The contents of the status register are latched on the falling edge of OE# or CE#, whichever occurs last in the read cycle. OE# or CE# must be toggled to V_{IH} before further reads to update the status register latch. The Read Status Register command functions when $V_{PP} = V_{PPL}$ or V_{PPH}.

4.4 Clear Status Register Command

The erase status and byte write status bits are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see **Table 3**). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The status register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

Additionally, the V_{PP} status bit (SR.3) must be reset by system software before further byte writes or block erases are attempted. To clear the status register, the Clear Status Register command (50H) is written to the CUI. The Clear Status Register command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

4.5 Erase Setup/Erase Confirm Commands

Erase is executed one block at a time, initiated by a two-cycle command sequence. An Erase Setup command (20H) is first written to the CUI, followed by the Erase Confirm command (D0H). These commands require both appropriate sequencing and an address within the block to be erased to FFH. Block preconditioning, erase and verify are all handled internally by the WSM, invisible to the system. After the two-command erase sequence is written to it, the LH28F008SA-K/SAH-K automatically output status register data when read (see **Fig. 2**). The CPU can detect the completion of the erase event by analyzing the output of the RY/BY# pin, or the WSM status bit of the status register.

When erase is completed, the erase status bit should be checked. If erase error is detected, the status register should be cleared. The CUI remains in read status register mode until further commands are issued to it.

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, reliable block erasure can only occur when $V_{PP} = V_{PPH}$. In the absence of this high voltage, memory contents are protected against erasure. If block erase is attempted while $V_{PP} = V_{PPL}$, the V_{PP} status bit will be set to "1". Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

4.6 Erase Suspend/Erase Resume Commands

The Erase Suspend command allows block erase interruption in order to read data from another block of memory. Once the erase process starts, writing the Erase Suspend command (B0H) to the CUI requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The LH28F008SA-K/SAH-K continue to output status register data when read, after the Erase Suspend command is written to it. Polling the WSM status and erase suspend status bits will determine when the erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to V_{OH}.

At this point, a Read Array command can be written to the CUI to read data from blocks other than that which is suspended. The only other valid commands at this time are Read Status Register (70H) and Erase Resume (D0H), at which time the WSM will continue with the erase process. The erase suspend status and WSM status bits of the status register will be automatically cleared and RY/BY# will return to V_{OL}. After the Erase Resume command is written to it, the LH28F008SA-K/SAH-K automatically output status register data when read (see **Fig. 4**). V_{PP} must remain at V_{PPH} while the LH28F008SA-K/SAH-K are in erase suspend.

4.7 Byte Write Setup/Write Commands

Byte write is executed by a two-command sequence. The Byte Write Setup command (40H or 10H) is written to the CUI, followed by a second write specifying the address and data (latched on the rising edge of WE#) to be written. The WSM then takes over, controlling the byte write and write verify algorithms internally. After the two-command byte write sequence is written to it, the LH28F008SA-K/SAH-K automatically outputs status register data when read (see **Fig. 3**). The CPU can detect the completion of the byte write event by analyzing the output of the RY/BY# pin, or the WSM status bit of the status register. Only the Read Status Register command is valid while byte write is active.

When byte write is complete, the byte write status bit should be checked. If byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until further commands are issued to it. If byte write is attempted while $V_{PP} = V_{PPL}$, the V_{PP} status bit will be set to "1". Byte write attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

Table 3 Status Register Definition

WSMS	ESS	ES	BWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
- 1 = Ready
- 0 = Busy

SR.6 = ERASE SUSPEND STATUS (ESS)
- 1 = Erase Suspended
- 0 = Erase in Progress/Completed

SR.5 = ERASE STATUS (ES)
- 1 = Error in Block Erase
- 0 = Successful Block Erase

SR.4 = BYTE WRITE STATUS (BWS)
- 1 = Error in Byte Write
- 0 = Successful Byte Write

SR.3 = V_{PP} STATUS (VPPS)
- 1 = V_{PP} Low Detect; Operation Abort
- 0 = V_{PP} OK

SR.2-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES :

RY/BY# or the write state machine status bit must first be checked to determine byte write or block erase completion, before the byte write or erase status bit is checked for success. If the byte write and erase status bits are set to "1"s during a block erase attempt, an improper command sequence was entered. Attempt the operation again.

If V_{PP} low status is detected, the status register must be cleared before another byte write or block erase operation is attempted. The V_{PP} status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the byte write or block erase command sequences have been entered and informs the system if V_{PP} has not been switched on. The V_{PP} status bit is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

SR.2-0 are reserved for future use and should be masked out when polling the status register.

5. EXTENDED BLOCK ERASE/BYTE WRITE CYCLING

The LH28F008SA-K/SAH-K are designed for 100 000 byte write/block erase cycles on each of the sixteen 64 k-byte blocks. Low electric fields, advanced oxides and minimal oxide area per cell subjected to the tunneling electric field combine to greatly reduce oxide stress and the probability of failure. A 20 M-byte solid-state drive using an array of LH28F008SA-K/SAH-K's has a MTBF (Mean Time Between Failure) of 33.3 million hours (NOTE 1), over 600 times more reliable than equivalent rotating disk technology.

NOTE :

1. Assumptions : 10 k-byte file written every 10 minutes. (20 M-byte array)/(10 k-byte file) = 2 000 file writes before erase required. (2 000 files writes/erase) x (100 000 cycles per LH28F008SA-K/SAH-K block) = 200 million file writes. (200 x 10^6 file writes) x (10 min/write) x (1 hr/60 min) = **33.3 x 10^6 MTBF**.

6. AUTOMATED BYTE WRITE

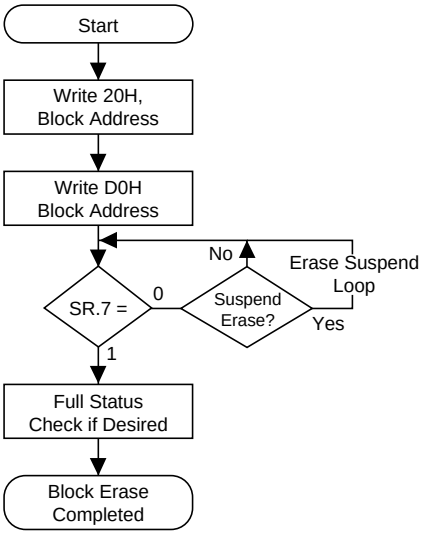
The LH28F008SA-K/SAH-K integrate the quick-pulse programming algorithm using the CUI, status register and WSM. On-chip integration dramatically simplifies system software and provides processor interface timings to the CUI and status register. WSM operation, internal verify and V_{PP} high voltage presence are monitored and reported via the RY/BY# output and appropriate status register bits. **Fig. 3** shows a system software flowchart for device byte write. The entire sequence is performed with V_{PP} at V_{PPH}. Byte write abort occurs when RP# transitions to V_{IL}, or V_{PP} drops to V_{PPL}. Although the WSM is halted, byte data is partially written at the location where byte write was aborted. Block erasure, or a repeat of byte write, is required to initialize this data to a known value.

7. AUTOMATED BLOCK ERASE

As above, the quick-erase algorithm is now implemented internally, including all preconditioning of block data. WSM operation, erase success and V_{PP} high voltage presence are monitored and reported through RY/BY# and the status register. Additionally, if a command other than Erase Confirm is written to the device following erase setup, both the erase status and byte write status bits will be set to "1"s. When issuing the Erase Setup and Erase Confirm commands, they should be written to an address within the address range of the block to be erased. **Fig. 2** shows a system software flowchart for block erase.

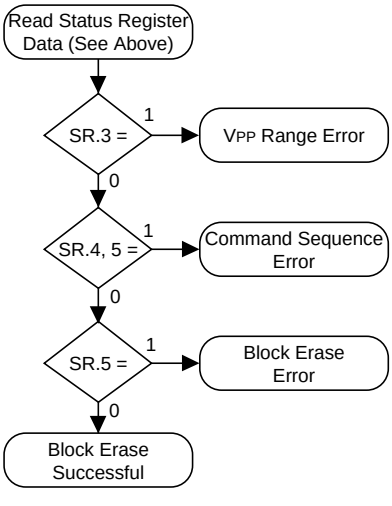
Erase typically takes 1.6 seconds per block. The Erase Suspend/Erase Resume command sequence allows suspension of this erase operation to read data from a block other than that in which erase is being performed. A system software flowchart is shown in **Fig. 4**.

The entire sequence is performed with V_{PP} at V_{PPH}. Abort occurs when RP# transitions to V_{IL} or V_{PP} falls to V_{PPL}, while erase is in progress. Block data is partially erased by this operation, and a repeat of erase is required to obtain a fully erased block.



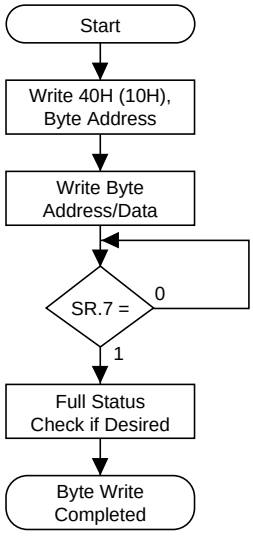
BUS OPERATION	COMMAND	COMMENTS
Write	Erase Setup	Data = 20H Address = Within Block to be Erased
Write	Erase	Data = D0H Address = Within Block to be Erased
Standby/ Read		Check RY/BY# V_{OH} = Ready, V_{OL} = Busy or Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle OE# or CE# to Update Status Register
Repeat for subsequent block erasures. Full status check can be done after each block erase or after a sequence of block erasures. Write FFH after the last block erase operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Optional Read		CPU may already have read status register data in WSM Ready polling above.
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
SR.3 must be cleared, if set during a block erase attempt, before further attempts are allowed by the WSM. SR.5 is only cleared by the Clear Status Register command in cases where multiple blocks are erased before full status is checked. If error is detected, clear the status register before attempting retry or other error recovery.		

Fig. 2 Automated Block Erase Flowchart



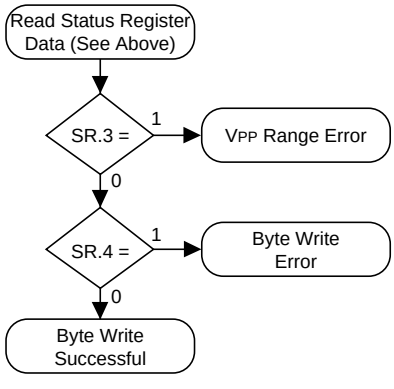
BUS OPERATION	COMMAND	COMMENTS
Write	Byte Write Setup	Data = 40H (10H) Address = Byte to be Wirtten
Write	Byte Write	Data to be written Address = Byte to be Written
Standby/ Read		Check RY/BY# V_{OH} = Ready, V_{OL} = Busy or Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle OE# or CE# to Update Status Register

Repeat for subsequent byte writes.

Full status check can be done after each byte write or after a sequence of byte writes.

Write FFH after the last byte write operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



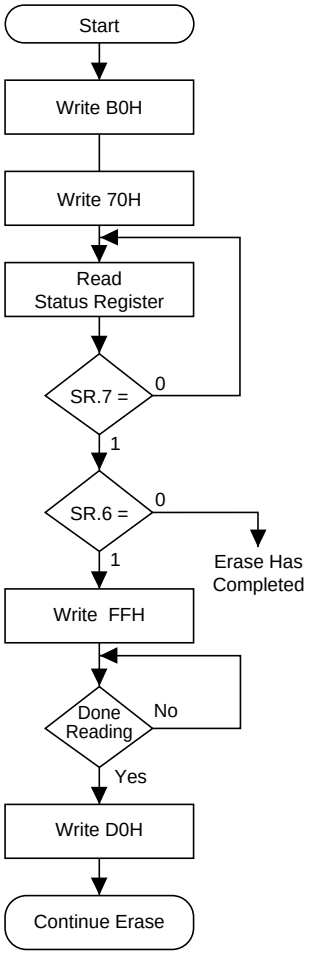
BUS OPERATION	COMMAND	COMMENTS
Optional Read		CPU may already have read status register data in WSM Ready polling above
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = Byte Write Error

SR.3 must be cleared, if set during a byte write attempt before further attempts are allowed by the WSM.

SR.4 is only cleared by the Clear Status Register command in cases where multiple bytes are written before full status is checked.

If error is detected, clear the status register before attempting retry or other error recovery.

Fig. 3 Automated Byte Write Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase Suspend	Data = B0H
Write	Read Status Register	Data = 70H
Standby/ Read		Check RY/BY# V_{OH} = Ready, V_{OL} = Busy or Read Status Register Check SR.7 1 = Ready, 0= Busy Toggle OE# or CE# to Update Status Register
Standby		Check SR.6 1 = Suspended
Write	Read Array	Data = FFH
Read		Read array data from block other than that being erased.
Write	Erase Resume	Data = D0H

Fig. 4 Erase Suspend/Resume Flowchart

8. DESIGN CONSIDERATIONS

8.1 Three-Line Output Control

The LH28F008SA-K/SAH-K will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for :

a) Lowest possible memory power consumption.
b) Complete assurance that data bus contention will not occur.

To efficiently use these control inputs, an address decoder should enable CE#, while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. Finally, RP# should either be tied to the system RESET#, or connected to V_{CC} if unused.

8.2 RY/BY# and Byte Write/Block Erase Polling

RY/BY# is a full CMOS output that provides a hardware method of detecting byte write and block erase completion. It transitions low time t_{WHRL} after a write or erase command sequence is written to the LH28F008SA-K/SAH-K, and returns to V_{OH} when the WSM has finished executing the internal algorithm.

RY/BY# can be connected to the interrupt input of the system CPU or controller. It is active at all times, not tristated if the LH28F008SA-K/SAH-K CE# or OE# inputs are brought to V_{IH}. RY/BY# is also V_{OH} when the device is in erase suspend or deep power-down modes.

8.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues; standby current levels (I_{SB}), active current levels (I_{CC}) and transient peaks produced by falling and rising edges of CE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high frequency, low inherent-inductance capacitors should be placed as close as possible to package leads. Additionally, for every 8 devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

8.4 V_{PP} Trace on Printed Circuit Boards

Writing flash memories, while they reside in the target system, requires that the printed circuit board designers pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for writing and erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

8.5 V_{CC}, V_{PP}, RP# Transitions and the Command/Status Registers

Byte write and block erase completion are not guaranteed if V_{PP} drops below V_{PPH}. If the V_{PP} status bit of the status register (SR.3) is set to "1", a Clear Status Register command must be issued before further byte write/block erase attempts are allowed by the WSM. Otherwise, the byte write (SR.4) or erase (SR.5) status bits of the status register will be set to "1"s if error is detected. RP# transitions to V_{IL} during byte write and block erase also abort the operations. Data is partially altered in either case, and the command sequence must be repeated after normal operation is restored. Device power-off, or RP# transitions to V_{IL}, clear the status register to initial value 10000 for the upper 5 bits.

The CUI latches commands as issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its state upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}, is read array mode.

After byte write or block erase is complete, even after V_{PP} transitions down to V_{PPL}, the CUI must be reset to read array mode via the Read Array command if access to the memory array is desired.

8.6 Power Up/Down Protection

The LH28F008SA-K/SAH-K are designed to offer protection against accidental block erasure or byte writing during power transitions. Upon power-up, the LH28F008SA-K/SAH-K are indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. Power supply sequencing is not required. Internal circuitry in the LH28F008SA-K/SAH-K ensure that the CUI is reset to the read array mode on power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

Finally, the device is disabled until RP# is brought to V_{IH}, regardless of the state of its control inputs. This provides an additional level of memory protection.

8.7 Power Consumption

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases usable battery life, because the LH28F008SA-K/SAH-K do not consume any power to retain code or data when the system is off.

In addition, the LH28F008SA-K/SAH-K's deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable PCs and other power sensitive applications, using an array of LH28F008SA-K/SAH-K's for solid-state storage, can lower RP# to V_{IL} in standby or sleep modes, producing negligible power consumption. If access to the LH28F008SA-K/SAH-K are again needed, the part can again be read, following the t_{PHQV} and t_{PHWL} wakeup cycles required after RP# is first raised to V_{IH}. See **Section 9.2.4 through 6.2.6 "AC CHARACTERISTICS - READ-ONLY and WRITE OPERATIONS"** and **Fig. 8**, **Fig. 9** and **Fig. 10** for more information.

9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings*

Operating Temperature

- LH28F008SA-K
  During Read, Block Erase
  and Byte Write ····· 0 to +70°C (NOTE 1)
  Temperature Under Bias ····· –10 to +80°C

- LH28F008SAH-K
  During Read, Block Erase
  and Byte Write ····· –25 to +85°C (NOTE 2)
  Temperature Under Bias ····· –25 to +85°C

Storage Temperature ····· –65 to +125°C

Voltage on Any Pin
(except V_{CC} and V_{PP}) ····· –2.0 to +7.0 V (NOTE 3)

V_{CC} Supply Voltage ····· –2.0 to +7.0 V (NOTE 3)

V_{PP} Program Voltage
During Block Erase
and Byte Write ····· –2.0 to +14.0 V (NOTE 3, 4)

Output Short Circuit Current ····· 100 mA (NOTE 5)

NOTICE : The specifications are subject to change without notice. Verify with your local SHARP sales office that you have the latest datasheet before finalizing a design.

**WARNING : Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES :

1. Operating temperature is for commercial product defined by this specification.
2. Operating temperature is for extended temperature product defined by this specification.
3. All specified voltages are with respect to GND. Minimum DC voltage is –0.5 V on input/output pins and –0.2 V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to –2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins, V_{CC} and RP# pins are V_{CC}+0.5 V which, during transitions, may overshoot to V_{CC}+2.0 V for periods < 20 ns.
4. Maximum DC voltage on V_{PP} may overshoot to +14.0 V for periods < 20 ns.
5. Output shorted for no more than one second. No more than one output shorted at a time.

9.2 Operating Conditions

SYMBOL	PARAMETER	NOTE	MIN.	MAX.	UNIT	VERSIONS
T_A	Operating Temperature	1	0	+70	°C	LH28F008SA-K
			–25	+85	°C	LH28F008SAH-K
V_{CC}	V_{CC} Supply Voltage (5.0±0.25 V)		4.75	5.25	V	LH28F008SA-K85/SAH-K85
V_{CC}	V_{CC} Supply Voltage (5.0±0.5 V)		4.50	5.50	V	

NOTE :

1. Test conditions : Ambient temperature

9.2.1 CAPACITANCE (NOTE 1)

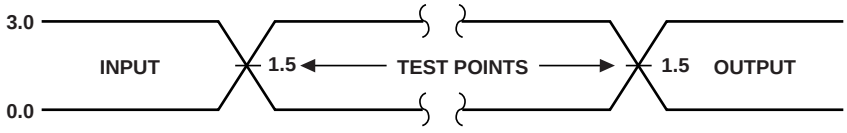
T_A = +25°C, f = 1 MHz

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITION
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0 V

NOTE :

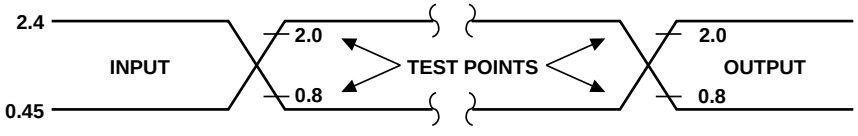
1. Sampled, not 100% tested.

9.2.2 AC INPUT/OUTPUT TEST CONDITIONS



AC test inputs are driven at 3.0 V for a Logic "1" and 0.0 V for a Logic "0". Input timing begins, and output timing ends, at 1.5 V. Input rise and fall times (10% to 90%) < 10 ns.

Fig. 5 Transient Input/Output Reference Waveform for V_{CC} = 5.0±0.25 V (High Speed Testing Configuration)



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) < 10 ns.

Fig. 6 Transient Input/Output Reference Waveform for V_{CC} = 5.0±0.5 V (Standard Testing Configuration)

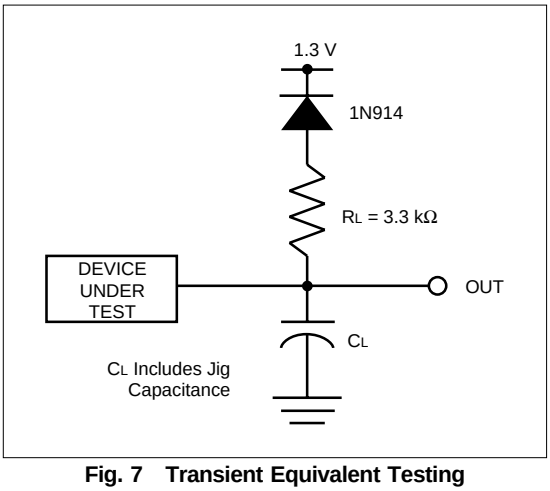


Fig. 7 Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

TEST CONFIGURATION	C_L (pF)
V_{CC} = 5.0±0.25 V (NOTE 1)	30
V_{CC} = 5.0±0.5 V	100

NOTE :

1. Applied to high speed products, LH28F008SA-K85 and LH28F008SAH-K85.

9.2.3 DC CHARACTERISTICS

SYMBOL	PARAMETER		NOTE	V_{CC} = 5.0±0.5 V			UNIT	TEST CONDITION
				MIN.	TYP.	MAX.		
I_{LI}	Input Load Current		1			±1.0	µA	V_{CC} = V_{CC} Max. V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current		1			±10	µA	V_{CC} = V_{CC} Max. V_{OUT} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current		1, 3		30	100	µA	CMOS Inputs V_{CC} = V_{CC} Max. CE# = RP# = V_{CC}±0.2 V
					1.0	2.0	mA	TTL Inputs V_{CC} = V_{CC} Max. CE# = RP# = V_{IH}
I_{CCD}	V_{CC} Deep Power-Down Current	LH28F008SA-K	1		0.2	10	µA	RP# = GND±0.2 V I_{OUT} (RY/BY#) = 0 mA
		LH28F008SAH-K			0.2	20		
I_{CCR}	V_{CC} Read Current		1		20	35	mA	CMOS Inputs V_{CC} = V_{CC} Max. CE# = GND f = 8 MHz, I_{OUT} = 0 mA
					25	50	mA	TTL Inputs V_{CC} = V_{CC} Max. CE# = V_{IL} f = 8 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Byte Write Current		1		10	30	mA	Byte Write in Progress
I_{CCE}	V_{CC} Block Erase Current		1		10	30	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current		1, 2		5	10	mA	Block Erase Suspended CE# = V_{IH}
I_{PPS}	V_{PP} Standby Current		1			+15/–300	µA	V_{PP} = GND
I_{PPD}	V_{PP} Deep Power-Down Current		1		0.1	5.0	µA	RP# = GND±0.2 V
I_{PPR}	V_{PP} Read Current		1			200	µA	V_{PP} > V_{CC}
I_{PPW}	V_{PP} Byte Write Current		1		10	30	mA	V_{PP} = V_{PPH} Byte Write in Progress
I_{PPE}	V_{PP} Block Erase Current		1		10	30	mA	V_{PP} = V_{PPH} Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current		1		90	200	µA	V_{PP} = V_{PPH} Block Erase Suspended

9.2.3 DC CHARACTERISTICS (contd.)

SYMBOL	PARAMETER	NOTE	V_{CC} = 5.0±0.5 V			UNIT	TEST CONDITIONS
			MIN.	TYP.	MAX.		
V_{IL}	Input Low Voltage		–0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	3			0.45	V	V_{CC} = V_{CC} MIN. I_{OL} = 5.8 mA
V_{OH1}	Output High Voltage (TTL)	3	2.4			V	V_{CC} = V_{CC} MIN. I_{OH} = –2.5 mA
V_{OH2}	Output High Voltage (CMOS)		0.85 V_{CC}			V	V_{CC} = V_{CC} MIN. I_{OH} = –2.5 mA
			V_{CC}–0.4				V_{CC} = V_{CC} MIN. I_{OH} = –100 µA
V_{PPL}	V_{PP} Voltage during Normal Operations	4	0.0		6.5	V	
V_{PPH}	V_{PP} Voltage during Erase/Write Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.0			V	

NOTES :

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0 V, V_{PP} = 12.0 V, T_A = +25°C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device deselected. If reading in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Includes RY/BY#.
4. Block erases/byte writes are inhibited when V_{PP} = V_{PPL} and not guaranteed in the range between V_{PPH} and V_{PPL}.

9.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS (NOTE 1)

• V_{CC} = 5.0±0.25 V, 5.0±0.5 V, T_A = 0 to+70°C or –25 to +85°C

VERSIONS				V_{CC}±0.25 V (NOTE 4) LH28F008SA-K85 LH28F008SAH-K85						UNIT
				V_{CC}±0.5 V		(NOTE 5) LH28F008SA-K85 LH28F008SAH-K85		(NOTE 5) LH28F008SA-K12 LH28F008SAH-K12		
SYMBOL		PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{AVAV}	t_{RC}	Read Cycle Time		85		90		120		ns
t_{AVQV}	t_{ACC}	Address to Output Delay			85		90		120	ns
t_{ELQV}	t_{CE}	CE# to Output Delay	2		85		90		120	ns
t_{PHQV}	t_{PWH}	RP# High to Output Delay			400		400		400	ns
t_{GLQV}	t_{OE}	OE# to Output Delay	2		40		45		50	ns
t_{ELQX}	t_{LZ}	CE# to Output Low Z	3	0		0		0		ns
t_{EHQZ}	t_{HZ}	CE# High to Output High Z	3		55		55		55	ns
t_{GLQX}	t_{OLZ}	OE# to Output Low Z	3	0		0		0		ns
t_{GHQZ}	t_{DF}	OE# High to Output High Z	3		30		30		30	ns
	t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		0		ns

NOTES :

1. See AC Input/Output Reference Waveform (**Fig. 5** and **Fig. 6**) for timing measurements.
2. OE# may be delayed up to t_{CE}-t_{OE} after the falling edge of CE# without impact on t_{CE}.
3. Sampled, not 100% tested.
4. See **Fig. 5 "Transient Input/Output Reference Waveform"** and **Fig. 7 "Transient Equivalent Testing Load Circuit"** (High Speed Configuration) for testing characteristics.
5. See **Fig. 6 "Transient Input/Output Reference Waveform"** and **Fig. 7 "Transient Equivalent Testing Load Circuit"** (Standard Configuration) for testing characteristics.

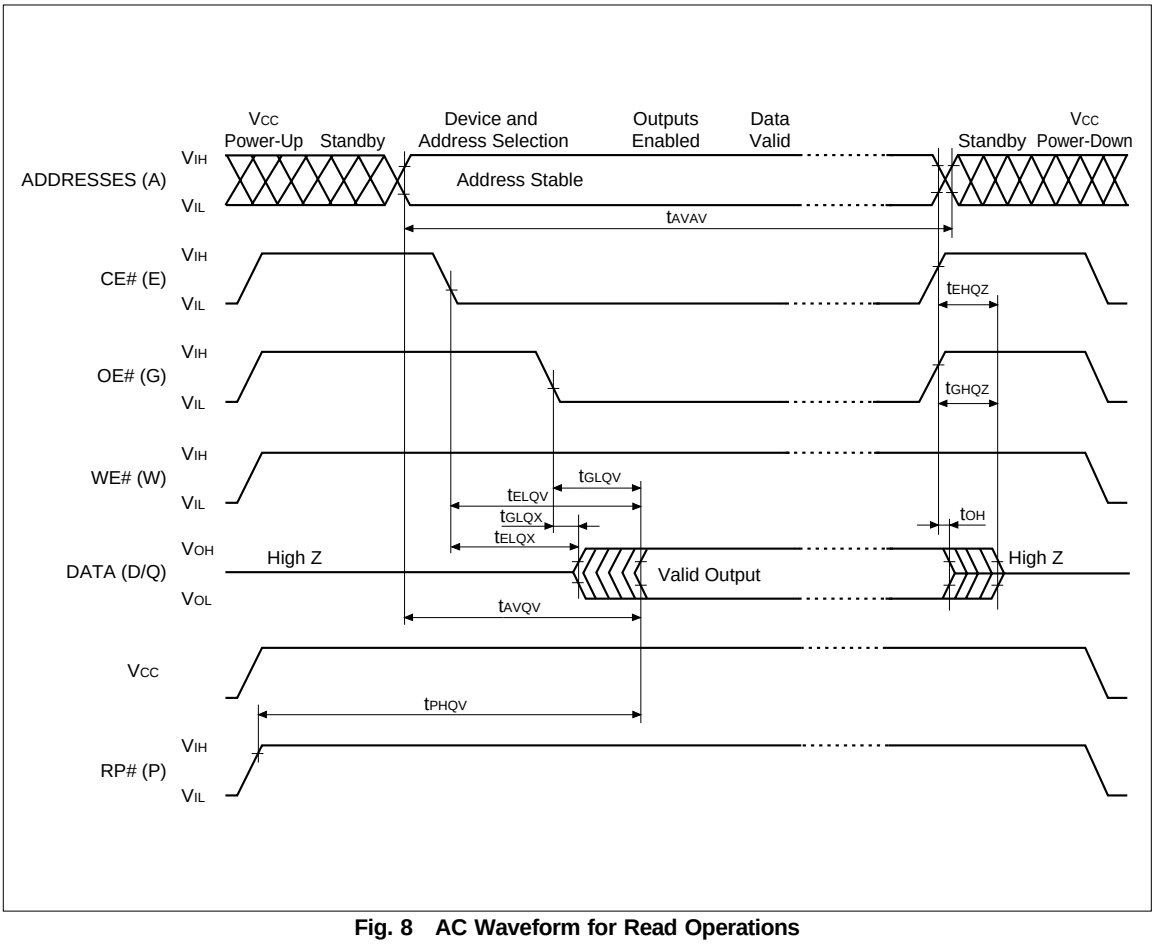


Fig. 8 AC Waveform for Read Operations

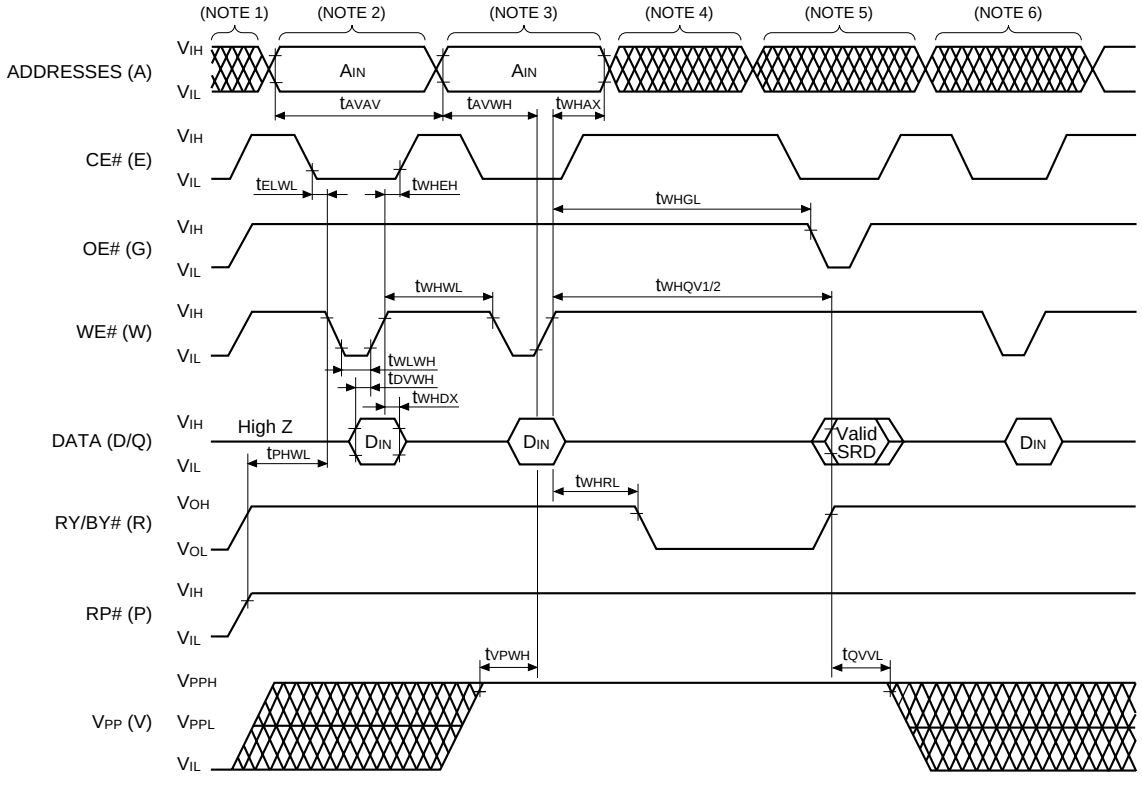
9.2.5 AC CHARACTERISTICS - WRITE OPERATIONS (NOTE 1)

• V_{CC} = 5.0±0.25 V, 5.0±0.5 V, T_A = 0 to +70°C or –25 to +85°C

VERSIONS			V_{CC}±0.25 V	(NOTE 7) LH28F008SA-K85 LH28F008SAH-K85						UNIT
			V_{CC}±0.5 V			(NOTE 8) LH28F008SA-K85 LH28F008SAH-K85		(NOTE 8) LH28F008SA-K12 LH28F008SAH-K12		
SYMBOL		PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{AVAV}	t_{WC}	Write Cycle Time		85		90		120		ns
t_{PHWL}	t_{PS}	RP# High Recovery to WE# Going Low	2	1		1		1		µs
t_{ELWL}	t_{CS}	CE# Setup to WE# Going Low		10		10		10		ns
t_{WLWH}	t_{WP}	WE# Pulse Width		40		40		40		ns
t_{VPWH}	t_{VPS}	V_{PP} Setup to WE# Going High	2	100		100		100		ns
t_{AVWH}	t_{AS}	Address Setup to WE# Going High	3	40		40		40		ns
t_{DVWH}	t_{DS}	Data Setup to WE# Going High	4	40		40		40		ns
t_{WHDX}	t_{DH}	Data Hold from WE# High		5		5		5		ns
t_{WHAX}	t_{AH}	Address Hold from WE# High		5		5		5		ns
t_{WHEH}	t_{CH}	CE# Hold from WE# High		10		10		10		ns
t_{WHWL}	t_{WPH}	WE# Pulse Width High		30		30		30		ns
t_{WHRL}		WE# High to RY/BY# Going Low			100		100		100	ns
t_{WHQV1}		Duration of Byte Write Operation	5, 6	6		6		6		µs
t_{WHQV2}		Duration of Block Erase Operation	5, 6	0.3		0.3		0.3		s
t_{WHGL}		Write Recovery before Read		0		0		0		ns
t_{QVVL}	t_{VPH}	V_{PP} Hold from Valid SRD, RY/BY# High	2, 6	0		0		0		ns

NOTES :

1. Read timing characteristics during erase and byte write operations are the same as during read-only operations. Refer to **Section 9.2.4 "AC CHARACTERISTICS"** for read-only operations.
2. Sampled, not 100% tested.
3. Refer to **Table 2** for valid A_{IN} for byte write or block erasure.
4. Refer to **Table 2** for valid D_{IN} for byte write or block erasure.
5. The on-chip WSM incorporates all byte write and block erase system functions and overhead of standard SHARP flash memory, including byte program, verify (byte write) and block precondition, precondition verify, erase and erase verify (block erase).
6. Byte write and block erase durations are measure to completion (SR.7 = 1, RY/BY# = V_{OH}). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR.3/4/5 = 0).
7. See **Fig. 5 "Transient Input/Output Reference Waveform"** and **Fig. 7 "Transient Equivalent Testing Load Circuit"** (High Speed Configuration) for testing characteristics.
8. See **Fig. 6 "Transient Input/Output Reference Waveform"** and **Fig. 7 "Transient Equivalent Testing Load Circuit"** (Standard Configuration) for testing characteristics.



NOTES :

1. V_{CC} power-up and standby.
2. Write Byte Write or Erase Setup command.
3. Write valid address and data (byte write) or Erase Confirm command.
4. Automated byte write or erase delay.
5. Read status register data.
6. Write Read Array command.

Fig. 9 AC Waveform for WE#-Controlled Write Operations

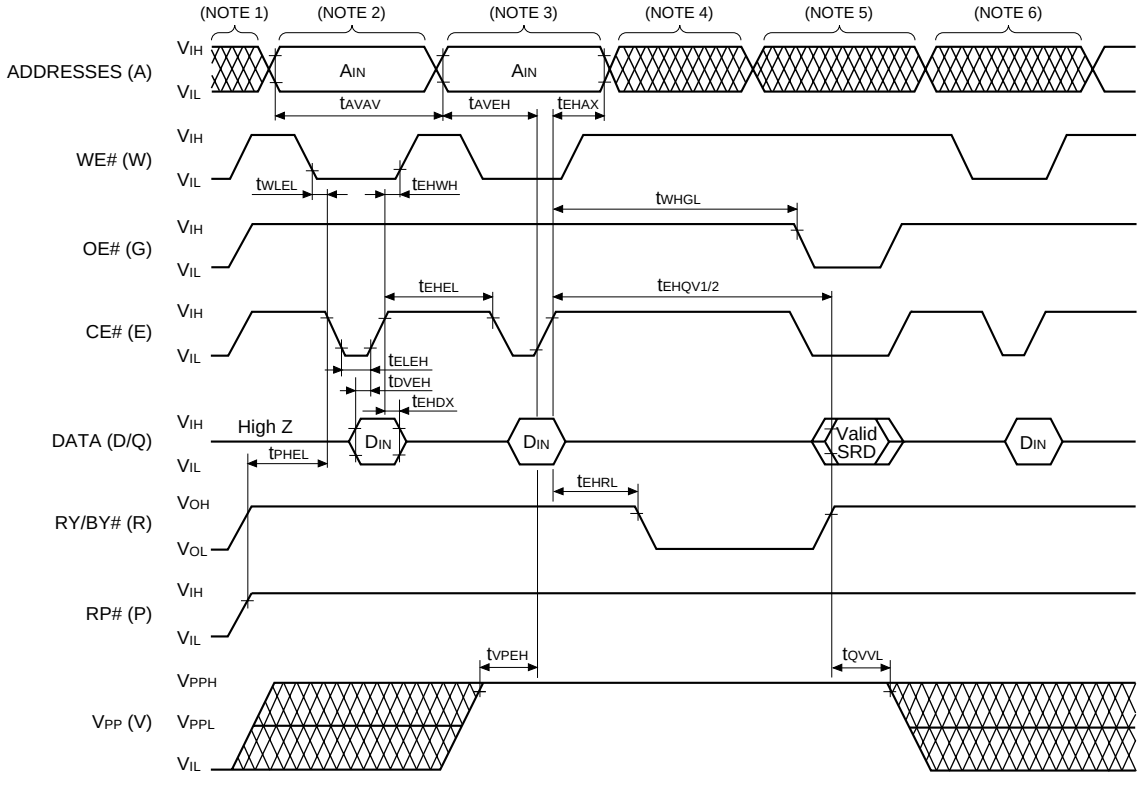
9.2.6 ALTERNATIVE CE#-CONTROLLED WRITES (NOTE 1)

• V_{CC} = 5.0±0.25 V, 5.0±0.5 V, T_A = 0 to +70°C or –25 to +85°C

VERSIONS			V_{CC}±0.25 V	(NOTE 6) LH28F008SA-K85 LH28F008SAH-K85						UNIT
			V_{CC}±0.5 V			(NOTE 7) LH28F008SA-K85 LH28F008SAH-K85		(NOTE 7) LH28F008SA-K12 LH28F008SAH-K12		
SYMBOL		PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{AVAV}	t_{WC}	Write Cycle Time		85		90		120		ns
t_{PHEL}	t_{PS}	RP# High Recovery to CE# Going Low	2	1		1		1		µs
t_{WLEL}	t_{WS}	WE# Setup to CE# Going Low		0		0		0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width		50		50		50		ns
t_{VPEH}	t_{VPS}	V_{PP} Setup to CE# Going High	2	100		100		100		ns
t_{AVEH}	t_{AS}	Address Setup to CE# Going High	3	40		40		40		ns
t_{DVEH}	t_{DS}	Data Setup to CE# Going High	4	40		40		40		ns
t_{EHDX}	t_{DH}	Data Hold from CE# High		5		5		5		ns
t_{EHAX}	t_{AH}	Address Hold from CE# High		5		5		5		ns
t_{EHWH}	t_{WH}	WE# Hold from CE# High		0		0		0		ns
t_{EHEL}	t_{EPH}	CE# Pulse Width High		25		25		25		ns
t_{EHRL}		CE# High to RY/BY# Going Low			100		100		100	ns
t_{EHQV1}		Duration of Byte Write Operation	5	6		6		6		µs
t_{EHQV2}		Duration of Block Erase Operation	5	0.3		0.3		0.3		s
t_{EHGL}		Write Recovery before Read		0		0		0		ns
t_{QVVL}	t_{VPH}	V_{PP} Hold from Valid SRD, RY/BY# High	2, 5	0		0		0		ns

NOTES :

1. Chip-Enable Controlled Writes : Write operations are driven by the valid combination of CE# and WE#. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to **Table 2** for valid A_{IN} for byte write or block erasure.
4. Refer to **Table 2** for valid D_{IN} for byte write or block erasure.
5. Byte write and block erase durations are measure to completion (SR.7 = 1, RY/BY# = V_{OH}). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR.3/4/5 = 0).
6. See **Fig. 5 "Transient Input/Output Reference Waveform"** and **Fig. 7 "Transient Equivalent Testing Load Circuit"** (High Speed Configuration) for testing characteristics.
7. See **Fig. 6 "Transient Input/Output Reference Waveform"** and **Fig. 7 "Transient Equivalent Testing Load Circuit"** (Standard Configuration) for testing characteristics.



NOTES :

1. V_{CC} power-up and standby.
2. Write Byte Write or Erase Setup command.
3. Write valid address and data (byte write) or Erase Confirm command.
4. Automated byte write or erase delay.
5. Read status register data.
6. Write Read Array command.

Fig. 10 AC Waveform for CE#-Controlled Write Operations

9.2.7 RESET OPERATIONS

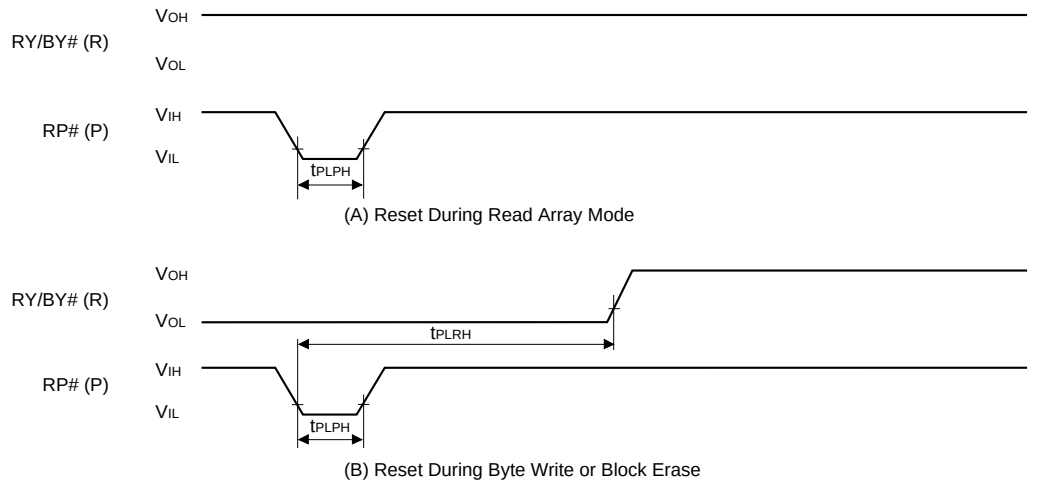


Fig. 11 AC Waveform for Reset Operation

Reset AC Specifications (NOTE 1)

SYMBOL	PARAMETER	NOTE	V_{CC} = 5.0±0.5 V		UNIT
			MIN.	MAX.	
t_{PLPH}	RP# Pulse Low Time (If RP# is tied to V_{CC}, this specification is not applicable)		100		ns
t_{PLRH}	RP# Low to Reset during Block Erase or Byte Write (If RP# is tied to V_{CC}, this specification is not applicable)	2, 3		12	µs

NOTES :

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase or byte write operation is not executing, the reset will complete within 100 ns.
3. A reset time, t_{PHQV}, is required from the latter of RY/BY# or RP# going high until outputs are valid.

9.2.8 BLOCK ERASE AND BYTE WRITE PERFORMANCE

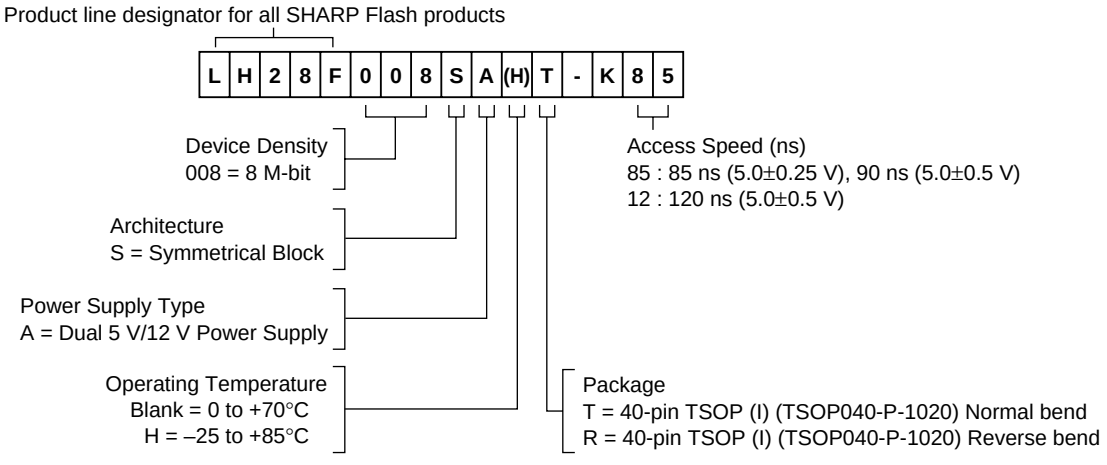
• V_{CC} = 5.0±0.25 V, 5.0±0.5 V, T_A = 0 to +70°C or –25 to +85°C

PARAMETER	NOTE	V_{PP} = 12.0±0.6 V			UNIT
		MIN.	TYP. (NOTE 1)	MAX.	
Block Erase Time	2		1.6	10	s
Block Write Time	2		0.6	2.1	s
Byte Write Time			8	(NOTE 3)	µs

NOTES :

1. 25°C, 12.0 V V_{PP}.
2. Excludes system-level overhead.
3. Contact your SHARP representative for information on the maximum byte write specification.

10 ORDERING INFORMATION



OPTION	ORDER CODE	VALID OPERATIONAL COMBINATIONS	
		V_{CC} = 5.0±0.5 V 100 pF load, TTL I/O Levels	**V_{CC} = 5.0±0.25 V 30 pF load, 1.5 V I/O Levels**
1	LH28F008SAXX-K85	90 ns	85 ns
2	LH28F008SAXX-K12	120 ns	

40 TSOP (TSOP040-P-1020)