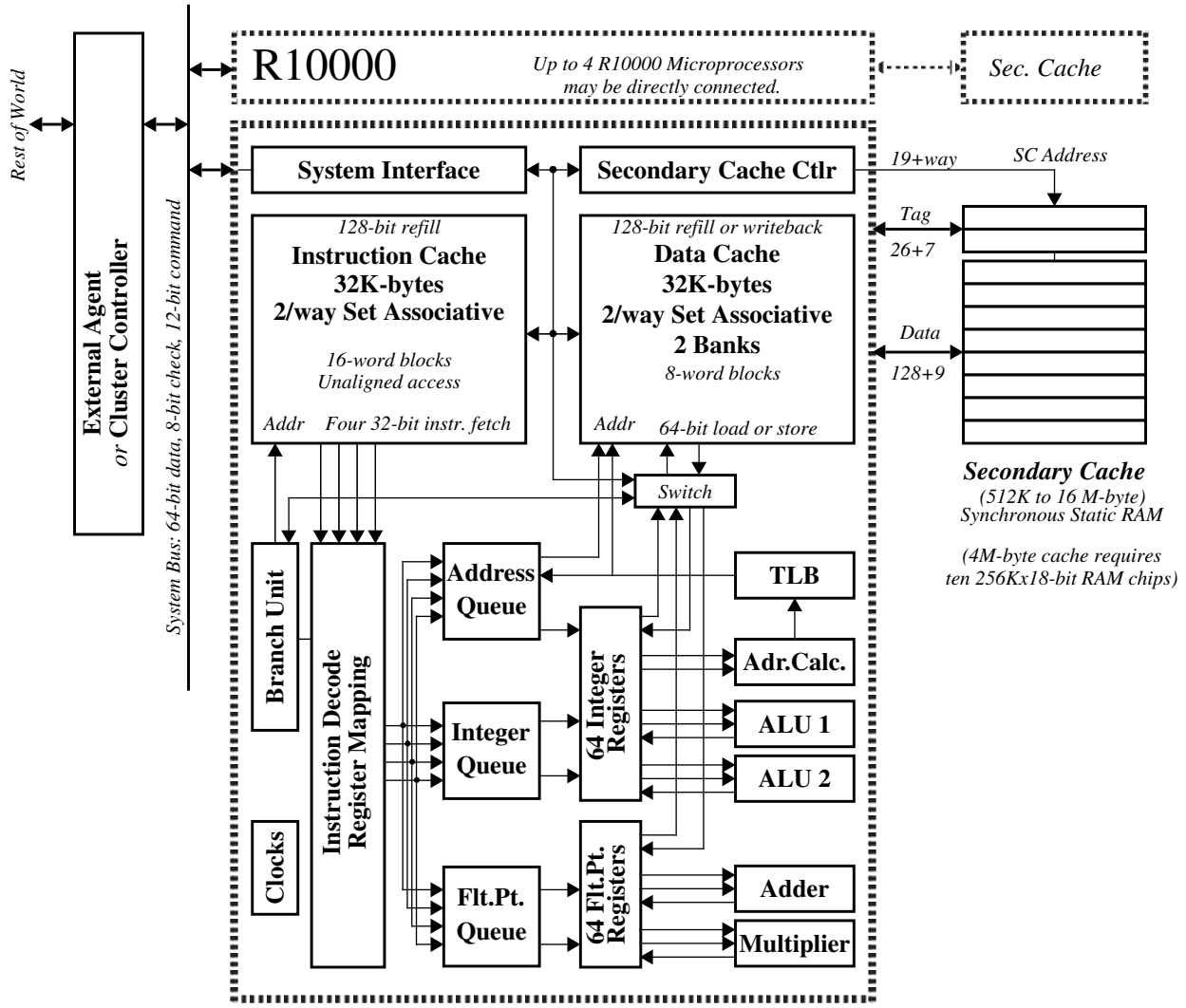
Rest of World
External Agent
or Cluster Controller
System Bus: 64-bit data, 8-bit check, 12-bit command
R10000
Up to 4 R10000 Microprocessors
may be directly connected.
Sec. Cache
System Interface
Secondary Cache Ctlr
19+way
SC Address
Tag
26+7
Data
128+9
128-bit refill
Instruction Cache
32K-bytes
2/way Set Associative
16-word blocks
Unaligned access
Addr
Four 32-bit instr. fetch
128-bit refill or writeback
Data Cache
32K-bytes
2/way Set Associative
2 Banks
8-word blocks
Addr
64-bit load or store
Switch
Secondary Cache
(512K to 16 M-byte)
Synchronous Static RAM
(4M-byte cache requires
ten 256Kx18-bit RAM chips)
Branch Unit
Clocks
Instruction Decode
Register Mapping
Address
Queue
Integer
Queue
Flt.Pt.
Queue
64 Integer
Registers
64 Flt.Pt.
Registers
TLB
Adr.Calc.
ALU 1
ALU 2
Adder
Multiplier