Hardware

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Chapter 1

Hardware

1.1 Amiga® Hardware Reference Manual: C Enhanced Chip Set

This appendix contains information on the Enhanced Chip Set (ECS). ↩
The
Enhanced Chip Set consists of the Agnus (8372-R3) and Denise (8373-R3) custom Amiga chips. These chip revisions support advanced features in addition to all of the standard features previously available.

The ECS is standard in the A3000. The enhanced Agnus and Denise chips are plug-compatible replacements for the originals in the A500 or A2000. There are no provisions for installing the ECS in the original A1000. The A2000, when jumpered for one megabyte of chip memory, will function normally with the ECS chips installed, under both V1.3 and V2.0 Amiga System software.

The ECS chips are designed to function with either NTSC or PAL Amigas. However, the chips from the US factory are configured for NTSC mode. In order to use them on a PAL system, you may have to reset the motherboard jumpers for proper performance.

1.2 C Enhanced Chip Set / New Features of the Enhanced Chip Set

The new features of the Enhanced Chip Set are as follows:

New Blitter Range

New Genlock Capabilities

New Mode Resolutions

Built-in A2024 support

1.3 C / New Features of the Enhanced Chip Set / New Memory Limits

The A3000 has 1 MB of Chip memory, and with proper jumpering of the motherboard, an additional 1 MB can be added. On the A2000, the enhanced Agnus can access up to 1 megabyte of Chip memory with proper jumpering of the motherboard. This provides programs with more blitter-accessible memory for animation and graphics applications.

1.4 C / New Features of the Enhanced Chip Set / New Blitter Range

The enhanced Agnus provides rectangular blits up to 32k by 32k pixels in size.

1.5 C / New Features of the Enhanced Chip Set / New Mode Resolutions

The enhanced Denise chip provides the new SuperHires mode with up to 1280 horizontal pixels per scanline on a standard NTSC or PAL display.

All of the standard display resolutions and depths of the original chip set are supported with the ECS.

1.6 C / New Features of the Enhanced Chip Set / New Monitor Scan Rates

The V2.0 Kickstart and ECS chips support a new high resolution Productivity mode. With the addition of a multi-sync monitor, this mode allows 640 x 480, non-interlaced screens in up to four colors. All programs which open and operate in the Workbench screen will automatically benefit from Productivity text and graphics. In addition, new programs can open their own Productivity screens in a system standard fashion.

1.7 C / New Features of the Enhanced Chip Set / New Genlock Capabilities

```
                The enhanced Denise chip provides the following four
                 new genlock
                features:
```

- Chromakey
- BitPlaneKey
- BorderBlank
- BorderNotTransparent

```
ChromaKey allows any color register to control the video overlay.
BitPlaneKey allows any bitplane to enable the video overlay. BorderBlank
creates a transparent "frame" surrounding the active area.
BorderNotTransparent makes an opaque "frame" surrounding the active area.
```

1.8 C / New Features of the Enhanced Chip Set / Built-in A2024 Support

```
Version 2.0 Kickstart ROMS have built-in support for the A2024
scan-converter monitor which displays 1008 x 800 pixels (1008 x 1024 in
PAL mode) in four monochrome levels, non-interlaced.  In conjunction with
1 megabyte of Chip memory, this allows very high resolution Workbench
screens, as well as support for "full page" text and CAD applications.
```

1.9 C Enhanced Chip Set / ECS Hardware and the Graphics Library

```
                The Enhanced Chip Set consists of compatible revisions to the  ↩
                   Agnus and
Denise custom chips.  The V36 graphics.library software makes it possible
for these chips to display images in new resolutions, at new monitor scan
rates and with new sprite and genlock abilities.

With the enhanced Agnus, the V36 graphics.library supports the new
programmable scan rate registers to provide multi-sync and bi-sync monitor
capability. The new SuperHires mode provides 35ns pixel rates and sprite
positioning at 70ns rates.  Support for big blits (up to 32k x 32k) is
provided for all graphics functions if the ECS Agnus is present.

With the enhanced Denise, the V36 graphics.library provides display window
start and stop with explicit control over larger ranges than was possible
before.  There are new color register interpretations as part of the
SuperHires mode.  Genlock control has been expanded for more flexibility.
Borders may be explicitly transparent or opaque, color registers other
than zero can control video overlay and a bitplane mask may be used for
special-purpose video masking concurrently with the other genlock features.

   Warning:
   --------
   With these new features come certain  new responsibilities when
   using the graphics.library.
```

1.10 C / ECS Hardware and the Graphics Library / Determining Chip Revisions

The V36 graphics.library field GfxBase->ChipRevBits0 contains bit definitions to tell you whether ECS is currently installed and activated. These bits are derived from the new or changed registers in the ECS chips.

The bit GFXF_HR_AGNUS indicates that enhanced HiRes Agnus is installed. This is derived from the Agnus VPOSR register. The VPOSR register is defined as follows:

```
   VPOSR - Read vertical most significant bits (and frame flop)

    Bit   15 14 13 12 11 10 09 08  07 06 05 04 03  02 01 00
    Use  LOF I6 I5 I4 I3 I2 I1 I0 LOL -- -- -- -- v10 v9 V8
```

I0-I6 (bits 8-14) provide the chip identification. At present there are four possible settings. A value of 20 or 30 indicates that the enhanced Hires Agnus is present.

```
   8361 (regular NTSC) or 8370 (fat NTSC) = 10 for NTSC Agnus
   8367 (regular PAL)  or 8371 (fat PAL)  = 00 for PAL Agnus
   8368 (hr)           or 8372 (fat-hr)   = 20 for PAL, 30 for NTSC
```

Similarly, the graphics.library flag GFXF_HR_DENISE is derived from the Denise register DENISEID. This is a new register which can have one of two values. The original Denise (8362) does not have this register, so whatever value is left over on the bus from the last cycle will be there. The enhanced HighRes Denise (8373) will return $FC in the lower 8 bits. The upper 8 bits are reserved.

1.11 C / ECS Hardware and the Graphics Library / SuperHires Mode

```
                SuperHires mode provides a 35ns pixel display rate - twice the  ↩
                   horizontal
resolution of Hires mode, and four times the Lores rates. The nominal
resolution of a SuperHires viewport is 1280 pixels. The maximum plane
depth for a SuperHires viewport is 2 bitplanes which saturates DMA
bandwidth as much as four Hires bitplanes. This mode is controlled by the
graphics.library by writing to the BPLCON0 register in the LOF copperlist
(/SHF if interlaced).

   BPLCON0  chg  W  A,D  Bitplane control register (misc control bits)

            Bit      Use
            ---      ---
            15       HIRES       Set it to zero if SHRES enabled
            14       BPU2 \
            13       BPU1  }     Depth of SuperHires mode (1 or 2)
            12       BPU0 /
            11       HAM         Incompatible w/ SuperHires mode
            10       DPF         Compatible with SuperHires mode
            09
            08
            07
            06       SHRES       SuperHires 35ns pixel enable bit
            05       BPLHWRM
            04       SPRHWRM
            03       LPEN        Compatible with SuperHires mode
            02       LACE        Compatible with SuperHires mode
            01

                 00
                   Warning:
   --------
   Programmers must not rely on interpreting ViewPort->Modes bits
   directly when determining the mode of a ViewPort.

   Beginning with the V36 graphics.library, the ViewPort->Modes field is
   used for backward compatibility only.

   Under V1.3 and earlier the ViewPort->Modes field mirrored some of the
   BPLCON0 bits most notably Hires and Lace. However, other logical
   defines in this field such as the Viewport->Modes PF2PRI bit conflict
   with the SHRES bit assignment in the actual hardware.

   For this reason, in release 2.0 of the operating system
   (graphics.library V36 and later), programmers will need to use the
   new DataBase/ModeID scheme to determine their ViewPort's mode, and to
   specify a mode when creating, cloning, or copying ViewPorts.
```

1.12 C / ECS Graphics Library / SuperHires Mode and Denise Color Registers

```
SuperHires mode has a coarser granularity of color control than either
```

Hires or Lores modes. This is because the timing of color conversions at these very high pixel rates requires special "tricks". There are only two bits of red, green and blue color resolution per hires pixel.

In order to decode sprite and bitplane color information in SuperHires mode, certain multiplexing occurs in the use of the registers. Instead of 4 bits of red, green, and blue for bitplane registers 0-3 stored as 0x0RGB in four color registers, SuperHires bitplane colors are specially encoded in the sixteen lower color registers:

	R	G	B
Bitplane (Color 0) :	ab--	cd--	ef--
Bitplane (Color 1) :	gh--	ij--	kl--
Bitplane (Color 2) :	mn--	op--	qr--
Bitplane (Color 3) :	st--	uv--	wx--

	BIT	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
C	00	.	.	.	.	a	b	a	b	c	d	c	d	e	f	e	f
O	01	.	.	.	.	g	h	a	b	i	j	c	d	k	l	e	f
L	02	.	.	.	.	m	n	a	b	o	p	c	d	q	r	e	f
O	03	.	.	.	.	s	t	a	b	u	v	c	d	w	x	e	f
R	04	.	.	.	.	a	b	g	h	c	d	i	j	e	f	k	l
	05	.	.	.	.	g	h	g	h	i	j	i	j	k	l	k	l
R	06	.	.	.	.	m	n	g	h	o	p	i	j	q	r	k	l
E	07	.	.	.	.	s	t	g	h	u	v	i	j	w	x	k	l
G	08	.	.	.	.	a	b	m	n	c	d	o	p	e	f	q	r
I	09	.	.	.	.	g	h	m	n	i	j	o	p	k	l	q	r
S	0A	.	.	.	.	m	n	m	n	o	p	o	p	q	r	q	r
T	0B	.	.	.	.	s	t	m	n	u	v	o	p	w	x	q	r
E	0C	.	.	.	.	a	b	s	t	c	d	u	v	e	f	w	x
R	0D	.	.	.	.	g	h	s	t	i	j	u	v	k	l	w	x
	0E	.	.	.	.	m	n	s	t	o	p	u	v	q	r	w	x
	0F	.	.	.	.	s	t	s	t	u	v	u	v	w	x	w	x

SuperHires sprites are encoded in the upper sixteen color registers using a similar scheme:

	R	G	B
Sprite (Color 16) :	AB--	CD--	EF--
Sprite (Color 17) :	GH--	IJ--	KL--
Sprite (Color 18) :	MN--	OP--	QR--
Sprite (Color 19) :	ST--	UV--	WX--

	BIT	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
C	10	.	.	.	.	A	B	A	B	C	D	C	D	E	F	E	F
O	11	.	.	.	.	G	H	A	B	I	J	C	D	K	L	E	F
L	12	.	.	.	.	M	N	A	B	O	P	C	D	Q	R	E	F
O	13	.	.	.	.	S	T	A	B	U	V	C	D	W	X	E	F
R	14	.	.	.	.	A	B	G	H	C	D	I	J	E	F	K	L
	15	.	.	.	.	G	H	G	H	I	J	I	J	K	L	K	L
R	16	.	.	.	.	M	N	G	H	O	P	I	J	Q	R	K	L
E	17	.	.	.	.	S	T	G	H	U	V	I	J	W	X	K	L

```
G  18   .   .   .   .   A   B   M   N   C   D   O   P   E   F   Q   R
I  19   .   .   .   .   G   H   M   N   I   J   O   P   K   L   Q   R
S  1A   .   .   .   .   M   N   M   N   O   P   O   P   Q   R   Q   R
T  1B   .   .   .   .   S   T   M   N   U   V   O   P   W   X   Q   R
E  1C   .   .   .   .   A   B   S   T   C   D   U   V   E   F   W   X
R  1D   .   .   .   .   G   H   S   T   I   J   U   V   K   L   W   X
   1E   .   .   .   .   M   N   S   T   O   P   U   V   Q   R   W   X
   1F   .   .   .   .   S   T   S   T   U   V   U   V   W   X   W   X
```

```
About SuperHires color.
-----------------------
SuperHires color encryption is not reflected in the ColorTable.
The color encoding is, however, reflected in the ViewPort's
copper lists generated by graphics via MakeVPort(), SetRGB4(), etc.
```

Keep in mind that because of the loss of lower bits of precision in specifying SuperHires colors, pastel colors in a closely graduated color scheme may be visually difficult to distinguish from each other.

1.13 C / ECS Hardware Graphics Library / SuperHires 70ns Sprite Positioning

SuperHires mode has a finer granularity of sprite positioning than either Hires or Lores modes. This allows for positioning the sprite every other SuperHires pixel on 70ns boundaries. The ECS registers SPRxPOS and SPRxCTL work together as position, size and sprite feature control registers. They are usually loaded by the sprite DMA channel, during horizontal blank, however they may be loaded by the processor.

The two registers are defined as follows:

```
SPRxPOS W   A D     Sprite x vertical-horiz start position data

     Bit      Use
     ----     ----
     15-08
     07-00  SH8-SH1  Start horizontal value. Low bit (SH0) in SPRxCTL.
```

```
SPRxCTL W   A D     Sprite x position and control data

     Bit      Use
     ----     ----
     15-08
     07
     06
     05
     04      SHSH1     Start horizontal (SHR mode) 70ns increment
     03      SHSH0     Start horizontal (SHR mode) 35ns (unimplemented)
     02
     01
     00      SH0       Start horiz. value Low bit 140 ns increment
```

```
   Note: bits 3 and  4 are in the ECS chips only.

   Warning:
   --------
   70ns sprite positions are only available in SuperHires mode.
   Attempting to use 70ns sprite positioning with Hires mode under
   the current system may lead to unpredictable results.
```

1.14 C / ECS Hardware and Graphics Library / Multi-Sync and Bi-Sync Monitors

```
The enhanced Agnus now includes registers for setting a standard
programmable scan rate. The scan rates supported in the  V36
graphics.library include:

   NTSC (525 lines, 227.5 colorclocks per scan line)
   PAL  (625 lines, 227.5 colorclocks per scan line)
   VGA  (525 lines, 114.0 colorclocks per scan line)

The V36 graphics.library controls the variable number of colorclocks on
each horizontal scan line with a combination of registers.  Each
combination of registers provides a different frequency of scan rate and
number of lines per display field:

   HTOTAL    W   A     Highest number count in horizontal line

         Bit  15 14 13 12 11 10 09 08 07 06 05 04 03 02 10 00
         Use   0  0  0  0  0  0  0  0 h8 h7 h6 h5 h4 h3 h2 h1

The value in this register represents the number of 280ns increments on
the horizontal line.

   VTOTAL    W   A     Highest numbered vertical line

VTOTAL contains the line number at which to reset the vertical position
counter.  This value represents the number of lines in a field(+1). The
exception is if the INTERLACE bit is set (BPLCON0). In this case this
value represents the number of lines in the long field (+2) and the number
of lines in the short field (+1).

Programmable synchronization is implemented through five new enhanced
Agnus registers:

   VSSTRT    W   A     Vertical line position for VSYNC  start
   VSSTOP    W   A     Vertical line position for VSYNC  stop
   HSSTRT    W   A     Horizontal line position for HSYNC  start
   HSSTOP    W   A     Horizontal line position for HSYNC  stop
   HCENTER   W   A     Horizontal position for Vsync on interlace

A reasonable composite can be generated by setting HCENTER half a
horizontal line from HSSTRT, and HBSTOP at (HSSTOP-HSSTRT) before HCENTER,
with HBSTRT at (HSSTOP-HSSTRT) before HSSTRT.

Programmable blanking is implemented through four new ECS Agnus registers:

   HBSTRT    W   A     Horizontal line position for HBLANK start
```

```
HBSTOP    W   A     Horizontal line position for HBLANK stop
VBSTRT    W   A     Vertical   line position for VBLANK start
VBSTOP    W   A     Vertical   line position for VBLANK stop
```

1.15 C / ECS Hardware and the Graphics Library / New BEAMCON0 Register

A new register in the enhanced Agnus, BEAMCON0, provides a programmable signal generator.

```
BEAMCON0  W   A     Beam counter control register

        Bit     Use
        ---     ---
        15
        14    HARDDIS    Disable hardwired vertical/horizontal blank
        13    LPENDIS    Ignore latched pen value on vertical pos read
        12    VARVBEN    Use VBSTRT/STOP disable hard window stop
        11    LOLDIS     Disable long line/short line toggle
        10    CSCBEN     Composite sync redirection
         9    VARVSYEN   Variable vertical sync enable
         8    VARHSYEN   Variable horizontal sync enable
         7    VARBEAMEN  Variable beam counter comparator enable
         6    DUAL       Special ultra resolution mode enable
         5    PAL        Programmable pal mode enable
         4    VARCSYEN   Variable composite sync
         3    BLANKEN    Composite blank redirection
         2    CSYTRUE    Polarity control for C sync pin
         1    VSYTRUE    Polarity control for V sync pin
         0    HSYTRUE    Polarity control for H sync pin
```

```
Warning:
--------
Programmable changes between PAL and NTSC modes are new for V2.0.
They rely on hardware sync and blank in the Agnus/Denise chip set to
guarantee necessary signals for a correctly displayed picture.

Other modes, such as VGA (31 KHz programmable mode) disable the hard
stops on display sync and blank.  Do not write to this register.

Incorrectly writing directly to BEAMCON0 has the (remote) possibility
of destroying your multisync monitor.
```

1.16 C / ECS Hardware and Graphics Library / Display Window Specification

The new graphics.library and the ECS provide a more powerful display window specification. The registers DIWSTRT and DIWSTOP control the display window size and position:

```
DIWSTRT   W   A D     Display Window Start (upper left  vert-hor pos)
DIWSTOP   W   A D     Display Window Stop  (lower right vert-hor pos)

      Bit   15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
```

```
        Use   V7 V6 V5 V4 V3 V2 V1 V0 H7 H6 H5 H4 H3 H2 H1 H0
```

The way these two registers work has changed. DIWSTRT used to be vertically restricted to the upper 2/3 of the display (V8=0), and horizontally restricted to the left 3/4 of the display (H8=0). DIWSTOP used to be vertically restricted to the lower 1/2 of the display and horizontally restricted to the right 1/4 of the display (H8=1).

The V36 graphics.library now supports explicit display window start and stop positions within a larger and more useful range of values, via control of the the new DIWHIGH register in the ViewPort copper lists:

```
   DIWHIGH   W   A D     Display Window upper bits for  start,stop

           Bit     Use
           ---     ---
           15       0
           14       0
           13       H8      Horizontal stop, most significant bit.
           12       0
           11       0
           10       V10 \
            9       V9   }  Vertical stop, most significant 3 bits.
            8       V8  /
            7       0
            6       -
            5       H8      Horizontal start, most significant bit.
            4       0
            3       0
            2       V10 \
            1       V9   }  Vertical stop, most significant 3 bits.
            0       V8  /
```

This is an added register for the ECS chips, and allows larger start and stop ranges. If it is not written, the old scheme for DIWSTRT and DIWSTOP described above holds. If this register is written last in a sequence of setting the display window, it sets direct start and stop positions anywhere on the screen.

```
   A note on ECS compatibility.
   ----------------------------
   With the enhanced Denise chip present, the graphics.library will set
   up copperlists using the new, explicit display window controls.
   Programs which consistently call MakeVPort(), MrgCop() and Loadview()
   when changing the vertical position of their ViewPort (DxOffset) will
   continue to behave normally.

   Programs which failed to call MakeVPort() when moving the ViewPort
   vertically may not be displayed correctly on a system with ECS.
```

1.17 C / ECS Hardware and the Graphics Library / Genlock Extensions

The V36 graphics.library supports the new genlock capabilities of the enhanced Denise chip in PAL or NTSC modes. Any color registers may be chosen as controlling video overlay (COLORKEY). A single bitplane may be

chosen to control video overlay as well (BITPLANEKEY). The border areas surrounding the active display window may also be set to be opaque or transparent.

```
BPLCON0   W   A,D     Bitplane control (miscellaneous control bits)
BPLCON1   W     D     Bitplane control (horizontal scroll control)
BPLCON2   W     D     Bitplane control (video priority control)
BPLCON3   W     D     Bitplane control (enhanced features)
```

Bit	BPLCON0	BPLCON1	BPLCON2	BPLCON3	
15					
14			ZDBPSEL2 \		
13			ZDBPSEL1 }		Select bitplane
12			ZDBPSEL0 /		
11			ZDBPEN		Use BITPLANEKEY
10			ZDCTEN		Use COLORKEY
09			KILLEHB		Kill halfbrite
08					
07					
06					
05				BRDRBLNK	Border blank
04				BRDNTRAN	Border opaque
03					
02					
01					
00	ENBPLCN3				Enable new BLPCON3 register.

The ECS genlock features are enabled on a ViewPort by ViewPort basis.

```
Warning:
--------
Genlock has been designed to work with NTSC and PAL modes only.
Genlock and 31 KHz programmable scan rates are not compatible modes.
```

1.18 C / ECS Hardware and the Graphics Library / Big Blits

The V36 graphics.library supports the ECS Agnus Blitter enhancements, which provide for contiguous blits of up to 32768 x 32768 pixels at a time. Under the original chip set 1024 x 1024 was the maximum:

```
BLTSIZE   W   A    Old Blitter size and start (window width, height)

     Bit   15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
     Use   h9 h8 h7 h6 h5 h4 h3 h2 h1 h0 w5 w4 w3 w2 w1 w0

         h = Height (10 bit height = 1024 lines  max)
         w = Width  (6 bit width  = 1024 pixels max)
```

Two new registers have been added which make larger blits possible:

```
BLTSIZV   W   A       ECS Blitter V size
```

```
        Bit   15 14  12  12  11  10  09 08 07 06 05 04 03 02 01 00
        Use    0 h14 h13 h12 h11 h10 h9 h8 h7 h6 h5 h4 h3 h2 h1 h0

           h = Height (15 bit height = 32768 lines  max)


  BLTSIZH   W   A       ECS Blitter Horizontal size & start

        Bit   15 14  13  12  11  10  09 08 07 06 05 04 03 02 01 00
        Use    0  0   0   0   0  w10 w9 w8 w7 w6 w5 w4 w3 w2 w1 w0

           w = Width  (11 bit width  = 32768 pixels max)
```

With these two registers, blits up to 32K by 32K are now possible - much larger than the original chip set could accept. The original commands are retained for compatibility. BLTSIZV should be written first, followed by BLTSIZH, which starts the blitter.

The existence of the enhanced Agnus Blitter is reflected in the state of the GfxBase->ChipRevBits bit definition GFXB_BIG_BLITS and is initialized by the graphics.library at powerup. Note that the <hardware/blits.h> constant MAXBYTESPERROW has been redefined to reflect the larger range of legal blitter operations.

About RastPort Sizes.

If the ECS Blitter is accessible, the graphics.library supports its use for all graphics functions including areafill, gels, line and ellipse drawing functions.

If the ECS Blitter is not installed, programmers should limit the absolute size of their RastPorts to values that the old BLTSIZE register can address.

1.19 C / ECS Hardware and the Graphics Library / Other ECS Modifications

The preceding sections cover most of the ECS registers appearing in the ECS register map. This section briefly describes the remaining modifications to the Enhanced Chip Set registers.

The following registers now have two additional bits for addressing larger segments of memory, when the Enhanced Chip Set is present:

```
  DSKPTH    020   W   A      Disk pointer
                                 (high 5 bits, was 3 bits)
  BLTxPTH   050   W   A      Blitter pointer to x
                                 (high 5 bits, was 3 bits)
  COP1LCH   080   W   A      Coprocessor 1st location
                                 (high 5 bits,was 3 bits)
  COP2LCH   084   W   A      Coprocessor 2nd location
                                 (high 5 bits,was 3 bits)
  AUDxLCH   0A0   W   A      Audio channel x location
                                 (high 5 bits was 3 bits)
```

The Strobe Long Line register (STRLONG) can be disabled if the Disable Long Line (LOLDIS) bit is set in the BEAMCON0 register.

```
   STRLONG   03E   S   D      Strobe for identification of long horiz line
```

See the Multi-Sync and Bi-Sync Monitors section in this appendix for the bit descriptions in BEAMCON0.

Bit 7 (DOFF) of the BLTCON1 register, when set, disables the output of the Blitter hardware on channel D.

```
   BLTCON1   042   W   A      Blitter control register 1
```

This allows inputs to channels A, B and C and certain address modification if necessary, without the Blitter outputting over channel D.

The BLTCON0L register writes the low bits of BLTCON0, thereby expediting the set up of some blits and generally speeding up the software, since the upper bits are often the same.

```
   BLTCON0L  05A   W   A      Blitter control 0, lower 8 bits (minterms)
```

1.20 C / ECS Hardware and Graphics Library / Interpretational Differences

The following registers have the same functionality as the standard chip set, however, their behavior is interpreted differently.

The POT0 and POT1 registers each read a pair of 8-bit pot counters as before.

```
   POT0DAT   012   R   P      Pot counter data left pair
                                  (vertical, horiz)
   POT1DAT   014   R   P      Pot counter data right pair
                                  (vertical, horiz)
```

However, with programmable scan rates, the values read from these registers will differ. Generally, the faster the scan rate, the smaller these values become. Adjustments to the scan rate are reflected in these values. See Appendix A for more detail on standard operation of these registers.

Another register where the interpretation has been extended for the ECS is COPCON.

```
   COPCON    02E   W   A      Coprocessor control
```

This 1-bit register, the danger bit (CDANG), when set allows the Coprocessor to write to the Blitter hardware. In the standard chip set, if this is set, the Copper can access the address range from $DFF03E through $DFF07E. Now, in the ECS, if this bit is set, the Copper can access all of the Amiga chip registers. If this bit is clear, the Copper can access the address range from $DFF03E through $DFF07E, the same range as when the danger bit is set in the standard chip set.

The AUDxPER register is another register value that varies according to

the programmable scan rate.

```
   AUDxPER   0A6   W   P      Audio channel x period
```

With programmable scan rates, the maximum value read from this register will differ. Generally, the faster the scan rate, the smaller the maximum period becomes. Adjustments to the scan rate are reflected in this maximum value.

For more information on the AUDxPER register, and any other register in the Amiga standard chip set, see Appendix A and Appendix B .

1.21 C Enhanced Chip Set / ECS Registers

The register map listed below shows the changes and new registers in the Amiga's Enhanced Chip Set.

ADD	REGISTER	V2.0	R/W	CHIP	FUNCTION
004	VPOSR	chg	R	A	Read vertical most sig. bits (and frame flop)
012	POT0DAT	chg	R	P	Pot counter data left pair (vertical, horiz)
014	POT1DAT	chg	R	P	Pot counter data right pair (vertical, horiz)
020	DSKPTH	chg	W	A	Disk pointer (high 5 bits, was 3 bits)
02E	COPCON	chg	W	A	Coprocessor control
03E	STRLONG	chg	S	D	Strobe for identification of long horiz line
042	BLTCON1	chg	W	A	Blitter control register 1
050	BLTxPTH	chg	W	A	Blitter pointer to x (high 5 bits, was 3 bits)
05A	BLTCON0L	new	W	A	Blitter control 0, lower 8 bits (minterms)
05C	BLTSIZV	new	W	A	Blitter V size (for 15 bit vertical size)
05E	BLTSIZH	new	W	A	Blitter H size and start (for 11 bit H size)
07C	DENISEID	new	R	D	Chip revision level for Denise (video out chip)
080	COP1LCH	chg	W	A	Coprocessor 1st location(high 5 bits,was 3 bits)
084	COP2LCH	chg	W	A	Coprocessor 2nd location(high 5 bits,was 3 bits)
0A0	AUDxLCH	chg	W	A	Audio channel x location(high 5 bits was 3 bits)
0A6	AUDxPER	chg	W	P	Audio channel x period
100	BPLCON0	chg	W	A,D	Bitplane control (miscellaneous control bits)
104	BPLCON2	chg	W	D	Bitplane control (video priority control)
106	BPLCON3	new	W	D	Bitplane control (enhanced features)
142	SPRxCTL	chg	W	A	Sprite x position and control data
1C0	HTOTAL	new	W	A	Highest number count, horiz line (VARBEAMEN=1)
1C2	HSSTOP	new	W	A	Horizontal line position for HSYNC stop
1C4	HBSTRT	new	W	A	Horizontal line position for HBLANK start
1C6	HBSTOP	new	W	A	Horizontal line position for HBLANK stop
1C8	VTOTAL	new	W	A	Highest numbered vertical line (VARBEAMEN=1)
1CA	VSSTOP	new	W	A	Vertical line position for VSYNC stop
1CC	VBSTRT	new	W	A	Vertical line for VBLANK start
1CE	VBSTOP	new	W	A	Vertical line for VBLANK stop
1DC	BEAMCON0	new	W	A	Beam counter control register (SHRES,UHRES,PAL)
1DE	HSSTRT	new	W	A	Horizontal sync start (VARHSY)
1E0	VSSTRT	new	W	A	Vertical sync start (VARVSY)
1E2	HCENTER	new	W	A	Horizontal position for Vsync on interlace
1E4	DIWHIGH	new	W	A,D	Display window - upper bits for start, stop

A=Agnus chip, D=Denise chip, P=Paula chip, W=Write, R=Read, S=Strobe