PowerPC Processors (601, 603)

	PowerPC 601 ™	**PowerPC 603** ™	**Pentium** ™	
Positioning	Strong price/performance Strong multiprocessor support	Strong price/performance Low power consumption	Strong performance; Software compatibility	
Instruction architecture	RISC	RISC	CISC/RISC	
Cache	32 KB unified	8 KB data; 8 KB instruction	8 KB data; 8 KB instruction	
Cache - write policy	Write-back or write-thru	Write-back or thru (data) Write-back or thru (instruction)	Write-back or thru (data) Write-thru (instruction)	
Cahce - organization	8 way set associative	2 way set associative (both)	2 way set associative (both)	
Cache - parity	Parity in cache	No	Parity in cache	
Parity	Parity on all data and address transfers	Parity on all data and address transfers	Parity on all data and address transfers	
Superscalar issue	3 instructions total per cycle (branch, integer, floating point)	3 instructions total per cycle (branch, integer, floating point)	2 integers per cycle or 2 floating point per cycle	
Superscalar execution	3 instructions total per cycle (branch, integer, floating point)	5 instructions total per cycle (each execute unit)	2 integers per cycle or 2 floating point per cycle	
Execution units	1 fixed point unit 1 floating point unit 1 branch processing unit	1 fixed point unit 1 floating point unit 1 branch processing unit 1 load/store unit 1 system register unit	2 fixed point units 1 floating point unit	
External data bus	64 bits	64 bits	64 bits	
External address bus	32 bits	32 bits	32 bits	
Word size	32 bits	32 bits	32 bits	
User registers	32 GPR, 32 FPR	32 GPR, 32 FPR	8 GPR, FP stack	
Cache line size	64 bytes (Two 32 byte sectors)	32 byte	32 byte	
Out-of-order instructions	Yes	Yes	No	
Branch prediction	Static (based on rules)	Static (based on rules)	Dynamic (based on history)	
Die area	120 sq mm (74 for 100 MHz)	85 sq mm	294 sq mm (P5);	163 sq mm (P54C)
Technology	0.8u/0.6u CMOS (0.5u for 100 MHz)	0.5u CMOS	0.8u BiCMOS (P5);	0.6u BiCMOS (P54C)
Supply voltage	3.6 volts (2.5 for 100 MHz)	3.3 volts	5.0 volts (P5);	3.3 volts (P54C)
Power (typical/maximum)	8/9.2 watts; 80 MHz (4 for 100 MHz)	2/3 watts (80 MHz)	13/16 watts (P5);	4/10 watts (P54C)
Transistors	2.8 million	1.6 million	3.1 million	
Package	304 pin quad flat pack	240 pin quad flat pack	273 pin grid array (P5); 296 pin (P54C)	
Price	$ 298 (66 MHz - 1K qty)	$ Not available	$ 675 (66 MHz - 1K qty); $849 (P54C)	
Multiple processors	Built in hardware support for symmetrical multiprocessor	Limited support for multiprocessing	Built in hardware support for symmetrical multiprocessors	
Frequency	50, 66, 80, 100 MHz	66, 80 MHz	60, 66 MHz (P5);	100/66, 90/60 (P54C)
Performance (all at 66 MHz)	62 SPECint92 72 SPECfp92	60 SPECint92 70 SPECfp92	70 SPECint92 (P5); 57 SPECfp92 (P5);	90 (P54C-90) 73 (P54C-90)
Other		3 user programmable power saving modes: doze, nap, sleep		

(2POWER) Compiled by Roger Dodson, IBM. June 1994