Local Bus Architectures

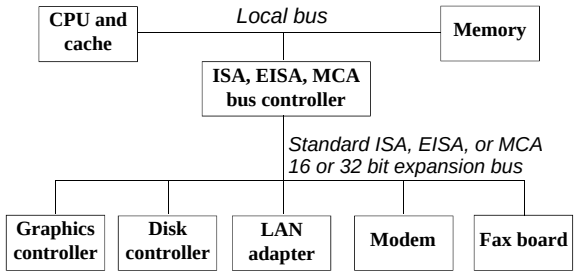
The first local bus known as **VESA local bus *(VL-Bus)*** was developed by the Video Electronics Standards Association. A second competing standard called **Peripheral Component Interconnect *(PCI)*** was developed by Intel® as a high end alternative to VL-Bus. Neither require new software and both have numerous vendor support. PCs incorporating either local bus **still have an ISA, EISA, or Micro Channel® bus** to handle slower peripherals (modems, printers) and so a user can still use existing I/O adapter cards.

	ISA	EISA	MCA	VL-Bus [2]	PCI
Max bus width (bits)	16 bits	32 bits	32 bits [1]	32 bits [1]	32 bits [1]
Max clock speed (MHz)	8 MHz	8 MHz	10 MHz	25 MHz+	20-33 MHz
Max sustained throughput	5 MB/s	33 MB/s	40 MB/s	132 MB/s	132 MB/s
Max number of peripherals	>12	>12	15	3	10
Busmaster support	1 only	Yes	Yes	Limited	Yes
Auto-configuration	No	Only EISA cards	Yes	No	Yes

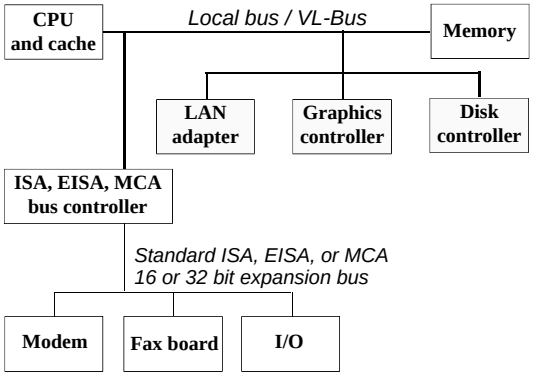
1: Micro Channel, VL-Bus, and PCI have a specification for 64 bit transfers, but no system has implemented to date; 2: Info on sheet applies to VL-Bus 1.0 and 2.0

	VL-Bus	PCI
Availability date	late 92	late 93
Availability of cards	Many	Less
Cost	Lower	Higher
Concurrent CPU/bus operation	Rarely	Yes
Direct connection of peripherals to CPU signals	Yes	No
Local bus isolated from processor	Rarely	Yes
CPU and busmaster work concurrently	No	Yes
Auto-configuration	No	Yes
Exists with ISA, EISA, MCA bus	Yes	Yes
Works with non-80x86 processors	No	Yes
Share physical slot with ISA, MCA, or EISA	Yes	Yes
Pins of local bus components (less is better)	> 80	< 50

STANDARD ISA, EISA, or MCA BUS



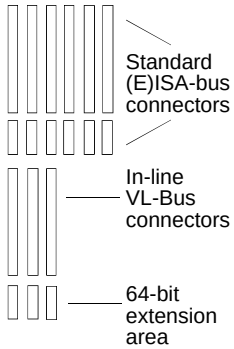
VL-BUS



Direct connection of peripheral devices to the CPU's signals lowers the complexity and pin count for system-logic chip sets for 486 systems and lets VL-Bus support higher frequencies than PCI's maximum 33 MHz.

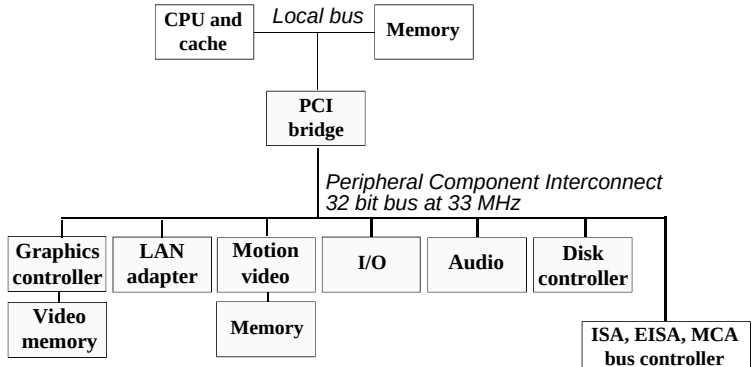
No more than two add-in cards can run on a VL bus as running three peripherals requires at least one to be integrated on the planar. Each additional local bus peripheral degrades performance. The simple *unbuffered* VL-Bus design results in wait states when CPU speeds are over 33 MHz.

Slot Configurations



VL-Bus connectors are implemented as in-line **extensions** to the ISA, EISA, or MCA bus connectors.

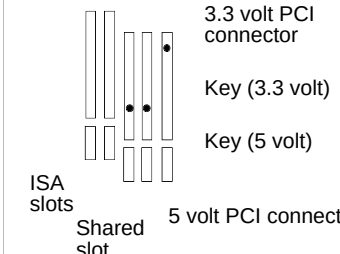
PCI



PCI puts a complex managing layer between the CPU and peripherals which buffers the signals allowing ten peripherals (max of five add-in cards) to maintain high performance. PCI's buffered design does not run faster than 33 MHz, avoiding critical timing problems and ensuring consistent adapter designs. PCI allows peripherals to communicate with each other while the CPU handles other instructions.

Isolating the CPU from the local bus lets PC manufacturers design a motherboard to work with several generations of PCs without having to redesign the motherboard's I/O subsystem for each new processor. Potentially allows a broader set of peripheral products since do not have to use different bus interface chips/logic on each platform version of their peripherals.

Slot Configurations



PCI connectors, by contrast, may be either shared (in a side-by-side layout) or standalone.

(1LOCAL) Compiled by Roger Dodson, IBM. July 1994