

PC Processors (386SX to Blue Lightning)

PS/2 [®] , ValuePoint [™] , ThinkPad [®] Megahertz		Paths	Standard Features	ALL 386 SX PROCESSORS AND ABOVE		
				Modes	Addressable Memory	Operating Systems
80386 SX L40, N51, CL57, 700T 35, 40, 55, 56, 57, 65 16, 20, 25, 33 MHz	16 Bit Data Path 32 Bit Processor 24 Bit Address Path	←	⇒ Address pipelining	REAL	1 MB	DOS
				PROTECT	16 MB	OS/2 1.3, Windows 3.X DOS Extenders
80386 SL N45, 300 16, 20, 25 MHz	16 Bit Data Path 32 Bit Processor 24 Bit Address Path		⇒ Address pipelining * Power management	NATIVE	4 GB	OS/2 2.X, Windows NT DOS Extenders, AIX PS/2
				PROTECT		
80386 DX 70, P70, 80 16, 20, 25, 33 MHz	32 Bit Data Path 32 Bit Processor 32 Bit Address Path		⇒ Address pipelining	VIRTUAL	Multiple 640 KB	OS/2 2.X, Windows 3.X, NT DOS Extenders AIX PS/2 DOS Merge
				8086		
80386 SLC 325T, N51, 56, 57, (Upgrade for 56, 57) 16, 20, 25 MHz	Same as 80386SX except 32 bit data path between CPU and memory cache ¹		⇐ 8 KB internal cache (2 way ; write-thru; w/ parity) ⇒ Optimized instructions ⇒ Address pipelining * Power management	<p>The 386 SX through the Pentium processor all offer the same modes which only means that applications run faster on a Pentium. Operating systems and applications written for the 386 family will be compatible with the 486 and Pentium processor.</p> <p>The 386 SX and all SLC processors can only address 16 MB of memory, although 64 TB of virtual memory, because of its 24 bit address path.</p> <p>The 486 SLC2, 486 DX2, and Blue Lightning run twice as fast internally (50 MHz) as externally (25 MHz).</p> <p>The 486 SLC3 and Blue Lightning run three times as fast internally (75 MHz) as externally (25 MHz).</p> <p>Note 1: Although the SLC's have a 16 bit data bus like the 386 SX, the memory cache is integrated on the processor chip (not external) so the memory cache transfers to the CPU in 32 bits.</p> <p>The 386 SX, 386 SL, and 386 DX are developed and manufactured by Intel[®]. The SLC and Blue Lightning processors are developed and manufactured by IBM[®].</p> <p>Address pipelining: decodes next instruction's address while the current instruction is in progress. Optimized instructions: instructions execute in fewer clock cycles.</p>		
80486 SLC2 53, 56, 57, 500, 720, 720/C (Upgrade for 56, 57, 700, 700C) 40/20, 50/25 MHz	Same as 80386SX except 32 bit data path between CPU and memory cache ¹		⇐ Same as 80486SLC above			
Blue Lightning 50/25, 66/33 MHz 75/25, 100/33 MHz	32 Bit Data Path 32 Bit Processor 32 Bit Address Path		⇐ 16 KB internal cache (4 way ; write-thru; w/ parity) ⇒ Optimized instructions ⇒ Address pipelining * Power management			

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(INTEL) Compiled by Roger Dodson, IBM. March 1994