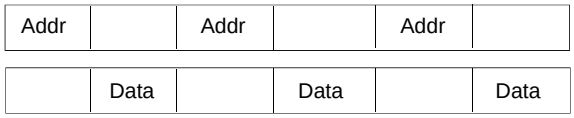
Bus Architectures

	ISA	EISA	MCA	PCMCIA 2.01	VL-Bus	VL-Bus 2.0	PCI (2.0)
Max bus width (today)	16 bits	32 bits	32 bits	16 bits	32 bits	32 bits	32 bits
Max bus width (future)	16 bits	32 bits	64 bits	32 bits (V3.0)	32 bits	64 bits	64 bits
Max clock speed (MHz)	8 MHz	8 MHz	10 MHz	10 MHz	external bus	external bus	20-33 MHz
Typical clock speed	8 MHz	8 MHz	10 MHz	10 MHz	25, 33 MHz	25, 33, 50	33 MHz
Max burst throughput [1]	8 MB/s	33 MB/s	40 MB/s	<10 MB/s	132 MB/s	132 MB/s	132 MB/s
Max non-burst throughput	2 MB/s	16 MB/s	20 MB/s	<10 MB/s	66 MB/s	66 MB/s	44 MB/s (writes) 33 MB/s (reads)
Max number of peripherals	>12	>12	16	4	3	3	10
Busmaster support	1 only	Supported	Supported	No	Supported	Supported	Supported
Concurrent CPU/bus operation	Rarely	Possible	Yes	No	Rarely	Optional	Yes
Burst mode (addr, data, data, ...)	No	Yes	Yes (streaming)	No	No	Yes	Yes
Auto-configuration	No	Only EISA cards	Yes	Yes	No	No	Yes
Plug and Play	Future cards and systems	No known plans	Will support (see below)	Yes	Might in future	Might in future	Will support
% of self configuring Adapters	1% (growing)	10%	100%	75%	0%	0%	100%
Power-on insertion	No	No	No	Yes	No	No	No
Adapters supported	ISA	ISA, EISA	MCA	PCMCIA	ISA, VL-Bus	ISA, VL-Bus	PCI
Relative cost per card	1	1.3 - 2	1.3 - 2	2 - 3	1.1	1.1	1.2 - 2
Works with non-80x86 CPU	Possible	Possible	Yes	Yes	No	Possible	Yes
Data parity	No	No	Supported	No	No	No	Always
Address parity	No	No	Supported	No	No	No	Always
Year introduced	1984	1990	1987 PS/2 Model 50+	1992	1992	1994	1993

BURST MODE

Note 1: Maximum rates are based on burst/streaming modes where a single address cycle is followed by multiple data cycles in sequential memory locations. In reality, few bus transfers utilize this mode, and if so, only for brief microseconds (but more common on VL-Bus and PCI).

NON-BURST



BURST / STREAMING

PCI DATA TRANSFER RATES

Best case as slow agents (master or slave) can slow the data rate by inserting wait states

Non-burst:

33 MB/sec for reads (address, bus turnaround, data, idle)
44 MB/sec for writes (address, data, idle)
66 MB/sec for writes (address, data) if same master is writing to different targets

Burst rates:

96 MB/sec for read of 32 bytes
105.6 MB/sec for write of 32 bytes
126 MB/sec for read of 256 bytes
128 MB/sec for write of 256 bytes
131.743 MB/sec for write of 4 KB

PLUG AND PLAY

The new "Plug and Play" provides full automatic configuration of the total system hardware and operating system/driver software.

Plug and Play requires:

- Operating system support (expected in Chicago and OS/2 2.2)
- Plug and play adapters
- Plug and play BIOS and compatible system board logic; older systems may or may not be upgradeable

All Micro Channel systems support automatic installation now, but some user interaction is required. Micro Channel systems using a future Plug and Play operating system and device drivers will no longer ask the user if want to configure system, but will do it automatically when adapter changes are made.

A VL-Bus and PCI 64 bit bus is not expected in systems until 1996.

(BUS) Compiled by Roger Dodson, IBM. July 1994