SYLLABUS

ECE 426: Digtal Computer Design 3(3,0)
Section 1 – Spring Semester, 1998

Goals:	Understand design of high-speed ALUs Understand design of control and timing circuitry Understand design of memory and I/O systems Understand modern design methodologies (CAD and HDL)
Instructor:	Walt Ligon, EIB 335, 656-1224, walt@eng.clemson.edu
Office Hours:	MWF 10:05 to 11:05 or by appointment
Lecture Hours:	MWF 11:15 to 12:05 Riggs 223
TA/Grader:	Fred Stivers, Riggs 315, 656-1142
Text:	Mano, Digital Design (recommended) Skahill, VHDL for Programmable Logic
Grading:	Homework: 10% Mid-Term Exam: 25% Design Projects: 40% Final Exam: 25%
Attendance:	Required. No late work accepted. Make-up tests by prior appointment only. Wait 15 minutes for late instructor.
Academic Honesty:	All work on quizzes, tests, design assignments, and labs is to be wholly your own. Possessing, using, providing, or exchanging improperly acquired written, verbal, or electronic information will be considered a violation of the academic honor code. Violations will result in a grade of F for the semester. Honor Pledge to be written on each assignment and signed.

ECE426 - Topic List

- Design Methodology
  - Definition
  - Design
  - Produce and Test
- CAD Tools
  - Schematic Capture
  - Hardware Description Languages
    - VHDL
    - Verilog
    - ABEL
  - Simulation, Place and Route, etc.
- Programmable Logic
  - ROMs
  - PLAs
  - PALs
  - FPGAs
- State machine design and implementation
  - FSM design
  - Asynchronous logic
  - Performance issues
- ALU design
  - Adder/Subtractors
  - Multipliers
- Design Projects