Programmable Logic Devices

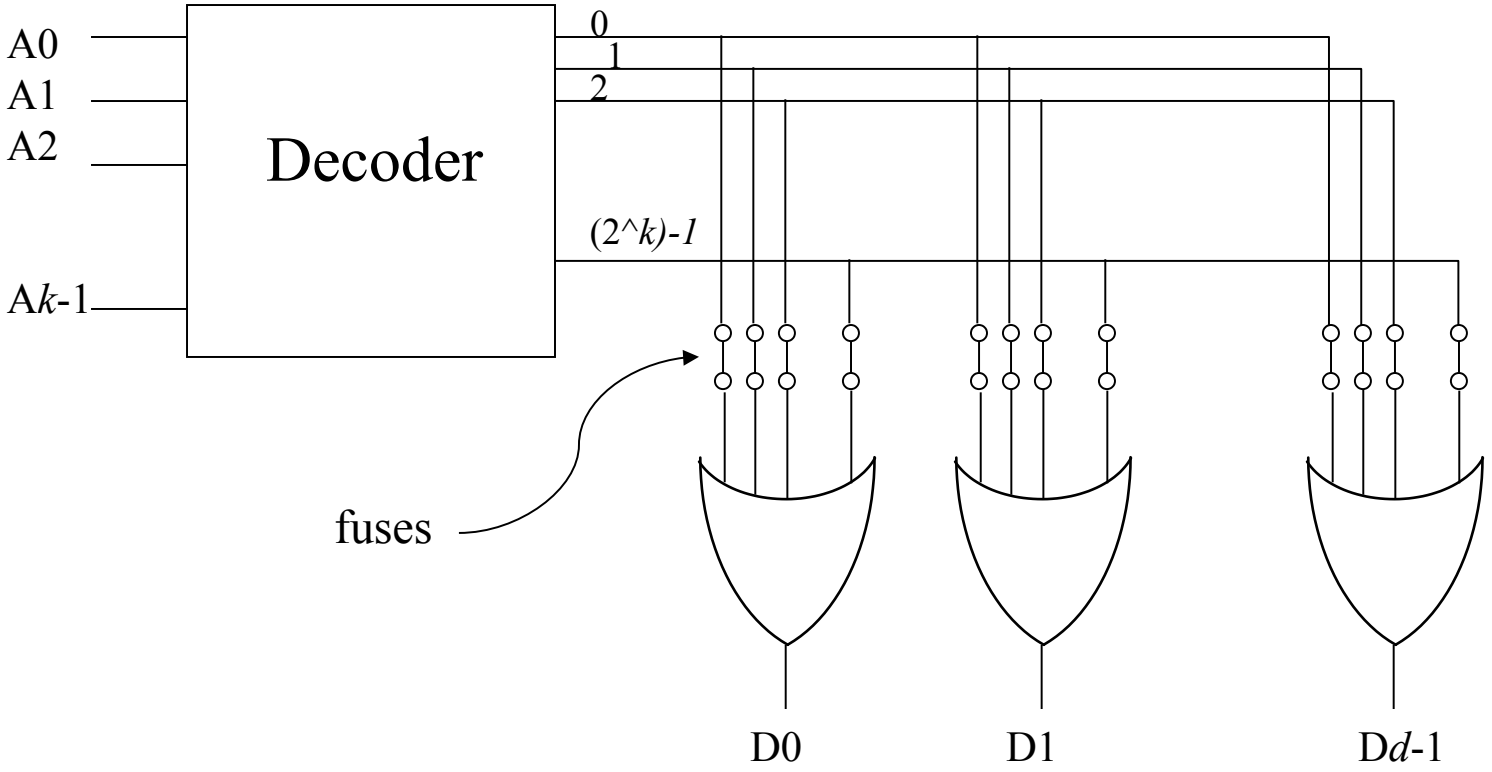
- Read Only Memory (ROM)
  - mask programmable
  - PROM, EPROM, EEPROM
- Programmable Logic Array (PLA)
- Programmable Array Logic (PAL)
- Field Programmable Gate Array (FPGA)
  - Mux based
  - LUT based

ROMs

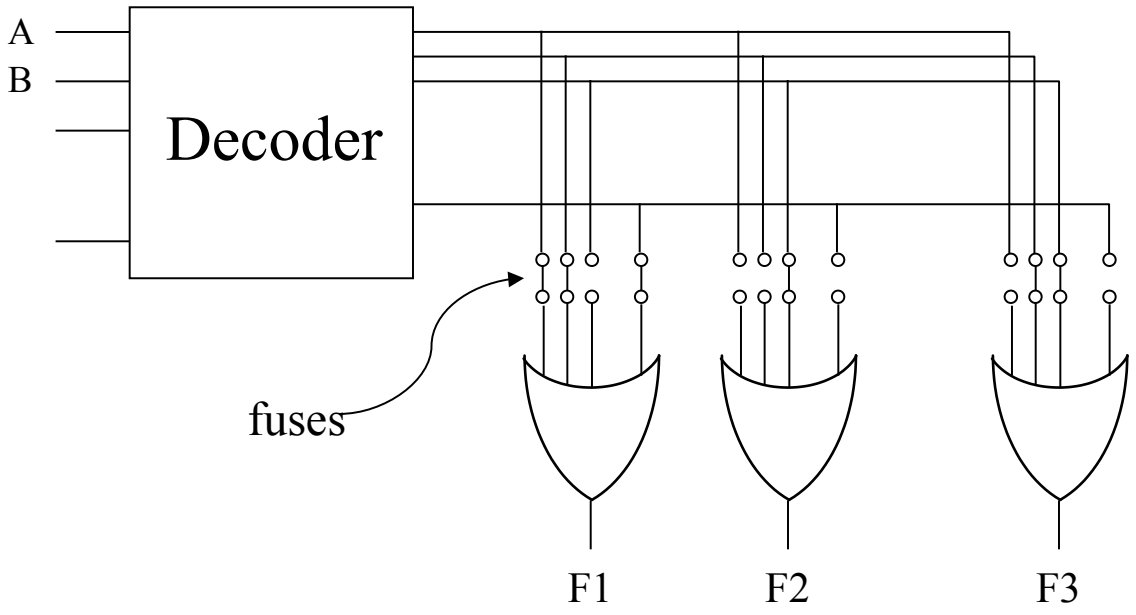
- Input: *k* Address lines (A)
- Output: *d* Data lines (D)
- Function:

  Each possible value of A [0..(2^*k*)-1] has a unique set of *d* bits that are output on D when the corresponding “address” is provided on A

ROMs



Implementing Logic in ROMs

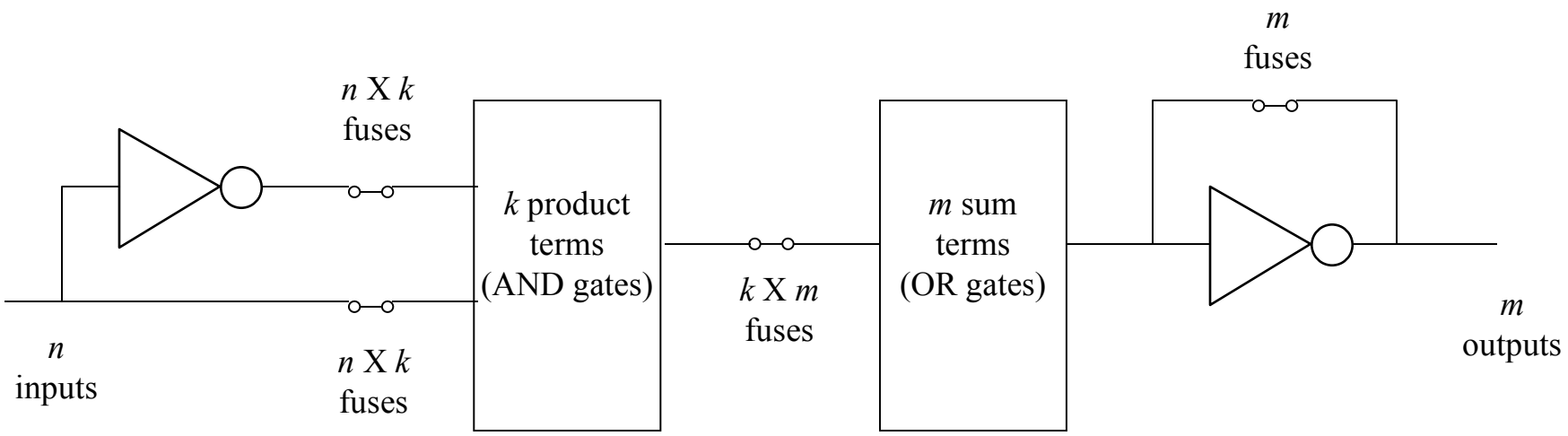


A	B	F1	F2	F3
0	0	1	0	0
0	1	1	0	1
1	0	0	1	1
1	1	1	0	0

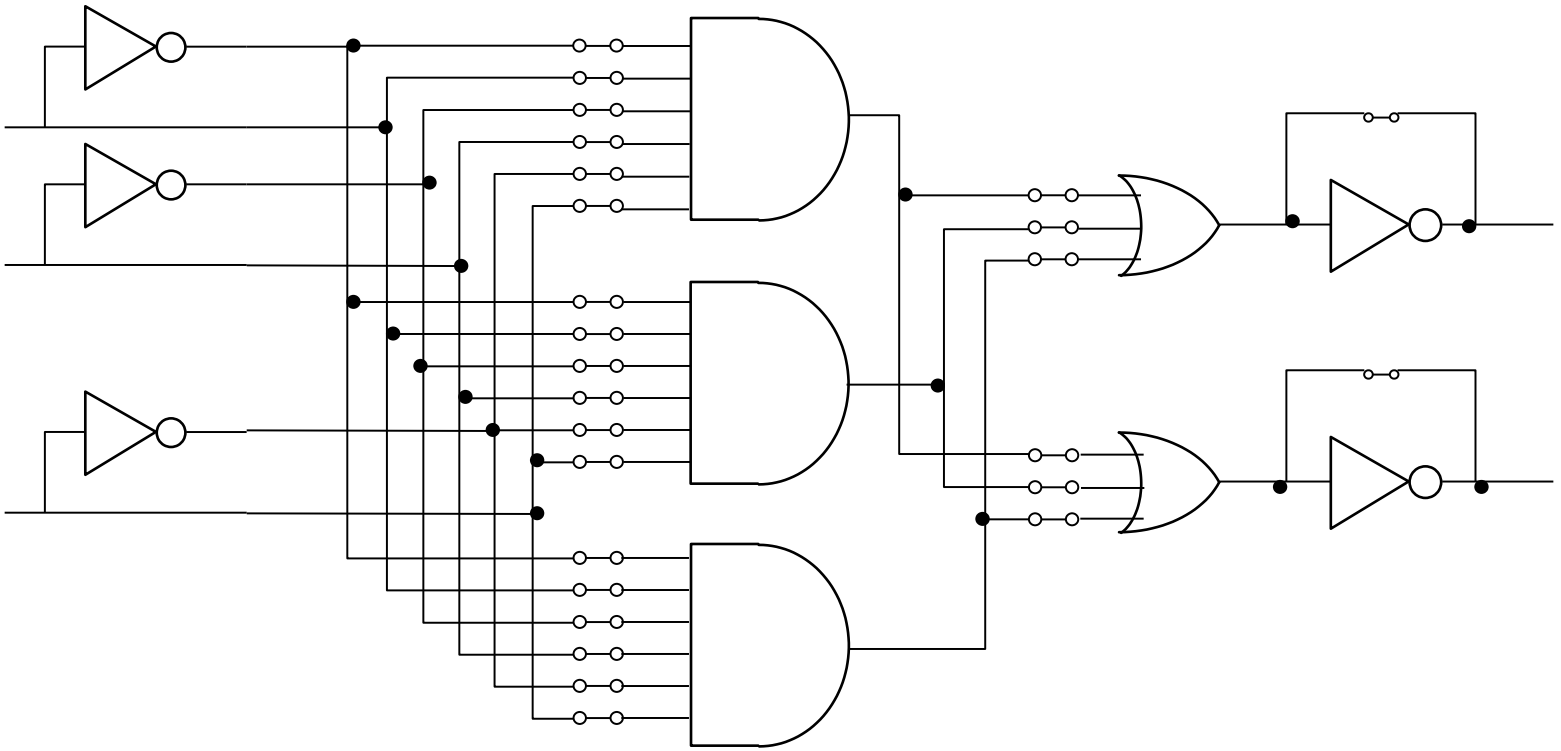
ROM Types

- Mask programmable ROM
  - fuses programmed during manufacture
- Programmable ROM (PROM)
  - 0's programmed by blowing fuses or "burning"
- Erasable PROM (EPROM)
  - programming erased by UV light
- Electrically erasable PROM (EEPROM)
  - programming erased via control signals

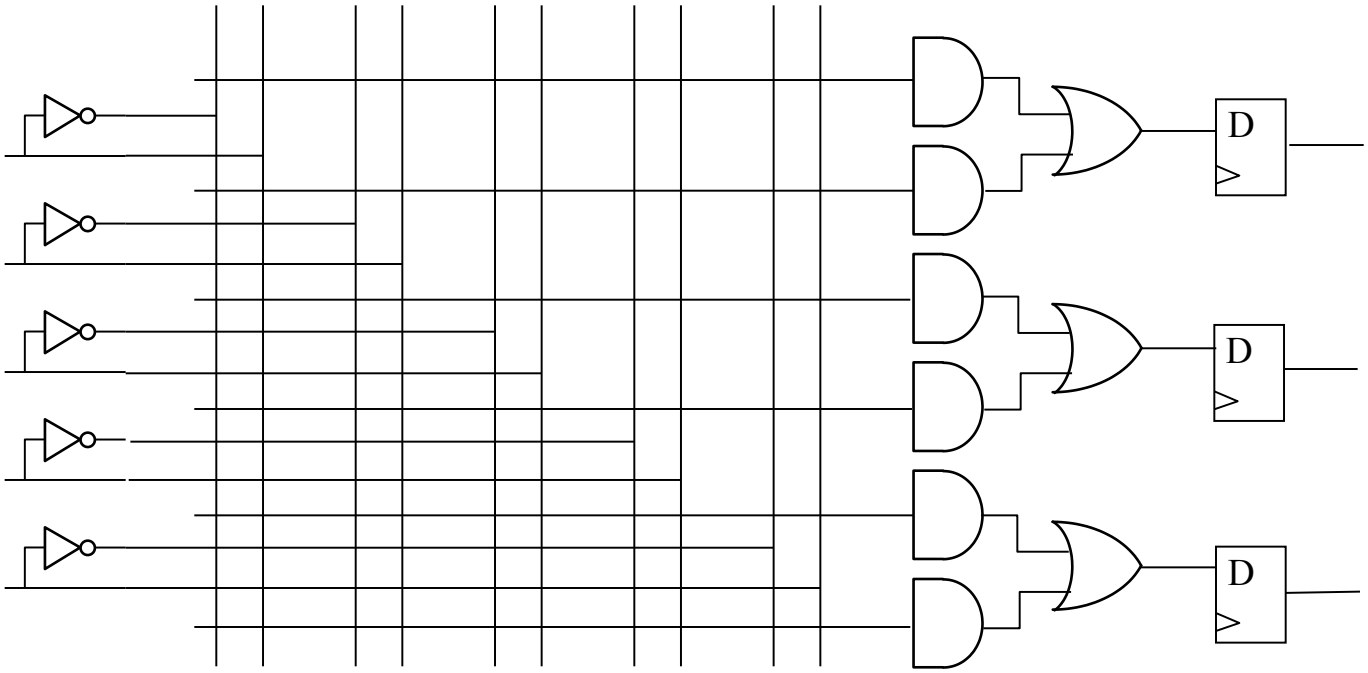
Programmable Logic Array (PLA)



Programmable Logic Array (PLA)



Programmable Array Logic (PAL)



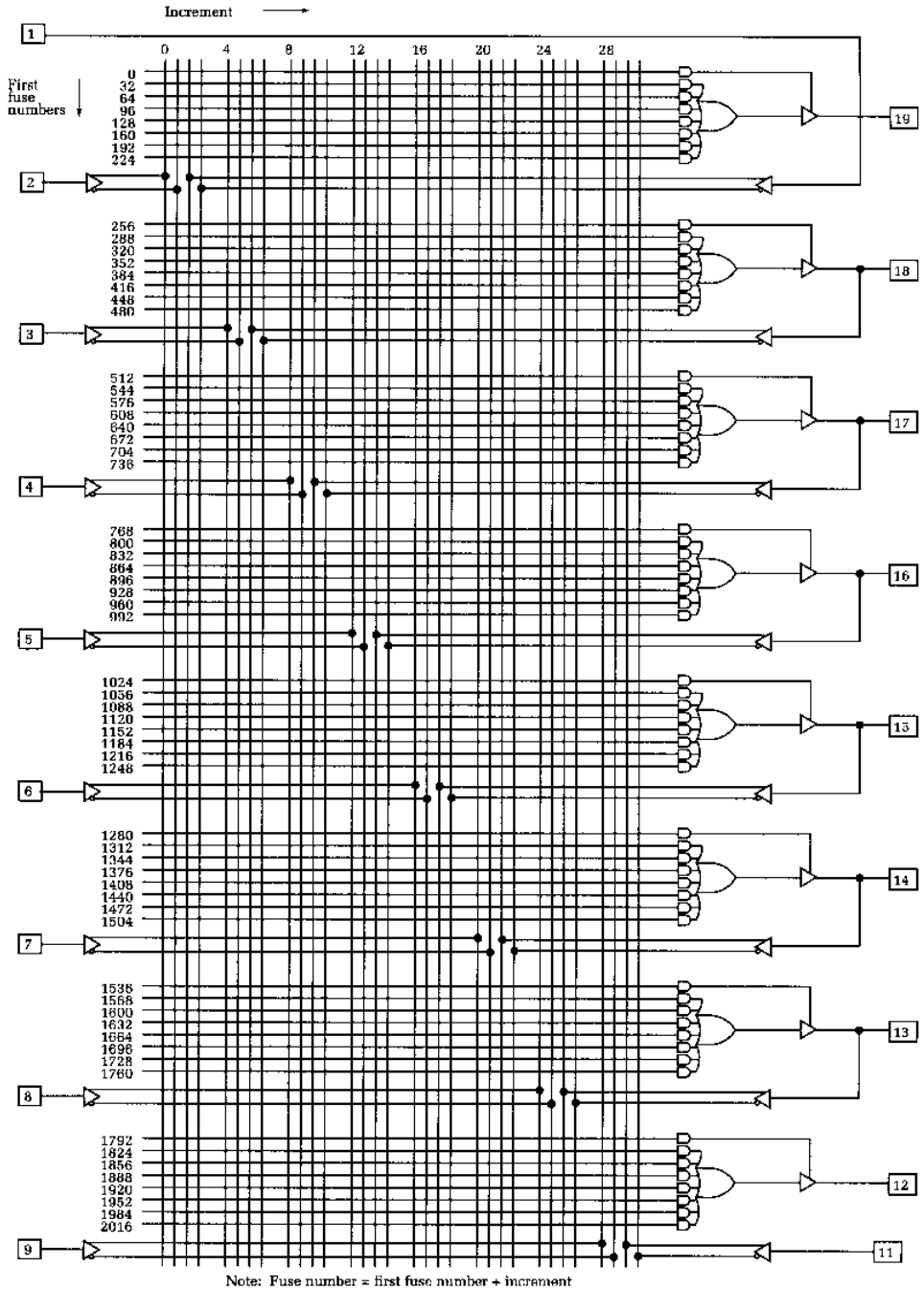


Figure 4.72 P16H8 PAL programming map.

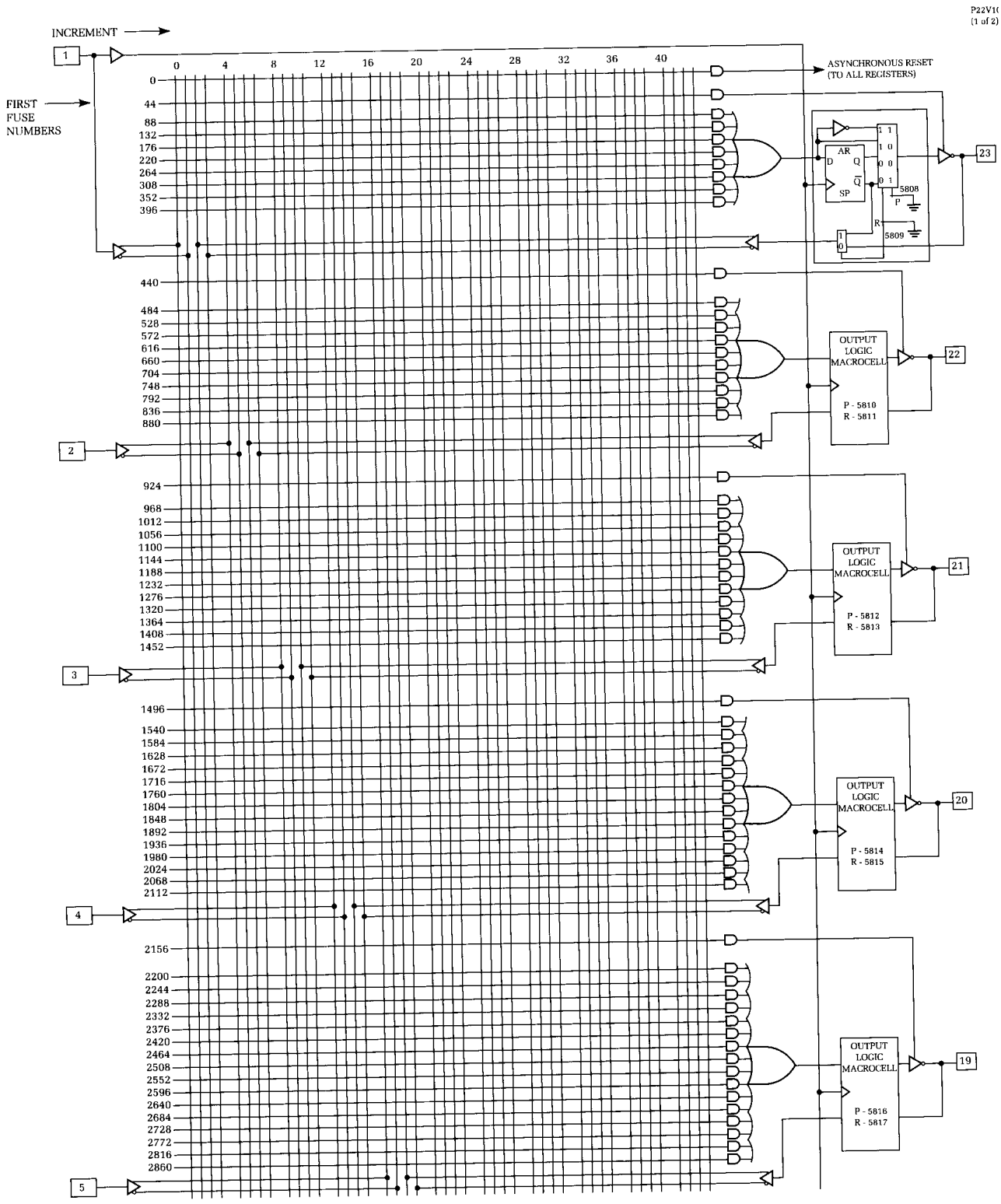


Figure 10.28 P22V10 PAL.