ECE 426 Fall 1998
Project 1
Asynchronous Design – Designing a JK Flip-Flop

Assignment: Use the package ***async_parts*** created in Assignment 3 to design a JK Flip-Flop. Use the delays (in nanoseconds) shown in the table for the gates used. Implement and simulate the design in VHDL. Calculate the setup and hold time for both the J and K inputs. Also, calculate the maximum clock frequency for the design.

Gate	1 input	2 input	3 input	4 input
and	X	4	5	5
or	X	6	8	11
not	2	X	X	X
nor	X	4	6	9
xor	X	5	8	10
nand	X	2	3	3
xnor	X	4	7	9
tristate	2	X	X	X

What to turn in:
- Simulation waveform for the JK flip-flop
- State diagram, flow table, implication table, merger diagram, final flow table, and logic diagram for the asynchronous design
- Calculations for the setup and hold time
- Calculations for the maximum clock frequency