ECE 426 Fall 1998
Assignment 2
Troubleshooting Designs using a Testbench and the Waveform Viewer

Copy the following files from *~fstiver/TA426/test_proj1* into a working directory:

> *testbench.vhd*
> *.synopsys_vss.setup*
> *sig.all*

Create an *analyze* directory.

Look at the *testbench.vhd* file. You will notice that the testbench instantiates a part named **count_example** and creates a clock. This part is a 5 bit synchronous counter which has a reset, enable and load. All are high_active. After a reset, the initial count will start at 00000. When the enable is high, the counter will increment on the rising edge of each clock cycle. When the load is high, the counter will load the value on the data_in lines. If both the load and enable are high, the load will take precedence. The value on data_in will be loaded. When the load goes low, the value will be incremented normally. The counter does not stop at 11111, but rolls over to 00000 and continues.

This specific part has 5 architectures associated with it. Only 1 of the architectures works per the above specifications. The other 4 architectures contain a flaw. You do not have access to the VHDL code for the counter. You must determine what is wrong (and which version is correct) for each architecture by testing the part with a testbench and the waveform viewer.

The architectures can be changed by the following steps:

> In *testbench.vhd* at the bottom of the file, change the following line:
>
> use entity F98_PROJ1.count_example(version1);
>
> To:
>
> use entity F98_PROJ1.count_example(version2); or 3 or 4 or 5
>
> Re-analyze *testbench.vhd*.
> Use the Restart command in the debugger.

Assignment: Write a testbench(es) to determine which version is correct and what is wrong with the other versions.

What to turn in: Simulation waveforms for each of the 5 versions (run for 2000 ns). Label each version, mark the correct version and describe and mark what is wrong with the other 4.

You will have to modify the testbench in order to fully test each architecture.