The drawings contain in this Recommendation have been done in Autocad.
Recommendation Q.781

MTP LEVEL 2 TEST SPECIFICATION

1 Introduction

protocol. These tests intend to validate the protocol specified in Recommendation Q.703.

This Recommendation conforms to Recommendation Q.780 which describes the basic rules of the Test Specification. In addition the conditions which are specific to level 2 tests are described in the following sections.

2 General principles of level 2 tests

2.1 *Presentation of test descriptions*

The level 2 tests aim at testing the level 2 protocol conformance in a given implementation.

Each test description indicates in the “type of test” column; “Validation” (VAT) or “Validation” (VAT) and “compatibility” (CPT).

Although signal units are transmitted and received continuously on level 2, only the signal units which cause and/or indicate the changes of level 2 status are shown in the EXPECTED SIGNAL UNIT SEQUENCE column of each test description.

2.2 *Presentation of the test list*

These tests as a whole, aim at a complete validation of the level 2 protocol without redundancies. Each test is described as simply as possible to check precisely each elementary function of the protocol, which is referred in the columns “reference”, “title” and “sub–title” of each test description.

This list is presented in the form of a succession of tests. The presentation order is essentially functional. However, the operator performing these tests may change this order, taking into account some other practical criteria such as: use pre–test conditions to order the list, the end of a given test may be the pre–test condition of another test.

3 Test configuration

A single link will be used for level 2 tests. Figure 1/Q.781 shows a single link between SP A and SP B. Test specifications are written to test the level 2 of the SP A.

4 Test environment

See Recommendation Q.780, § 6.2.

5 Test list

Note – Compatibility test items are indicated in this list by an asterisk (*).

– The abbreviations *PO*, *LPO*, *RPO*, *EM* and *EDA* are used for processor outage, local processor outage, remote processor outage, emergency and expected delay of

acknowledgement respectively.

Link State Control – Expected signal units/orders **(Figures 8/Q.703 and 9/Q.703)**

* 1.1 Initialisation (Power–up)

* 1.2 Timer T2

1.3 Timer T3

1.4 Timer T1 and T4 (Normal)

* 1.5 Normal alignment – correct procedure (FISU)

1.6 Normal alignment – correct procedure (MSU)

1.7 SIO received during normal proving period

1.8 Normal alignment with PO set (FISU)

1.9 Normal alignment with PO set (MSU)

1.10 Normal alignment with PO set and clear

1.11 Set RPO when “Aligned not ready”

1.12 SIOS received when “Aligned not ready”

1.13 SIO received when “Aligned not ready”

1.14 Set and clear LPO when “Initial alignment”

1.15 Set and clear LPO when “Aligned ready”

1.16 Timer T1 in ““Aligned not ready” state

1.17 No SIO sent during normal proving period

1.18 Set and cease emergency prior to “start alignment”

* 1.19 Set emergency while in “not aligned state”

1.20 Set emergency when “aligned”

1.21 Both ends set emergency

1.22 Individual end sets emergency

1.23 Set emergency during normal proving

1.24 No SIO sent during emergency alignment

* 1.25 Deactivation during initial alignment

1.26 Deactivation during aligned state

1.27 Deactivation during aligned not ready

1.28 SIO received during link in service

* 1.29 Deactivation during link in service

1.30 Deactivation during LPO

1.31 Deactivation during RPO

* 1.32 Deactivation during the proving period

1.33 SIO received instead of FISUs

1.34 SIOS received instead of FISUs

1.35 SIPO received instead of FISUs

2 *Link State Control – Unexpected signal units/orders* (Figure 8/Q.703)

2.1 Unexpected signal units/orders in "Out of service" state

2.2 Unexpected signal units/orders in "Not aligned" state

2.3 Unexpected signal units/orders in "Aligned" state

2.4 Unexpected signal units/orders in "Proving" state

2.5 Unexpected signal units/orders in "Aligned ready" state

2.6 Unexpected signal units/orders in "Aligned not ready" state

2.7 Unexpected signal units/orders in "In service" state

2.8 Unexpected signal units/orders in "Processor outage" state

3 *Transmission failure* (Figure 8/Q.703)

3.1 Link aligned ready (Break Tx path)

3.2 Link aligned ready (Corrupt FIBs)

3.3 Link aligned not ready (Break Tx path)

3.4 Link aligned not ready (Corrupt FIBs)

* 3.5 Link in service (Break Tx path)

3.6 Link in service (Corrupt FIBs)

3.7 Link in processor outage (Break Tx path)

3.8 Link in processor outage (Corrupt FIBs)

4 *Processor Outage Control* (Figure 10/Q.703)

4.1 Set and clear LPO while link in service

4.2 RPO during LPO

4.3 Clear LPO when "Both processor outage"

5 *SU Delimitation, Alignment, Error Detection and Correction* (Figures 11/Q.703 and 12/Q.703)

5.1 More than seven "1"s between MSU opening and closing flags

5.2 Greater than maximum signal unit length

5.3 Below minimum signal unit length

5.4 Reception of single and multiple flags between FISUs

5.5 Reception of single and multiple flags between MSUs

6 *SUERM Check* (Figure 18/Q.703)

6.1 Error rate of 1 in 256 – Link remains in service

6.2 Error rate of 1 in 254 – Link into out of service

6.3 Consecutive corrupted SUs

6.4 Time controlled break of the link

7 *AERM check* (Figure 17/Q.703)

7.1 Error rate below the normal threshold

7.2 Error rate at the normal threshold

7.3 Error rate above the normal threshold

7.4 Error rate at the emergency threshold

8 *Transmission and reception control (Basic)* (Figures 13/Q.703 and 14/Q.703)

8.1 MSU transmission and reception

8.2 Negative acknowledgement of MSU

8.3 Check RTB full

8.4 Single MSU with erroneous FIB

8.5 Duplicated FSN

8.6 Erroneous retransmission – Single MSU

8.7 Erroneous retransmission – Multiple FISUs

8.8 Single FISU with corrupt FIB

8.9 Single FISU prior to RPO being set

8.10 Abnormal BSN – Single MSU

8.11 Abnormal BSN – Two consecutive FISUs

8.12 Excessive delay of acknowledgement

8.13 Level 3 Stop Command

9 *Transmission and reception control (PCR)* (Figures 15/Q.703 and 16/Q.703)

* 9.1 MSU transmission and reception

9.2 Priority control

9.3 Forced retransmission with the value N1

9.4 Forced retransmission with the value N2

9.5 Forced retransmission cancel

6 Test descriptions

MTP, LEVEL 2

TEST NUMBER:

PAGE:

REFERENCE:
STD: Fig.

TITLE:

SUB TITLE:

PURPOSE:

PRE–EST CONDITIONS:

CONFIGURATION:
1

TYPE OF TEST:

EXPECTED SIGNAL UNIT SEQUENCE:

SP

SP

Link

Link

1 – 0
SIOS

---------->

: Power ON

<----------

1 - 0
SIOS

TEST DESCRIPTION

1.

Check link enters correct state.

2.

At “Power – On” or Initialization the FIB, BIB, FSN, and BSN shall be as follows:
FIB = BIB = 1 : FSN = BSN = 127 (HEX 7F)

3.

Repeat test in reverse direction.

MTP, LEVEL 2

TEST NUMBER:

1.2

PAGE:

1 OF 1

REFERENCE:

Q.703 § 7

STD:

Fig. 8; Fig. 9, Fig. 11, Fig. 13; Fig. 14

TITLE:

Link State Control – Expected signal units/orders

SUB TITLE:

Timer T2

PURPOSE:

To check “Not Aligned” Timer T2

PRE–TEST CONDITIONS:

Link out of service

CONFIGURATION:
1

TYPE OF TEST:

VAT, CPT

EXPECTED SIGNAL UNIT SEQUENCE:

B

A

Link

Link

1 – 0
<----------

---------->

1 – 0

SIOS

: start

<----------

1 – 0

SIO

<----------

1 – 0

SIOS

TEST DESCRIPTION

1.

Timer T2 shall be in the range 5 secs to 150 secs.

MTP, LEVEL 2

TEST NUMBER:

1.3

PAGE:

1 OF 1

REFERENCE: Q.703 § 7
STD:
Fig. 9; Fig. 14

TITLE:

Link State Control – Expected signal units/orders

SUB TITLE: Timer T3

PURPOSE: To check “Aligned” Timer T3

PRE–TEST CONDITIONS:

Link out of service

CONFIGURATION:
1

TYPE OF TEST:

VAT

EXPECTED SIGNAL UNIT SEQUENCE:

SP

B

SP

A

Link

Link

<----------
1 – 0
SIOS

1 – 0

SIOS
----------->

: start

<----------

1 – 0

SIO

1 – 0

SIO

---------->

<----------

1 – 0

SIN

<----------

1 – 0

SIOS

TEST DESCRIPTION

1.

Timer T3 shall be in the range 1 sec to 1.5 secs.

MTP, LEVEL 2

TEST NUMBER:

PAGE:

REFERENCE: Q.703 § 7
STD: Fig. 8; Fig. 9

TITLE:

SUB TITLE:

PURPOSE:

PRE–TEST CONDITIONS:

Link out of service

CONFIGURATION: 1

TYPE OF TEST: VAT

EXPECTED SIGNAL UNIT SEQUENCE:

SP B

SP A

Link

Link

<----------

1 – 0 SIOS

1 – 0

SIOS

---------->

: start

<----------
1 – 0 SIO

1 – 0
SIO
---------->

<----------
1 – 0 SIN

1 – 0
SIN
---------->

<----------
1 – 0 FISU

<----------
1 – 0 SIOS

TEST DESCRIPTION

1.

At 64 kbit/s Timer T4 shall be in the range 7.5 secs (nominally 8.2 secs) and Timer T1 shall be in the range 40 secs to 50 secs.

2.

At 4.8 kbit/s Timer 74 shall be in the range 100 secs to 120 secs (nominally 110 secs) and Timer T1 shall be in the range 500 secs to 600 secs.