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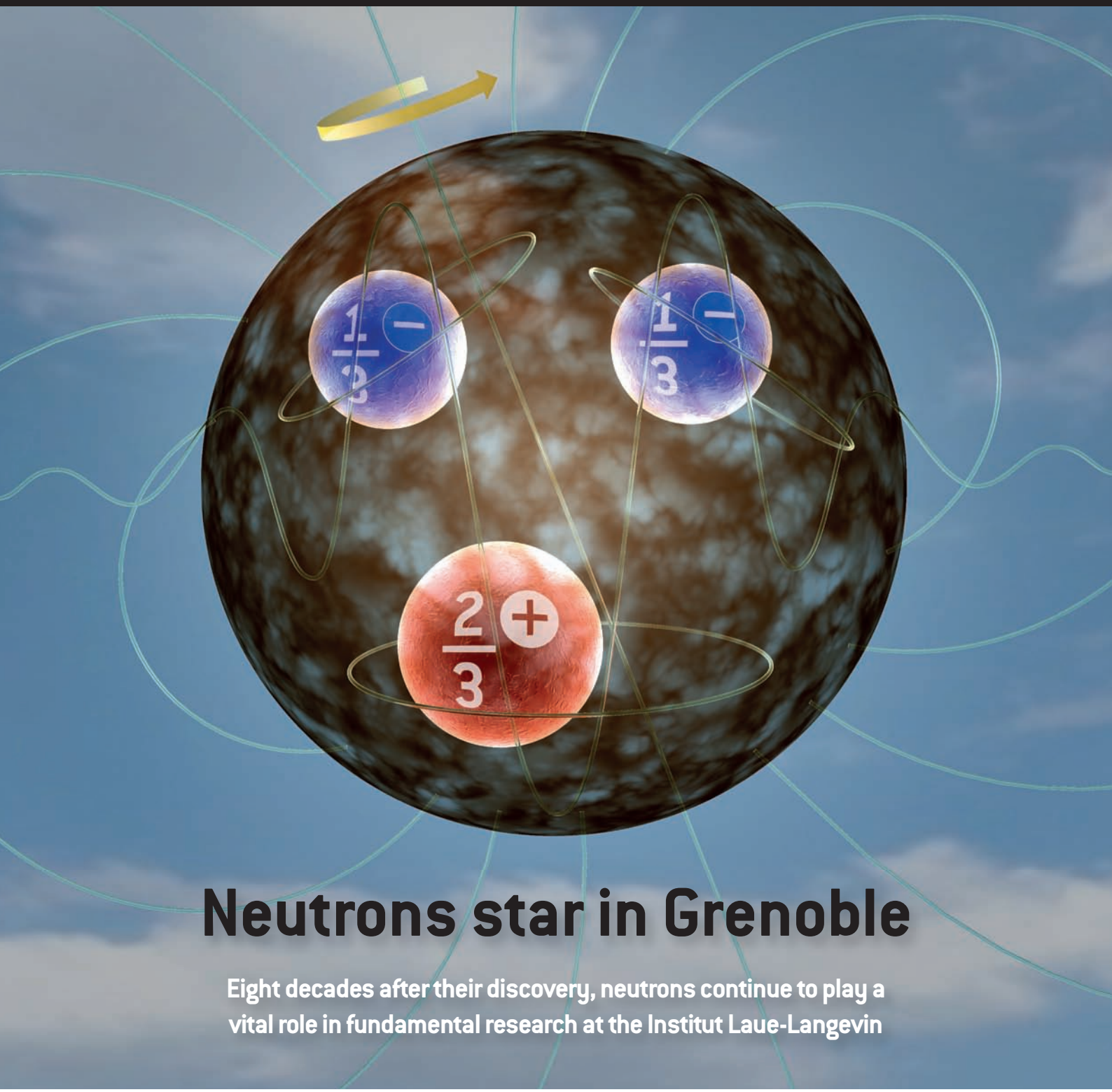
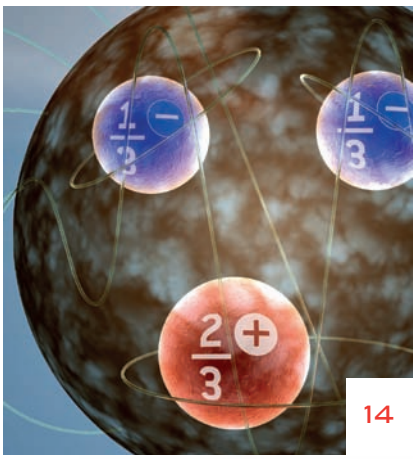
27 November 2012

TECHNOLOGY WATCH: LOW POWER RADIO • IMPROVING DYNAMIC A/D CONVERSION RANGE



Neutrons star in Grenoble

Eight decades after their discovery, neutrons continue to play a vital role in fundamental research at the Institut Laue-Langevin



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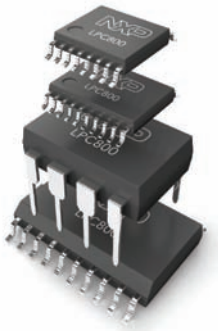

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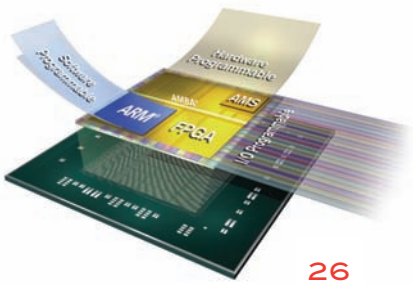

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Just goes to show

Attendance at electronica shows the electronics industry is in good health

Electronica – held every other year in Munich – is the world's largest electronics exhibition. As such, it's a bellwether for the industry. When times are hard, electronica feels it; when things are good, visitors have to force their way through the crowds.

It's a massive show which you have to see to appreciate. The 12 very large halls accommodate more than 2500 exhibitors and it's more than 1km from end to end. Such an event should regularly draw big crowds but, over the last few years, attendance has been declining; if only slowly. Given the current economic climate, there were many who thought this year would see another drop in visitor numbers. But that proved not to be the case; initial figures from the organiser put attendance at 72,000 – the same level as in 2010. Officially, there's 'cautious optimism' for the future.

Not surprisingly, Europe provides the bulk of the visitors, with Germany the largest of all. With the European economy officially in recession and Germany's economy only just showing growth, it would been understandable for companies to cancel travel plans. But they didn't – and what can we read from that?

Two things come to mind: firstly, engineers value exhibitions and their associated conferences as an excellent source of information. But there's another aspect to why they go. When New Electronics talked to exhibitors, one common observation was that engineers paid far more attention to product road maps than they would normally. That suggests they are looking further ahead than might be expected. In turn, that suggests that many companies have decided to scrap the next generation of their products in favour of bringing forward an innovative design featuring the latest available technology.

While electronica could be dismissed as an exception to the rule due to its size, exhibitions remain a valuable means of communication – whether you are an engineer or a supplier – and should be embraced.

Graham Pitcher, Group Editor (gpitcher@findlay.co.uk)

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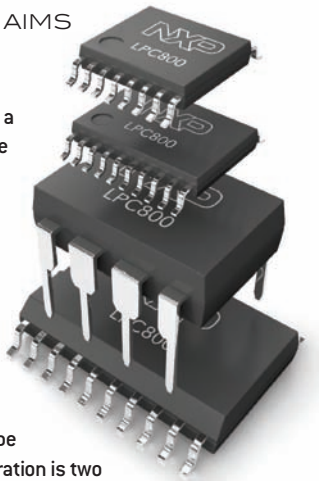
8bit simplicity, 32bit power

NXP LAUNCHES CORTEX-M01 BASED MCU AND AIMS FOR SIMPLICITY. **GRAHAM PITCHER** REPORTS.



Looking to make 8bit architectures obsolete, NXP has unveiled the LPC800 – a 32bit mcu designed specifically for 8bit applications. The device, based on the ARM Cortex-M0+ core, is designed to bring flexibility without complexity.

Jan Jaap Bezemer, director of mcu marketing, said: "We believe nobody delivers what 8 and 16bit users want, but we didn't want to design a 32bit entry level part; rather, we've developed an 8bit part with 32bit technology."

One of the features which enables the device to be offered in low pin count packages is a flexible switch matrix which allows on chip peripheral I/O to be assigned to nearly any pin. "We have also assigned system critical functions to the same pins," Bezemer continued, "which means designers can lay out a board for the 20pin version, but use a 16pin part initially."

Another further innovation is a state configurable timer (SCT), which can be customised to meet specific application requirements. The basic SCT configuration is two 16bit PWMs with four capture inputs and four match outputs, with each match register shadowed. This is said to allow the LPC800 to deliver most timing or PWM functions found on 8bit mcus.

The LPC800 uses 64byte page flash to simplify code management and this can be used to emulate eeprom for data storage.

Power semiconductor manufacturers push efficiency

Fairchild announced silicon carbide (SiC) solutions for power conversion systems. Among the first products in its SiC portfolio is a family of SiC bipolar junction transistors (BJTs) that offer high efficiency, high current density, robustness and high temperature operation. Fairchild claims the parts enable higher switching frequencies due to lower conduction and switching losses, while providing up to 40% more output power. The 1200V devices are suitable for use at operating temperatures of 175°C and come in to247 packages.

Infineon says Trenchstop 5, the latest generation of its thin wafer igbt technology, sets a 'new benchmark' in igbt performance. There are two product families. HighSpeed 5 is a soft high speed igbt designed for ease of use and the plug and play replacement of existing igbts, while HighSpeed 5 FAST is said to be the most efficient igbt yet.

Improvements in efficiency mean a Trenchstop 5 device in a to220 package has a case temperature 15% less than an H3 part in a to247.

Finally, International Rectifier launched its Gen8 igbt range. The 1200V platform uses IR's trench gate field stop technology to offer high performance in industrial and energy saving applications. Produced on thinned wafers to improve thermal resistance and increase the maximum junction temperature to 175°C, the Gen8 range has 10 members, with a maximum rating of 200A.

Specialist division launched to address power technology

Future Electronics is looking to improve technical and supply chain service to OEM buyers of power components and modules with the launch of Future Power Solutions (FPS), its latest specialist division.

FPS has been organised to offer in depth, specialist technical and market understanding of power technology, while drawing on Future's global supply chain capabilities. It will sell a range of discrete power components, power modules and standard and configurable power supplies, as well as developing and producing custom power solutions via its System Design Centres.

Steve Carr, pictured, technical and vertical markets director, said: "We have built an ecosystem aimed mainly at industrial customers. Two teams are available – power and analogue specialists – and we're looking to target everything from ac to point of load."

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VISIT THE GALLERY

Atmel announced Atmel Gallery, an app store for development tools and embedded software that provides easy access to free and commercial extensions for Atmel Studio. It also launched Atmel Spaces, a cloud based collaboration workspace for hosting software and hardware projects targeting Atmel mcus. The company says Spaces makes it easy for designers to collaborate, resulting in a community of developed tools and embedded software for Atmel mcus.

330W FROM LOW PROFILE PACKAGE

Vicor launched the VI BRICK AC Front End module. Operating from a universal ac input, the device delivers a fully isolated and power factor correction regulated 48V/330W output. Supplied in a package measuring 95 x 49 x 10mm, the module has a power conversion density of 7.5W/cm^3.

MORE THAN A GESTURE

Microchip believes its GestIC technology will enable the development of intuitive, gesture based, non contact user interfaces for a broad range of applications.

GestIC technology – with a range of up to 15cm – uses sensing electrodes made of any conductive material, including pcb traces. It is said to provide for 100% surface coverage and to eliminate 'angle of view' blind spots.

The first in the range is the MGC3130, which consumes as little as 150μW in its active sensing state.

QUAD CORE AUTO MCU

Freescale and Continental have jointly designed a quad core mcu optimised for electronic braking systems and for chassis control. The first device in the Quasar family integrates four Power Architecture e200z4 cores, with two pairs of cores in redundant lockstep.

Dr Adrian Traskov, ic development manager for Continental's Chassis and Safety Electronic Brake Systems business unit, said: "Creating a device of such complexity has required close collaboration between Continental and Freescale. We're working in unison to develop what we think will be a breakthrough in multicore technology for the automotive industry."

Quasar integrates 4.75Mbyte of flash, 256Kbyte of sram and Continental's fail safe technology, which meets ISO26262 and SIL 3 requirements.

Briefs

DECT ULE module

RTX showcased what it claims is the world's first IPv6 enabled DECT ULE wireless module – the RTX 1050/1055. It provides connectivity to the internet for battery powered equipment or metering applications within a 300m range.

DECT ULE – the 'ultra low energy' variant of DECT – uses the 1.9GHz band and is said to suffer less interference than Bluetooth, WiFi and Zigbee.

Protection device

TE Circuit Protection introduced the 2Pro AC, said to offer an integrated, resettable approach to protecting sensitive downstream electronics against overcurrent and overvoltage.The part integrates a polymeric positive temperature coefficient device and a thermally enhanced metal oxide varistor.

LIN based control

Melexis says the MLX8110 is the first LIN RGB led slave to be incorporated on to one die. Designed for LIN based automotive rgb ambient lighting systems, the device can drive up to four leds directly, and each output can be programmed to a maximum current of 35mA.

Improving lighting

Power Integrations' LYTSwitch family of led drivers is said to deliver tight regulation and high efficiency for tube replacements and high bay lighting. The devices combine power factor correction and constant current in one switching stage, increasing driver efficiency to more than 90% in typical applications, delivering a power factor greater than 0.95 and meeting EN61000-3-2C requirements for total harmonic distortion.

Intelligent displays

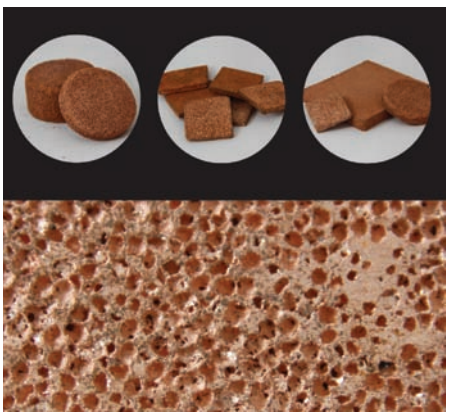
At 10.2in, demmel's DPP-CT1060A features a faster DPC3090 processor, a brighter display and 12Mbyte of flash. Execution and transmission times are said to have been improved by more than 50%. CEO Herbert Demmel told *New Electronics*: "It's now even easier have to a solution ready for the market."

Testing solution

Goepel introduced G-TAP, designed for contacting electronic assemblies – in particular the JTAG bus – during test and programming. The module can be used in standalone operations, as well as in existing electronic and optical test systems, such as flying probers, in circuit test or AOI systems.

Next generation heat transfer

Microporous metallic material set to meet board level heat transfer challenges. **Simon Fogg** reports.



Versarien unveiled a microporous metallic material that it claims could radically change the field of thermal management.

VersarienCu is said to be up to 10 times more effective at transferring heat than conventional microchannel heat sinks of equivalent size – with a heat transfer coefficient of approximately 150 to 200kW/m^{2}K.

"We believe this technology could be the next generation of thermal management and could lead to much faster devices for consumers and industry," Versarien ceo Neill Ricketts told *New Electronics*.

Developed through research at the University of Liverpool, the Lost Carbonate Sintering process creates a homogeneous distribution of micro fine pores throughout the copper base material. This open cell porous metal structure permits a reduction in heat sink weight and physical dimensions, thereby enabling considerably smaller form factors.

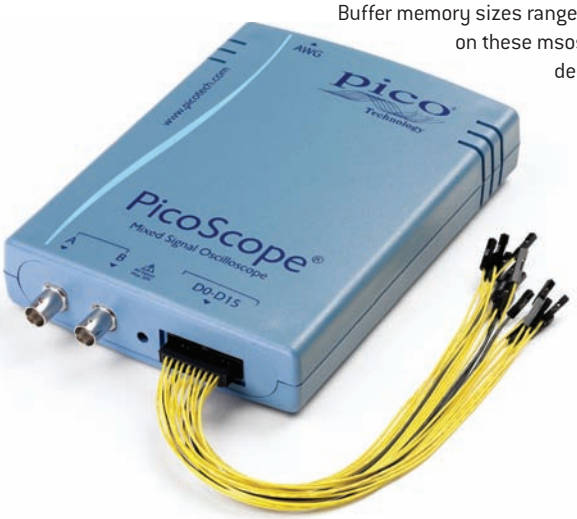
"The fine, open, interconnected pores formed allow major performance improvements to be realised – with thermal transfer levels that are an order of magnitude better than what alternative thermal management solutions currently on the market are capable of," added Ricketts.

Pore diameters ranging from 20μm to 1mm can be specified, with porosity levels of up to 85%. The material is targeted at cooling mechanisms in space constrained system designs, including applications in data communications, renewable energy, power distribution, avionics, defence, automotive, transportation, gaming and motorsport.

MSO is 'complete test bench'

Picoscope showcased a new range of mixed signal oscilloscopes (mso), said to offer a complete test bench in a compact, usb powered device.

The Picoscope 3000 series features a 16 channel logic analyser, a built in function generator and an arbitrary waveform generator. There are two analogue channels with bandwidths from 60 to 200MHz, a maximum single channel sampling rate of 500Msample/s, and 10MHz digital inputs.



Buffer memory sizes range from 8 to 128Mpts. "The deep memory on these msos works especially well with the serial decoding feature," explained Alan Tong, Pico's managing director. "You can capture serial data using any of the two analogue and 16 digital inputs, giving you up to 18 channels. All of these can be decoded concurrently, even if you have a mixture of serial protocols."

Serial data in i^{2}c, uart/RS232, spi, CAN bus, LIN and FlexRay formats can be decoded and displayed in binary, decimal or hexadecimal formats. The 16 logic inputs are organised in two banks, each of which has its own adjustable logic threshold to allow testing of mixed logic designs.

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- Superior color uniformity
- Uniform light distribution
- Optimized color mixing

SRGB2 (PLCC6) **SRGB-S**

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- Black reflector type
- High brightness
- Superior color mixing
- 4 Pin / 6 Pin types

Stepping ahead

Researchers give graphene a useable bandgap. **Graham Pitcher** reports.

Graphene, viewed by many as a future replacement for silicon, has been limited by its small bandgap. However, by fabricating graphene structures on top of nanometre sized 'steps' etched into silicon carbide, researchers from Georgia Tech have created a bandgap of 0.5eV in the material, which could make it suitable for room temperature electronics.

Professor Edward Conrad from Georgia Tech's School of Physics said: "We can now look seriously at making fast transistors from graphene. And, because our process is scalable, if we can make one transistor, we can potentially make millions of them."

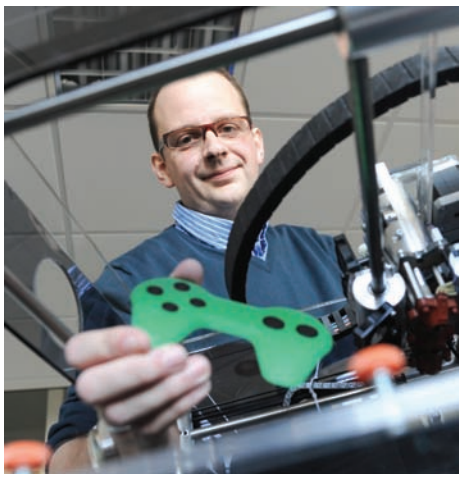
The method, which bends 1.4nm graphene nanoribbons into 20nm deep steps in SiC wafers, is said to potentially enable the fabrication of entire integrated circuits from graphene nanoribbons. "We can make thousands of these trenches and we can make them anywhere we want on the wafer," said Prof Conrad. "This is more than just semiconducting graphene; the material at the bends is semiconducting and it's attached to graphene continuously on both sides. It's basically a Schottky barrier junction."

Time for grid to get smarter say CEOs

The ceo roundtable at this year's electronica took a look at the smart grid and how semiconductors can boost energy efficiency. It's no surprise that major semiconductor manufacturers see power efficiency as a technology in which they can focus.

All participants agreed there was a lot of opportunity to improve the efficiency of power networks and that semiconductors will bring big benefits. Areas where semiconductors can be applied included better use of the grid's existing capacity and a focus on sensors and M2M. NXP ceo Rick Clemmer believes that M2M can provide for energy reduction and a better quality of life. "We see the opportunity for everything to have an IP address. With that, apps will allow you to control everything." Freescale ceo Gregg Lowe believes intelligence can be added through sensors. "We need to understand what's happening; smart thermostats, for example." STMicroelectronics' ceo Carlo Bozotti noted: "About 20% of the grid is only there to meet peak demand. There's a lot of opportunity to improve efficiency and semiconductors can really bring benefits." And newly installed ceo of Infineon Reinhard Ploss said: "We need to switch from ac to dc transmission and get rid of reactive power. While semiconductors might help with transport issues, we can't solve the problem overnight; we have to add intelligence and balance supply and demand."

The panellists were, from the left, Gregg Lowe, Carlo Bozotti, Rick Clemmer and Reinhard Ploss, with moderator Killian Reichert.



Composite could allow printable electronic devices

Researchers at the University of Warwick have developed a conductive plastic composite that can be used to produce electronic devices on low cost 3d printers.

The material, nicknamed 'carbomorph', enables users to lay down electronic tracks and sensors as part of a 3d printed structure – allowing, for example, the creation of touch sensitive areas, which can then be connected to a simple pcb.

Dr Simon Leigh, from the Department of Engineering, said: "We set about trying to find a way in which we could print out a functioning electronic device from a 3d printer.

"In the long term, this technology could revolutionalise the way we produce the world around us, making products such as personal electronics a lot more individualised and unique and, in the process, reducing electronic waste."

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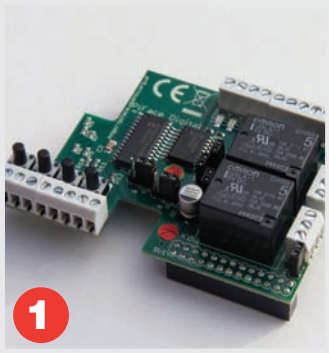

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Neutrons star in Grenoble

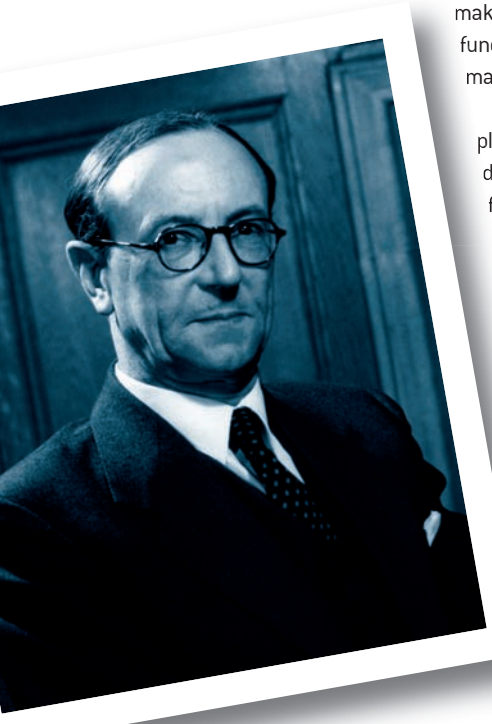
Eight decades after their discovery, neutrons continue to play a vital role in fundamental research. By **David Boothroyd**.

The dictionary definition of 'neutral' includes 'not taking part or giving assistance' and 'of no particular kind, indefinite', which might not sound particularly promising if what you are looking for is a particle enabling you to probe precisely the ultimate constituents of matter. But that is exactly what the atom's electrically neutral component, the neutron, has done.

It has been 80 years since the neutron – the third basic component of the atom, along with the proton and the electron – was discovered. The English physicist James Chadwick made the discovery in Cambridge in 1932, though its existence had been predicted for many years. Because the neutron is neutral – and therefore lacks any charge – isolating and identifying it was a major technical challenge.

Yet it is the neutron's very neutrality that makes it such a powerful tool; it means neutrons can penetrate more deeply into matter than alternative kinds of probes. However, their path is not completely clear and interactions with atomic nuclei do deviate them and change their speeds. These interactions make it possible to examine the fundamental properties of materials.

The result is the neutron has played a central role in discoveries of great significance for the electronics and computing industries. Many of these took place at one of the world's leading neutron research centres, the Institut Laue-Langevin (ILL), based in Grenoble, and funded and managed by the UK, France and Germany.



Sir John Chadwick worked with Sir Ernest Rutherford at the Cavendish Laboratory, investigating atomic structures through bombardment with alpha particles. As a result of this work, he proved the existence of neutrons in 1932 – an achievement rated as one of the most important scientific discoveries of the 20th Century. In recognition of his work, Chadwick won the 1935 Nobel Prize in Physics.

Today, the Institute operates one of the most intense neutron sources in the world, feeding beams of neutrons to a suite of 40 high performance instruments. Some 1500 researchers from more than 40 countries visit the ILL each year, including chemists, physicists, biologists, crystallographers, specialists in magnetism and nuclear physics.

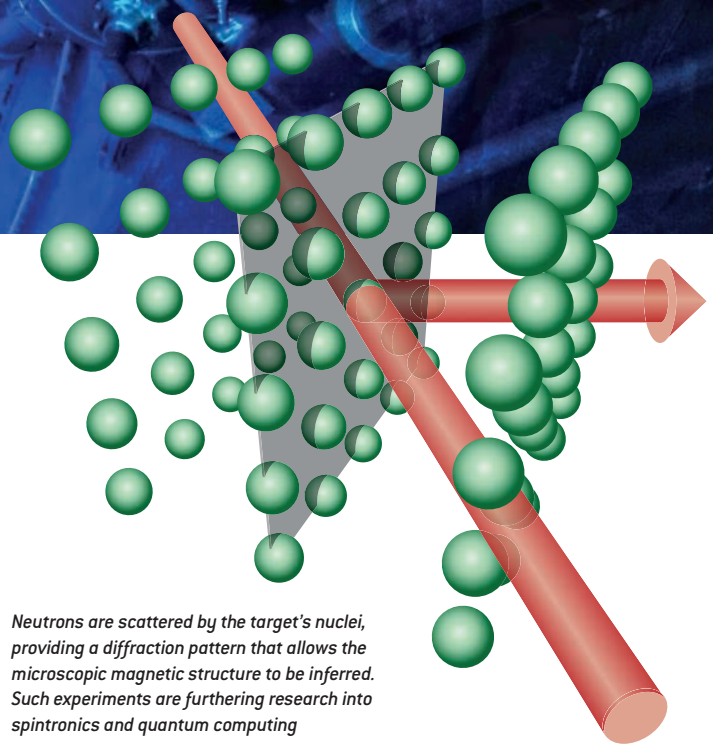
It is not only their lack of charge that makes neutrons a powerful tool. The neutron is the only probe capable of seeing both the nuclei of atoms and, at the same time, the magnetic interactions of their electrons. Because neutrons possess a magnetic dipole moment, it makes them sensitive to magnetic fields generated by unpaired electrons in materials. This means extremely precise data about the materials' magnetic behaviour at the atomic level can be collected.

In addition, the scattering power of a neutron off an atomic nucleus depends on the orientation of the neutron and the spin of the atomic nuclei in a sample. This makes the neutron a powerful instrument for detecting the nuclear spin order, giving it great potential value in the field of spintronics.

Several neutron techniques are used at the ILL, including a form of tomography, neutron diffraction or scattering, and reflectometry. The latter approach provides data for many applications, including the structure of thin film magnetic systems and biological membranes. Here, a neutron beam is aimed at an extremely flat surface and measurements are taken of the intensity of reflected radiation as a function of the angle or the neutron wavelength. The reflectivity profile provides detailed information about the structure of the surface, including the thickness, density and roughness of any thin films layered on the substrate.

"Neutrons have the advantage here because they can penetrate very deeply, so you can see layers beneath the surface; which is increasingly important as more complex heterostructure materials come to be developed," says Laurent Chapon, a senior fellow at ILL.

One field in which Chapon is working is magneto electrics. The aim here is



Neutrons are scattered by the target's nuclei, providing a diffraction pattern that allows the microscopic magnetic structure to be inferred. Such experiments are furthering research into spintronics and quantum computing

to build materials where it is possible to control the electrical and magnetic properties. So you could control or 'tune' the magnetic properties with an electric field, or vice versa. Neutrons are being used to try to understand at the microscopic level what are the mechanisms responsible for this coupling between electricity and magnetism. The field of spintronics could benefit from this; sensors would be another potential application.

"Why does a system that is not interesting in an electrical sense when it is magnetically disordered, suddenly become ferroelectric – why does it have a spontaneous electrical polarisation, suddenly when it is magnetically ordered?" Chapon explains.

Although neutron diffraction is well established, there have been significant enhancements to it. In the last few years, it has become much easier to polarise the neutron beam, aligning the magnetic moment of the beam in a particular direction.

"This makes for a much more sensitive technique, and one potential application is in thin film technology, especially where there are several layers involved. A lot of the data about the materials cannot be obtained optically," Chapon notes.

There are many application areas for neutron studies in IT. Some are already widely in use, like the giant magnetoresistance (gmr) effect exploited by hard disk technology, and superconductivity.

GMR was introduced commercially by IBM at the end of 1997, offering far greater sensitivity than conventional magnetoresistive heads and playing a major role in making terabyte disks commonly available.

"Industry seized on it to manufacture magnetic probes and for information storage," says Chapon. "Much research during the last 30 years has gone into magnetoresistive systems and progress has been remarkable. However, a deeper understanding of the underlying phenomena is needed to improve performance. This requires the magnetism of the material to be analysed at the atomic scale and neutrons are a convenient tool for doing that."

Many ILL projects are research programmes, where neutrons are used to study with great precision the fundamental properties of materials, such as multifunctional materials. These can exhibit a variety of valuable physical properties, like optical activity, laser properties and piezoelectricity. The basic mechanisms allowing these properties to coexist within a single compound are still poorly understood.

One example is the langasite family (lanthanum gallium silicate compounds), which exhibit striking piezoelectric and nonlinear optical

Chapon: "Neutrons have the advantage because they can penetrate very deeply, so you can see layers beneath the surface."

properties and have potential application in bulk acoustic wave and surface acoustic wave devices, as well as in nonlinear optics and electro-optics.

Another interesting family of materials where neutron studies have played an important role is electroceramics for microwave communication. Commercial components are used in applications like multilayer capacitors, thermistors, and piezoelectric transducers/actuators.

New ceramic materials also enabled the revolution in superconductivity during the 1980s, when superconduction was seen at much higher temperatures than had previously been thought possible. Here, the ILL's expertise in neutron diffraction played a key role in many major developments.

"Although it is not yet fully understood at a detailed level, it is thought the interactions that enable materials to be superconductors are mediated through some kind of magnetic fluctuations," says Chapon. "Neutron diffraction is an ideal tool for studying them."

Even though it is more than 25 years since the first high temperature superconductors were discovered by IBM, work in the field is still extremely active, as new kinds of materials have been found recently, including iron based compounds.

Attractive work

ILL is also helping with the study of tiny magnets, a project being carried out by the University of Manchester's Molecular Magnetism Group, as the group's Eric McInnes explains.

"There is much interest in the crossover regime between large scale matter and molecular materials that are governed by the laws of quantum mechanics, especially in the magnetic properties. As you go from very small to very large molecules, at what stage do they start to behave like bulk magnets? Molecular magnetism is the study of properties of complex magnetic molecules."

Magnetism is all to do with the quantum mechanical property of electron spin, which gives rise to magnetic moment. These moments cancel out in most materials because electrons pair up, but in many metal based compounds there are unpaired electrons, making them magnetic.

The question is, what happens if you bring together lots of these individual magnetic centres in one molecule? How do they interact with each other? Normally, they would be probed indirectly, but inelastic neutron scattering is making it possible to examine such systems directly, a key target for the Manchester group.

"It is similar to the development of atomic force microscopy," McInnes says. "This showed actual images of atoms, which until then had been no more than a piece of theory, a mathematical function. Similarly, the recent work has shown directly the phenomenon of spin correlation, rather than it just an element in a theoretical model.

"The Institute has developed wonderful advances in instrumentation, in terms of both sensitivity and the amount of data they collect over 3d space. This enables you to analyse the interactions directly, without having any assumed model – which is how you would normally do it. Getting this kind of data is the only way you can truly understand what is going on and, from there, develop better materials for applications you are looking to create."

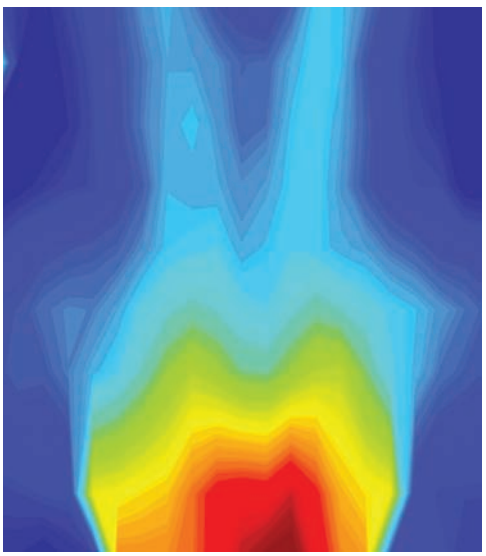
In inelastic neutron scattering, a beam of neutrons is fired at a magnetic sample, which absorbs some of the neutrons' energy and momentum. From the way in which the neutrons are scattered by the material, together with the knowledge of how they were previously, characteristics of the material can be deduced.

"The data on what happens to the neutron beam has to be collected over a range of angles and previously this has been limited," McInnes says. "The ILL's arrays of detectors let you access a huge space of scattered neutrons, which gives you much more information.

"A major result is that we have shown you can actually do the experiment – that it is possible to get information about this class of molecular materials, to get a far more detailed picture of how these magnetic centres interact with each other within a molecule. These are the things that determine the molecule's magnetic behaviour and understanding these is vital to create applications exploiting spintronics, for example."

Creating qubits

Another potential application of molecular magnetism for computing in the future is the creation of the basic component of a quantum computer, a qubit. The principle behind this is that a molecular magnet ultimately is governed by quantum mechanical laws, and it is possible to take advantage of the quantum nature of the magnetic properties – in effect, control and manipulate them, to build a quantum computer.



While practical application for this work is still some way in the future, qubits have already been created on a limited scale using other techniques and McInnes thinks the same will soon be done with molecular magnets. However, turning that into something computationally useful is a much larger step.

Even so, the ILL's neutron capabilities are likely to play a key role in the qubit work, because they will hopefully enable the team to link two qubits and then measure their quantum 'entanglement' directly. Entanglement is the exclusively quantum effect when two particles become intimately connected so that action taken on one instaneously affects the other, whatever their separation.

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Which wireless?

It seems that, nowadays, everyone wants to include wireless connectivity in their products. In many of these designs, wireless connectivity makes sense; passing information from one device to another can help to improve efficiency. But the question that is to the fore is which method of wireless communication is best?

Not so long ago, that was a question easily answered. Today, however, engineers are faced with a range of approaches: from mobile phone based technologies at one end of the spectrum to ultra short range approaches, such as Near Field Communications, at the other. In between is a burgeoning number of technologies. Some, such as Bluetooth, ZigBee and Wi-Fi, are familiar. Others, such as white space, WirelessHART and ad hoc on demand distance vector (AODV) routing, may be less so.

Yet if they are to select the best solution for their design, engineers need to be familiar – or better – with all communications methods. And that's a challenge, because even the more familiar technologies continue to change.

Consider Wi-Fi. Since its original inception as IEEE802.11, the technology has spawned many subsets, each either boosting throughput or addressing a particular application. IEEE802.15.4 is another example. The basis for ZigBee has several PHYs, several updates and a choice of which part of the spectrum to use. Add in different data rates and a selection of transmission methods and what appears to be a standard turns out to be something else.

Even ZigBee is beginning to sprawl. Specifications have been released to address: home automation; smart energy; telecomms; health care; and remote controls. Specifications are being developed for building automation and retail and a further 'wrinkle' is the development of the ZigBee Light Link, which will allow the wireless control of domestic lighting.

With such a wide range of approaches, there will be casualties. But don't expect to have an 'either/or' choice in the near future.

Glenn Jarrett, head of electronics marketing, RS Components

Short range, low power radio is a hotbed of anarchy amid the highly regulated sections of the radio spectrum, reserved for access by the military, communications companies and TV channels.

The low power radio zones are tiny slices of spectrum where, as long as you obey the rules of transmission power, you can do more or less what you like. And, for decades, most companies have – choosing to define and operate their own protocols. However, in the past 10 years, standardisation efforts have accelerated with the aim of expanding the market for low power wireless and bringing disparate electronic systems onto the internet.

If there is one winner in this low power radio world, it is IEEE802.15.4. But that is largely because it benefits from the effect that Andrew Tanenbaum noticed when he quipped about standards. "The nice thing about standards is that you have so many to choose from." There is no single radio protocol in IEEE802.15.4 – it is a collection of physical layer interface specifications and media access layer control protocols that can be mixed and matched freely.

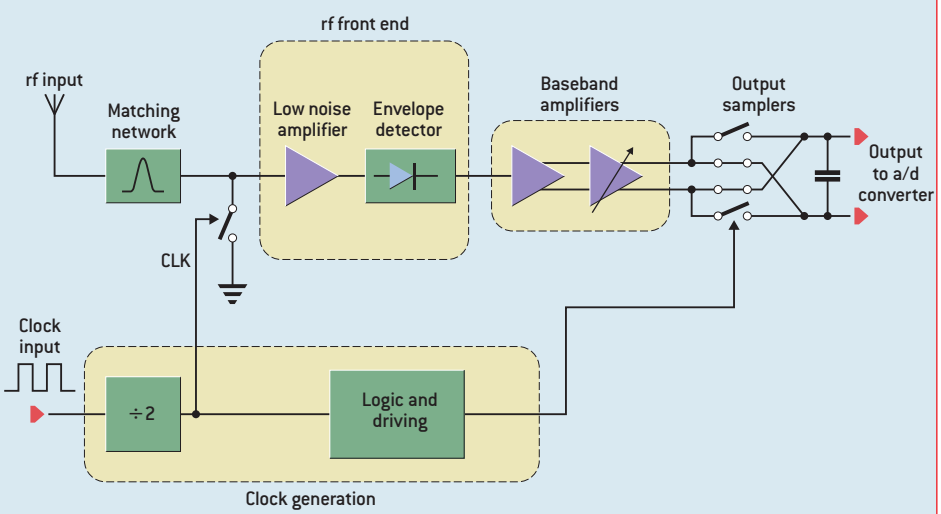
Since the release of the first version of IEEE802.15.4, which itself contained several options for the physical interface, the IEEE has

Elster's V200 digital water meter features ZigBee technology developed by Ember, now part of Silicon Laboratories.

Controlled chaos

There are a wide range of methods which designers can use to enable low power radio communications. By **Chris Edwards**.

Fig 1: Block diagram of the imec low power radio presented at ISSCC in 2010



followed with three updates that double the number of possible types of radio link. The original standard was based around three unlicensed bands. For Europe, it supports the 868MHz band, for the US, it's the 915MHz band. However, for greatest international support, most choose the increasingly congested 2.4GHz, which has to be shared with Bluetooth, WiFi and a variety of other unlicensed radio systems.

The original version of IEEE802.15.4 described the use of direct sequence spread spectrum (DSSS) techniques for each of the bands – running at up to 40kbit/s in the sub 1GHz region up to 250kbit/s in the 2.4GHz region, thanks to its greater bandwidth. Three years later, data rates for the sub 1GHz bands were increased and the revision introduced other modulation schemes, allowing the use of binary or offset quadrature phase shift keying or a combination of binary keying and amplitude shift keying. More recent work has opened bands for use in China – centred on 315MHz, 432MHz and 784MHz – and in Japan, with a 953MHz band. That's not all.

A decade ago, the 802.15.4 working group voted to establish a study group that would look at adopting a physical layer that used alternative types of radio transmission to traditional shift keying or spread spectrum techniques. One method proposed chirp spread spectrum for the 2.4GHz band instead of the conventional direct sequence or frequency hopping techniques. The other was ultrawideband (UWB).

Because it uses the spacing between broadband chirps to relay data, rather than modulating a bit pattern on to a narrowband carrier, UWB is not tied to a specific frequency band. In practice, UWB communications are limited to regions above several gigahertz or to sub 1GHz frequencies in order to avoid interference with sensitive spread spectrum protocols – such as the Global Positioning System – which also spread radio power over a sizeable bandwidth. Approval has been granted for UWB at more than 6GHz in Europe, with allowance for operation below that range at very low power levels, and between 3GHz and 10GHz in the US. However, operation in these regions tends to limit range and makes transmission more dependent on line of sight, which causes problems for some of the anticipated applications.

When the UWB version of 802.15.4 was being developed, the rationale for yet another radio interface was that a number of companies had identified problems with existing RF tag technologies. In a warehouse, the tags let you know there are pallets in range with certain contents, but a forklift operator armed with just a scanner will not be able to work out which one is which without checking each pallet individually. A network of three or four UWB-enabled receivers can use precisely measured time differences to pinpoint each transmitter and send that information to the operator's terminal.

At low data rates – typically less than 200kbit/s – the potential range of UWB is 100m or more. However, operation at frequencies well into the gigahertz range will limit the potential range and push up the number of receiver nodes. Even so, if the UWB version of 802.15.4 takes off, it might lead to a TV remote control that tells you that it's fallen down the back of the sofa.

One approach to the RF physical layer that is not covered by any part of 802.15.4 is the concept of white space radio. Frequency hopping protocols such as Bluetooth already use a limited form of white space radio – constantly shifting the transmitting frequency to 'hop' out of the way of interference. White space radio opens the concept to a much wider range of the radio spectrum, looking for gaps in transmission both in frequency and time, using those for communication until an interfering station starts broadcasting. White space radio is still in its infancy, although it has been bolstered

by the formation of the Weightless group, which numbers ARM, Cable & Wireless and Neul among its members. The group is working on a protocol that can be used from short ranges to up to 10km to support applications such as remote meter reading.

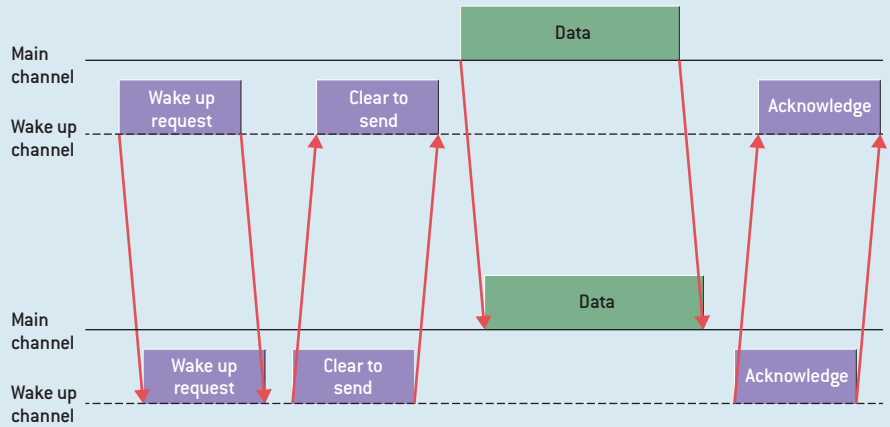
With 802.15.4, the question of which standard to use gets worse as you move into the transport and application layers of the protocol stack. A baffling array of companies and groups have opted to use 802.15.4 as the substrate for their own wireless networking protocols.

The most famous right now is Zigbee, which has captured a large number of supporters, but has yet to translate that support into a market that rivals more widely used protocols such as Bluetooth and WiFi. According to IMS Research, Ember – acquired earlier in 2012 by Silicon Laboratories – was the market leader in Zigbee chips in 2010, with a share of around 30%. By the end of 2010, the company had shipped 10million chips since its inception a decade earlier. That figure had grown to 25m by the time of the company's acquisition. According to IMS, wearable devices alone – many, such as sports watches, using proprietary low power radio protocols – saw shipments rise in 2011 to 14m a year. Extend that to mobile phones with Bluetooth and the number rises to hundreds of millions.

The Zigbee Alliance and its members promote the standard as being the driver for the 'internet of things', linking building automation controls and personal devices together wirelessly. But it has to compete with other specifications, such as 6LoWPAN; an adaptation of the core internet protocols for low power radio which also uses the 802.15.4 stack to provide the physical and media access layers. Because the existing internet is running out of addresses, 6LoWPAN takes advantage of the much larger IPv6 address space to make it possible, at least in principle, to give an IP based ID to every electronic device in the world for years to come.

A contender with its roots in the industrial market – and therefore a large installed base of equipment that already uses its wired equivalent – is WirelessHART. Dust Networks, one of the developers of the concept of the internet of things and recently acquired by Linear Technology, developed the time sequenced mesh protocol (TSMP) behind WirelessHART.

Fig 2: A typical sequence of operations in event driven radio



This protocol is used for the MAC layer in place of those defined in 802.15.4. Another protocol that has emerged in industrial process control is ISA100, which also employs TSMP. The attraction of protocols such as TSMP is power consumption.

With most protocols, the problem with having a receive channel is that the node does not know when a message will turn up and simply has to keep listening. This makes it hard to power down, which is bad news for a wireless sensor node, where long periods spent asleep punctuated by bursts of activity, provide the key to a 10 year service life on a single battery charge or make energy scavenging viable.

Applications which don't listen

Some applications can work around this problem by simply not listening to the radio environment. In Spring 2012, the IEC approved a standard based on EnOcean's low power communications protocol which revolves around this concept. The protocol is used in devices such as wireless light switches – force on a switch with a piezoelectric backing provides just enough energy to send a command over a short range wireless link.

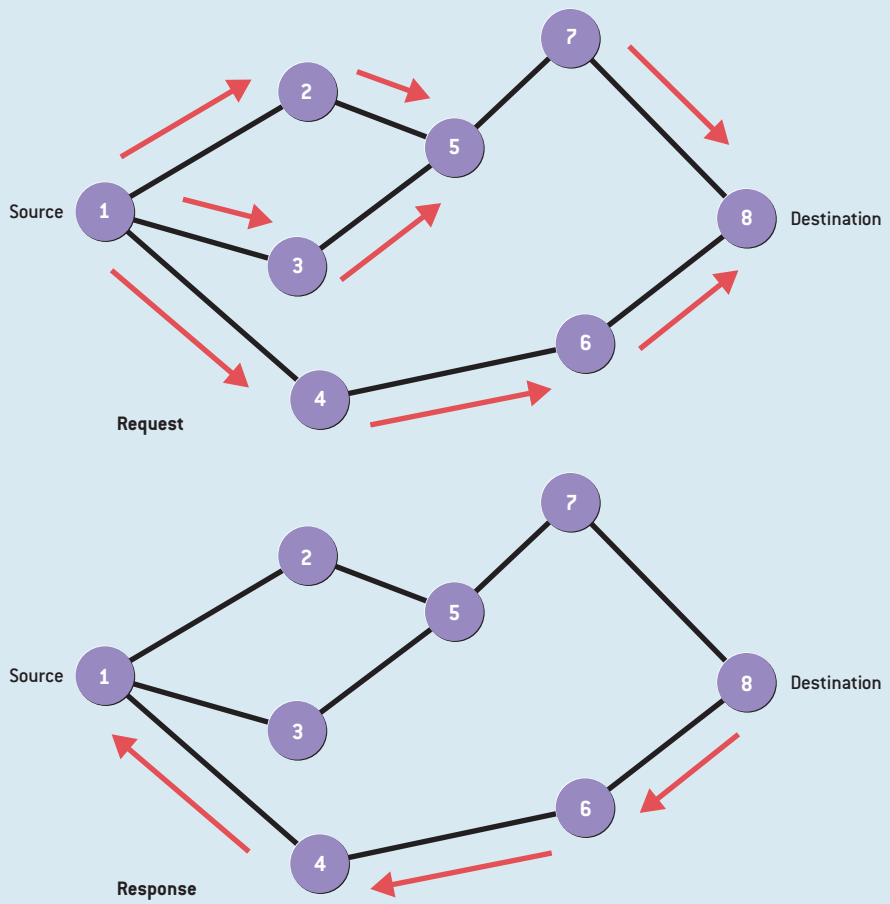
Although the instantaneous power draw of a transmitter is usually higher than that of an active receiver, the long term average consumption is usually much lower because the radio link only activates when there is data to communicate. Having a system that can only transmit presents some configuration issues – it's hard to verify automatically that a switch is still working remotely without sending someone out to test it physically.

One option is for a node to only listen when it is expecting to receive data, one of the philosophies behind protocols such as TSMP or the time synchronised protocol used by Zigbee. Nodes that employ the protocol can synchronise their clocks using received data packets to within 1ms to ensure there is not too much overlap between periods when two or more nodes are active. The time slotted nature of the protocol also reduces the probability of collision if more than one node attempts to transmit data, harking back to the time slotted version of the Aloha protocol used to connect computer users on the Hawaiian islands in the 1970s and which provided the inspiration for Ethernet.

One mechanism that promises greater energy savings, but which is not yet mainstream is the concept of event driven radio. This uses a second, very low data rate RF signal to alert nodes when a transmitter wants to contact them. Only then do those nodes activate the receiver for the main RF link to listen for the data. Once the data has been received, they put the main receiver to sleep, allowing just the event driven radio to function. Research institutes such as IMEC are continuing work on event driven radio and one of IMEC's designs has a power consumption of 50µW, ten times lower than that of the analogue section of a typical narrowband receiver (see fig 1).

IMEC's receiver dispenses with many of the analogue blocks common to just about every other RF processing unit in use today.

Fig 3: An AODV packet send request and a successful response



Oscillators and phase locked loops consume too much power and so have been excluded. The modulation is simple on-off keying because this allows the receiver to use simple energy detection to decode data. Using some passive components to tune the detector for the target frequency band, the received signal is amplified and passed almost directly to an A/D converter for downsampling and processing in the digital domain which, thanks to the low datarate, can be handled by low energy logic.

Because the receiver wakes up almost as soon as something happens, rather than wait for a time slot to roll around, the average response time is much better, providing greater energy savings over conventional radio systems if an application is latency sensitive. Event driven radio (see fig 2) may solve one of the problems that faces a number of the low power radio protocols.

A further question is that of network structure. Protocols such as Zigbee allow for a mesh structure – theoretically more robust and easier to manage than classical network designs such as stars and rings. The mesh structure puts more intelligence into the nodes themselves so they can find an effective route for a packet to reach its destination through an arbitrary mesh.

Zigbee uses a technique developed at the Nokia Research Centre, University of California, and the University of Cincinatti. Known as ad hoc on demand distance vector (AODV) routing, the approach only looks for a route between two nodes when one wants to send data to the other. A similar protocol has been proposed for 6LowPAN. These approaches are unlike IP networks, in which routing tables are predefined and updated at regular intervals using specialised route discovery packets.

With AODV, a node broadcasts a message asking for routes when it needs a connection (see fig 3). This results in a flood of responses. Nodes with a known route to the destination relay their proposed directions to the node that made the requested through the mesh until they reach the requester. The requesting node then picks the one with the lowest number of hops and caches it in order to avoid having to go through the same procedure for each packet it sends.

The AODV protocol is relatively simple, but can be problematic in terms of energy consumption because it demands responses from many nodes when setting up a route – and nodes have to listen constantly for those packets. The Zigbee group is working on a low power version of the network to allow use with energy harvesting nodes. These nodes will not be full members of the network, but will use other nodes as proxies for routing data into the network to avoid them having to participate in these activities.

Some groups are using wireless networking to develop more exotic forms of routing. For example, MyriaNed uses the idea of human gossip to disseminate data across a network. Nodes talk to their neighbours in the hope that the data will eventually find its way to the intended destination.

That networks such as MyriaNed are being developed show how far low power radio has to go in terms of development and standardisation.

While proprietary protocols are beginning to give way to more widely supported standards, it will take a long time before there is a clear winner – if that ever becomes the case.

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Creating a dynamic solution

Stretching the dynamic range of a/d converters.
By **Robert Fifield**.

Whether your application is focused on wireless communications or instrumentation, the performance bottleneck is often the dynamic range of the a/d converter.

Dynamic range is often a key parameter within signal processing systems and a shortfall can limit the quality and range of signals that can be received. The technical progress made on improving this gateway between the analogue and digital world has not kept pace with Moore's law because the challenges are more fundamental than simply reducing transistor sizes. Methods to increase a/d converter dynamic range are therefore always of interest, although each solution often suits particular applications.

As an example of pushing a/d converter dynamic range beyond what is currently available, the engineers at RFEL were confronted with an application where the customer required an a/d conversion process with a 74dB dynamic range at 800Msample/s. Most commercially available a/d converters capable of sampling at this rate typically offered a dynamic range of 52dB, equivalent to an effective number of bits – or ENOB – of 8.3. ENOB can be calculated as follows:

ENOB = (dynamic range – 1.76)/6.02

This left a shortfall in dynamic range of 22dB; something which had to be resolved in order for the project to be feasible.

Various techniques for extending dynamic range were considered, taking into account their advantages and disadvantages.

• *Increase the sample rate*. The quantisation noise floor of an a/d converter can be reduced by sampling at a higher rate and subsequently band limiting and decimating the output. This has the effect of filtering out-of-band noise sources and, in theory (assuming all noise is incoherent in nature), the dynamic range can be increased by 3dB for each doubling of sample rate. However, at higher sample frequencies, the gains are modest because the ENOB performance of high rate a/d converters also degrades. The cost of the a/d converter should also be considered as this usually increases with sample rate.

Fifield: "Dynamic range is often a key parameter within signal processing systems."

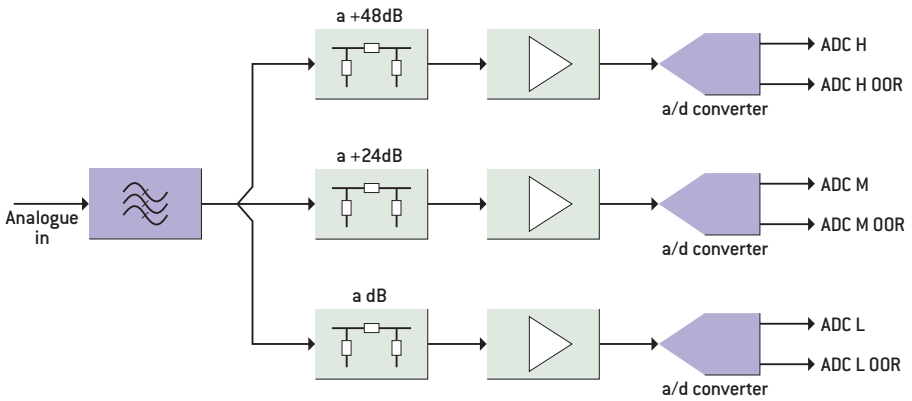
• *Interleaved a/d converters*. A more common solution is to use multiple lower rate a/d converters, which inherently have a better ENOB, to sample the input signal consecutively in an interleaved manner. The dynamic range gains are dependent upon the ENOB improvement of the lower rate converters, which tends to be more significant when targeting high sample rates. To retain any performance gains, careful consideration must be given to amplitude and phase matching between a/d converters. This can involve gain matching, PLL selection and attention to pcb layout. The input bandwidth of the lower rate a/d converters must, of course, be sufficient for the bandwidth of the signal of interest.

• *Non linear gain stage*. If the input signal is passed through a device with a non linear gain, the target dynamic range of the input signal can be mapped onto the available input range of the a/d converter. This effectively produces an a/d converter quantisation step size which increases with the amplitude of the input signal. A disadvantage of this technique is that the signal must be restored by subsequent signal processing, which often requires signal training to guarantee accuracy. Meanwhile, quantisation noise is dominated by the largest part of the signal.

• *Stacked a/d converters*. To make a significant improvement in dynamic range, a stacked a/d converter architecture can be used. In this approach, the signal is split into multiple paths, each with a different gain before input to the a/d converter. If, for example, three a/d converters are used, they would capture large, medium and small signals respectively and the final output would be selected from the most appropriate a/d converter. This approach has an obvious problem; although one signal can be tracked over a large dynamic range, the instantaneous dynamic range – the ability to receive large and small signals at the same time – is degraded. Another potential issue is that each path must be matched carefully to align phase, amplitude and frequency responses.

For the project, the 22dB increase in dynamic range could not be realistically achieved using the first two approaches. The third technique was feasible, but was rejected due to the large quantisation steps for large input signals and the

Fig 1: The stacked a/d converter configuration



overhead of signal training. Further analysis of the system requirements revealed the customer's monitoring application did not require a high instantaneous dynamic range, therefore the feasibility of fourth option was investigated further.

Achieving 74dB of dynamic range requires roughly 12 (74/6) bits. However, the minimum signal to noise ratio (snr) required by the system needs to be added; in this case, approximately 4bit. The total signal range is therefore roughly 16bit. Because phase and amplitude matching is important, identical a/d converters in a dual, triple or quad packaged device would be ideal.

The best option, having considered device cost and performance, was e2v's EV8AQ160, an 8bit quad packaged device. To meet the dynamic range and snr requirements, three of the four packaged a/d converters were used to cover the full 16bit range. The converters were allocated such that the most sensitive – ADC_Low – detected bits 1 to 8. ADC_Mid detected bits 4 to 12 and ADC_High handles bits 8 to 16 (see fig 1). This allows the full 16bit range to be covered, meeting the dynamic range requirement and providing a 4bit overlap to satisfy the snr requirement.

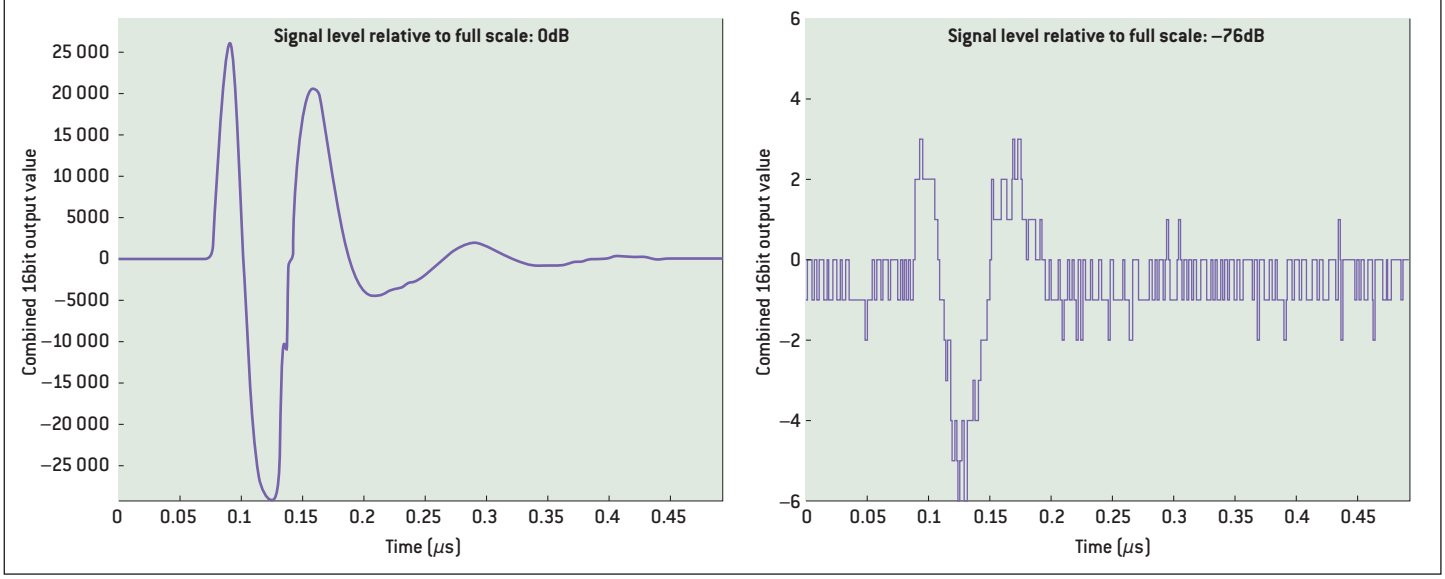
The design and layout of the analogue input network is another potential minefield; particularly because the input signal is split into three different gain paths (see fig 1). To maintain consistent amplitude, phase and frequency response, each path contains an identical active gain stage preceded by a passive attenuator of 0dB, 24dB and 48dB for the high (bits 1 to 8), medium (bits 4 to 12) and low (bits 8 to 16) gain paths respectively. Linear power regulators were used to reduce noise and the high gain signal path was positioned away from other potential sources of noise.

The analogue and digital components were designed, simulated and fabricated onto a 14 layer pcb, allowing multiple bgas to be routed within a small area. The design was tested over the complete signal range under various environmental and emc conditions to ensure robust operation. Figure 2 shows the combined 16bit output for an input signal at full scale (low gain path active) and after it has been attenuated by 76dB (high gain path active). The pulse shape can clearly be observed in both figures. The second figure shows the efforts to mitigate noise have paid off as the system can operate successfully close to the device's quantisation noise floor.

This article has focused upon extending the dynamic range of the a/d conversion process. In the final product, this was the first enabling step before useful information within the input signals could be extracted through digital signal processing. The processing was carried out within multiple high speed fpgas before results were sent out over a network connection.

Author profile:
Robert Fifield is senior digital systems design engineer with RFEL.

Fig 2: Performance at full scale and full scale – 76dB



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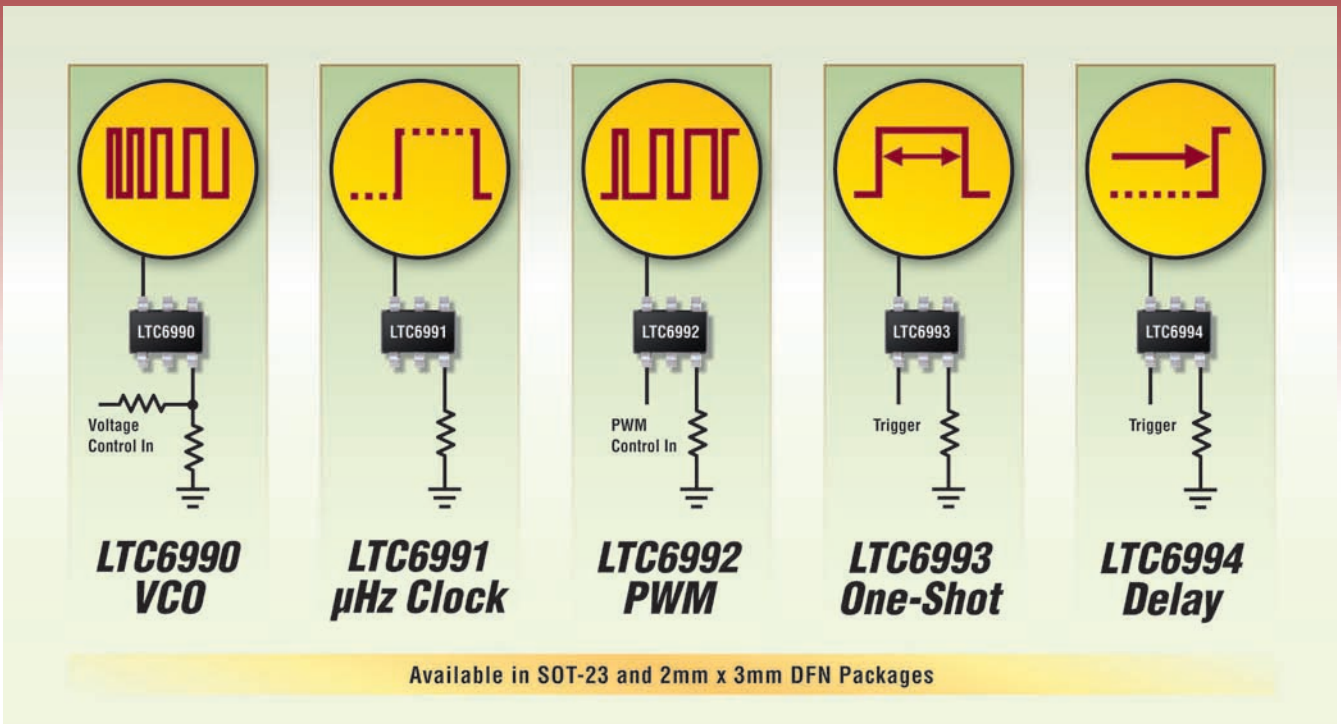

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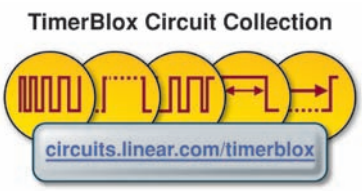
LTC6992-1	PWM	0% to 100% Pulse Width Control	3.8Hz to 1MHz
LTC6992-2		5% to 95% Pulse Width Control	3.8Hz to 1MHz
LTC6992-3		0% to 95% Pulse Width Control	3.8Hz to 1MHz
LTC6992-4		5% to 100% Pulse Width Control	3.8Hz to 1MHz
LTC6993-1	One-Shot	Rising Edge Trigger	1µs to 34s
LTC6993-2		Rising Edge Trigger, Retriggerable	1µs to 34s
LTC6993-3		Falling Edge Trigger	1µs to 34s
LTC6993-4		Falling Edge Trigger, Retriggerable	1µs to 34s
LTC6994-1	Delay	Rising or Falling Edge Trigger	1µs to 34s
LTC6994-2		Rising & Falling Edge Trigger	1µs to 34s

Info and Purchase



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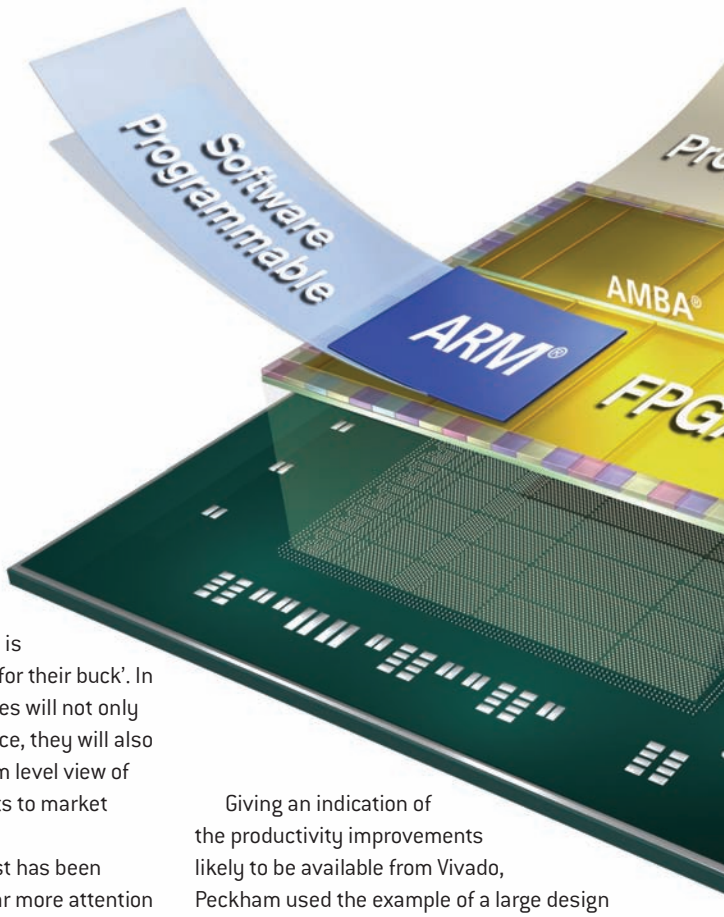
Small process, big ambitions

FPGA developers square off at 20nm. By **Graham Pitcher**.



Programmable logic is one of the first technologies to be manufactured on the latest process node. In the past, fpga developers have taken advantage of this to bring larger capacity devices to market as soon as possible in an effort to meet the needs of leading edge customers.

Until recently, the two market leaders – Altera and Xilinx – tended to compete on the basis of what customers could use. But lately the focus has moved to what customers might be able to use at some unspecified time in the future. And their battle is now centred on 20nm technology.

Altera made the first move in the campaign at the beginning of October 2012, outlining what its customers might see at 20nm. A number of claims were made by Brad Howe, senior vp for R&D. Amongst them were a 60% reduction in power consumption, greater transistor density and even higher speed transceivers. The devices will start to appear in 2014, Howe claimed.

"Our innovations at 20nm will allow us to deliver a highly efficient, highly flexible mixed system fabric that features optimal levels of dedicated circuitry with the latest 20nm fpga process technology," said Howe. "The result is a device that delivers the industry's highest levels of integration, performance and bandwidth at the lowest power."

Now, it's Xilinx' turn. Claiming it was first to ship 28nm devices, the company says it is keen to maintain what it calls a 'generation lead'. Giles Peckham, European marketing director, said: "[The 20nm strategy is] building on what Xilinx can offer at 28nm, where we announced a breakout strategy that moved programmable logic on towards all programmable logic, including SoCs and 3d ics."

Central to Xilinx' 20nm plans is offering developers 'more bang for their buck'. In Peckham's opinion, 20nm devices will not only offer the best power/performance, they will also allow engineers to take a system level view of their designs and to get products to market more quickly.

Whereas the focus in the past has been almost entirely on the silicon, far more attention is now being paid to the design tools. The subtext here suggests that if you don't have design tools that are up to the job, there's no way that you will be able to take advantage of 20nm technology.

"Designers need tools," Peckham asserted. And Xilinx' offering is Vivado, something which it believes will cut the design effort from months to weeks. "Already, all customers for the V2000T have used Vivado, as have 80% of high end designs," Peckham continued. "At the 20nm node, Vivado will be the foundation for design and the way to get the best out of the technology."

Tools bring IP centric design approach

One of the benefits claimed for Vivado is that it introduces an IP centric approach to high level design. "People looking to use 20nm technology will need to move to higher levels of abstraction," Peckham counselled. Vivado will also be capable of taking C/C++/SystemC code and converting it to hardware.

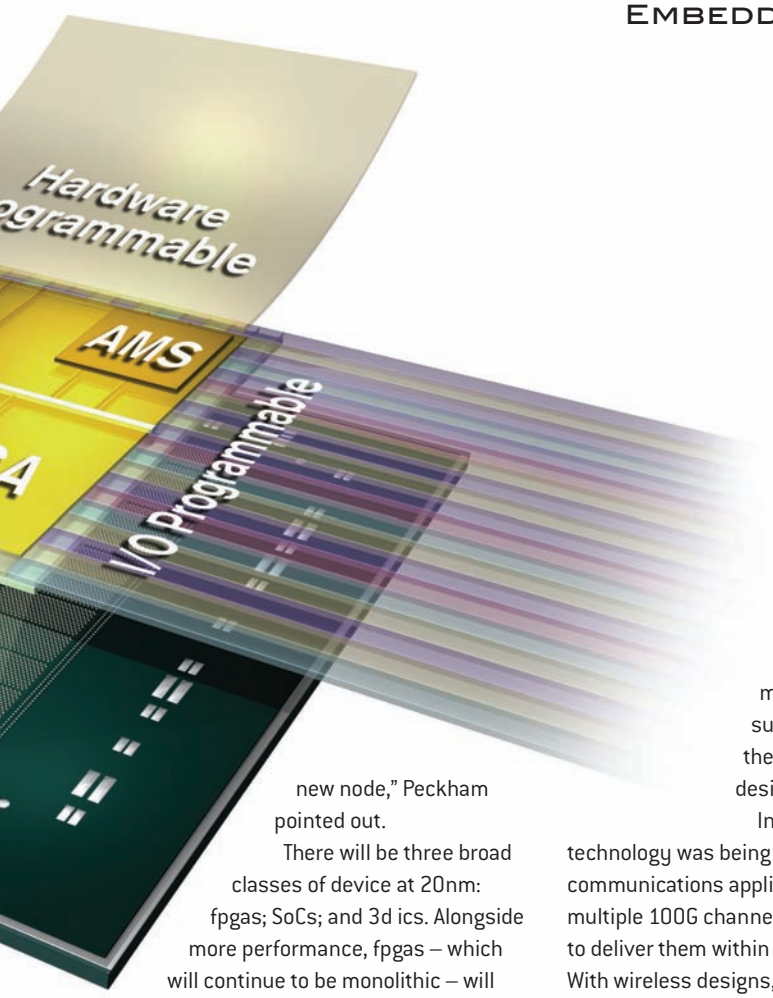
Vivado will also help designers deal with bugs. A common database approach supports cross processing, allowing designers to look back in time to see where issues originated. "It will be easier to solve problems at the rtl level, rather than at place and route," Peckham observed.

Giving an indication of the productivity improvements likely to be available from Vivado, Peckham used the example of a large design locked down, with no late changes and with reuse of design elements from a previous product. "Using older tools, two to three months to design is a reasonable estimate. Vivado will cut that to two to three weeks."

But it's the silicon that will do the work and, according to Peckham, the 20nm offerings will bring 'additional dimensions' compared to current devices. "Alongside programmable digital, there will be programmable analogue," he said, "and 3d ics will move to a multichip programming solution. All of this is intended to improve performance and power consumption at the system level, as well as to improve the Bill of Materials."

The 20nm node will see all devices made using one base process. "We developed one technology at 28nm in association with TSMC," said Peckham, "allowing us to hit a 'sweet spot'. While the HPLP process didn't offer the highest performance or the lowest power, we can tweak it to create a range of products."

Xilinx says it will use this process as a means of driving towards a higher level of system integration, but it is also developing a new metric – power/performance per Watt – to help customers understand the capability of new devices. "We are committed to a 30 to 50% increase in price/performance per Watt at each



At the 20nm node, second generation SoCs will feature heterogeneous multicore architectures, with optimised interfaces between the processor subsystem and the fpga fabric.

new node," Peckham pointed out.

There will be three broad classes of device at 20nm: fpgas; SoCs; and 3d ics. Alongside more performance, fpgas – which will continue to be monolithic – will have enhanced analogue and mixed signal capabilities. "Customers are looking for the ability to do 12bit conversions at 1Msample/s," Peckham said. "They also have higher expectations about IP, so we will be moving to the block subsystem level to help them complete larger designs."

In general, he said fpga technology was being driven by communications applications. "Designers want multiple 100G channels," he said, "and we have to deliver them within the same power budget. With wireless designs, customers are looking to balance power and performance while having access to more dsp functionality."

At the 20nm node, fpgas will feature 33G transceivers and the largest device planned will have more than 100 transceivers. System level performance is said to be doubled and, by tuning the architecture, Peckham said it would be possible to use more than 90% of the die without routing issues.

Meanwhile, at the process level, TSMC has managed to reduce the underlying power consumption, while Xilinx has 'tweaked' the transistors and logic cells, with the result that power consumption will be halved.

More capabilities will be available from second generation SoCs. These will move to heterogeneous multicore architectures, with optimised interfaces between the processor subsystem and the fpga fabric. "We will have the opportunity to double the number of logic cells," Peckham said, "unlike monolithic parts, where the shrink will only increase that figure by 50%."

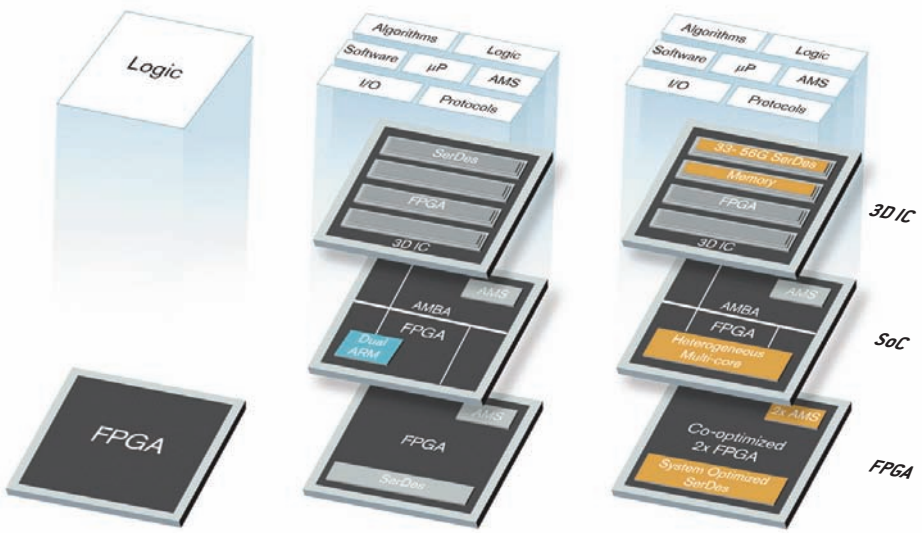
Applications driving SoC developments include imaging, video analytics, machine vision and broadcast.

Finally, 3d ics will support heterogeneous and homogeneous approaches, offering wider memory interfaces and higher level transceivers; potentially 56G. "Customers for these parts are looking for high performance and peak processing," said Peckham.

Interposer technology is critical to the 3d device and Xilinx will be offering two approaches: one supporting heterogeneous dice; the other for homogenous parts. Designs with up to 40m asic equivalent gates may be suited to these parts.

As to when the 20nm parts might be available, Peckham wasn't giving anything away. "We will be delivering fpgas as soon as TSMC finishes running test chips and so on." But he said Xilinx was already working with lead customers to help them develop next generation products.

Fig 1: The features likely to be available in Xilinx' devices at the 20nm node



Programmable logic devices
programmable logic

28nm technology
all programmable devices

20nm technology
all programmable devices

Keep the noise down

How noise cancellation techniques may boost data rates over copper. By **Roy Rubenstein**.

Using a dsp based technique called vectoring to cancel crosstalk, the performance of very high speed digital subscriber line 2 (VDSL2) technology can be pushed close to its theoretical limit.

Several broadband access equipment vendors have recently detailed vectoring solutions, including Adtran, Alcatel-Lucent and ZTE. Alcatel-Lucent has trialled its technology with more than 24 telecom operators and believes at least six will deploy it.

Vectoring is being welcomed by operators as it enables them to increase broadband rates using their existing copper infrastructure. Even if operators are transitioning to fibre based access networks, these require significant investment and years to roll out. Vectoring provides a parallel approach to achieve very high speed broadband.

Using vectoring, VDSL2 data rates can be boosted to some 100Mbit/s downstream and 40Mbit/s upstream over a 400m link. This compares to 50Mbit/s and 20Mbit/s, respectively, using VDSL2 alone. There is also a large uncertainty in the resulting bit rate for a given loop length but, with vectoring, this uncertainty is removed almost entirely.

Typically, a cable bundle can comprise several hundred telephone copper pairs and crosstalk means the signal in one copper pair leaks into neighbouring ones.

"All my neighbours get a little bit of the signal sent on my pair, and vice versa," said Paul Spruyt, xDSL technology strategist at Alcatel-Lucent. "The signal I receive is not only the useful signal, but also noise contributed from my active VDSL2 neighbours The resulting signal to noise ratio on each pair dictates the overall achievable data rate to the user and, on short loops, crosstalk is the main noise culprit."

To tackle noise, the crosstalk coupling into each VDSL2 line is measured and used to generate an anti noise signal at the digital subscriber line access multiplexer (dslam) equipment to null the crosstalk on each VDSL2 line (see fig 1).

To calculate the crosstalk coupling between the pairs in the cable bundle, use is made of the 'sync' symbol, sent after every 256 data symbols. This equates to a sync symbol being sent every 64ms.

Each sync symbol is modulated with one bit of a pilot sequence. The length of the pilot sequence is dependent on the number of VDSL2 lines in the vectoring group: in a system with 192 VDSL2 lines, 256bit long pilot sequences are used (the next highest power of two).

Moreover, each twisted pair is assigned a unique pilot sequence, with the pilots usually chosen such that they are mutually orthogonal. "If you take two orthogonal pilot sequences, multiply them bit wise and take the average, you always find zero," said Spruyt. "This characteristic speeds and simplifies crosstalk estimation."

The user's DSL modem expects to see the modulated sync symbol but, in reality, sees a modulated sync symbol distorted with crosstalk from the modulated sync symbols transmitted on the neighbouring lines.

The modem measures the error – the crosstalk – and sends it back to the dslam (see fig 2). The dslam correlates the received error values on the 'victim' line with the pilot sequences transmitted on all other 'disturber' lines. By doing this, the dslam gets a measure of the crosstalk coupling for every disturber-victim pair.

The final step is the generation of anti noise within the dslam. This anti noise is injected into

Fig 1: VDSL2 vectoring basics

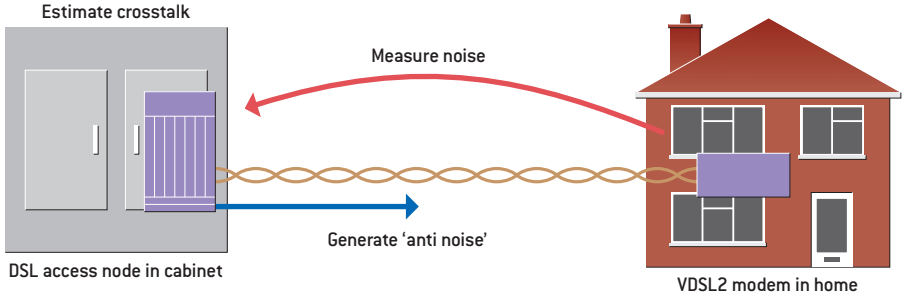
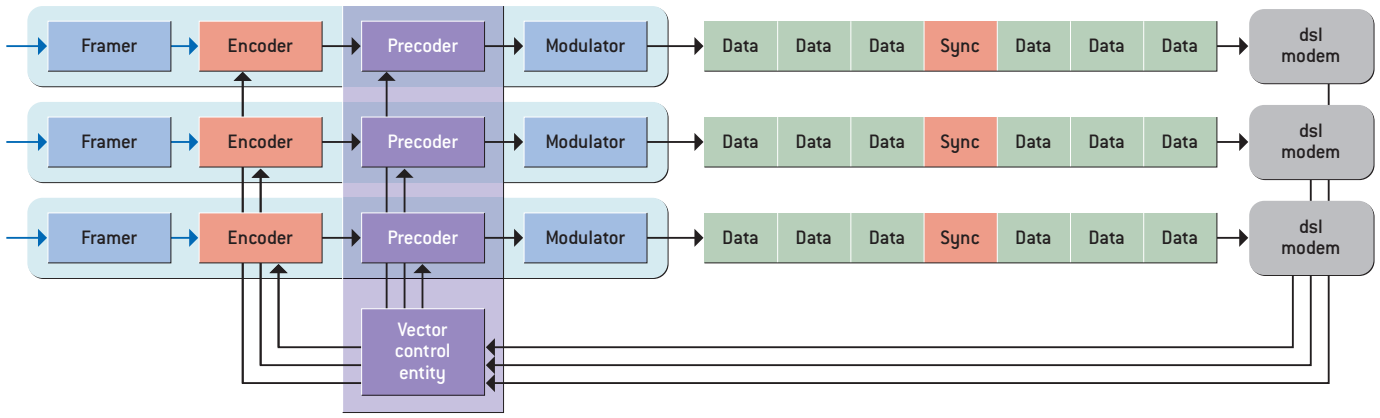


Fig 2: How VDSL vectoring is performed



the victim line on top of the transmit signal such that it cancels the crosstalk signal picked up over the telephone pair. This process is repeated for each line.

VDSL2 uses discrete multitone (DMT) modulation, where each DMT symbol consists of 4096 tones, split between the upstream and the downstream transmissions. All tones are processed independently in the frequency domain. The resulting frequency domain signal, including the anti noise, is converted back to the time domain using an inverse fast Fourier transform.

It is only recently that advances in silicon have enabled the processing performance needed for vectoring. A fully vectored 200 line VDSL2 system needs a processing ability of some 2.6TMAC/s; one with 400 lines would require four times as much processing power – about 10TMAC/s.

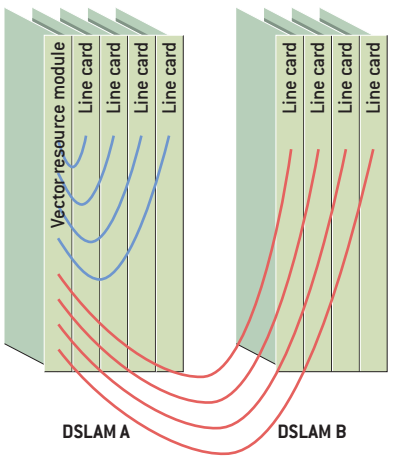
Typically, a VDSL2 line card has 48 ports and performing vectoring on one card – board level vectoring – is relatively straightforward. "It gets more challenging with system level vectoring [across boards and even platforms] and you need significantly more processing horsepower to get to 192 or even 384 ports," said Robert Conger, Adtran's director of product management (see fig 3).

Conger says that what is still missing is the general availability of mass market vectoring asics from merchant VDSL2 chip vendors: companies such as Broadcom, Ikanos Communications and Lantic. Certain chip vendors allow system vendors to use their own vectoring processor while they are also developing their own silicon, said Conger.

System vendors that have already demonstrated vectoring are either using fpgas or their own in house asic. "FPGAs are great for field evaluations, but the difference between fpgas and asics is that the the fpgas consume a lot more power and are not as cost effective," said Conger. "Operators are very conscious of power – if they can wait for the power efficient asic, they prefer that." Most VDSL2 chipset vendors will come to market with their own silicon next year.

Alcatel-Lucent implements its own vector processor, but will not detail its hardware design. What the company has said is that its first generation vectoring system, released in 2011, could process 192 lines. At the Broadband World Forum in October 2012, Alcatel-Lucent unveiled a second-generation system that doubles the capacity to 384 lines.

Fig 3: Multisystem vectoring with one VRM



Adtran can demonstrate system level vectoring now using fpgas, but there will be a further iteration once the asics become available in 2013.

There are other hardware challenges: there is a large amount of data to be transferred within the dslam associated with vectoring. According to Alcatel-Lucent, a 48port VDSL2 card can generate up to 20Gbit/s of vectoring data.

A further practical challenge that operators face when upgrading to vectoring is that not all the users' VDSL2 modems deployed may support vectoring.

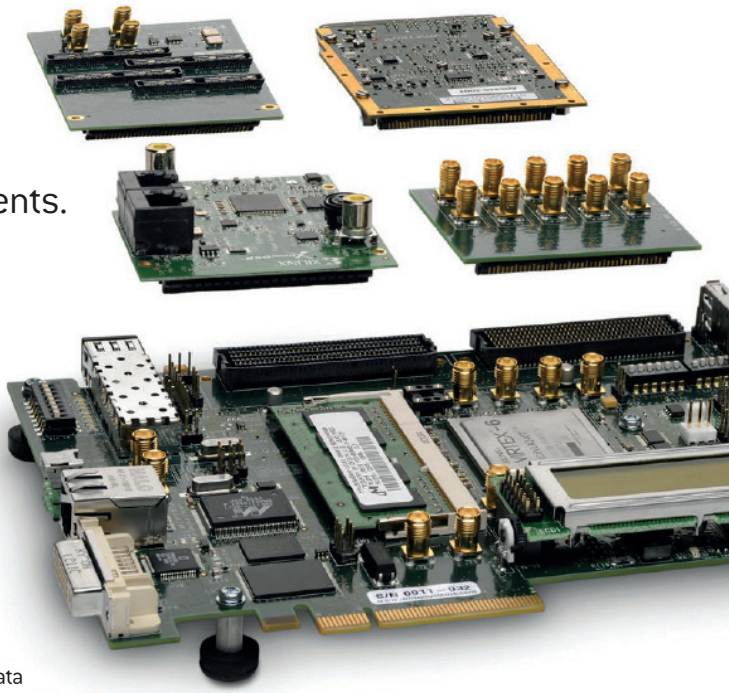
"To get maximum benefit, you need to remove all the noise," says Stefaan Vanhastel, marketing director for wireline fixed access at Alcatel-Lucent. "That means you have to be able to measure and cancel the crosstalk from each line in the bundle, even the ones that are on VDSL2."

To tackle this, certain legacy VDSL2 modems can be software upgraded to support vectoring. Those that can't be upgraded to vectoring can be software upgraded to a 'vector friendly' mode. Crosstalk from such a vector friendly line into neighbouring vectored lines can be cancelled, but the 'friendly' line itself does not benefit from the vectoring gain.

But even firmware upgrading is a considerable undertaking, especially when it involves tens or hundreds of thousands of modems. However, not all equipment can be upgraded, even to a friendly mode. To this end, Alcatel-Lucent has developed a 'zero touch' approach that allows crosstalk from legacy VDSL2 lines into vectored lines to be cancelled without equipment upgrade. "This significantly facilitates and speeds up the rollout of vectoring," Spruyt concluded.

It's in the cards

Mezzanine cards cope with changing I/O requirements. By **Malachy Devlin**.



Front panel I/O functionality has typically been fixed on 3U and 6U form factor cards and changing this functionality meant redesigning the cards – which can be an expensive undertaking. While the advent of PMC and XMC modules has allowed configurable front panel I/O, these modules use much of the 3U and 6U carrier card area.

More I/O flexibility is being provided through the FPGA Mezzanine Card – or FMC – specification, as defined in VITA 57. Connecting to an fpga or any other device with reconfigurable I/O, FMC modules can be used on a range of popular board formats, including VME, VPX, CompactPCI, AdvancedTCA and MicroTCA.

The FMC standard, which is fpga architecture independent, is designed to:

- Maximise data throughput
- Minimise latency
- Reduce fpga design complexity
- Minimise system cost, and
- Reduce system overhead, including power consumption and cooling needs.

VITA 57 introduces an electromechanical standard that creates a low overhead bridge between front panel I/O on the mezzanine module and an fpga on the board carrying that module.

Essentially, FMC removes the need to inject protocol data into the raw data to be processed, something which happens with a defined bus interface. By assuming the fpga has a relationship with the I/O mezzanine module, the FMC standard can capitalise on the ability of fpgas to process raw data formats. Rather than defining pin functionality, the FMC specification simply defines the upper limit of connections for both parallel lines and multigigabit serial signals.

The FMC specification has two defined module sizes – single and double width. The single width module is 69mm wide, while the double width module is 139mm wide. Both are 76.5mm deep. The FMC standard specifies a 400 pin high speed array connector, but a mechanically compatible connector with 160 pins can also be used.

FMC modules can handle up to 80 differential signal pairs with a signalling speed of 2Gbit/s. However, up to 20 differential pair signals can be connected to 10 multigigabit transceivers running at up to 10Gbit/s. Together, they deliver a bandwidth of more than 40Gbyte/s.

"FMC has rapidly become the de facto standard for daughtercards in the fpga industry," said Raj Seelam, senior marketing manager, Platform Solutions, with Xilinx. "The FMC standard reduces design costs and time to market by bringing the benefits of modular design much closer to the fpga user community."

Dave Lautzenheiser, from Faster Technology, noted: "With all the standards out there, FMC makes it a lot easier for the system designer to build something, becoming a component choice at the board subsystem level. They can then focus on the application."

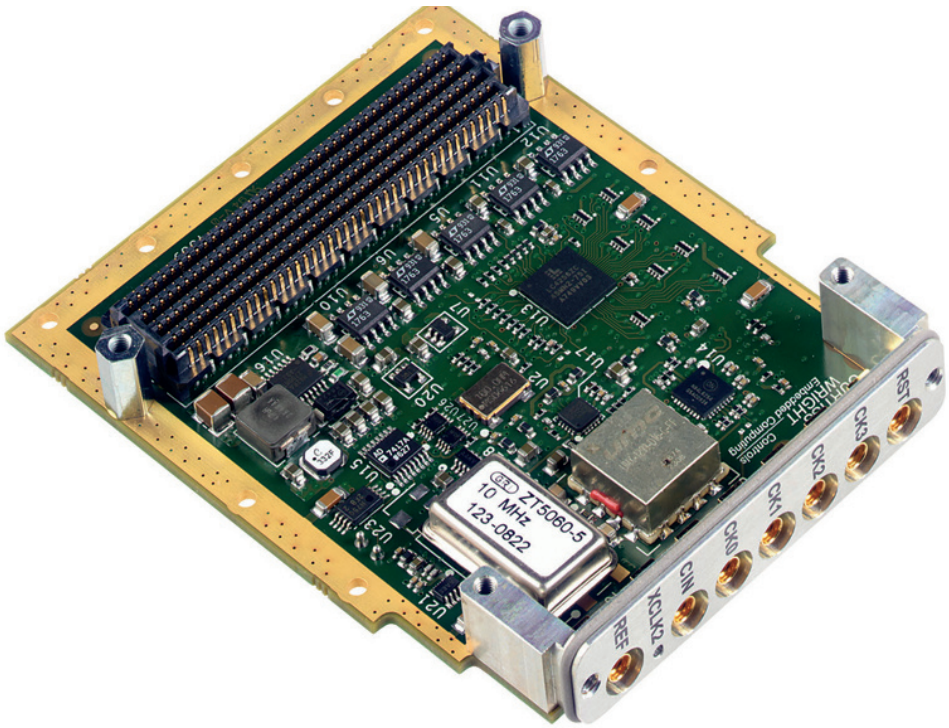
FMCs are most commonly used in applications that need low latency I/O. Getting the high speed data to fpga quickly for processing and then turning it around as output without the need to transfer around the buses in a system has great advantages.

"The speed and number of connections that an FMC format module uses, together with direct fpga-to-I/O devices, means the FMC format is particularly suited to applications benefitting from multi gigabyte per second I/O with low latency," said Jeremy Banks from Curtiss-Wright Controls Defense Solutions.

There are complementary specifications to ANSI/VITA 57.1. For example, VITA 57.2 defines an 'electronic datasheet' metadata standard to provide automated validation of FMC configurations and performance capability. In short, VITA 57.2 helps users to determine the compatibility of FMC products from different vendors before products are purchased. It also allows pin description files to be created automatically, which can then be loaded in fpga design tools.

(left) FMC carrier card and multiple FMC mezzanine card options from Xilinx

(right) The FMC-XCLK2, from Curtiss-Wright Defense Solutions, is a high frequency clock generator module in FMC format that can provide up to four synchronised sample clocks for high speed I/O products



Meanwhile, VITA 57.3 defines logic interfaces for the firmware that resides in the carrier card fpga that communicates with the FMC module. Effectively, this acts as a 'device driver' layer.

While FMCs can ease the pain of system development, using them is not without challenge. "Many system designers will ask which carriers to use with a specific FMC," said Lautzenheiser. "They want a level of assurance that they can get past the integration issues quickly, getting onto the challenge of working on their application software."

Seelam agrees that compatibility is the biggest challenge. "With so much flexibility, there is an inherent increase in risk factor: is this going to work with this or that card?"

Lautzenheiser feels there is something missing at the application level. "Is there a way to define clearly and consistently what the carrier can support?," he asked. He says he is looking for something that would package and deliver a known reference point, but doesn't know exactly how that might be done. While the physical level is covered in the work of the VITA 57.2 committee, he believes 'something above that' is missing.

One way of seeing how various devices interoperate is through PlugFests. FMC PlugFest 2012, held in August in California, gave developers the opportunity to find out just how compatible their parts were. The event was also the first outing for FMC Check, a set of tools intended to help system developers, integrators and module designers to validate FMC module and carrier designs and their interoperability. At the PlugFest, a combination of 23 FMC modules and 13 fpga based boards were used to test a range of applications.

PlugFest proves interoperability

Altera, one of the more recent companies to join the FMC Marketing Alliance, took part in the PlugFest. Charles Pryor, manager of the company's high speed board group, said: "Our first two FMC carrier cards passed 100% of all electrical testing with three modules from Faster Technology. Altera looks forward to broadening its FMC testing with more module vendors, both using the VITA57.2 FMC Check tool, as well as full electrical testing."

Although FMCs are supporting the demands of current generations of fpgas in terms of I/O and power, it is important that the specification is developed. For example, companies such as National Semiconductor that launched 1GHz digitisers are now sampling parts running at 5GHz and even 10GHz. While the current revision of VITA 57 can handle these data rates, the standard will need to look forward continually in order to match the increasing capabilities of fpgas and external I/O interfaces.

Marc Couture, Mercury Computer Systems' director of product management, microwave and digital solutions, believes that, in the future, there will be an FMC 2.0, with more pins and/or with pins that can sustain higher digital bandwidths. "FMC 2.0, I believe, will need to be faster and wider in terms of the bandwidth that can be sent from the mezzanine card to the baseboard," he said.

Curtiss Wright's Banks added: "More serial paths will need to be defined, either through a more dense connector or by redeploying parallel lines to serial."

However, a different approach is being pursued by French company Techway. "Stacking multiple FMCs to gain more front panel space or creating an extended pcb with FMC connectors, making a wider FMC, is something that Techway is exploring," said Patrick Mechan. While this does not impact the electrical specification, it does offer a creative way of getting more I/O into the system.

Author profile:
Malachy Devlin is chairman of the FMC Marketing Alliance. For more information, go to: **www.vita.com/fmc**

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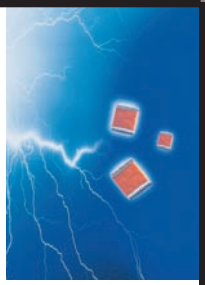

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New Gecko™ connectors save space; deliver high performance at commercial price levels

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New Zero Insertion Force Quad Lock Connector for diagnostic and imaging medical equipment from ITT Cannon

Miniature ZIF QLC - smaller and lighter than traditional DL connectors with enhanced robustness and functionality

The leading global connector manufacturer and supplier ITT Cannon has recently released a new Zero Insertion Force (ZIF) Quad Lock Connector (QLC) for use in medical imaging and diagnostic equipment. The device is an industry first which achieves a reduction in interconnect packaging whilst accommodating robust performance requirements and functional enhancements such as press-fit. Reducing the spacing from the standard DL line to 0.8mm made it possible for ITT ICS' engineers to design the ZIF QLC portable connector system with a full 260 pin configuration and a reduced package size - it is up to 65% smaller than existing DL products and competitive QLC products currently on the market. This enables customers to achieve a drastic reduction in the overall size of diagnostic equipment.

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TTI, Inc. adds innovative new 1W DC-DC converter from Murata Power Solutions

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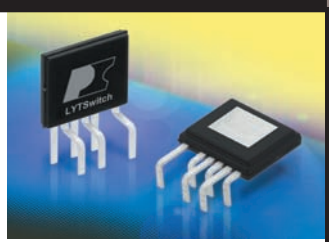
Power Integrations' LYTSwitch LED-Driver ICs improve performance of commercial lighting and deliver excellent dimming for consumer bulb applications



New IC family delivers fast start-up with no pop-on, no dead travel

Power Integrations (Nasdaq: POWI), the leader in high-efficiency, high-reliability LED driver ICs, today introduced its latest family of LED-driver ICs, aimed at consumer, commercial and industrial lighting applications. The new LYTSwitch™ IC family delivers tight regulation and high efficiency for tube replacements and high-bay lighting, while providing exceptional performance in TRIAC-dimmable bulb applications.

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Thermal Imaging Cameras

www.reichelt.com

Preventive Maintenance instead of Waiting

reichelt elektronik uses FLIR thermal imaging cameras for the preventive maintenance

Anyone who just like the electronics specialist reichelt ships more than 7,000 deliveries from its warehouse on a daily basis, cannot afford delays or system failures in its logistics. In order to detect technical problems already in their initial stages, reichelt uses a FLIR thermal imaging camera of the type i3 from its own product portfolio to carry out the preventive maintenance. Instead of waiting until a problems occur and only then trying to find the fault and remedy it, reichelt decided on an proactive, preventive maintenance strategy. All electric installations are inspected every three months.

@: info@reichelt.de
✆: +49 (0) 4422 955-333

Voltage Regulator

www.a-powerusa.com

New accurate efficient linear voltage regulator from Advanced Power Electronics Corp

APU1205-3 suits handheld battery-powered equipment

Advanced Power Electronics Corp. (USA), a leading manufacturer of MOS power semiconductors for DC-DC power conversion applications, has announced an efficient linear voltage regulator with better than 2% initial voltage accuracy. The APU1205-3 family features a very low drop-out voltage and very low ground current and is targeted at handheld battery powered applications. Stable with a simple low cost ceramic capacitors, the APU1205-3 has a dropout voltage of only 270mV at 300mA or 170mV at 150mA. Quiescent current at shutdown is 5μA. It also features TTL-compatible enable/shutdown control input, current limiting and thermal shutdown. The APU1205-3 is available in fixed and adjustable output voltage versions in a small SMT 5 pin SOT-23 package.

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