FPGAs and DSPs Make a Complete Signal Processing Solution

The best solution for military signal processing applications is a hybrid architecture that takes advantage of the strengths of both FPGAs and DSPs.

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In technical publications over the past year, the question of whether FPGAs will replace DSPs in various applications, including signal processing, has been posed ad nauseam. Although this may be an interesting topic of discussion, the truth remains that DSPs and FPGAs are, in fact, very different technologies with different strengths and weaknesses. FPGAs can be very good at solving well-defined, high-speed, repetitive problems. DSPs are better at implementing highly complex algorithms as well as applications that involve some sort of decision-making, adaptive processing or algorithms that may change frequently.

Real-world, embedded military signal processing applications often require both of these types of processing and would benefit from having access to both technologies. Therefore, the optimal solution for a general-purpose signal processing board should include both FPGAs and DSPs, thus creating the need for developing hybrid signal processing architectures that leverage the strengths of both.

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Issues to Overcome in Hybrid Architectures

Although hybrid architectures are simple in concept, i.e., integrating DSPs and FPGAs onto one board, significant issues must be addressed for the final architecture to be effective. The crux of the problem is how to best handle data flow both between the FPGA and DSP compute elements, and to and from the hybrid architecture through real-world data interfaces. Another noteworthy complication is how to best enable the host access to the compute elements for command and control.

One of the biggest challenges faced when designing a hybrid architecture, i.e., the one that most directly impacts signal processing performance, is how to handle the communication between the FPGA and DSP compute elements. Of course, these interfaces must be tightly coupled, have low latency and be deterministic.

Less obvious is the fact that, in most scenarios, the communication speed between the DSP and the FPGA must be significantly faster than the board's I/O bandwidth since it is possible that the data will need to move from DSP to FPGA several times before signal processing is complete.

On BittWare's GT-3U-cPCI Hybrid Signal Processing board (GT3U), all data enters the board through the FPGA I/O interface (Figure 1). Once the data has entered the FPGA, the option exists to provide pre-processing before sending it along to the DSP(s) via dedicated communication link ports.

At this point, depending on the pre-processing algorithm being used, the data rate may decrease, remain the same or increase slightly. The transfer rate between the FPGA and DSP(s) must, then, at minimum, equal the I/O data rate. More optimally, that transfer rate must be many times faster that of the I/O. Each link port provides 500 Mbytes/s bi-directionally for a total of 8 Gbytes/s of data transfer between the DSPs and the FPGA.

Given the advantages of using the FPGA for straightforward, repetitive processing, it makes sense to have all onboard I/O enter through the FPGA. In addition to providing powerful front-end processing, system designers also gain the ability to support a wide variety of data transfer mechanisms and protocols. Many newer board formats that support high-speed serial interfaces (SerDes) can benefit greatly from this architecture, since the FPGA can implement several different protocols. The I/O flexibility provided by the FPGA has become increasingly important as the days of one or two dominant I/O standards has faded.

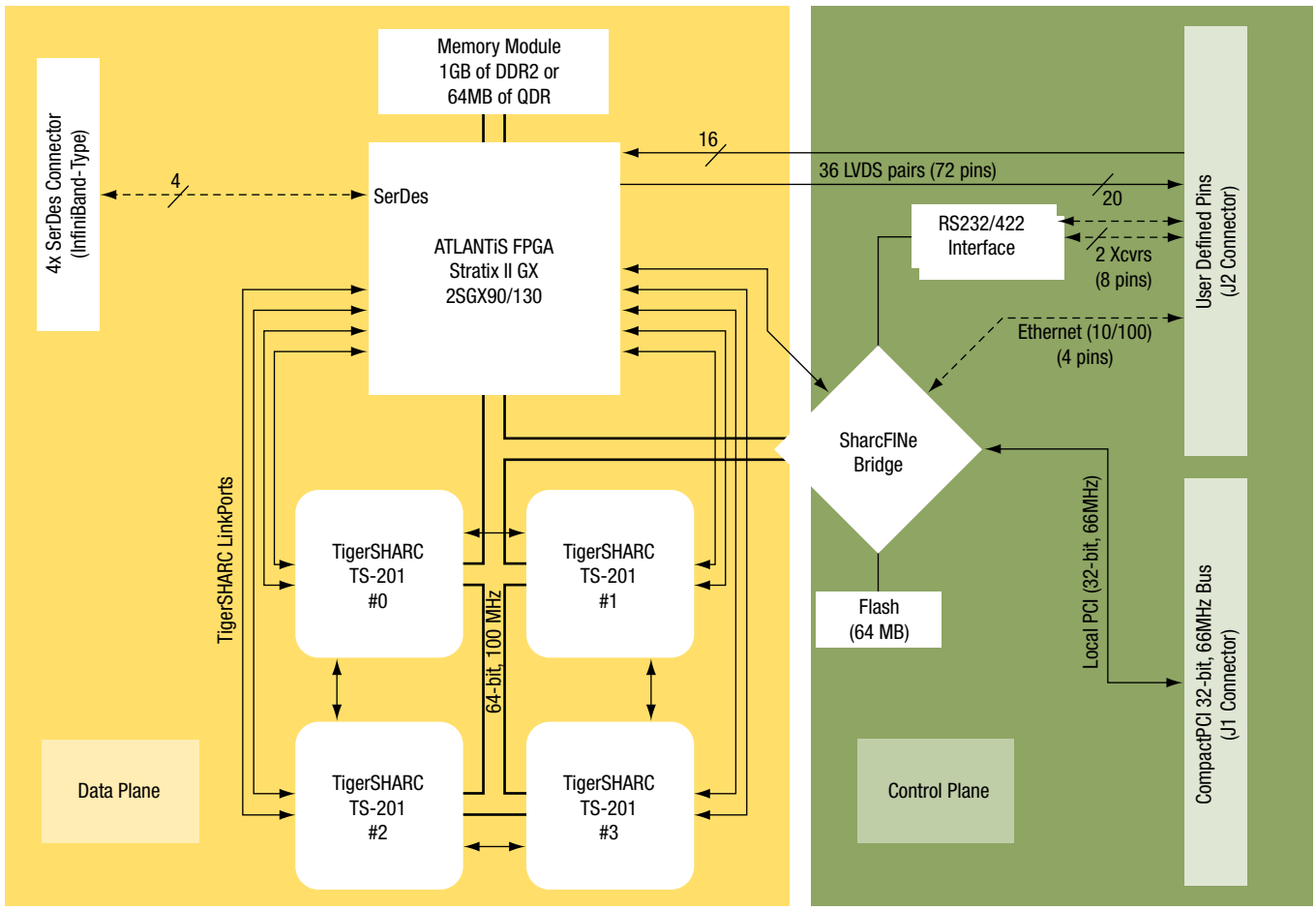

Figure 1

Hybrid signal processing block diagram details communication paths between the FPGA and DSPs.

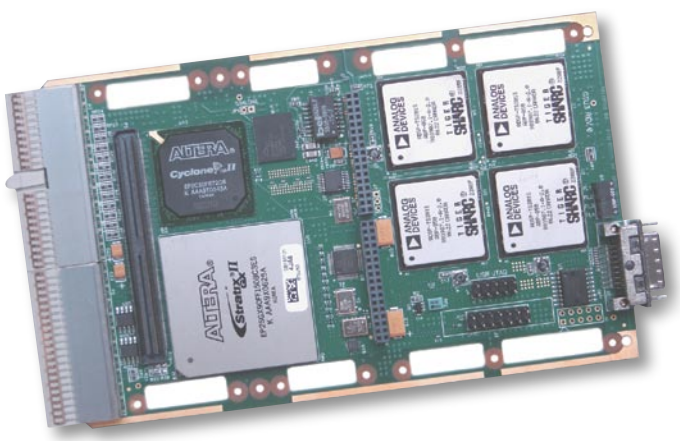

Figure 2

A ruggedized 3U CompactPCI hybrid signal processing board, designed for demanding multiprocessor-based applications requiring complete flexibility and adaptability, combines both a high-density FPGA and a DSP processing cluster.

Another challenge for a hybrid architecture is how to seamlessly integrate the diverse compute elements into a system. This is primarily a requirement for host interface and control mechanisms that connect the hybrid compute resources to standard host interfaces. In most systems today, this is done via PCI and/or Ethernet.

An optimal solution is to route all host communication through a separate control plane, orthogonal to the data flow. In the GT3U, this is handled by the SharcFINe host bridge, implemented in an Altera Cyclone II. This bridge connects the PCI bus to an onboard command and control bus that extends to each onboard FPGA and DSP. Since the control bus is independent of the data link ports, it allows the host to directly access and control each onboard compute resource without impacting data flow.

Using a Hybrid Architecture

Although the DSPs might do much of the heavy lifting in regard to signal processing, the FPGA is responsible for handling all transfer of data on and off the board, and between itself and the DSP(s), while also providing user-defined pre-, co- or post-processing. Developing the application processing IP is challenging. Integrating it into an FPGA in a hybrid architecture with fixed pinouts and external interfaces is even harder.

An FPGA framework that can facilitate this is required, one that also supports software-controlled data routing between all modules within the FPGA and enables the user to easily insert processing modules at any point in the data flow. With an FPGA framework such as this in place, the command and control bus can configure the data flows for a given application among the I/O interfaces, IP processing modules and DSP(s).

The ATLANTiS architecture, implemented in each onboard FPGA on the GT3U, provides such a framework, thus enabling the DSP(s) to communicate with all other I/Os connected to the board in a point-to-point, multicast or broadcast fashion. The I/Os can be connected or disconnected from each other as requirements dictate without the need for recompiling or changing cables.

This architecture consists of all of the hardware interface modules along with one or more data switches that are connected to a configuration register controlled by the user via control software running on the DSPs or the host. The routing can be changed at any point by reprogramming the configuration registers. Since all I/Os connected to the board are input into the FPGA, and thus into the framework itself, standard and/or custom FPGA processing blocks can be easily inserted into the data flow at any point.

The Future in Hybrid Design

The brute force method of adding either more DSPs or more FPGAs to a single board slot has not only failed to keep up with the demands of real-world applications, but also limits military system designers to the strengths and weaknesses of a single technology. Signal processing vendors should be focused on providing their customers with hybrid signal processing boards that are architected to mitigate the weaknesses and risks of each technology. The GT3U (Figure 2) utilizes a hybrid signal processing architecture that features a high-gate count Altera Stratix II FPGA and four ADSP-TS201S TigerSHARC processors from Analog Devices, giving system designers the best of both worlds. ■

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