Wireless Basestation Design Using Reconfigurable AMCs

Kristen Zaffini, Marketing Manager, BittWare Inc.

Ron Huizen, VP of Technology, BittWare Inc.

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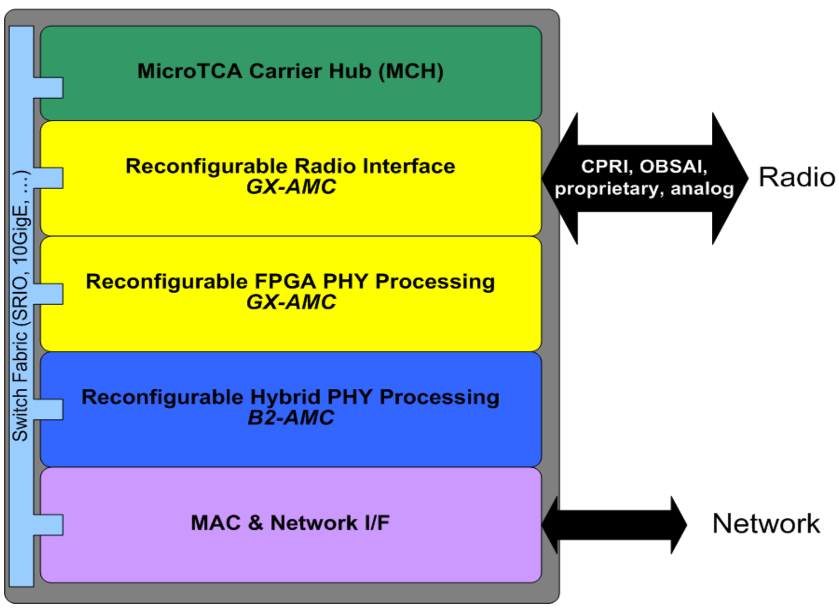
Wireless Basestation Architecture

A wireless basestation is a good example of how one reconfigurable AMC can be used to provide the many building blocks of a complex wireless system. The system architecture of a wireless basestation is comprised of four pieces. The radio interface provides an analog signal or digital Intermediate Frequency (IF) to the system. Next is the physical layer processing (PHY), which provides the baseband processing (and modem). The last two blocks in the system are data link layer processing (media access controller (MAC)), and the network interface. BittWare's GX-AMC is an FPGA-based AMC that can be used for both the radio interface and the physical layer processing. If a DSP is required, BittWare's hybrid signal processing AMC - the B2-AMC - can be used for the PHY processing. Both boards provide a reconfigurable interface that can be tailored to the required task.



Radio Interface

The radio interface is the interface between the radio and the physical layer processing. Analog IF requires A/D converters (ADCs) and Digital Down Converters (DDCs) for the receive path. On the transmit path, analog IF requires Digital Up Converters (DUC) and D/A converters (DACs). If the interface is digital IF, the requirements depend on the protocol being employed. For CPRI or OBSAI, SerDes transceivers - many times optical - are needed. If there is a proprietary protocol being employed, then the transceivers can be SerDes, LVDS, or DIO.

To enhance flexibility, a reconfigurable radio interface board can be used to bridge the radio to a switch fabric. BittWare's GX-AMC is one example of a reconfigurable radio interface. The Altera Stratix II GX-based board provides: front panel copper or optical SerDes supporting CPRI and OBSAI, a front panel I/O module for proprietary radios, an IF front panel module for analog radios, and two configurable 4x fat pipes on the AMC backplane - supporting Serial RapidIO and 10 GigE (among other standards).

Physical Layer Processing

The physical layer processing requires both DSPs and FPGAs to accomplish it's task - although industry opinion on the role that each should play differs. DSP vendors claim that most of the processing resources should be supplied by the DSP, with a small FPGA providing the Forward Error Correction (FEC). FPGA vendors, on the other hand, claim that FPGAs can provide most of the processing resources, with a DSP used for some bit level processing. The industry trend is to use both, with FPGAs adding signal processing resources, and DSPs adding dedicated processing blocks.

A reconfigurable AMC greatly increases the flexibility of the PHY processing. BittWare's GX-AMC provides an FPGA-based solution. The two configurable 4x fat pipes on the AMC backplane can support Serial RapidIO and 10GigE. A front panel module is available for additional processing, and the on-board DDR and QDR memory provides ample storage space.

BittWare's B2-AMC provides a hybrid solution with four TigerSHARC TS201 DSPs, an Altera Stratix II FPGA, and a configurable 4x fat pipe, supporting Serial RapidIO and 10GigE, on the AMC backplane.

Data Link & Network Interface

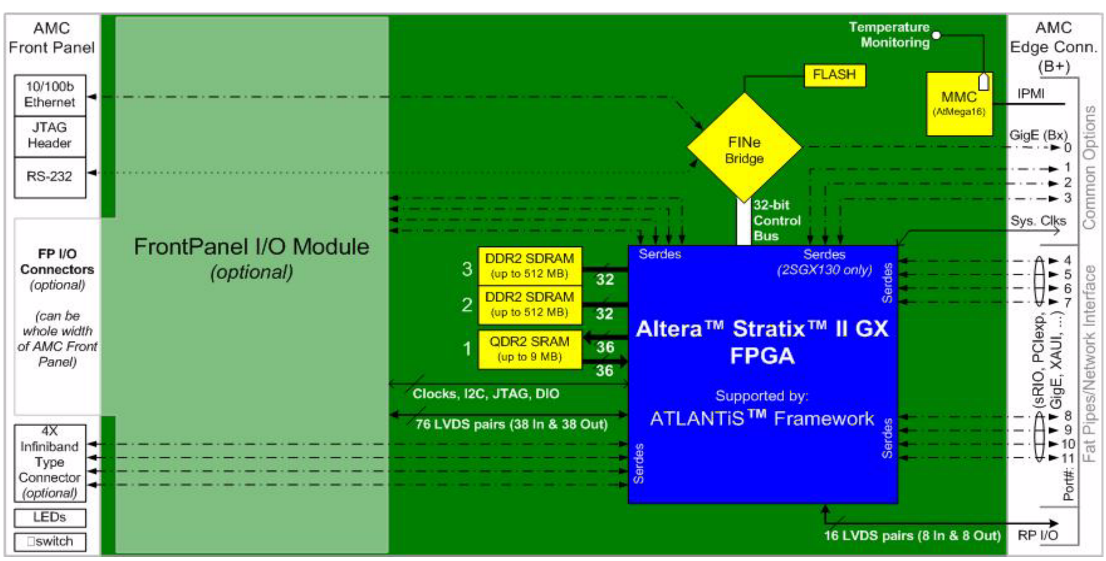
There are three required functions of the data link and network interface. There needs to be a MAC which can be implemented in a general purpose processor. The interface to the PHY must provide RapidIO, GigE, and 10GigE. The network interface must provide GigE or 10GigE, and, like the MAC, can also be implemented in the general purpose processor.

To enhance the system flexibility, a switch fabric can be used for the PHY interface, and the PHY processing board should provide reconfigurable fabric interfaces.

Reconfigurable FPGA-based AMC

BittWare's GX-AMC (GXAM) is an FPGA-based AMC that is in-system reconfigurable via a control plane interface to the host, providing a front panel module for adaptable I/O, and fully connected to all AMC clocks and ports.

Based on Altera's Stratix II GX FPGA, BittWare's GXAM is a mid-size, single wide AMC that can be used in MicroTCA systems and attached to AdvancedTCA (Advanced Telecom Compute Architecture) carriers or other cards equipped with AMC bays. The GXAM features a high-density Altera® Stratix® II GX FPGA, BittWare's ATLANTiS™ framework (implemented in the FPGA), a front panel I/O interface, a control plane interface via BittWare's FINe® interface bridge, an IPMI system management interface, and a configurable 11x SerDes interface supporting a variety of protocols, and rear panel I/O. It also provides 10/100 Ethernet, Gigabit Ethernet, two banks of DDR2 SDRAM,



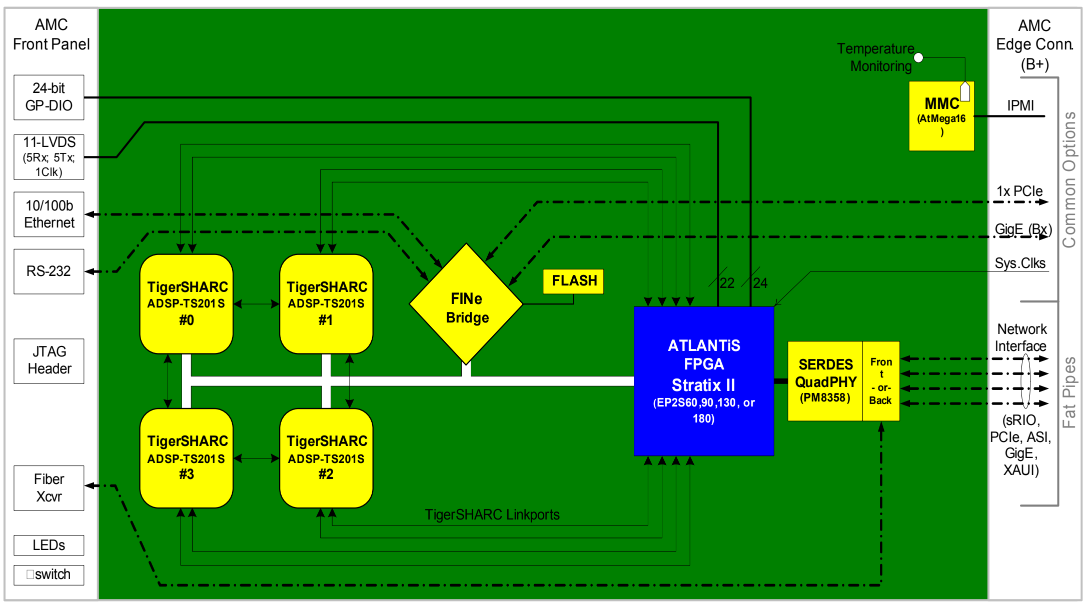
one bank of QDR2 SRAM, and Flash memory for booting the FPGA and FINe.

The state-of-the-art Altera Stratix II GX FPGA is at the heart of the GXAM and has been specifically designed for serial I/O-based applications providing up to 19 full-duplex high-performance, multi-gigabit transceivers supporting PCI Express, XAUI, Gigibit Ethernet, Serial RapidIO, and SerialLite II standards. The Stratix II GX contains up to 132,540 equivalent LEs, over 6.7 Mbits of RAM, 252 embedded 18x18 multipliers, 63 DSP blocks, and 8 PLLs. BittWare's ATLANTiS framework, which enables seamless routing of the I/O, is implemented in the FPGA.

BittWare's FINe Bridge provides Gigabit Ethernet on port 0 of the common options region. It also provides 10/100 Ethernet and RS-232 on the AMC front panel. The Stratix II GX provides four SerDes and 76 pairs of LVDS I/O to the BittWare front-panel I/O module, and 16 LVDS pairs (8 IN, 8 OUT) are provided for rear panel I/O via the AMC connector (ports 12 - 15, and 17 - 20). All AMC clocks are also connected to the Stratix II GX. The GXAM implements the standard Module Management Control Interface (IPMI).

Reconfigurable Hybrid AMC

Featuring a hybrid signal processing architecture that couples an Altera® Stratix® II FPGA with four



The Altera Stratix II GX FPGA facilitates all off-board I/O and provides communications routing and processing. Efficient routing is achieved using BittWare's ATLANTiS framework, which tightly integrates the I/O peripherals and the FPGA, and allows any combination of serial ports and off-board I/O interfaces to be routed together, providing nearly infinite options for configuring the I/O. The Stratix II GX interfaces to three SerDes ports (1, 2, & 3) in the AMC common options region, and eight SerDes ports in the AMC fat pipes (4 - 11). These 11 ports provide a network data and control switch fabric interface on the AMC connector, configurable to support PCI Express, Serial RapidIO, GigE, or XAUI.

ADSP-TS201S TigerSHARC® processors, BittWare's B2-AMC (B2AM) is an AdvancedMC that supports universal baseband processing for wireless communications infrastructure such as 2G, 2.5G, 3G, WiMAX and SDR. A full-height, single wide AMC, the B2AM attaches to AdvancedTCA (Advanced Telecom Compute Architecture) carriers or other cards equipped with AMC bays and is completely hot-swappable. The B2AM combines an Altera Stratix II FPGA, four TigerSHARCs, a variety of front and back panel I/O interfaces, and a configurable 4x network interface supporting a variety of protocols. It also provides a 10/100 Ethernet interface and a Gigabit Ethernet interface for command, control, and reprogramming, as well as Flash memory for booting the DSPs and FPGAs.

At the heart of the B2AM is a state-of-the-art Altera Stratix II FPGA containing up to: 179,400 equivalent LEs, 9.3 Mbits of RAM, 384 embedded 18x18 multipliers, 96 DSP blocks, and 12 PLLs. The FPGA provides pre-, post-, or co-processing to complement the TigerSHARC processing cluster, while also enabling seamless routing of the TigerSHARC I/O via BittWare's ATLANTiS™ framework.

The B2AM features a single cluster of four ADSP-TS201S TigerSHARC DSPs from Analog Devices, providing a total of 14.4 GFLOPS of floating point processing power and 57.5 GOPS of 16-bit fixed point processing power. In addition to 24 Mbits of on-chip RAM, each TigerSHARC also boasts four high-speed LVDS link ports. Each full-duplex link port is comprised of a 4-bit transmit and a 4-bit receive channel, and can support up to 500 MBytes/s in each direction for a total maximum throughput of 1 GByte/s. Two link ports from each DSP are used to create an interprocessor communications ring, and the remaining two link ports are routed to the on-board FPGA.

The Altera Stratix II FPGA facilitates off-board I/O and provides communications routing and processing. It implements eight TigerSHARC link ports and supports a variety of external I/O, flags, and interrupts. Efficient routing is achieved using BittWare's ATLANTiS architecture, which tightly integrates the DSPs with the I/O peripherals and the FPGA and allows any combination of link ports and off-board I/O interfaces to be routed together, providing nearly infinite options for configuring the I/O.

The Stratix II interfaces to four ports in the AMC fat pipes via PMC Sierra's QuadPHY SerDes. The four ports provide a network data and control switch fabric interface on the AMC connector, configurable to support PCI Express, Advanced Switching Interconnect (ASI), Serial RapidIO, GigE, or XAUI. Alternatively, a single SerDes port can be run via a front panel fiber transceiver.

BittWare's FINe Bridge provides Gigabit Ethernet via the common options region, or can be optionally configured for PCI Express. It also provides 10/100 Ethernet and RS- 232 on the AMC front panel.

The Stratix II provides 11 pairs of LVDS I/O (5 Rx, 1 Rx clk, 5 Tx) for proprietary antenna or network interfaces and 24 bits of general purpose digital I/O available on the AMC front panel.

Conclusion

Wireless basestation design is one example where the inherent flexibility of MicroTCA combined with a reconfigurable AMC creates a system that can easilty be upgraded or modified without having to change the actual system hardware. BittWare's FPGA-based and hybrid AMCs can be used as the building blocks for highly complex systems.