

Hardware

COLLABORATORS

	<i>TITLE :</i> Hardware		
<i>ACTION</i>	<i>NAME</i>	<i>DATE</i>	<i>SIGNATURE</i>
WRITTEN BY		July 23, 2024	

REVISION HISTORY

NUMBER	DATE	DESCRIPTION	NAME

Contents

1	Hardware	1
1.1	main	1

Chapter 1

Hardware

1.1 main

Table 1-1: Summary of Amiga Memory Configurations
Table 2-1: Interrupting the 680x0
Table 2-2: Copper Instruction Summary
Table 3-1: Colors in a Single Playfield
Table 3-2: Portion of the Color Table
Table 3-3: Contents of the Color Registers
Table 3-4: Sample Color Register Contents
Table 3-5: Setting the Number of Bitplanes
Table 3-6: Lines in a Normal Playfield
Table 3-7: Playfield Memory Requirements, NTSC
Table 3-8: Playfield Memory Requirements, PAL
Table 3-9: DIWSTRT and DIWSTOP Summary
Table 3-10: Playfield 1 Color Registers -- Low resolution Mode
Table 3-11: Playfield 2 Color Registers -- Low resolution Mode
Table 3-12: Playfields 1 and 2 Color Registers -- High resolution Mode
Table 3-13: Maximum Allowable Vertical Screen Video
Table 3-14: Maximum Allowable Horizontal Screen Video
Table 3-15: Color Register Contents
Table 3-16: Some Register Values and Resulting Colors
Table 3-17: Low resolution Color Selection
Table 3-18: High resolution Color Selection
Table 3-19: Color Selection in Hold-and-modify Mode
Table 4-1: Sprite Data Structure
Table 4-2: Sprite Color Registers
Table 4-3: Color Registers for Sprite Pairs
Table 4-4: Data Words for First Line of Spaceship Sprite
Table 4-5: Color Registers in Attached Sprites
Table 4-6: Color Registers for Single Sprites
Table 4-7: Color Registers for Attached Sprites
Table 5-1: Sample Audio Data Set for Channel 0
Table 5-2: Volume Values
Table 5-3: DMA and Audio Channel Enable Bits
Table 5-4: Data Interpretation in Attach Mode
Table 5-5: Channel Attachment for Modulation
Table 5-6: Sampling Rate and Frequency Relationship
Table 5-7: Equal-tempered Octave for a 16 Byte Sample
Table 5-8: Five Octave Even-tempered Scale
Table 5-9: Decibel Values and Volume Ranges

Table 6-1:	Table of Common Minterm Values
Table 6-2:	Typical Blitter Cycle Sequence
Table 6-3:	BLTCON1 Code Bits for Octant Line Drawing
Table 7-1:	Bits in BPLCON2
Table 7-2:	Priority of Playfields Based on Values of Bits PF1P2-PF1P0
Table 7-3:	CLXDAT Bits
Table 7-4:	CLXCON Bits
Table 7-5:	Contents of the Beam Position Counter
Table 7-6:	Contents of DMA Control Register
Table 8-1:	Typical Controller Connections
Table 8-2:	Determining the Direction of the Mouse
Table 8-3:	Interpreting Data from JOY0DAT and JOY1DAT
Table 8-4:	POTGO (\$DFF034) and POTINP (\$DFF016) Registers
Table 8-5:	Disk Subsystem
Table 8-6:	DSKLEN Register (\$DFF024)
Table 8-7:	DSKBYTR Register
Table 8-8:	ADKCON and ADKCONR Register
Table 8-9:	SERDATR / ADKCON Registers
Table K-1:	Memory Space Type Codes
