Hitachi America, Ltd.

Application Engineering
TechNote

<u>H8/338 EVB vs H8/330 EVB Differences</u>

The H8/330 evaluation board is quickly and easily converted to an H8/338 series EVB by simply swapping out the H8/330 H8/330 for a H8/338 controller. Due to differences between the chips, there are some minor differences in the interrupt vector initialization and memory map assignments.

Please refer to the respective Hardware Manuals for details of the memory maps. The H8/330 EVB monitor assigns two blocks of upper addresses to RAM for monitor support. Locations H'FB70 to H'FBFF act as the monitor stack area. Locations H'FC00 to H'FD7F are defined as the monitor's data storage area. Since these locations overlap into H8/338 on-chip RAM, modifying on-chip RAM within these blocks could re-define system variables or cause the EVB to stop operating. If one of these conditions occurs the EVB is brought back to normal operation by removing power. The current version of H8/330 EVB Monitor actually uses the following locations:

<div align="center">

AVOID !   H'FB70 -- H'FB7F
H'FBD0 -- H'FC2F
H'FC50 -- H'FC5F
H'FC80 -- H'FD0F

</div>

The H8/330 monitor supports up to 125 interrupt vectors from locations h'06 to h'ff. All H8/338 vectors are available, however, access to un-initialized vectors for the second 8-bit timer and A/D converter result in an incorrectly labeled error message.

Other than the limitations described above, all monitor functions are fully operational.   Additional features and memory of the H8/338 are not evaluated during self check diagnostics.

The pin-outs for the external connectors will change slightly due to the H8/338's extra serial port, the H8/338's D/A controller and the fact that the '338 does not support E clock operation or DPR. To simplify work with both boards, connector pin-outs with the associated pin functions are shown below.

H8/330 J1

Port	Signal	Pin
	Vss	1
P4.0	TMCI_0	3
P4.1	TMO_0	5
P4.2	TMRI_0	7
P4.3	TMCI_1	9
P4.4	TMO_1	11
P4.5	TMRI_1	13
P4.6	PW0	15
P4.7	PW1	17
	Vss	19
P8.0	RS0 \ E	21
P8.1	RS1 \ $\overline{\text{IOS}}$	23
P8.2	RS2	25
P8.3	RS3	27
P8.4	CTxD \ $\overline{\text{IRQ3}}$	29
P8.5	CRxD \ $\overline{\text{IRQ4}}$	31
P8.6	CSCK \ $\overline{\text{IRQ5}}$	33
	Vss	35
	$\overline{\text{MD1}}$	37
	$\overline{\text{MD0}}$	39
	N/C	41
	$\overline{\text{STBY}}$	43
	$\overline{\text{RESET}}$	45
	$\overline{\text{NMI}}$	47
	Vss	49

H8/330 J1

H8/338 J1

Port	Signal	Pin
	Vss	1
P4.0	TMCI_0	3
P4.1	TMO_0	5
P4.2	TMRI_0	7
P4.3	TMCI_1	9
P4.4	TMO_1	11
P4.5	TMRI_1	13
P4.6	PW0	15
P4.7	PW1	17
	Vss	19
P8.0		21
P8.1		23
P8.2		25
P8.3		27
P8.4	TxD1 \ $\overline{\text{IRQ3}}$	29
P8.5	RxD1 \ $\overline{\text{IRQ4}}$	31
P8.6	SCK1 \ $\overline{\text{IRQ5}}$	33
	Vss	35
	$\overline{\text{MD1}}$	37
	$\overline{\text{MD0}}$	39
	N/C	41
	$\overline{\text{STBY}}$	43
	$\overline{\text{RESET}}$	45
	$\overline{\text{NMI}}$	47
	Vss	49

H8/338 J1

H8/330 J2

Port	Signal	Pin
	Vss	1
P3.0	DDB0 \ D0	3
P3.1	DDB1 \ D1	5
P3.2	DDB2 \ D2	7
P3.3	DDB3 \ D3	9
P3.4	DDB4 \ D4	11
P3.5	DDB5 \ D5	13
P3.6	DDB6 \ D6	15
P3.7	DDB7 \ D7	17
	Vss	19
P1.0	A0	21
P1.1	A1	23
P1.2	A2	25
P1.3	A3	27
P1.4	A4	29
P1.5	A5	31
P1.6	A6	33
P1.7	A7	35
	Vss	37
		39
		41
		43
		45
		47
		49

$\overline{\text{EXTIO}}$
RESET
$\overline{\text{RESET}}$, $\overline{\text{NMI}}$, $\overline{\text{STBY}}$

H8/330 J2

H8/338 J2

Port	Signal	Pin
	Vss	1
P3.0	D0	3
P3.1	D1	5
P3.2	D2	7
P3.3	D3	9
P3.4	D4	11
P3.5	D5	13
P3.6	D6	15
P3.7	D7	17
	Vss	19
P1.0	A0	21
P1.1	A1	23
P1.2	A2	25
P1.3	A3	27
P1.4	A4	29
P1.5	A5	31
P1.6	A6	33
P1.7	A7	35
	Vss	37
		39
		41
		43
		45
		47
		49

$\overline{\text{EXTIO}}$
RESET
$\overline{\text{RESET}}$, $\overline{\text{NMI}}$, $\overline{\text{STBY}}$

H8/338 J2

H8/330 J1

Port	Signal	Pin
	Vss	2
	AVss	4
P7.0	AN0	6
P7.1	AN1	8
P7.2	AN2	10
P7.3	AN3	12
P7.4	AN4	14
P7.5	AN5	16
P7.6	AN6	18
P7.7	AN7	20
	AVcc	22
	Vss	24
P6.0	FTCI	26
P6.1	FTOA	28
P6.2	FTIA	30
P6.3	FTIB	32
P6.4	FTIC	34
P6.5	FTID	36
P6.6	FTOB \ $\overline{IRQ6}$	38
P6.7	$\overline{IRQ7}$	40
	Vss	42
	+5v	44
		46
		48
		50

H8/330 J1

H8/338 J1

Port	Signal	Pin
	Vss	2
	AVss	4
P7.0	AN0	6
P7.1	AN1	8
P7.2	AN2	10
P7.3	AN3	12
P7.4	AN4	14
P7.5	AN5	16
P7.6	AN6 \ DA0	18
P7.7	AN7 \ DA1	20
	AVcc	22
	Vss	24
P6.0	FTCI	26
P6.1	FTOA	28
P6.2	FTIA	30
P6.3	FTIB	32
P6.4	FTIC	34
P6.5	FTID	36
P6.6	FTOB \ $\overline{IRQ6}$	38
P6.7	$\overline{IRQ7}$	40
	Vss	42
	+5v	44
		46
		48
		50

H8/338 J1

H8/330 J2

Port	Signal	Pin
	Vss	2
P2.0	A8	4
P2.1	A9	6
P2.2	A10	8
P2.3	A11	10
P2.4	A12	12
P2.5	A13	14
P2.6	A14	16
P2.7	A15	18
	Vss	20
P5.0	ASCK	22
P5.1	ARxD	24
P5.2	ATxD	26
	Vss	28
	+5v	30
	Vss	32
P9.0	$\overline{IRQ2}$ \ $\overline{ADTRG}$	34
P9.1	$\overline{IRQ1}$	36
P9.2	$\overline{IRQ0}$	38
P9.3	$\overline{CS}$ \ $\overline{RD}$	40
P9.4	$\overline{OE}$ \ $\overline{WR}$	42
P9.5	$\overline{RDY}$ \ $\overline{AS}$	44
P9.6	Φ	46
P9.7	$\overline{WE}$ \ $\overline{WAIT}$	48
	Vss	50

H8/330 J2

H8/338 J2

Port	Signal	Pin
	Vss	2
P2.0	A8	4
P2.1	A9	6
P2.2	A10	8
P2.3	A11	10
P2.4	A12	12
P2.5	A13	14
P2.6	A14	16
P2.7	A15	18
	Vss	20
P5.0	SCK0	22
P5.1	RxD0	24
P5.2	TxD0	26
	Vss	28
	+5v	30
	Vss	32
P9.0	$\overline{IRQ2}$ \ $\overline{ADTRG}$	34
P9.1	$\overline{IRQ1}$	36
P9.2	$\overline{IRQ0}$	38
P9.3	$\overline{RD}$	40
P9.4	$\overline{WR}$	42
P9.5	$\overline{AS}$	44
P9.6	Φ	46
P9.7	$\overline{WAIT}$	48
	Vss	50

H8/338 J2

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