Hitachi America, Ltd.

Application Engineering TechNotes

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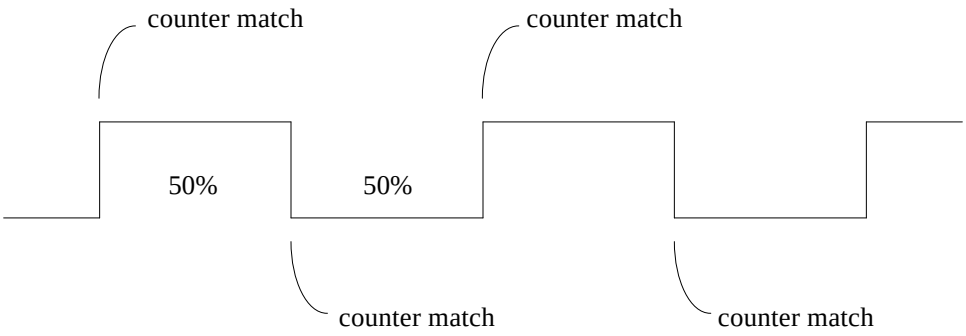
Using the H8/3XX-Series to generate various frequency pulses

The 8-bit timer module of the H8/3XX series can be used to generate pulses within a range of discrete frequencies depending upon the system clock, its prescaled values, and the count value stored in one of the Time Constant Registers, TCORA or TCORB.

The system clock (SCLK) is provided by an external crystal oscillator whose frequency is halved by an internal divider. Its frequency can range between 0.5 and 10MHz. An internal prescaler scales it down to the 3 possible frequencies SCLK/8, SCLK/64, or SCLK/1024, as selected by bits 2-0 of the Timer Control Register (TCR) in order to provide the internal clock for the counter timing. The count value is stored in one of the 2 Time Constant Registers, TCORA or TCORB. Since these registers are 8-bits wide, the range of the counter is between 00H-FFH (0-255).

During the counting process, the Timer Counter Register (TCNT) contents are incremented on each consecutive falling edge of the internal clock. Programming bits 4 and 3 of the TCR to 01 or 10 clears the counter register when its contents match the count value stored in TCORA or TCORB, and counting resumes again. Depending whether the count value is stored in TCORB or TCORA, bits 3-2 or 1-0 of the Timer Control/Status Register (TCSR) can be programmed to 11, thus forcing the timer outputs TMO1 or TMO0 to toggle each time TCNT is cleared. Hence, the desired pulse frequency is generated as illustrated below:



TMO1/TMO0 Output

Given the internal clock value and the desired pulse rate, the counter match value that should be programmed in TCORA or TCORB can be easily calculated using the formula:

Match value = Internal Clock / 2 x Pulse Rate

There are 256 possible frequencies that can be generated for each internal clock value. Therefore, if the calculated match value is a decimal number, it should be rounded off to the nearest integer, and used to re-calculate the closest possible frequency to the desired pulse rate. If the calculated match value is 256, then TCORA or TCORB have to be programmed to 0. To illustrate the possible frequency range of the pulses, a system clock of 10MHz allows a pulse range between 19.1Hz and 625KHz, while a SCLK of 0.5MHz will permit a pulse range between 1Hz and 31.25KHz.

Example:

Calculate the counter match value needed to be programmed into TCORA in order to generate a 55Hz pulse at the TMO0 pin. Assume a 50% duty cycle and a system clock of 10MHz.

Solution:

If we choose to program bits 2-0 of the TCR register to 011, the internal timer clock rate will be:
Internal clock = 10MHz/1024 = 9.766KHz.
The needed match value is calculated according to the formula given above:
Match value = 9.766KHz / 2 x 55Hz = 88.78 = {round off to nearest even digit} = 89 = 59H.
The nearest possible frequency will be:
Pulse rate = 9.766KHz / 2 x 89 = 54.8Hz.

Code:

```
; Timer 0 (TMO0) is used to produce a 54.8Hz pulse
        MOV.b   #h'59, r1l
        MOV.b   r1l, @tmr0_TCORA   ;load TCORA with counter match value
        MOV.b   #h'03, r1l
        MOV.b   r1l, @tmr0_TCSR   ;output toggles on match A
        MOV.b   #h'0B, r1l
        MOV.b   r1l, @tmr0_TCR   ;set SCLK/1024 internal clock, clear on match A and re-start
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