Hitachi Single-Chip Embedded Processor

H8/300 Series Overview

PRELIMINARY

HITACHI®

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Table of Contents

Introduction

The Hitachi H8 Series of single-chip microcomputers currently consists of four Series: H8/500, H8/300H, H8/300, and H8/300L. The accompanying Table lists their distinctive features.

Series	Features
H8/500	Highly orthogonal instruction set, instruction-level support for high-level languages, general register architecture, address space expandable to 16 megabytes
H8/300H	32-bit CPU backwardly compatible with the H8/300 CPU, 16-megabyte linear address space, streamlined instruction set, powerful lineup of 8-, 16-, and 32-bit arithmetic and logic instructions
H8/300	CPU with general register architecture, 64-kilobyte address space, streamlined instruction set, powerful bit manipulation instructions
H8/300L	H8/300-compatible CPU, up to 64-kilobyte on-chip memory space, streamlined instruction set, low-voltage operation with reduced power consumption, onboard peripherals for consumer applications

This document provides brief descriptions of the H8/300 Series, its features, and the related development environment.

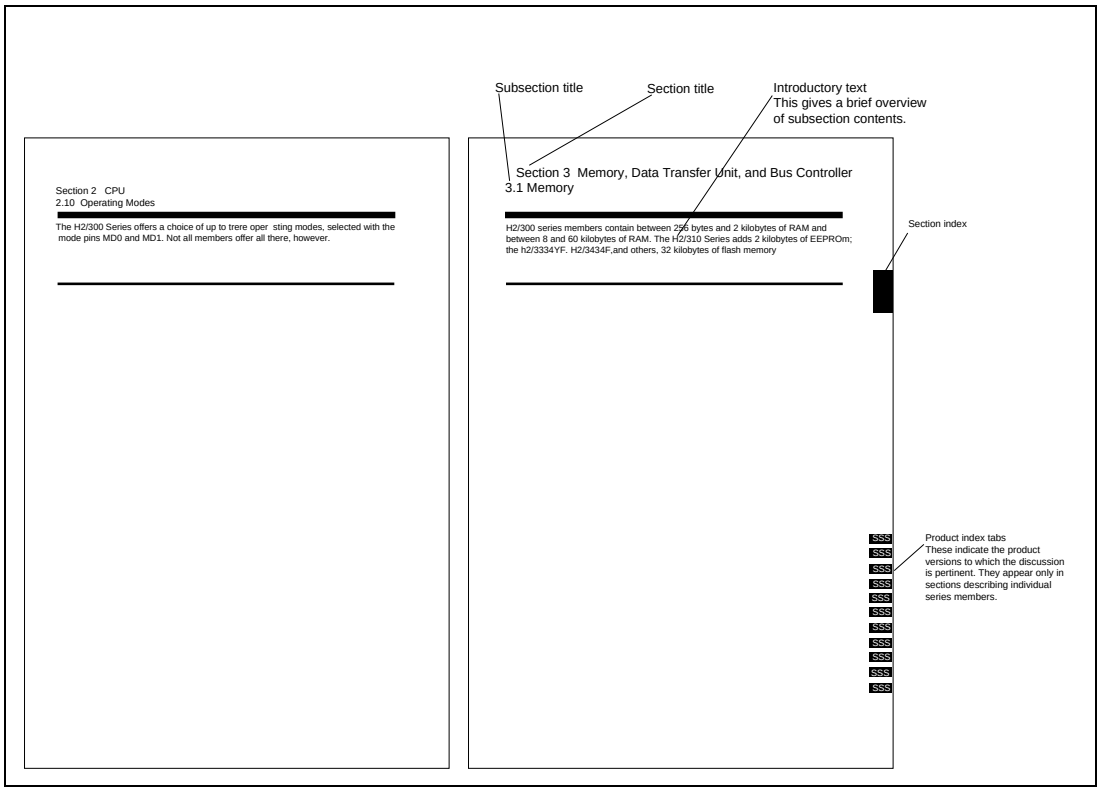
Who Should Read This Manual?

This manual is aimed at those with basic microcomputer understanding and a desire to learn the features and basic functionality of the H8/300 Series. Those wishing to design systems around Series members or otherwise needing detailed specifications are advised to read the relevant hardware manuals and the H8/300 Series Programming Manual.

Using This Manual

See the Table of Contents for a complete listing of all section and subsection headings. There is also an index at the end of this volume. Finally, there is a separate index for onboard peripherals.

Page Layout



Product Index

The product index tabs group product versions into the following subseries:

H8/310 Series: H8/310, H8/3101, H8/3102

H8/325 Series:	H8/322, H8/323, H8/324, H8/325, H8/3256, H8/3257
H8/329 Series:	H8/326, H8/327, H8/328, H8/329
H8/3297 Series:	H8/3292, H8/3294, H8/3296, H8/3297
H8/330:	H8/330
H8/3314:	H8/3314

H8/3334 Series:	H8/3332, H8/3334
H8/3337 Series:	H8/3334Y, H8/3336Y, H8/3337Y
H8/3397 Series:	H8/3394, H8/3396, H8/3397
H8/338 Series:	H8/336, H8/337, H8/338
H8/3427 Series:	H8/3434, H8/3436, H8/3437
H8/350:	H8/350

Product Index Tabs

The product index tabs provide a quick way of cross-referencing the onboard peripheral descriptions in Sections 3 through 6 with the individual production descriptions in Section 7.

Section 2 CPU
2.10 Operating Modes

The H2/300 Series offers a choice of up to trere oper sting modes, selected with the mode pins MD0 and MD1. Not all members offer all there, however.

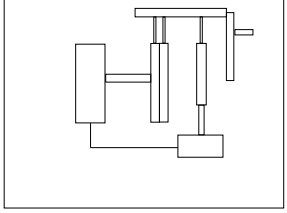
Section 3 Memory, Data Transfer Unit, and Bus Controller
3.1 Memory

H2/300 series members contain between 256 bytes and 2 kilobytes of RAM and between 8 and 60 kilobytes of RAM. The H2/310 Series adds 2 kilobytes of EEPROm; the h2/3334YF. H2/3434F,and others, 32 kilobytes of flash memory

To read a description of a particular onboard peripheral available with the product

Section 2 CPU

The H2/300 Series



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To read a description of a particular product offering the onboard peripheral

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Related Documents

Those wishing to design systems around Series members or otherwise needing detailed specifications are advised to read the relevant hardware manuals and the H8/300 Series Programming Manual.

H8/300 Series Programming Manual (ADE-602-025)

H8/310 Hardware Manual (AD-602-024)

H8/3101 Hardware Manual (ADE-602-043)

H8/3102 Hardware Manual (ADE-602-084)

H8/325 Series Hardware Manual (ADE-602-092B)

H8/329 Series Hardware Manual (ADE-602-046)

H8/330 Hardware Manual (ADE-602-026A)

H8/3332 Series Hardware Manual (ADE-602-061)

H8/3297 Series Hardware Manual (ADE-602-080)

H8/3337 Series Hardware Manual (ADE-602-078)

H8/3397 Series Hardware Manual (ADE-602-078)

H8/338 Series Hardware Manual (ADE-602-039)

H8/350 Hardware Manual (ADE-602-037)

Section 1 H8/300 Series Features

1.1 H8/300 Series Features

The H8/300 Series, built around the H8/300 CPU, incorporate ROM, RAM, timers, serial communications interfaces, A/D converters, and other peripherals required by many applications into single-package microcomputers for compact, high-performance systems. The extensive product lineup includes versions with keyboard controllers, analog conversion capabilities, energy conservation facilities, etc.

Also available are ZTAT™[*1] and F-ZTAT™ [*2] versions that help reduce turnaround time (TAT) and address the need for diverse and diversified systems.

Note: 1. ZTAT™ (zero turn-around time) is a registered trademark of Hitachi, Ltd.
2. F-ZTAT™ (flexible-ZTAT) is a trademark of Hitachi, Ltd.

High-Speed CPU Architecture

- General register machine
  - Sixteen 8-bit general registers that may also be paired to form eight 16-bit registers
- Instruction set designed for high-speed operation
  - Number of instructions: 57
  - All instructions two or four bytes long
  - High-speed multiplication and division instructions plus powerful bit manipulation instructions
- 64-kbyte address space
- Choice of three operating modes
  - Mode 1: Enhanced mode with onboard ROM disabled (full 64-kbyte address space available)
  - Mode 2: Enhanced mode with onboard ROM enabled (full 64-kbyte address space available)
  - Mode 3: Single-chip mode (only onboard ROM, RAM, and registered available)

Operating Voltages, Clock Speeds, Clock Oscillators

				Clock Oscillator			
				Frequency Divider	Ratio	Oscillator	
		Operating Voltage Range	System Clock Range	1/2	1/1	Crystal	External
H8/310, H8/3101		4.5 to 5.5 V	5 MHz to 500 kHz	•	–	–	•
H8/3102	5-V version	4.5 to 5.5 V	5 MHz to 500 kHz	•	–	–	•
	3-V version	2.7 to 3.3 V	2.5 MHz to 500 kHz				
H8/325 Series	5-V version	4.5 to 5.5 V	10 MHz to 500 kHz	•	–	•	•
	3-V version*	2.7 to 5.5 V	5 MHz to 500 kHz				
H8/329 Series	5-V version	4.5 to 5.5 V	10 MHz to 500 kHz	•	–	•	•
	3-V version	2.7 to 5.5 V	5 MHz to 500 kHz				
H8/3297 Series	5-V version	4.5 to 5.5 V	16 MHz to 2 MHz	–	•	•	•
	3-V version	2.7 to 3.6 V	10 MHz to 2 MHz				
H8/350		4.5 to 5.5 V	10 MHz to 500 kHz	•	–	•	•
H8/330		4.5 to 5.5 V	10 MHz to 500 kHz	•	–	•	•
H8/3314		4.5 to 5.5 V	10 MHz to 500 kHz	•	–	•	•
H8/338 Series	5-V version	4.5 to 5.5 V	10 MHz to 500 kHz	•	–	•	•
	3-V version	2.7 to 3.3 V	5 MHz to 500 kHz				
H8/3334 Series	5-V version	4.5 to 5.5 V	10 MHz to 500 kHz	•	–	•	•
	3-V version	2.7 to 5.5 V	5 MHz to 500 kHz				
H8/3337 Series	5-V version	4.5 to 5.5 V	16 MHz to 2 MHz	–	•	•	•
	3-V version	2.7 to 3.6 V	10 MHz to 2 MHz				
H8/3397 Series	5-V version	4.5 to 5.5 V	16 MHz to 2 MHz	–	•	•	•
	3-V version	2.7 to 3.6 V	10 MHz to 2 MHz				
H8/3437 Series	5-V version	4.5 to 5.5 V	16 MHz to 2 MHz	–	•	•	•
	3-V version	2.7 to 3.6 v	10 MHz to 2 MHz				

Note: * H8/3256, H8/3257 only

Memory, Data Transfer Unit, and Bus Controller

- ROM
  - Versions contain between 8 and 60 kbytes of ROM in the form of masked ROM, PROM, or flash memory.
  - This memory accesses in only two clock cycles.
- RAM
  - Versions contain between 256 bytes and 2 kbytes of RAM.
  - This memory accesses in only two clock cycles.
- EEPROM (H8/310 Series)
  - This version has 8 kbytes of onboard EEPROM accessible with CPU instructions for rewriting contents.
  - This memory accesses in only two clock cycles.
- E clock interface (H8/325 and H8/330 Series)
  - This clock output has a frequency that is one-eighth the system clock.
  - There are two data transfer instructions with E clock synchronization.
- Wait state controller (H8/3297, H8/3397, H8/3337, and H8/3437 Series)
  - There is a choice of three operating modes.
- Data transfer unit (H8/3314)
  - This 4-channel data transfer unit supports direct memory access transfers and an 8-bit parallel buffer interface.
  - I/O transfer sources and destinations supported include the serial communications interface, the 16-bit free-running timer, programmable timing pattern controller, and A/D converter data registers.
  - PBI transfers allow a master CPU easy read/write access to up to 256 bytes of onboard RAM as dual-port RAM.

Parallel and Serial Interfaces

- Parallel communications with master CPU via dual-port RAM.
  - The H8/330 Series includes 15 bytes of dual-port RAM.
  - The H8/3314 Series' DTU/PBI transfer DPRAM mode allows the master CPU to access up to 256 bytes of the onboard RAM as dual-port RAM.
- Parallel handshake interface
  - The H8/325 Series uses a port data latch and input strobe interrupts to support parallel communications with a master CPU.
  - The H8/3314 Series DTU/PBI handshake mode supports 8-bit parallel handshake operation.
- Hose interface (H8/3334 Series, H8/3337 Series, H8/3437 Series)
  - Two independent parallel communications channels are available.
  - The input data, output data, and status registers are all freely accessible from both the onboard and host CPUs as addresses within the respective address spaces.
  - There is a choice of normal or high-speed GATE A20 output.
- Asynchronous/synchronous serial communications interface (all versions except H8/310)
  - Support for full-duplex operation
  - Onboard baud rate generator
- 8/16-bit synchronous serial communications interface (H8/350)
  - Choice or 8- or 16-bit operation
  - Continuous communications through use of separate buffer registers for both transmitting and receiving.
- I^2C bus interface (option for H8/3337 and H8/3437 Series)
  - Compliance with Philips Inter IC (I^2C) bus interface standard

Timers

- 16-bit free-running timer[*1]
  - — Output compare and input capture functions
- 8-bit multifunction timer[*1]
  - — Two independent comparators plus timer output
- 8-bit PWM timer[*2]
  - — Resolution of 1/250 and choice of duty rations between 0% and 100% for output pulses
- 14-bit PWM timer (H8/350 only)
  - — Connection of a low-pass filter enables operation as a digital-to-analog converter
- Watchdog timer (H8/3297 Series, H8/3314 Series, H8/3334 Series, H8/3337 Series, H8/3397 Series, H8/3437 Series)
  - — Choice of watchdog timer and interval timer operation
- Timer network (H8/350 only)
  - — Timer network controlling connections between nine onboard timers (four types) and the I/O pins
- Programmable timing pattern controller (H8/3314)
  - — Capable of producing up to 16 bits of pulse output using a timer base from a 16-bit free-running timer

Notes: 1. H8/325 Series, H8/329 Series, H8/3297 Series, H8/330, H8/3314, H8/338 Series, H8/3334 Series, H8/3337 Series, H8/3397 Series and H8/3437 Series

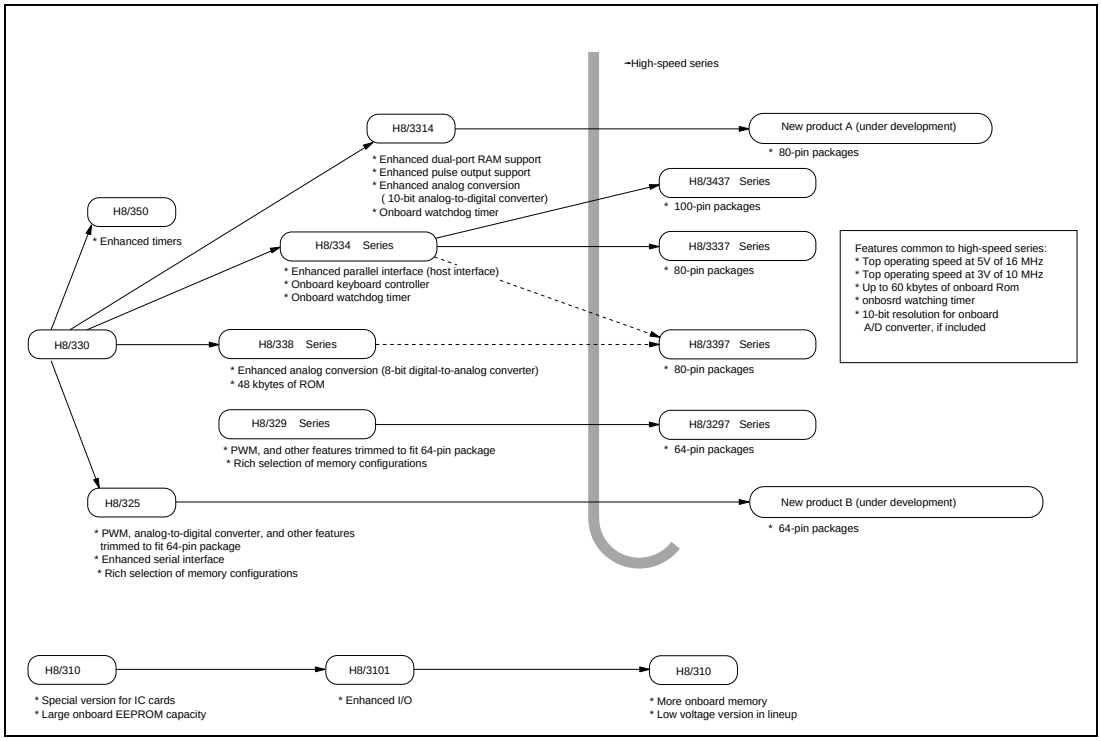
2. H8/330, H8/338 Series, H8/3334 Series, H8/3337 Series, H8/3397 Series, and H8/3437 Series

Analog Conversion Functions

- 8[*1]- or 10[*2]-bit A/D converter
  - — Choice of single-channel and scan modes
  - — Support for initiating processing with an external trigger
  - — Built-in simple and hold circuit
- 8-bit D/A converter (H8/338 Series, H8/3337 Series, H8/3437 Series)
  - — Two channels of analog output

Notes: 1. H8/329 Series, H8/350, H8/330, H8/338 Series, and H8/3334 Series
2. H8/3297 Series, H8/3314, H8/3337 Series, H8/3397 Series, and H8/3437 Series

Product Hierarchy



1.3 ZTAT™ and F-ZTAT™ Versions

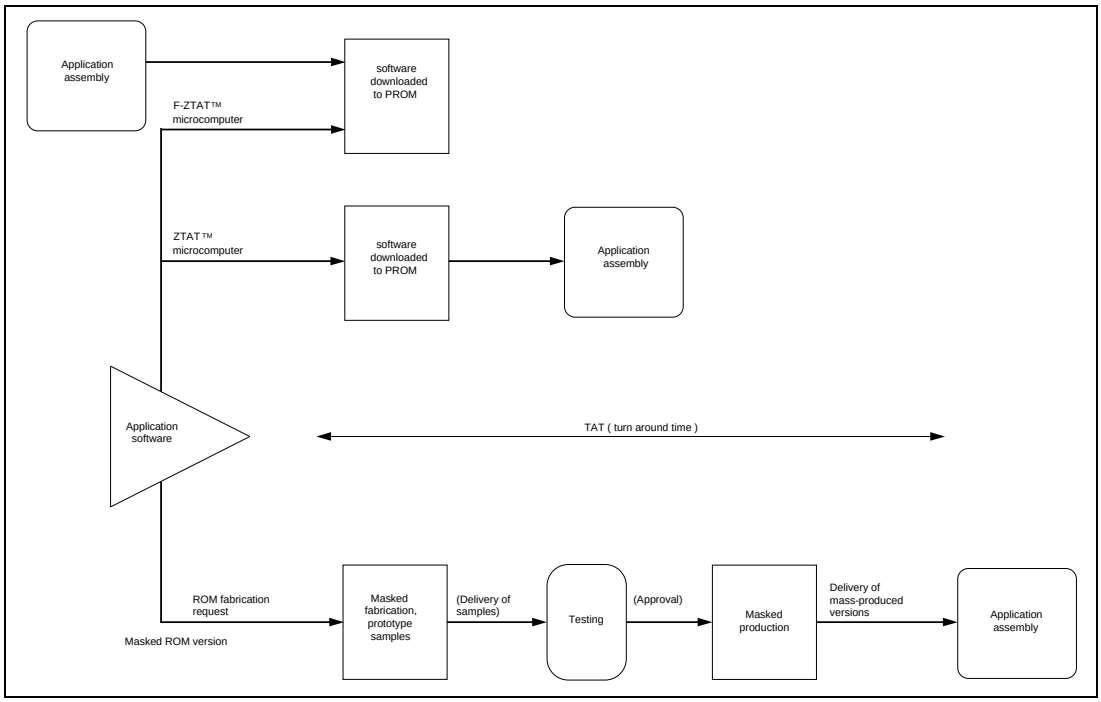
Most members of the H8/300 Series are available in both masked ROM and ZTAT™ versions. These latter are microcomputers with user-programmable ROMs. The ability to download to these ROMs software immediately after it has been developed means vastly shorter turnaround times for users. There are also versions (H8/3334YF-ZTAT™ and H8/3434F-ZTAT™) substituting flash memory for the ROMs.

ZTAT™ Microcomputers

- Shorter turnaround times and lower costs for development
  - — Users download software themselves rather than waiting for the manufacturer.
- Ideal for small-lot, multiversion applications
  - — For small production runs, ZTAT™ is more economical than masked ROM.
  - — This versatility is ideal for areas where specifications change frequently.
- Designed for standard PROM writer
  - — Special socket adapters change the pin configurations for use with a standard PROM writer.

F-ZTAT™ Microcomputers

- Shorter development turnaround times
  - — Hardware can lead development since the software can be adjusted at any time-even after the microcomputer has been installed in the hardware.
- Lower development costs
  - — The software may be upgraded over and over again during development.
  - — Producing multiple versions can be as easy as modifying portions of the software.
  - — A mode is also supported in which programming is possible simply by connecting a special socket adapter to a standard PROM writer.
- System flexibility
  - — Software upgrade facility enables fine-turning at the individual unit level.
  - — Software can be modified with the chip still in place.
  - — Field upgrades entail changing only the software, not the circuit board or chip.


Application assembly
software downloaded to PROM
F-ZTAT™ microcomputer
ZTAT™ microcomputer
software downloaded to PROM
Application assembly
Application software
TAT (turn around time)
ROM fabrication request
Masked ROM version
Masked fabrication, prototype samples
(Delivery of samples)
Testing
(Approval)
Masked production
Delivery of mass-produced versions
Application assembly

Section 2 CPU

2.1 Features

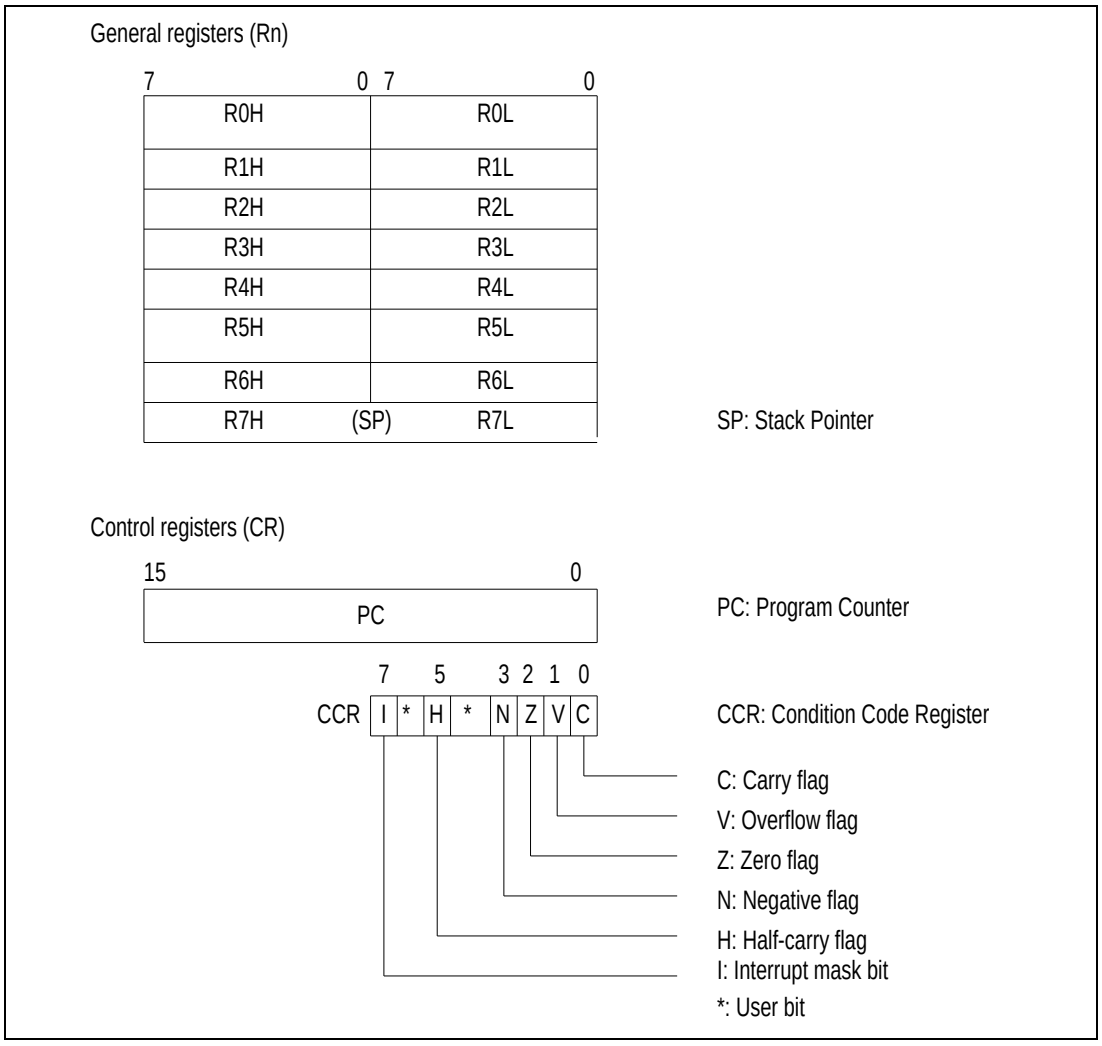
H8/300 Series members feature sixteen 8-bit general registers and a highly orthogonal instruction set optimized for high-speed operation.

The high-speed H8/300 Series CPU has the following features.

- General register machine
  - — Sixteen 8-bit general registers that may also be paired to form eight 16-bit registers
- High-speed operation
  - — Series members offer clock speeds from 5 MHz to 16 MHz
  - — High-speed arithmetic
    Addition of 8- or 16-bit registers: 2 clock cycles
    Multiplication of 8-bit quantities: 14 clock cycles
    Division of a 16-bit quantity by an 8-bit one: 14 clock cycles
- Instruction set designed for high-speed operation
  - — Number of instructions: 57
  - — All instructions two or four bytes long
  - — High-speed multiplication and division instructions
  - — Powerful bit manipulation instructions
- 64-kbyte address space

2.2 Register Configuration

H8/300 Series members feature sixteen 8-bit general registers (R0H to R7H, R0L to R7L), a 16-bit program counter (PC), and an 8-bit condition code register (CCR).



General Registers

H8/300 Series members have sixteen 8-bit general registers. These are functionally interchangeable and are available for independent use with addresses or data.

These registers may also be paired for use as eight of 16-bit registers (R0-R7). When used with data, the two halves may be accessed as independent 8-bit registers (H and L) or as a single 16-bit register.

When used as address registers, they are used as 16-bit registers. Usage varies with the instruction, however.

General register R7 doubles as the stack pointer (SP) and is altered by exceptions and subroutine calls.

Control Registers

- Program Counter (PC)
  This 16-bit counter indicates the address of the next instruction to be executed.

- Condition Code Register (CCR)
  This 8-bit register contains the interrupt mask (I) and user (*) control flag bits plus the carry (C), overflow (V), zero (Z), negative (N), and half-carry (H) status flag bits automatically set by the CPU as the result of arithmetic operations. The register may be read and the control flag bits set with the CCR access instructions.

  — Bit 7--Interrupt Mask Bit (I)
    A `1' in this position enables masking of all interrupts except the non-maskable interrupt. For further details, see Section 2.8 "Exception Processing."

  — Bit 6--User Bit (*)
    The CCR access instructions provide read/write access to this bit for application use.

  — Bit 5--Half Carry Flag (H)
    A `1' in this position results if there is a carry or borrow between the fourth and fifth most significant bits for an add, subtract, compare, or negate instruction--that is, at bit 3 for the ADD.B, ADDX.B, SUB.B, SUBX.B, CMP.B, and NEG.B instructions or at bit 11 for the ADD.W, SUB.W, and CMP.W instructions. Otherwise, the bit is `0'. The DAA and DAS decimal adjust instructions implicitly use this bit.

  — Bit 4--User Bit (*)
    The CCR access instructions provide read/write access to this bit for application use.

— Bit 3--Negative Flag (N)

Tracks the high-order (sign) bit of the arithmetic result.

— Bit 2--Zero Flag (Z)

A `1’ in this position indicates that all bits in the result are zero. Otherwise, the bit is `0’.

— Bit 1--Overflow Flag (V)

A `1’ in this position indicates overflow during the arithmetic operation. Otherwise, the bit is `0’.

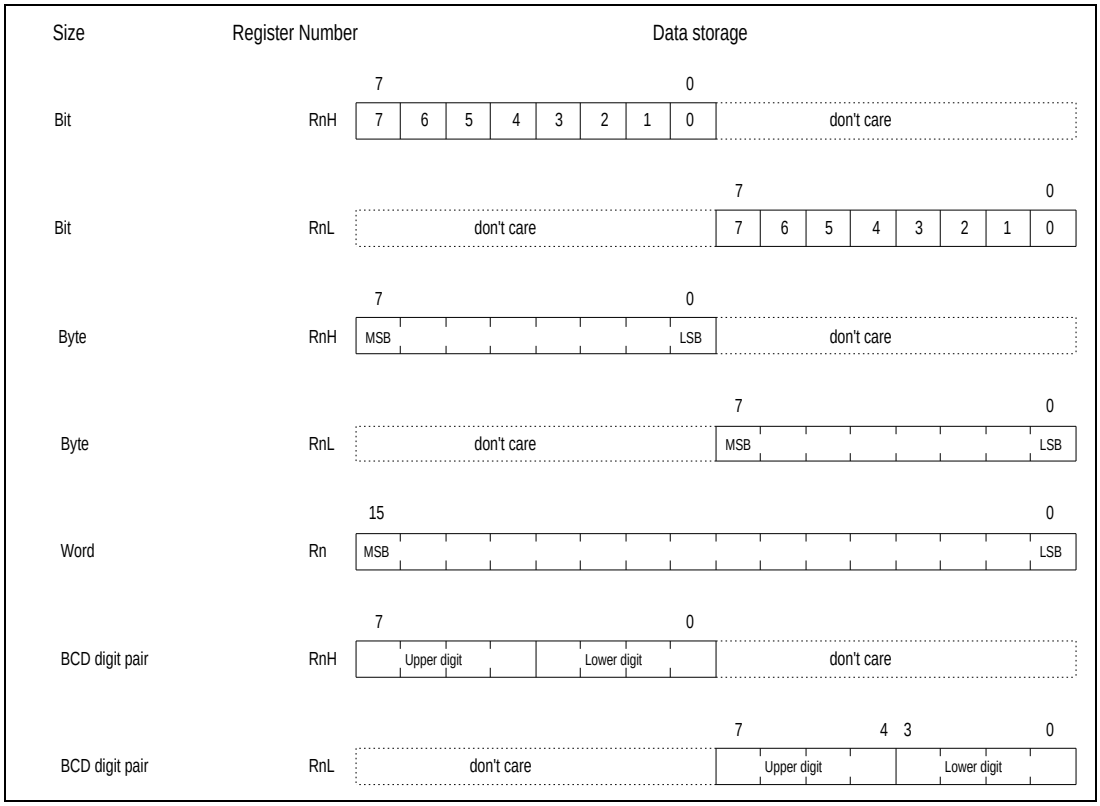
— Bit 0--Carry Flag (C)

A `1’ in this position indicates a carry out of borrow into the high-order bit during the arithmetic operation. Otherwise, the bit is `0’. It is used by add instructions to indicate a carry, by subtract instructions to indicate a borrow, by shift and rotate instructions to store the bit shifted past the end, and by bit manipulation instructions as a bit accumulator.

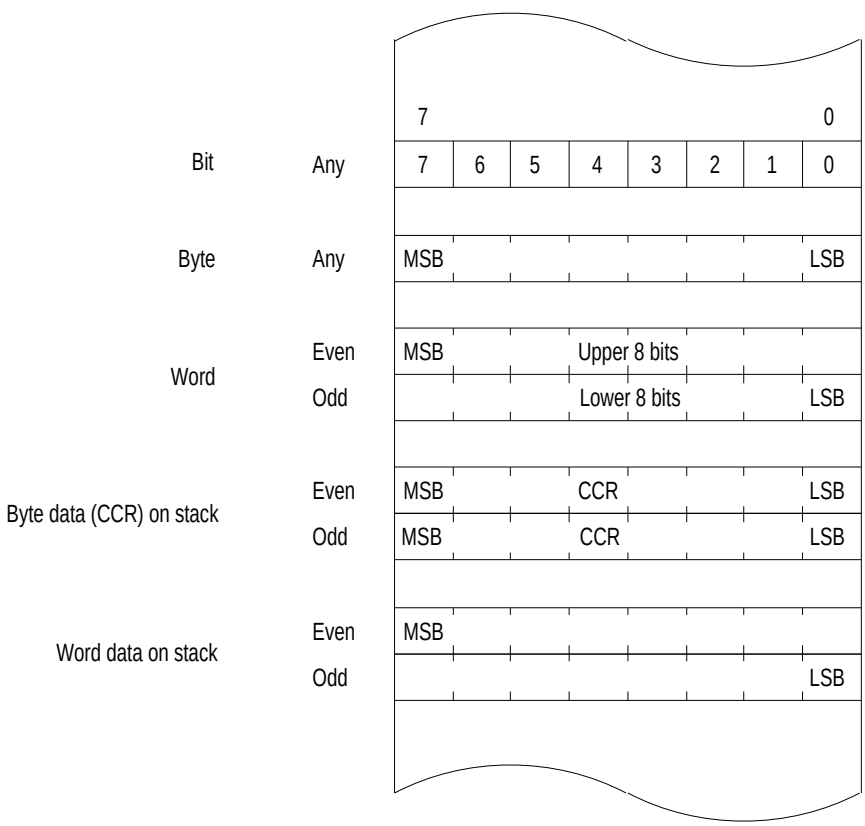
2.3 Data Formats

H8/300 Series members support four data sizes: single bits, 4-bit binary coded decimal (BCD) digits, 8-bit bytes, and 16-bit words. In general, byte data may be used with all instructions. Single-bit data is limited to the bit manipulation instructions; word-sized data, to data transfer instructions and a subset of the arithmetic instructions. The only instructions specifically for BCD data are the DAA and DAS decimal adjust instructions.

General Register Data Formats



Memory Data Formats



Note: Word data must be aligned on a word boundary-that is, must begin at an even address.

Legend:
CCR: Condition code register

Note: Word data must be aligned on a word boundary--that is, must begin at an even address.
Legend:
CCR: Condition code register

2.4 Addressing Modes

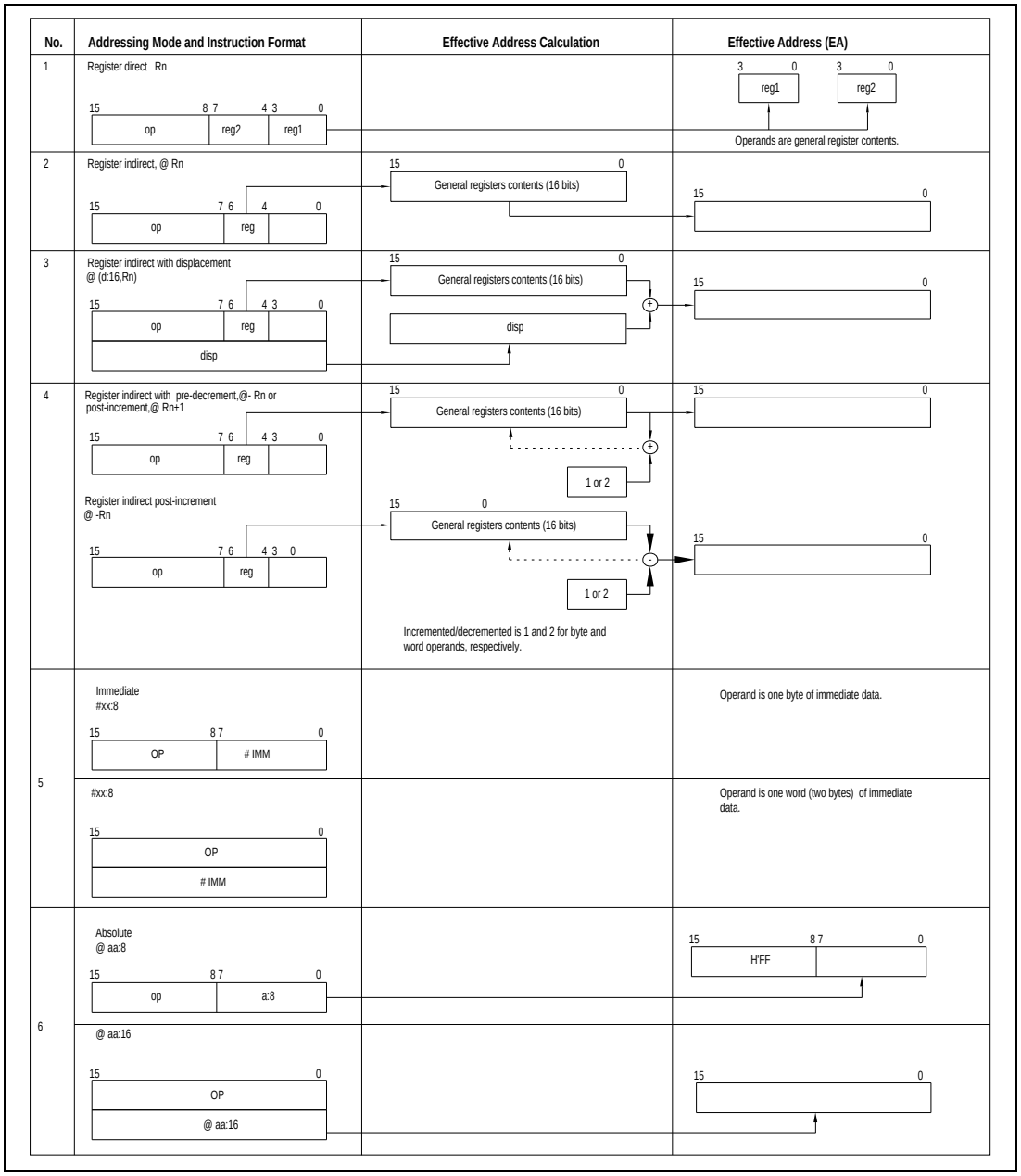
H8/300 Series members support the eight addressing modes listed in the accompanying Table: register direct, register indirect, register indirect with displacement, register indirect with pre-decrement or post-increment, immediate, absolute, program counter relative, and memory indirect.

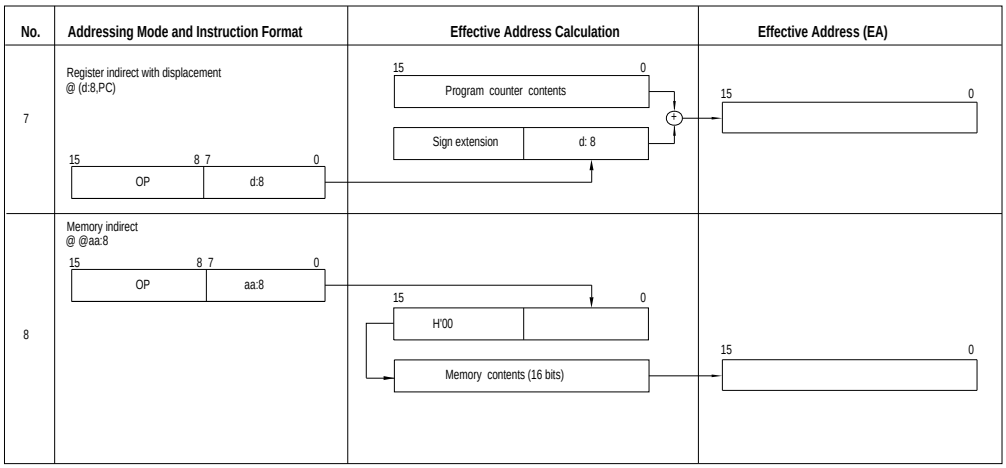
Summary of Addressing Modes

No.	Addressing Mode	Mnemonic
1	Register direct	Rn
2	Register indirect	@Rn
3	Register indirect with displacement	@(d:16,Rn)
4	Register indirect with pre-decrement	@–Rn
	Register indirect with post-increment	@Rn+
5	Immediate	#xx:8 or #xx:16
6	Absolute	@aa:8 or @aa:16
7	Program counter relative	@(d:8,PC)
8	Memory indirect	@ @aa:8

Note: Data transfers use only the first six modes.

Effective Address Calculations





Legend:

reg: General register
d: Displacement
#IMM: Immediate data
aa: Absolute address

2.5 Instruction Set

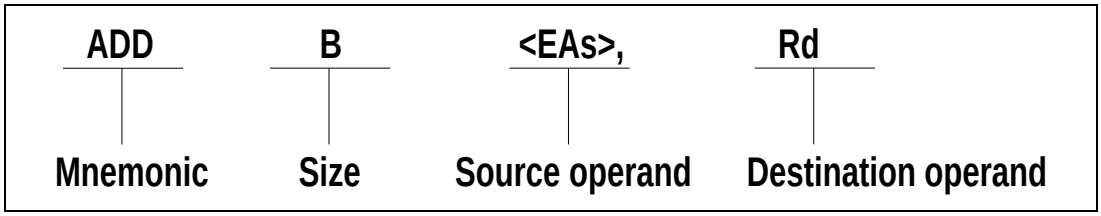
H8/300 Series members feature a highly orthogonal 57-member instruction set optimized for high-speed operation. Of particular interest are its high-speed multiply and divide instructions and powerful bit manipulation instructions.

Features

- Highly orthogonal instruction set optimized for speed
  All instructions are two or four bytes long.
- High-speed operation
  The most frequently used instructions execute in 2-4 clock cycles. Additions and subtractions between two 16-bit registers take only 2 clock cycles.
- General register architecture
- Powerful bit manipulation instructions
- Standard H Series mnemonics

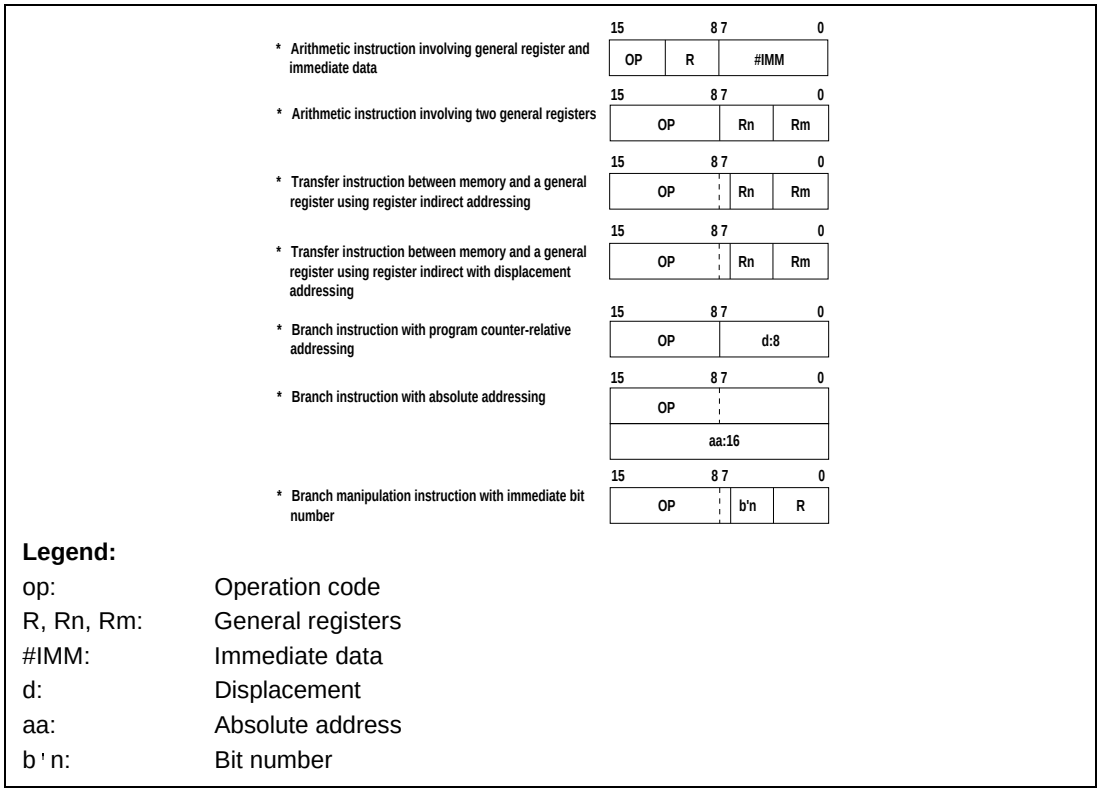
Assembler Format

The ADD instruction, for example, has the following format:



Major Instruction Formats

The accompanying figure lists the major instruction formats.



Legend:

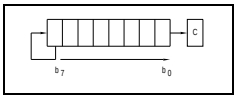
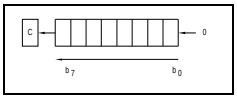
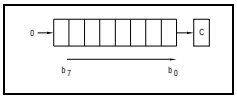
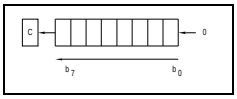
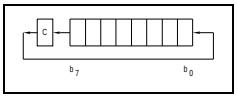
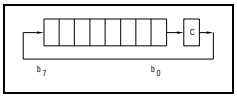
op:	Operation code
R, Rn, Rm:	General registers
#IMM:	Immediate data
d:	Displacement
aa:	Absolute address
b ' n:	Bit number

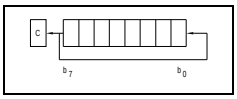
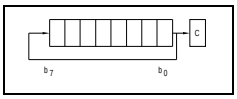
Instruction Set Summary

Mnemonic		Operand Size	Operation	Addressing Mode/Instruction Length								Condition Code (CCR)						
				#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa Implied	I	H	N	Z	V	C	No. of States
Data transfer	MOV.B Rs,Rd	B	Rs8 → Rd8		2							–	–	↕	↕	0	–	2
	MOV.B #xx:8,Rd	B	#xx:8 → Rd8	2								–	–	↕	↕	0	–	2
	MOV.B @ Rs,Rd	B	@ Rs 16 → Rd8			2						–	–	↕	↕	0	–	4
	MOV.B @ (d: 16,Rs),Rd	B	@ (d:16,Rs16) → Rd8				4					–	–	↕	↕	0	–	6
	MOV.B @ Rs+,Rd	B	@ Rs16 → Rd8,Rs 16+1 → Rs 16					2				–	–	↕	↕	0	↕	6
	MOV.B @ aa:8,Rd	B	@ aa:8 → Rd8						2			–	–	↕	↕	0	–	4
	MOV.B @ aa:16,Rd	B	@ aa: 16 → Rd8						4			–	–	↕	↕	0	–	6
	MOV.B Rs, @ Rd	B	Rs8 → @ Rd16			2						–	–	↕	↕	0	–	4
	MOV.B Rs, @ (d:16,Rd)	B	Rs8 → @ (d:16,Rd16)				4					–	–	↕	↕	0	–	6
	MOV.B Rs, @-Rd	B	Rs16-1 → Rd16,Rs8 → @ Rd16					2				–	–	↕	↕	0	–	6
	MOV.B Rs, @ aa:8	B	Rs8 → @ aa:8						2			–	–	↕	↕	0	–	4
	MOV.B Rs, @ aa:16	B	Rs8 → @ aa:16						4			–	–	↕	↕	0	–	6
	MOV.W Rs,Rd	W	Rs16 → Rd16		2							–	–	↕	↕	0	–	2
	MOV.W @ Rs,Rd	W	@ Rd16 → Rd16			2						–	–	↕	↕	0	–	4
	MOV.W @ (d:16,Rs),Rd	W	@ (d:16,Rs16) → Rd16				4					–	–	↕	↕	0	–	6
	MOV.W @ Rs+,Rd	W	@ Rs16 → Rd16,Rs16+2 → Rs 16					2				–	–	↕	↕	0	–	6
	MOV.W @ aa:16,Rd	W	@ aa:16 → Rd16						4			–	–	↕	↕	0	–	6
	MOV.W Rs, @ Rd	W	Rs16 → @ Rd16			2						–	–	↕	↕	0	–	4
	MOV.W Rs, @ (d:16,Rd)	W	Rs16 → @(d:16,Rd16)				4					–	–	↕	↕	0	–	6
	MOV.W Rs,.-Rd	W	Rd16-2 → Rd16,Rs16 → @ Rd16					2				–	–	↕	↕	0	–	6
	MOV.W Rs, @ aa:16	W	Rs16 → @ aa:16						4			–	–	↕	↕	0	–	6
	MOV.W #xx:16,Rd	W	#xx:16 → Rd	4								–	–	↕	↕	0	–	4
	POP Rd	W	@ SP → Rd, SP+2 →					2				–	–	↕	↕	0	–	6

Mnemonic		Operand Size	Operation	Addressing Mode/Instruction Length: #xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	Implied	Condition Code (CCR): I	H	N	Z	V	C	No. of States
			SP																
	PUSH Rs	W	SP-2 → SP, Rs16 → @ 16					2					–	–	↕	↕	0	–	6
	MOVFPE @ aa:16,Rd	W	@ aa:16 → Rd (synchronized with E clock)						4				–	–	↕	↕	0	–	⑤
	MOVTPE Rs, @ aa:16	W	Rs → @ aa:16 (synchronized with E clock)						4				–	–	↕	↕	0	–	⑤
	EEPMOV	–	if R4L≠0, Repeat @ R5 → @ R6 R5+1 → Rs,Rs6+1 → R6 R4L-1 → R4L Until R4L = 0 else next									4	–	–	–	–	–	–	④
Arith. Ops.	ADD.B #xx:8,Rd	B	Rd8+ #xx:8, Rd	2									–	↕	↕	↕	↕	↕	2
	ADD.B Rs,Rd	B	Rs8+Rd8 → Rd8		2								–	↕	↕	↕	↕	↕	2
	ADD.W Rs,Rd	W	Rs16+Rd16 → Rd16		2								–	①	↕	↕	↕	↕	2
	ADDX.B #xx:8,Rd	B	Rd8+#xx:8 +C → Rd8	2									–	↕	↕	②	↕	↕	2
	ADDX.B Rs, Rd	B	Rd8+Rd8 +C → Rd8		2								–	↕	↕	②	↕	↕	2
	ADDS.W #1,Rd	W	Rd16+1 → Rd16		2								–	–	–	–	–	–	2
	ADDS.W #2,Rd	W	Rd16+2 → Rd16		2								–	–	–	–	–	–	2
	INC.B Rd	B	Rd8+1 → Rd8		2								–	–	↕	↕	↕	–	2
	DAA.B Rd	B	Rd8 decimal adjust → Rd8		2								–	*	↕	↕	*	③	2
	NEG.B rd	B	0-Rd → Rd		2								–	↕	↕	↕	↕	↕	2
	SUB.B Rs,Rd	B	Rd8-Rs8 → Rd8		2								–	↕	↕	↕	↕	↕	2
	SUB.W Rs,Rd	W	Rd16-Rs16 → Rd16		2								–	①	↕	↕	↕	↕	2
	SUBX.B #xx:8,Rd	B	Rd8-#xx:8 -C → Rd8	2									–	↕	↕	②	↕	↕	2
	SUBX.B Rs,Rd	B	Rd8-Rs8 -C → Rd8		2								–	↕	↕	②	↕	↕	2
	SUBS.W #1,Rd	W	Rd16-1 → Rd16		2								–	–	–	–	–	–	2
	SUBS.W #2,Rd	W	Rd16-2 → Rd16		2								–	–	–	–	–	–	2

Mnemonic	Operand Size	Operation	Addressing Mode/Instruction Length								Condition Code (CCR)						
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	Implied	I	H	N	Z	V	C	No. of States
DEC.B Rd	B	Rd8-1 → Rd8		2								–	–	↕	↕	↕	–	2

				Addressing Mode/Instruction Length							Condition Code (CCR)						
Mnemonic		Operand Size	**Operation**	#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	Implied	I	H	N	Z	V	C	No. of States
Arithm-etic operations	DAS.B RD	B	Rd8 decimal adjust → Rd8		2								–	↕	↕	↕	↕	↕	2
	CMP.B #xx:8,Rd	B	Rd8–#xx:8	2									–	↕	↕	↕	↕	↕	2
	CMP.B Rs,Rd	B	Rd8–Rs8		2								–	↕	↕	↕	↕	↕	2
	CMP.W Rs,Rd	W	Rd16–Rs16		2								–	①	↕	↕	↕	↕	2
	MULXU.B Rs,Rd	B	Rd8xRs8 → Rd16		2								–	–	–	–	–	–	14
	DIVXU.B Rs,Rd	B	Rd16+Rs8 → Rd16 (RdH: remaninder, RdL: quotient)		2								–	–	⑥	⑦	–	–	14
Logic Operations	AND.B #xx:8,Rd	B	Rd8∧#xx:8 → Rd8	2									–	–	↕	↕	0	–	2
	AND.B Rs,Rd	B	Rd8∧Rs8 → Rd8		2								–	–	↕	↕	0	–	2
	OR.B #xx:8,Rd	B	Rd8∨#xx:8 → Rd8	2									–	–	↕	↕	0	–	2
	OR.B Rs,Rd	B	Rd8∨Rs8 → Rd8		2								–	–	↕	↕	0	–	2
	XOR.B #xx:8,Rd	B	Rd8⊕#xx:8 → Rd8	2									–	–	↕	↕	0	–	2
	XOR.B Rs,Rd	B	Rd8⊕Rs8 → Rd8		2								–	–	↕	↕	0	–	2
	NOT.B Rd	B	Rd → Rd		2								–	–	↕	↕	0	–	2
Shift Operations	SHAR.B Rd	B			2								–	–	↕	↕	0	↕	2
	SHAL.B Rd	B			2								–	–	↕	↕	↕	↕	2
	SHLR.B Rd	B			2								–	–	0	↕	0	↕	2
	SHLL.B Rd	B			2								–	–	↕	↕	0	↕	2
	ROTXL.B Rd	B			2								–	–	↕	↕	0	↕	2
	ROTXR.B Rd	B			2								–	–	↕	↕	0	↕	2

Mnemonic		Operand Size	Operation	Addressing Mode/Instruction Length							Condition Code (CCR)						
				#xx:8/16 Rn	@Rn	@(d:16, Rn) @-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	Implied	I	H	N	Z	V	C	No. of States
	ROTL.B Rd	B		2							–	–	↕	↕	0	↕	2
	ROTR.B Rd	B		2							–	–	↕	↕	0	↕	2
Bit manipu-lation	BSET #xx:3,Rd	B	(#xx:3 of Rd8) ← 1	2							–	–	–	–	–	–	2
	BSET #xx:3, @ Rd	B	(#xx:3 of @Rd16) ← 1		4						–	–	–	–	–	–	8
	BSET #xx:3, @ aa:8	B	(#xx:3 of @aa:8) ← 1				4				–	–	–	–	–	–	8
	BSET Rn,Rd	B	(Rn8 of Rd8) ← 1	2							–	–	–	–	–	–	2
	BSET Rd,@ Rd	B	(Rn8 of @ Rd16) ← 1		4						–	–	–	–	–	–	8
	BSET Rn, @ aa:8	B	(Rn8 of @ aa:8) ← 1				4				–	–	–	–	–	–	8
	BCLR #xx:3,Rd	B	(#xx:3 of Rd8) ← 0	2							–	–	–	–	–	–	2
	BCLR #xx:3, @ Rd	B	(#xx:3 of @Rd16) ← 0		4						–	–	–	–	–	–	8

Mnemonic		Operand Size	Operation	Addressing Mode/Instruction Length								Condition Code (CCR)						
				#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16 @(d:8, PC)	@@aa	Implied	I	H	N	Z	V	C	No. of States
Bit manipulation	BCLR #xx:3, @ aa:8	B	(#xx:3 of @ aa:8) ← 0						4			–	–	–	–	–	–	8
	BCLR Rn,Rd	B	(Rn8 of Rd8) ← 0		2							–	–	–	–	–	–	2
	BCLR Rn, @ Rd	B	(Rn8 of @ Rd16) ← 0			4						–	–	–	–	–	–	8
	BCLR Rn, @ aa:8	B	(Rn8 of @aa:8) ← 0						4			–	–	–	–	–	–	8
	BNOT #xx:3,Rd	B	(#xx:3 of Rd8) ← (#xx:3 of Rd8)		2							–	–	–	–	–	–	2
	BNOT #xx:3, @ Rd	B	(#xx:3 of @ Rd16) ← (#xx:3 of @ Rd16)			4						–	–	–	–	–	–	8
	BNOT #xx:3, @ aa:8	B	(#xx:3 of @ aa:8) ← (#xx:3 of @ aa:8)						4			–	–	–	–	–	–	8
	BNOT Rn,Rd	B	(Rn8 of Rd8) ← (Rn 8 of Rd8)		2							–	–	–	–	–	–	2
	BNOT Rn, @ Rd	B	(Rn8 of @ Rd16 ← (Rn8 of @ Rd16)			4						–	–	–	–	–	–	8
	BNOT Rn, @ aa:8	B	(Rn8 of @ aa:8) ← (Rn8 of @ aa:8)						4			–	–	–	–	–	–	8
	BTST #xx:3,Rd	B	(#xx:3 of Rd8) → Z		2							–	–	–	↕	–	–	2
	BTST #xx:3, @ Rd	B	(#xx:3 of @ Rd16) → Z			4						–	–	–	↕	–	–	6
	BTST #xx:3, @ aa:8	B	(#xx:3 of @ aa:8) → Z						4			–	–	–	↕	–	–	6
	BTST Rn,Rd	B	(Rn8 of Rd8) → Z		2							–	–	–	↕	–	–	2
	BTST Rn, @ Rd	B	(Rn8 of @ Rd16) → Z			4						–	–	–	↕	–	–	6
	BTST Rn, @ aa:8	B	(Rn8 of @ aa:8) → Z						4			–	–	–	↕	–	–	6
	BLD #xx:3,Rd	B	(#xx:3 of Rd8) → C		2							–	–	–	–	–	↕	2
	BLD #xx:3, @ Rd	B	(#xx:3 of @ Rd16) → C			4						–	–	–	–	–	↕	6
	BLD #xx:3, @ aa:8	B	(#xx:3 of @ aa:8) → C						4			–	–	–	–	–	↕	6
	BILD #xx:3, Rd	B	(#xx:3 of Rd8) → C		2							–	–	–	–	–	↕	2
	BILD #xx:3, @ Rd	B	(#xx:3 of @ Rd16) → C			4						–	–	–	–	–	↕	6
	BILD #xx:3, @ aa:8	B	(#xx:3 of @ dd:8) → C						4			–	–	–	–	–	↕	6
	BST #xx:3,Rd	B	C → (#xx:3 of Rd8)		2							–	–	–	–	–	–	2
	BST #xx:3, @ Rd	B	C → (#xx:3 of @ Rd16)			4						–	–	–	–	–	–	8
	BST # xx:3, @ aa:8	B	C → (#xx:3 of @ aa:8)						4			–	–	–	–	–	–	8

Mnemonic	Operand Size	Operation	Addressing Mode/Instruction Length								Condition Code (CCR)						
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	Implied	I	H	N	Z	V	C	No. of States
BIST #xx:3,Rd	B	$\overline{C} \rightarrow$ (#xx:3 of Rd8)	2									–	–	–	–	–	–	2
BIST #xx:3, @ Rd	B	$\overline{C} \rightarrow$ (#xx:3 of @ Rd16)			4							–	–	–	–	–	–	8
BIST #xx:3, @aa:8	B	$\overline{C} \rightarrow$ (#xx:3 of @ aa:8)						4				–	–	–	–	–	–	8
BAND #xx:3,Rd	B	C∧(#xx:3 of Rd8) → C	2									–	–	–	–	–	↕	2
BAND #xx:3, @ Rd	B	C∧(#xx:3 of @ Rd16) → C			4							–	–	–	–	–	↕	6
BAND #xx:3, @aa:8	B	C∧(#xx:3 of @aa:8) → C						4				–	–	–	–	–	↕	6
BIAND #xx:3, Rd	B	C∧($\overline{\#xx:3 \text{ of } Rd8}$) → C	2									–	–	–	–	–	↕	2
BIAND #xx:3, @ Rd	B	C∧($\overline{\#xx:3 \text{ of } @Rd16}$) → C			4							–	–	–	–	–	↕	6
BIAND #xx:3, @aa:8	B	C∧($\overline{\#xx:3 \text{ of } @aa:8}$) → C						4				–	–	–	–	–	↕	6
BOR #xx:3,Rd	B	C∨(#xx:3 of Rd8) → C	2									–	–	–	–	–	↕	2
BOR #xx:3, @ Rd	B	C∨ (#xx:3 of @ Rd16) → C			4							–	–	–	–	–	↕	6
BOR #xx:3, @ aa:8	B	C∨ (#xx:3 of @ aa:8) → C						4				–	–	–	–	–	↕	6
BIOR #xx:3,Rd	B	C∨($\overline{\#xx:3 \text{ of } Rd8}$) → C	2									–	–	–	–	–	↕	2
BIOR #xx:3, @ Rd	B	C∨($\overline{\#xx:3 \text{ of } @Rd16}$) → C			4							–	–	–	–	–	↕	6
BIOR #xx3:, @ aa:8	B	C∨($\overline{\#xx3 \text{ of } @aa:8}$) → C						4				–	–	–	–	–	↕	6
BXOR #xx:3,Rd	B	C⊕(#xx:3 of Rd8) → C	2									–	–	–	–	–	↕	2
BXOR #xx:3, @ Rd	B	C⊕(#xx:3 of @ Rd16) → C			4							–	–	–	–	–	↕	6
BXOR #xx:3, @ aa:8	B	C⊕(#xx:3 of @ aa:8) → C						4				–	–	–	–	–	↕	6
BIXOR #xx:3, Rd	B	C⊕($\overline{\#xx:3 \text{ of } Rd8}$) → C	2									–	–	–	–	–	↕	2
BIXOR #xx:3, @ Rd	B	C⊕($\overline{\#xx:3 \text{ of } @Rd16}$) → C			4							–	–	–	–	–	↕	6
BIXOR #xx:3, @ aa:8	B	C⊕($\overline{\#xx:3 \text{ of } @aa:8}$) → C						4				–	–	–	–	–	↕	**6**

Mnemonic		Operand Size	Operation	Addressing Mode/Instruction Length								Condition Code (CCR)						
				#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	Implied	I	H	N	Z	V	C	No. of States
Branching	BRA(BT)	–	PC ← PC+:8							2			–	–	–	–	–	–	4
	BRN(BF)	–	Nothing changes.							2			–	–	–	–	–	–	4
	BHI	–	if true then PC ← PC+d:8 else next							2			–	–	–	–	–	–	4
	BLS	–								2			–	–	–	–	–	–	4
	BCC(BHS)	–								2			–	–	–	–	–	–	4
	BCS(BLO)	–								2			–	–	–	–	–	–	4
	BNE	–								2			–	–	–	–	–	–	4
	BEQ	–								2			–	–	–	–	–	–	4
	BVC	–								2			–	–	–	–	–	–	4
	BVS	–								2			–	–	–	–	–	–	4
	BPL	–								2			–	–	–	–	–	–	4
	BMI	–								2			–	–	–	–	–	–	4
	BGE	–								2			–	–	–	–	–	–	4
	BLT	–								2			–	–	–	–	–	–	4
	BGT	–								2			–	–	–	–	–	–	4
	BLE	–								2			–	–	–	–	–	–	4
	JMP @ Rn.	–	PC ← Rn16		2								–	–	–	–	–	–	4
	JMP @ aa:16	–	PC ← aa:16						4				–	–	–	–	–	–	6
	JMP @ @ aa:18	–	PC ← @ aa:8								2		–	–	–	–	–	–	8
	BSR	–	SP–2 → SP PC → @ SP PC ← PC+d:8							2			–	–	–	–	–	–	6
	JSR @ Rn	–	SP–2 → SP PC → @ SP PC ← Rn16		2								–	–	–	–	–	–	6
	JSR @ aa:16	–	SP–2 → SP PC → @ SP PC ← aa:16						4				–	–	–	–	–	–	8
	JSR @ @ aa:8	–	SP–2 → SP PC → @ SP PC ← @ aa:8								2		–	–	–	–	–	–	8
	RTS	–	PC ← @ SP SP+2 → SP									2	–	–	–	–	–	–	8

Mnemonic		Operand Size	Operation	Addressing Mode/Instruction Length								Condition Code (CCR)						
				#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	Implied	I	H	N	Z	V	C	No. of States
System control	RTE	–	CCR ← @ SP SP+2 → SP PC ← @ SP SP+2 → SP									2	↕	↕	↕	↕	↕	↕	10
	SLEEP	–	Suspends CPU operation to conserve power									2	–	–	–	–	–	–	2
	LDC #xx:8,CCR	B	#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
	LDC Rs,CCR	B	Rs8 → CCR		2								↕	↕	↕	↕	↕	↕	2
	STC CCR,Rd	B	CCR → Rd8		2								–	–	–	–	–	–	2
	ANDC #xx:8,CCR	B	CCR∧#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
	ORC #xx:8,CCR	B	CCR∨#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
	XORC #xx:8,CCR	B	CCR⊕#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
	NOP	–	Nothing changes.									2	–	–	–	–	–	–	2

Notes: The number of states assume that both the instruction and the operands are in the onboard memory

① This bit is `1' if the instruction results in a carry or borrow between bits, 11 and 12; `0' otherwise.

② This bit remains unaffected if all bits in the result are zero. Otherwise, it is cleared to `0'.

③ This bit is `1' if the decimal adjustment instruction results in a carry. Otherwise, it remains unaffected.

④ If n is the number in R4L, the instruction executes in 4n+8 clock cycles. The upper limit for the H8/310 Series is 5 ms.

⑤ It is not possible to give the number of clock cycles for data transfers synchronized with the E clock.

⑥ Set to 1 if the divisor is negative; otherwise cleared to 0.

⑦ Cleared to 0 if the divisor is not zero; undetermined when the divisor is zero.

Number of States Required for Execution

The number of states required for execution in the preceding Table assume that both the instruction and the operands are in the onboard memory. The next Table gives the correction factors to be added when these are in on-chip supporting modules or external memory.

Access Conditions			Correction (Clock Cycles)	
Operand		On-chip supporting module	Byte data	1
			Word Data	4
		External Address	Byte data	1 + m
			Word data	4 + 2m
Instruction	Other than branch instruction	External Address	2-byte instruction	4 + 2m
			4-byte instruction	8 + 4m
	Branch instruction		2-byte instruction	8 + 4m
			4-byte instruction	

Note: m denotes the number of wait states for external memory access.

Abbreviations & Notations for Operation Column

Abbreviation/Notation	Description
PC	Program counter
SP	Stack pointer (R7)
CCR	Condition code register
Z	Zero flag (Z in CCR)
C	Carry flag (C in CCR)
Rs, Rd, Rn	General register: 8-bit (R0H to R7H and R0L to R7L) or 16-bit (R0 to R7)
d:8, d:16	Displacement: 8- or 16-bit
#xx:3/8/16	Immediate data: 3-, 8-, or 16-bit
→	Data transfer from left to right
+	Addition of the two operands
–	Subtraction of the right operand from the left one
x	Multiplication of the two operands
÷	Division of the left operand by the right one
∧	Logical product (AND) of the two operands
∨	Logical sum (OR) of the two operands
⊕	Exclusive OR (XOR) of the two operands
¬	One’s complement bit inversion
( ) < >	Contents at effective address

Notations for Condition Code Columns

Notation	Description
↕	Set according to the result
*	Undefined (Indeterminate)
0	Always set to `0’
--	Unaffected by the result

2.6 Basic Bus Timing

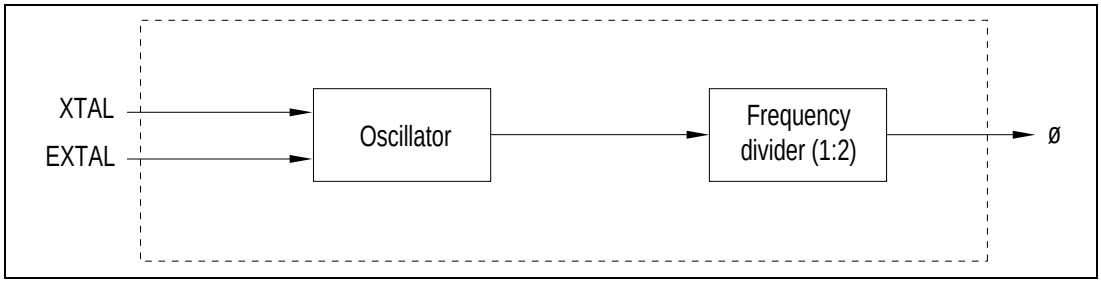
H8/300 Series timing is relative to the system clock. One complete cycle of the system clock is called a state, and bus cycles are two or three such cycles long. The onboard memory, on-chip supporting modules, and external devices have different access methods.

Basic Clock Timing

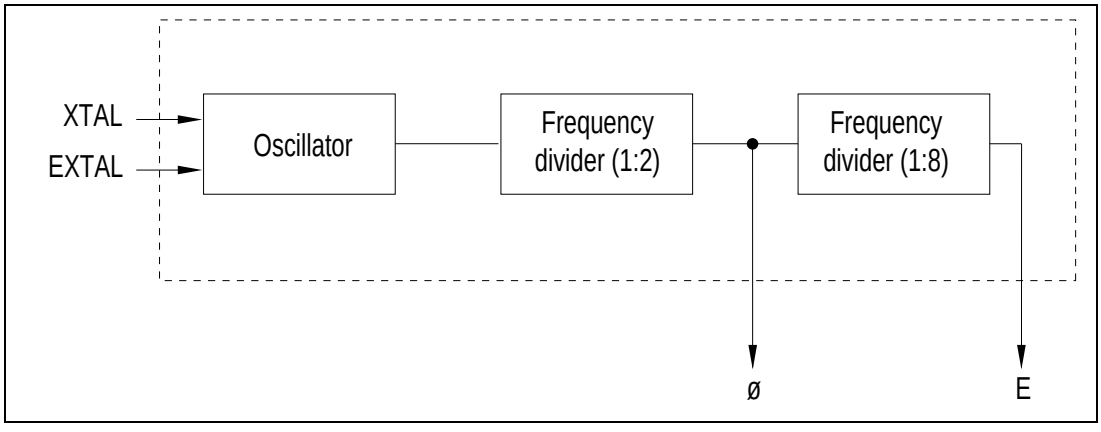
The system clock comes from either an external clock signal supplied to the EXTAL pin or a crystal oscillator connected across the XTAL and EXTAL pins.

The oscillator circuit varies with the H8/300 version.

- Type 1: H8/310, H8/329, H8/350, H8/3314, H8/338, and H8/3334 Series
  The chip divides the oscillator frequency in half to generate the system clock supplied to the CPU and onboard components.

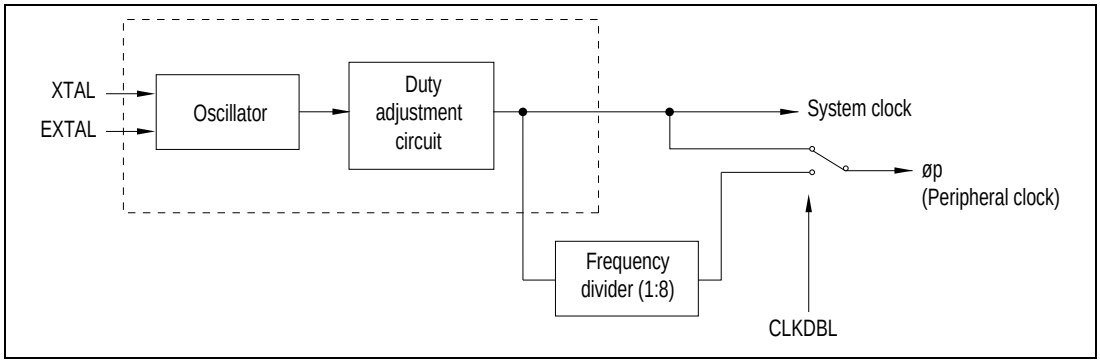


- Type 2: H8/325 and H8/330 Series
  The chip first divides the oscillator frequency in half to generate the system clock supplied to the CPU and onboard components and then divides the system clock by eight to generate the E clock.



- Type 3:H8/3297, H8/3337, H8/3397, and H8/3437 Series

  The system clock is the same frequency as the oscillator output. Software controls, via the CLKDBL bit, whether the onboard peripherals use the same frequency or half that.

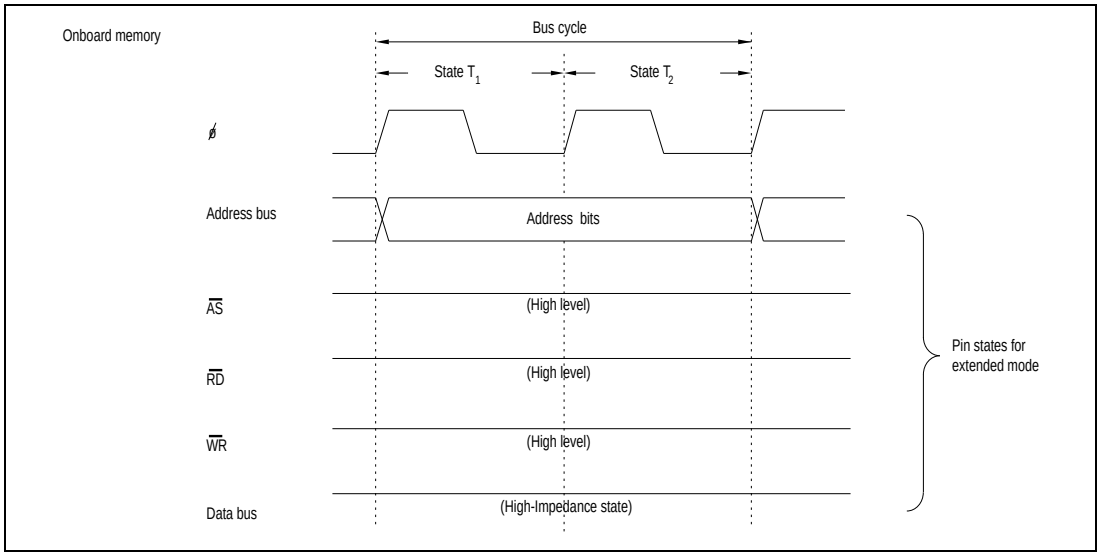


CPU Read & Write Cycles

H8/300 Series timing is relative to the system clock. One complete cycle of the system clock is called a state, and basic bus cycles are two or three such cycles long. These cycles differ depending on what is being accessed--onboard memory, on-chip supporting modules, or external devices.

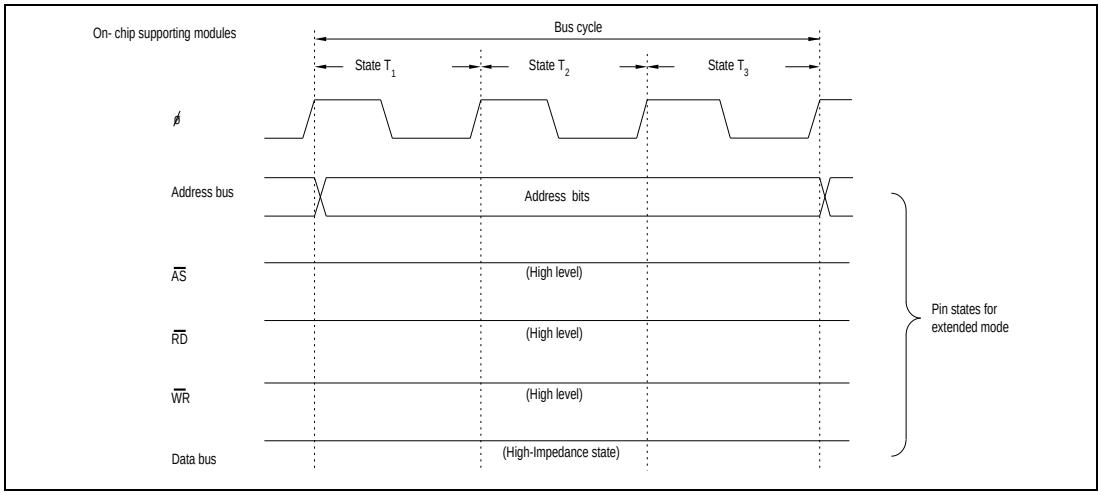
- Address access timing for onboard memory (RAM and ROM)

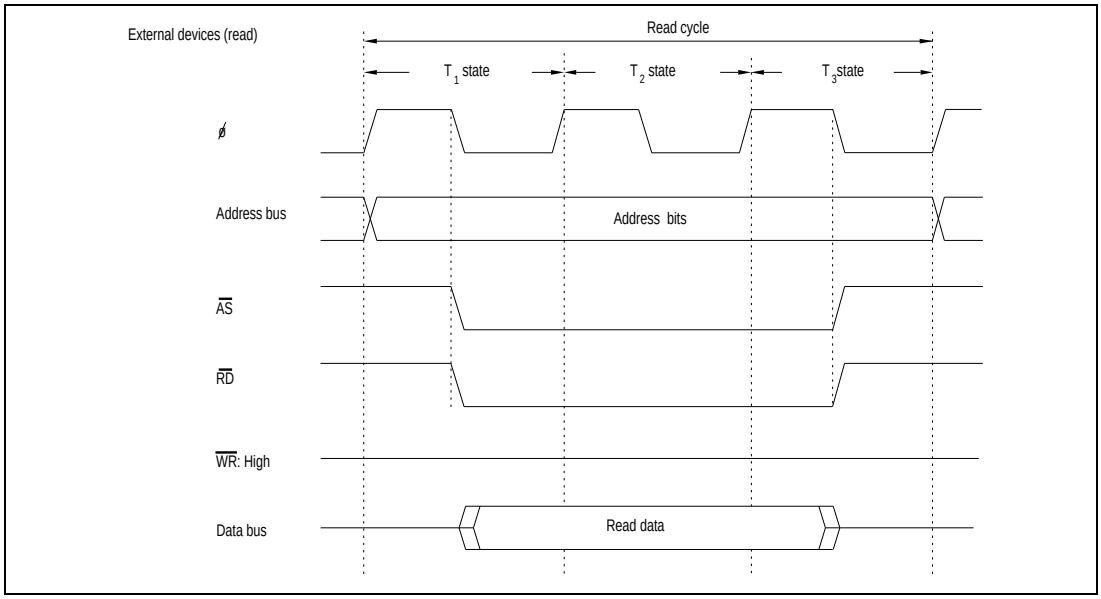
  Access to onboard memory takes two clock cycles. The data bus is 16 bits wide, permitting access by either byte or word.

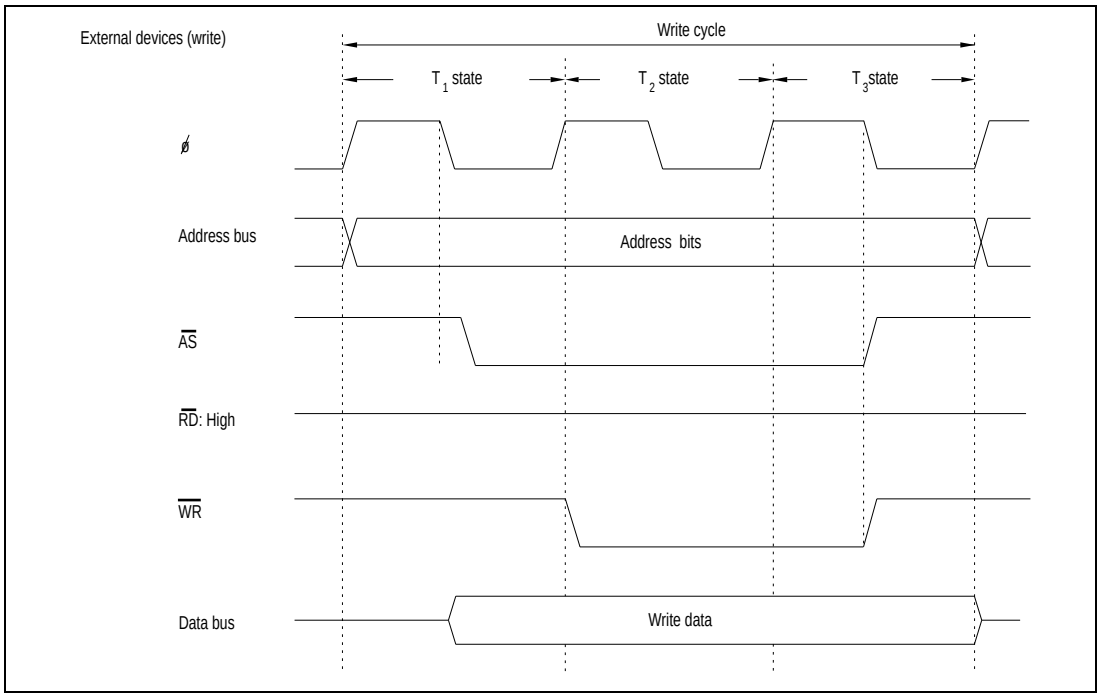


- Address access timing for on-chip supporting modules and external devices

  Access here takes three clock cycles. The data bus in only 8 bits wide, so word-sized data and instructions have to be fetched one byte at a time.

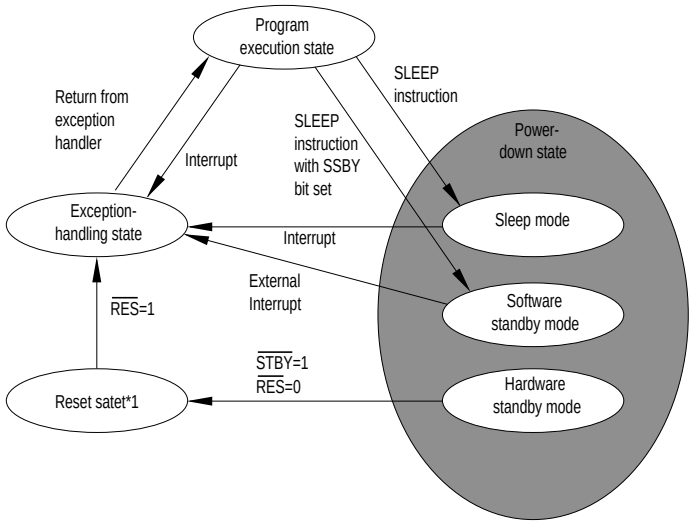





External devices (write)
Write cycle
T1 state
T2 state
T3state
ø
Address bus
Address bits
AS
RD: High
WR
Data bus
Write data

2.7 Processing States

The CPU has four main processing states: reset, program execution, exception-handling, and power-down state.



Notes: 1. With the exception of the hardware standby mode, pulling the $\overline{RES}$ pin low (to `0') switches to the reset state.
2. In all states, pulling the $\overline{STBY}$ pin low (to '0') switches to the hardware standby mode.

Reset State

This is the state that the CPU starts off in after a reset.

Program-Handling State

In this state, the CPU sequentially executes instructions.

Exception-Handling State

The CPU passes through this transitional state when a reset, interrupt, or other type of exception changes the execution flow. It pushes the program counter (PC) and condition code register (CCR) onto the stack indicated by the stack pointer (SP).

Power-Down State

In this state, the CPU shuts down to save power. There are three modes available: sleep mode, software standby mode, and hardware standby mode.

- Sleep Mode

  If the software standby bit (SSBY) is `0', the SLEEP instruction sends the CPU into the sleep mode, suspending CPU operation, but preserving the contents of the internal registers. Onboard peripherals and other chip components remain operational.

  The CPU remains in the sleep mode until it receives a reset signal or interrupt. It then returns to the program execution state via the exception-hundling state.

- Software Standby Mode

  If the software standby bit (SSBY) is `1', the SLEEP instruction sends the CPU into the software standby mode, shutting down the CPU, onboard peripherals, oscillator, and other components, but preserving the contents of the internal registers and RAM as well as the I/O port states.

  The CPU remains in the software standby mode until it receives an external interrupt. It gives the oscillator time to stabilize and then returns to the program execution state via the exception-handling state.

  Shutting down the oscillator allows this mode to save considerable amounts of power.

- Hardware Standby Mode

  Pulling the $\overline{\text{STBY}}$ pin low (to`0') switches to the hardware standby mode, which, like the software standby mode, shuts down the CPU, onboard peripherals, oscillator, and other components, but preserves the contents of the internal registers and RAM. The CPU remains in the hardware standby mode until the $\overline{\text{RES}}$ pin is pulled low (to `0') and the $\overline{\text{STBY}}$ pin returns to high (to `1'). It then restarts via the reset state.

As was the case with the software standby mode above, shutting down the oscillator allows this mode to save considerable amounts of power.

Mode	System Clock	CPU	Onboard Peripherals	Onboard RAM and CPU Registers	Exit Methods	
Sleep mode	Operational	Suspended	Operational	Preserved	Interrupt:	The CPU starts by processing the interrupt.
					$\overline{\text{RES}}$:	The CPU restarts in the reset state.
					$\overline{\text{STBY}}$:	The CPU switches to the hardware standby mode.
Software standby mode	Suspended	Suspended	Suspended	Preserved	External Interrupt:	The system clock generator circuit restarts, a timer waits the specified time for CPU starts by processing the interrupt.
					$\overline{\text{RES}}$:	After the system clock generator circuit has stabilized, the CPU restarts in the reset state.
					$\overline{\text{STBY}}$:	The CPU switches to the hardware standby mode.
Hardware standby mode	Suspended	Suspended	Suspended	Preserved	Pulling the $\overline{\text{RES}}$ pin low (to `0'), restoring the $\overline{\text{STBY}}$ pin to high (to `1'), and, after allowing sufficient time for the system clock generator circuit to stabilize, restoring the $\overline{\text{RES}}$ pin to high (to `'1) restarts the CPU via the reset state.	

2.8 Exception-Handling State

The CPU recognizes two types of exceptions: resets and interrupts. Resets have the highest priority. Interrupts are processed in order of decreasing priority.

The CPU starts processing an exception by pushing the program counter (PC) and condition code register (CCR) onto the stack indicated by the stack pointer (SP). It skips this step for resets. It then sets the interrupt mask bit (I) in the condition code register (CCR) to `1' and loads the program counter (PC) from the exception vector table.

Resets have the highest priority of all exceptions. If there are several interrupts outstanding, the CPU processing them in order of decreasing priority.

Priority	Exception Type	Trigger
1	Reset	Reset processing begins when the $\overline{\text{RES}}$ pin switches from low (`0') to high(`1').
2	Interrupt	Interrupt processing begins once the current executing instruction or interrupt handler finishes executing.

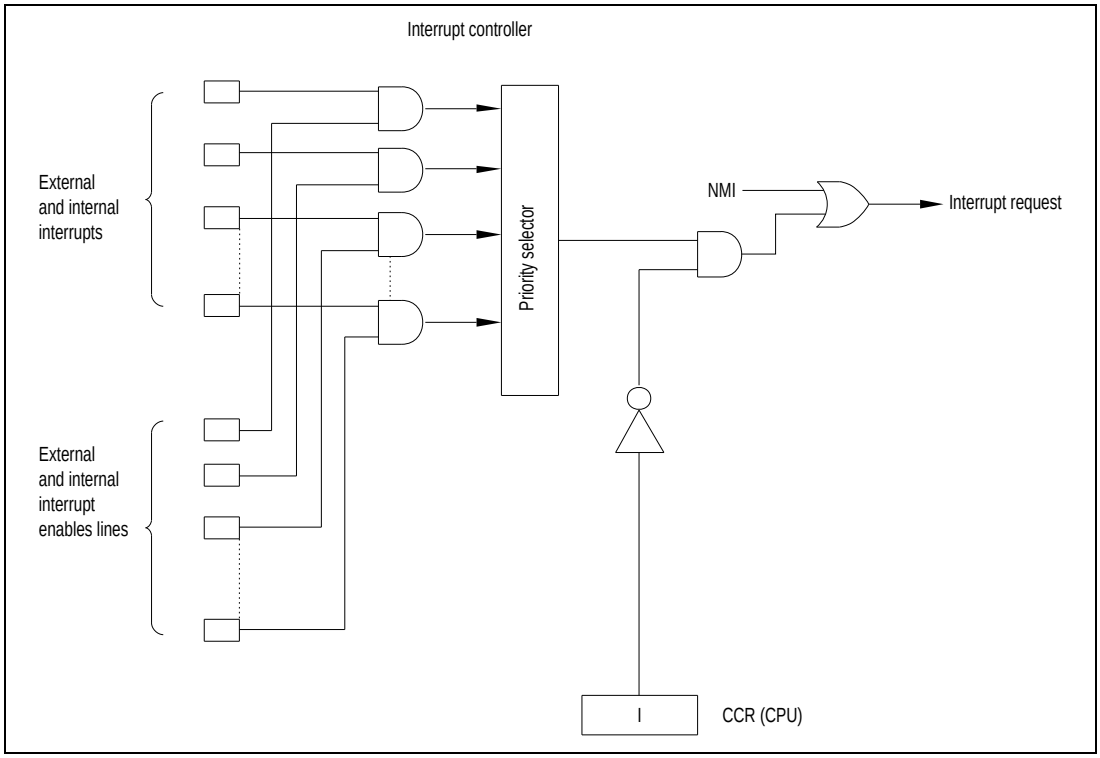
Note: Interrupts received during an ANDC, ORC, XORC, or LDC instruction are ignored.

Interrupt Processing

There are two types of interrupts: external ones from the interrupt pins and internal ones from onboard peripheral modules. The non-maskable interrupt has the highest priority of all and, as the name suggests, is always enabled. All others, whether external or internal, can be disabled via the interrupt mask bit (I) in the condition code register (CCR). Setting this bit to `1' masks all interrupts except NMI. Each interrupt is assigned its own interrupt vector.

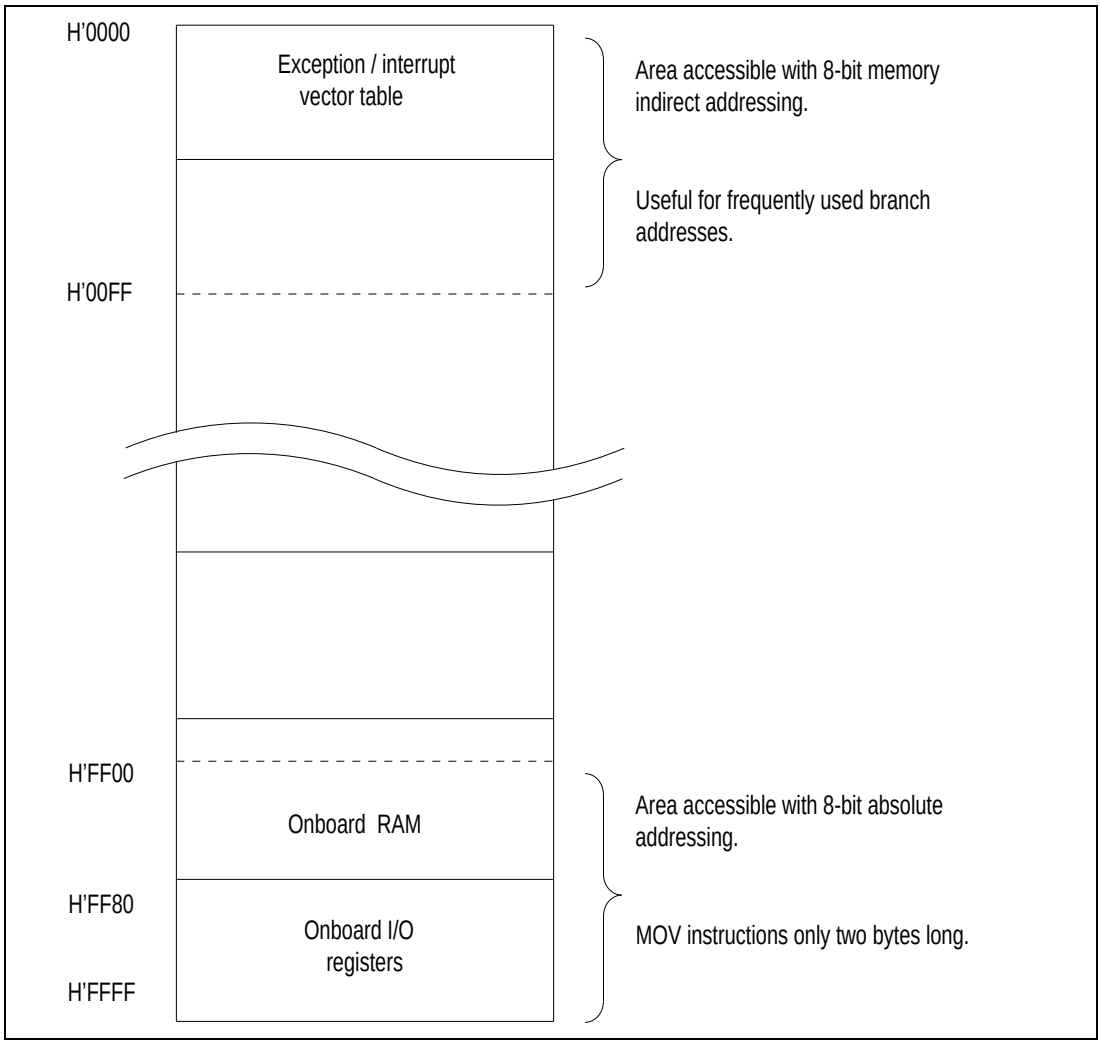
The interrupt controller is in charge of managing interrupts. If there are several interrupts outstanding, it passes the one with the highest priority on to the CPU and retains the others. The CPU responds to an interrupt by pushing the program counter (PC) and condition code register (CCR) onto the stack indicated by the stack pointer (SP) and branching to the interrupt service routine whose address is in the interrupt vector table.

Interrupt Controller Block Diagram



2.9 Memory Map

The H8/300 Series offers shorthand 8-bit addressing access to both ends of its 64-kilobyte address space: 8-bit memory indirect addressing for H'0000 through H'00FF and 8-bit absolute addressing for H'FF00 through H'FFFF. These addressing modes make instructions shorter and code more compact.



8-Bit Memory Indirect Addressing (H'0000-H'00FF)

The H8/300 Series reserves part of the ROM area for its exception/interrupt vector table. The mapping between interrupts and vectors varies between Series members. For further details, refer to the relevant hardware manual.

Overlapping this table in the address space is a 256-byte region (H'0000 through H'00FF) accessible with the H8/300 Series' 8-bit memory indirect addressing. Storing frequently used branch addresses here for access with the shorter, memory indirect addressing forms of branch commands is one way of reducing code size.

8-Bit Absolute Addressing (H'FF00-H'FFFF)

MOV and other H8/300 Series instructions support 8-bit absolute addressing versions that permit rapid access to a 256-byte region at the end of memory (H'FF00 through H'FFFF) using shorter instructions for code that is more compact.

The CPU maps the lower half (H'FF00 through H'FF7F) of this region to part of the onboard RAM and the upper half (H'FF80 through H'FFFF) to the onboard I/O registers so that 8-bit absolute addressing is available to speed up data handling in and between these two key regions.

2.10 Operating Modes

The H8/300 Series offers a choice of up to three operating modes, selected with the mode pins MD0 and MD1. Not all members offer all three, however.

Mode1: Enhanced Mode with Onboard ROM Disabled

This mode configures the address bus, data bus, and bus control pins doubling as I/O ports for accessing external memory and peripheral devices.

It disables the onboard ROM, freeing the corresponding addresses for external use.

The total address spaces available for internal and external devices is 64 kilobytes.

Mode 2: Enhanced Mode with Onboard ROM Enabled

This mode also enhances the chip for use with external devices, but after a reset leaves the address bus as input ports. Software must switch the individual data direction register (DDR) bits to enable address output.

This mode supports the same type of access to external devices as Mode 1 except for addresses occupied by the onboard ROM.

The total address spaces available for internal and external devices is 64 kilobytes.

Mode3: Single-Chip Mode

This mode, for stand-alone operation, does not support external addressing. The only memory devices are the onboard ones--ROM, RAM, and I/O registers--and the relevant pins are all I/O ports.

Section 3 Onboard Memory, Data Transfer Unit, and Bus Controller

3.1 Onboard Memory

H8/300 Series members contain between 256 bytes and 2 kbytes of Ram and between 8 and 60 kbytes of ROM. The H8/310 Series adds 8 kbytes of EEPROM; the H8/3334YF, H8/3434F, and others, 32 kbytes of flash memory.

3.1.1 ROM

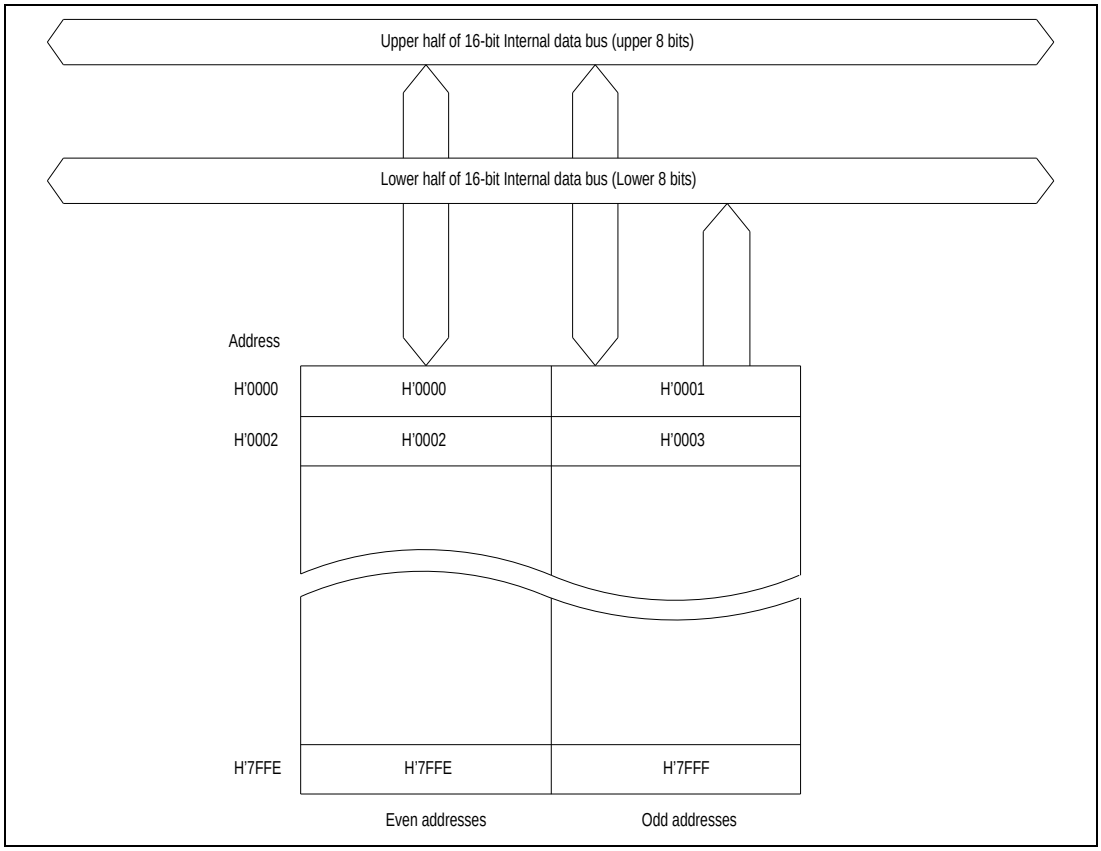
H8/300 Series members contain between 8 and 60 Kbytes of ROM in the form of masked ROM, PROM, or flash memory. This memory is connected to the CPU's 16-bit data bus for access as either bytes or words in only two clock cycles.

Special socket adapters for the ZTAT™ (PROM) and F-ZTAT™ (flash memory) versions change the pin configurations so that the user can download programs and data to them using a standard PROM writer. The latter type also supports onboard programming--that is, reprogramming the chip while it is still in place in the application system.

The H8/300 Series reserves part of the ROM area for its exception/interrupt vector table. The mapping between interrupts and vectors varies between Series members. For further details, refer to the relevant hardware manual.

Overlapping this table in the address space is a 256-byte region (H'0000through H'00FF) accessible with the H8/300 Series' 8-bit memory indirect addressing. Storing frequently used branch addresses here for access with the shorter, memory indirect addressing forms of branch commands is one way of reducing code size.

Block Diagram for 32 k ROM Version



3.1.2 Flash Memory

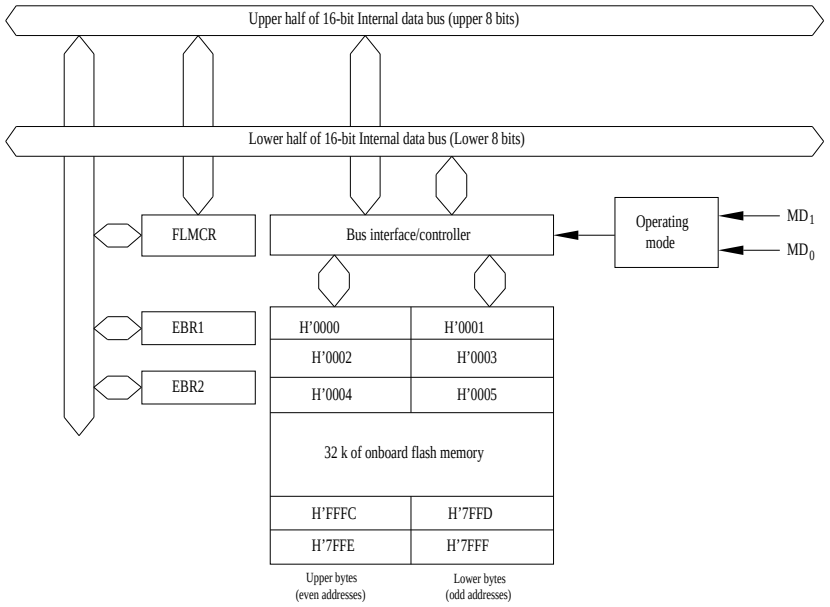
The H8/3334YF-ZTAT™ and H8/3434F-ZTAT™ Series include 32 kbytes of flash memory.

This memory is connected to the CPU's 16-bit data bus for access as either bytes or words in only two clock cycles. However, only byte data can be used when writing data to flash memory.

Modifying the pin configuration with a special socket adapter enables the onboard flash memory to be written to, erased, and verified using a standard PROM writer. Data can also be read, written, erased, or verified from off-chip after the chip has been mounted on the board, using the previously prepared boot mode procedure or a user-programmed procedure.

The flash memory address space is divided into a number of blocks, and specific blocks can be designated for erasure according to the contents of the erase block specification register.

Block Diagram



Legend:

FLMCR: Flash memory control register (8-bit)
EBR1: Erase block specification register 1 (8-bit)
EBR2: Erase block specification register 2(8-bit)

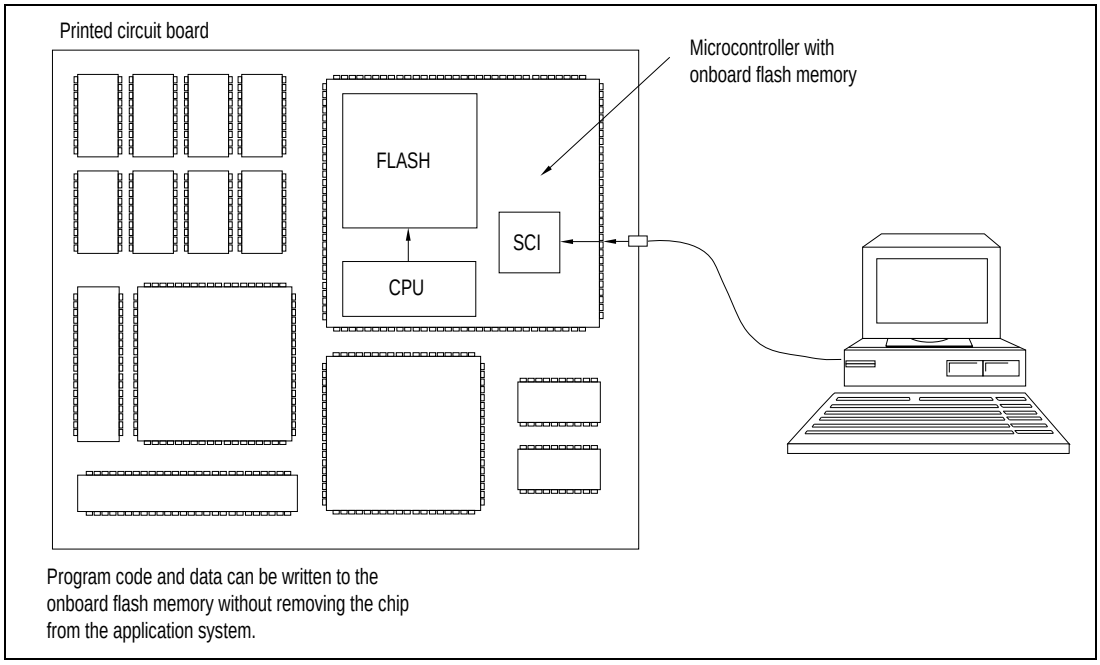
Writing/Erasing Flash Memory

There are two ways to write data to the flash memory: in place from the CPU with onboard programming or with a standard PROM writer.

- Onboard programming

  The H8/3334YF-ZTAT™ and H8/3434F-ZTAT™ Series onboard programming--that is, reprogramming the chip while it is still in place in the application system--when a 12.0.-V voltage is connected across the FVPP and STBY pins.

  The user program must first copy the software for reprogramming the chip from the F-ZTAT™, however.

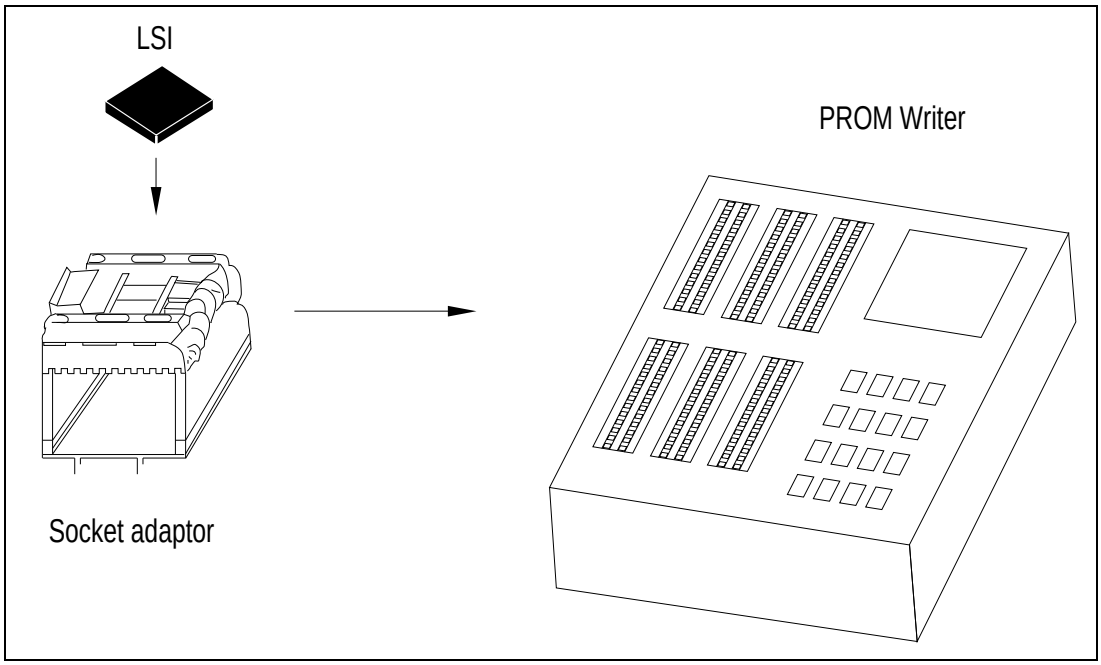


Onboard Programming

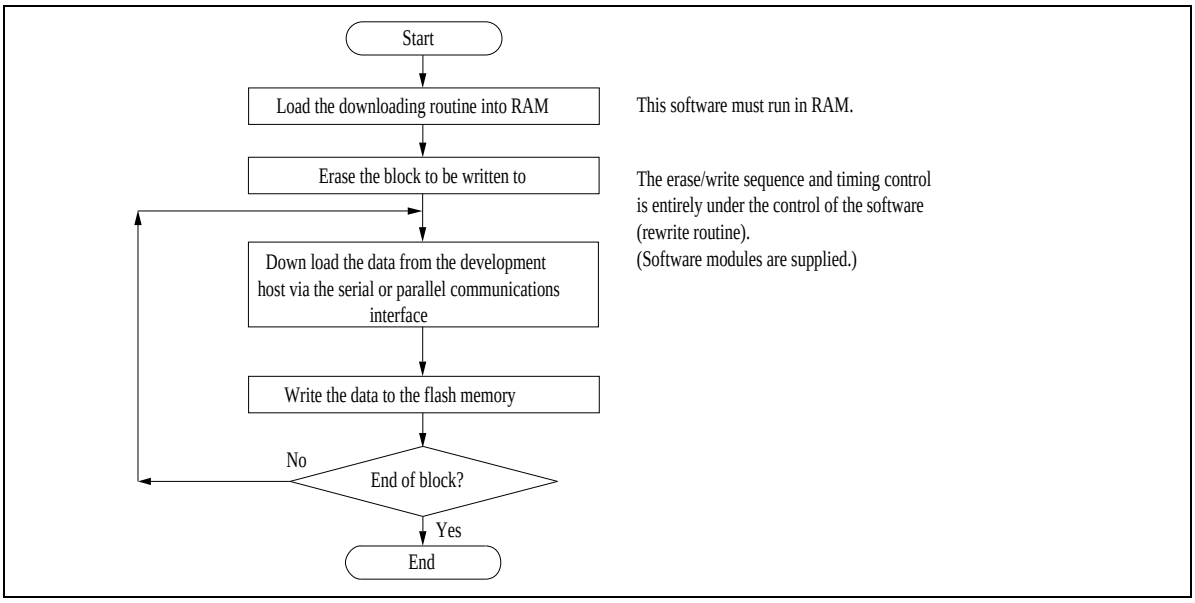
- Using a PROM writer

  Setting the H8/3334YF-ZTAT™ or H8/3434F-ZTAT™ Series chip to flash memory mode enables direct writing to the chip.

  Special socket adapters change the pin configurations so that the user can reprogram the flash memory using a standard PROM writer. Software can then write, erase, and verify this onboard flash memory with procedures matching the NH27F101 specifications.



PROM Writer and Socket Adapter


Start
Load the downloading routine into RAM
This software must run in RAM.
Erase the block to be written to
The erase/write sequence and timing control is entirely under the control of the software (rewrite routine).
(Software modules are supplied.)
Down load the data from the development host via the serial or parallel communications interface
Write the data to the flash memory
No
End of block?
Yes
End

3.1.3 RAM

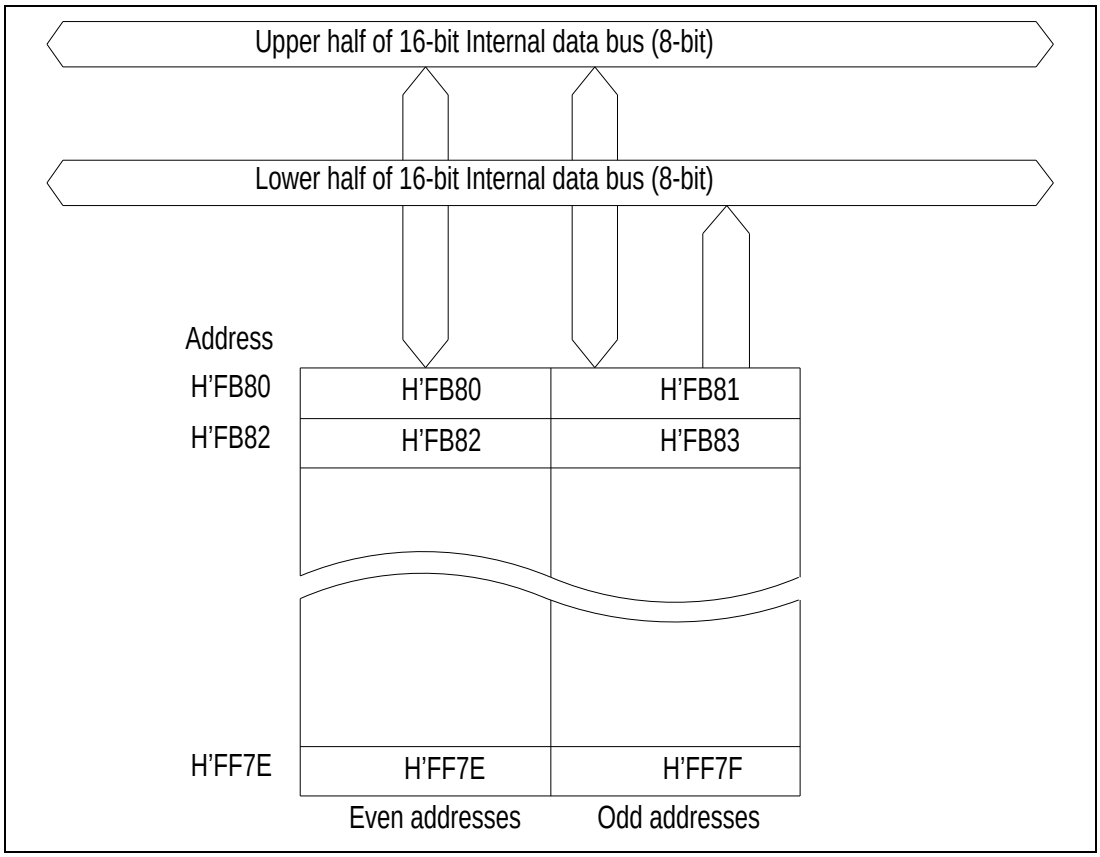
H8/300 Series members contain between 256 bytes and 2 kbytes of RAM.

This memory is connected to the CPU's 16-bit data bus for access as either bytes or words in only two clock cycles.

MOV and other H8/300 Series instructions support 8-bit absolute addressing versions that permit rapid access to a 256-byte region at the end of memory (H'FF00 through H'FFFF) using shorter instructions for code that is more compact.

The CPU maps the lower half (H'FF00 through H'FF7F) of this region to part of the onboard RAM so that 8-bit absolute addressing is available to speed up data handling in this region.

Block Diagram for 1 k RAM Version



3.1.4 EEPROM

The H8/310 Series adds 8 kbytes of EEPROM.

This memory lies within the CPU's onboard memory area and is accessible in the same two clock cycles as RAM and ROM.

This EEPROM may be used for either program code or data.

Features

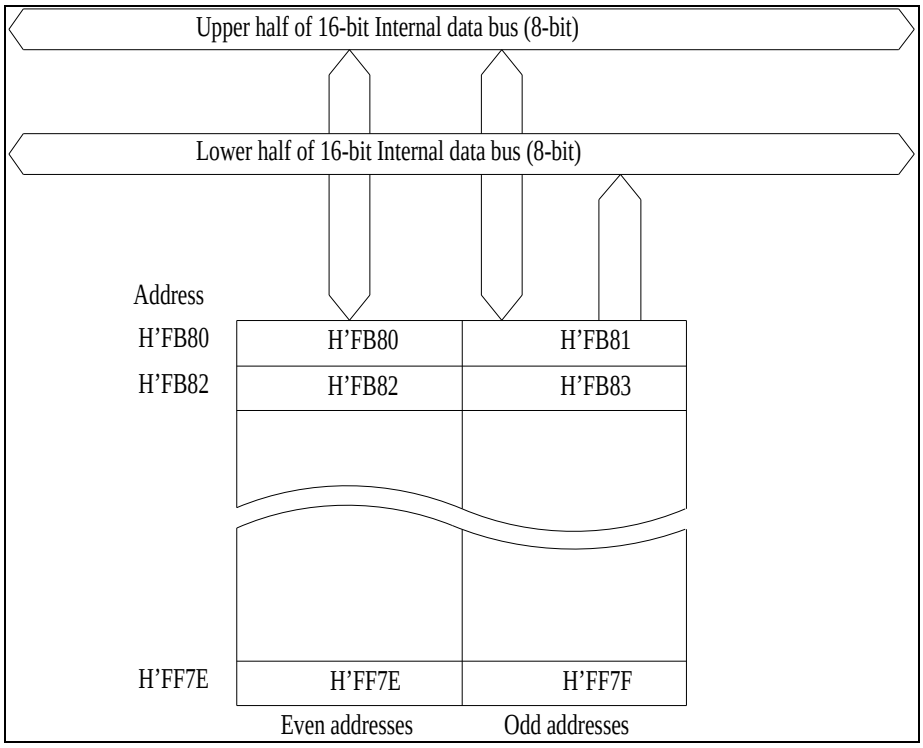
- Capacity of 8 kbytes
  - — Configured as 256 with 32 bytes each
  - — Located within the CPU's onboard memory area
- CPU instructions for rewriting contents
  - — EEPMOV instruction for writing/erasing contents
  - — Writing/erasing up to 32 bytes in the same page at a time
- Write/erase disable function
  - — Protective feature for data security
- Built-in-high-voltage circuit
  - — This circuit provides the voltage required to write/erase EEPROM contents.

Writing/Erasing

The CPU provides a special instruction, EEPMOV, for writing/erasing EEPROM contents.

This block transfer instruction takes its parameters from the R4L, R5, and R6 registers. Once these, the EEPROM control register (ECR), and the EEPROM protect register (EPR) have been set up, executing the EEPMOV instruction writes, overwrites, or erases EEPROM pages.

Block Diagram for 1 k RAM Version



3.2 E Clock Interface

H8/300 Series members provide two data transfer instructions with E clock synchronization (MOVTPE and MOVFPE) plus an E clock output pin. Together, these simplify the task of interfacing with peripheral devices requiring input with E clock synchronization.

Versions with Feature

H8/325 Series and H8/330

Functions

Interfacing with peripheral devices requiring input with E clock synchronization

Features

- E clock pin supplies E clock output with a frequency one-eight the system clock.
- Two data transfer instructions with E clock synchronization:
  - MOVTPE: Moves general address contents to an external memory location (on a peripheral chip) in synchronization with the E clock.
  - MOVFPE: Moves external memory contents (on a peripheral chip) to a general register in synchronization with the E clock.

3.3 Wait State Controller

H8/300 Series members support interfaces with low-speed external devices by inserting wait states in the bus cycle with either a pin wait function or an onboard wait state controller (WSC). The latter permits wait state control with software or pin inputs.

Versions with Feature

The following Series include onboard wait state controllers: H8/3297, H8/3397, H8/3337, and H8/3437.

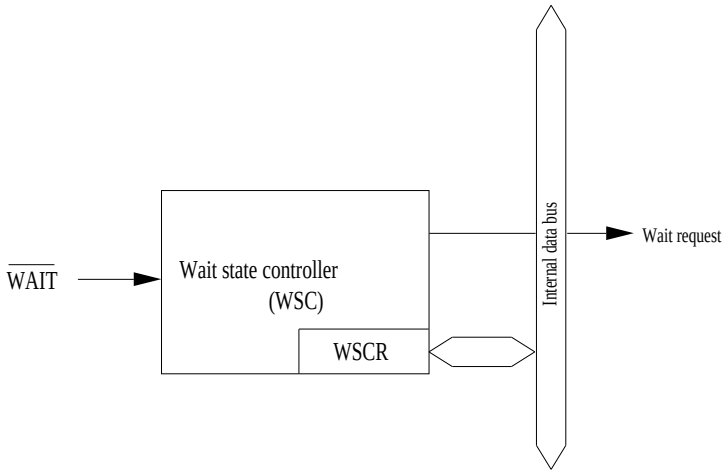
Functions

The controller inserts wait states between the T2 and T3 portions of the bus cycle so as to extend the latter for interfacing with low-speed external devices.

Features

- Choice of three operating modes:
  - Programmable wait mode
  - Pin wait mode
  - Pin auto wait mode
- Choice of 0, 1, 2, or 3 wait states
  - The pin wait mode boosts the number of wait states to 4 or more when the WAIT pin is pulled low (to ‘0’).

Block Diagram



Legend:
WSCR: Wait state controller register

3.4 Data Transfer Unit

The H8/3314 adds a 4-channel data transfer unit supporting direct memory access transfers and an 8-bit parallel buffer interface. Together, these two provide external devices easy read/write access to up to 256 bytes of onboard RAM as dual-port RAM. (See Section 4.1 “DPRAM and DPRAM Function.”)

Versions with Feature

H8/3314

Functions

- Single-address PBI transfers over the R channel
- Choice of PBI or I/O transfers over channels A and B
- Dual-address I/O transfers over the C channel

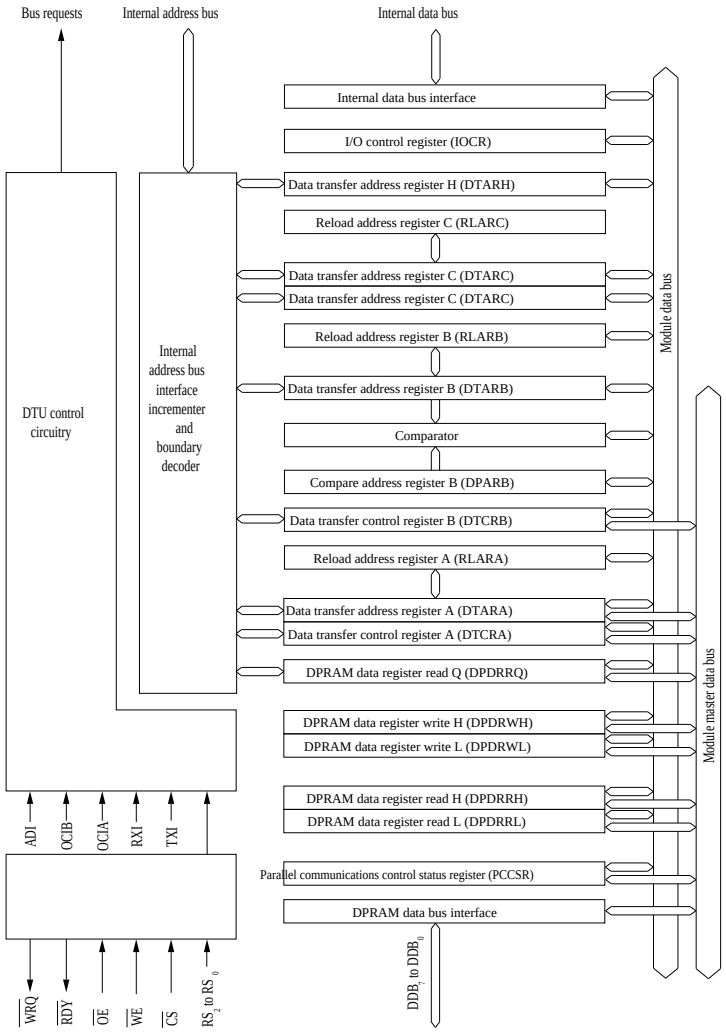
Features

- I/O transfers
  - — Channels A, B, and C support independent I/O transfers
  - — I/O transfer sources and destinations supported include the serial communications interface, the 16-bit free-running timer, programmable timing pattern controller, and analog-to-digital converter data registers.
  - — The number of bytes to transfer is determined from the starting address and the specified boundary.
  - — Transfers can access up to 256 bytes of RAM, but only 128 bytes per channel.
  - — Repeat mode available.
  - — Ring buffer (FIFO) mode∗ available for channel B.
  - — Transfer signals completion with a data transfer interrupt (DTIA, DTIB, or DTIC).

Note: ∗ This mode cyclically stores the transferred data in a ring buffer in FIFO order with the size determined from the boundary.

- PBI transfer DPRAM mode
  - The master CPU can access up to 256 bytes of the onboard RAM as dual-port RAM.
  - DPRAM query buffer mode permits random access by the master CPU to a single byte at the specified address via the R channel.
  - DPRAM bound buffer mode permits sequential read and write access by the master CPU to bytes at the specified address via the channels A and B, respectively.
  - DPRAM direct word mode permits direct access to register pairs DPDRRH & DPDRRL and DPDRWH & DPDRWL as 2-byte onboard dual-port RAM buffers, one each for reads and writes.
  - Transfers signals completion with a memory write end interrupt (MWEI), memory read end interrupt (MREI), or overrun error interrupt (CMP).
  - The mode signals the master CPU of interrupt and wait requests with the $\overline{\text{RDY}}$ and $\overline{\text{WRQ}}$ pins respectively.
- PBI transfer handshake mode
  - Handshaking available via the bus control signals $\overline{\text{OE}}$, $\overline{\text{WE}}$, $\overline{\text{RDY}}$, and $\overline{\text{WRQ}}$.
  - The rising edges of $\overline{\text{OE}}$ and $\overline{\text{WE}}$ trigger onboard CPU interrupts indicating the completion of output data processing and the confirmation of input data, respectively.
  - The mode signals the master CPU of interrupt and data I/O requests with the $\overline{\text{RDY}}$ and $\overline{\text{WRQ}}$ pin respectively.

Block Diagram



Legend:

IOCR: I/O control register
DTARH: Data transfer address register H
RLARC: Reload address register C
DTARC: Data transfer address register C
DTCRC: Data transfer control register C
RLARB: Reload address register B
DTARB: Data transfer address register B
DPARB: Compare address register B
DTCRB: Data transfer control register B
RLARA: Reload address register A
DTARA: Data transfer address register A
DTCRA: Data transfer control register A
DPDRRQ: DPRAM data register read Q
DPDRWH: DPRAM data register write H
DPDRWL: DPRAM data register write L

PCCSR: Parallel communications control status register
TXI, RXI, OCIA, OCIB, ADI: Interrupt requests from peripherals
RS2 TO RS0: Register select inputs
$\overline{CS}$: Chip select input
$\overline{WE}$, $\overline{OE}$, $\overline{RDY}$, $\overline{WRQ}$: Bus control signals

Section 4 Parellel and Serial Interfaces

4.1 Onboard DPRAM and DPRAM via DTU

H8/300 Series members provide 15 bytes of dual-port RAM accessible to both the onboard CPU and external devices. The single-chip mode supportsits use for parallel communications with a master CPU.

Setting the H8/3314 onboard data transfer unit to its PBI transfer DPRAM mode, on the other hand, allows the master CPU to access up to 256 bytes of the onboard RAM as dual-port RAM.

4.1.1 H8/330 Onboard DPRAM

Versions with Feature

H8/330 Series (15 bytes)

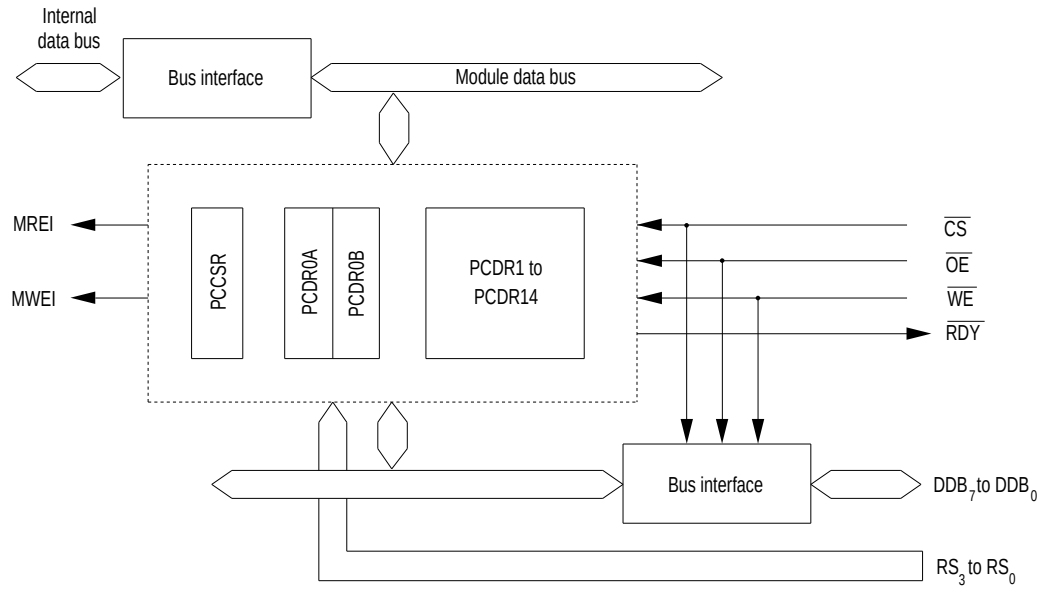
Functions

- In a master-salve configuration with the H8/300 Series member as the slave, this dual-port RAM provides parallel communications between the two devices over an 8-bit data bus.

Features

- Fifteen byte-sized data registers
- Standard memory interface--to simplify connection to the external CPU
- Simple protocol for managing communications between the master and salve
- Interrupt requests for master CPU

Block Diagram



Legend:

PCCSR: PCCSR: Parallel communications control/status register (8-bit)

PCDR0 to PCDR14: PCDR0 to PCDR14: Parallel communications data registers 0 to 14 (8-bit)

4.1.2 DPRAM via DTU/PBI

Versions with Feature

H8/3314

Functions

- The DTU DPRAM modes use the data transfer unit and parallel buffer interface together to provide external devices read/write access to up to 256 bytes of on board RAM as dual-port RAM.
- There are three such modes: query buffer mode, bound buffer mode, and direct word mode.

Features

- DPRAM query buffer mode

This parallel interface uses PBI transfer over DTU channel R to permit random read access by the master CPU to any byte within up to 256 bytes of onboard RAM.

A write by the master CPU to DPDRRQ sets the QREF flag to `1', triggering a DTU channel R transfer request from the byte in onboard RAM whose address is formed using DTARH as the upper half and DPDRRQ as the lower to DPDRRQ. Once the transfer is complete, and the QREF flag reset to `0', the master CPU reads the contents of DPDRRQ.

- DPRAM bound buffer mode

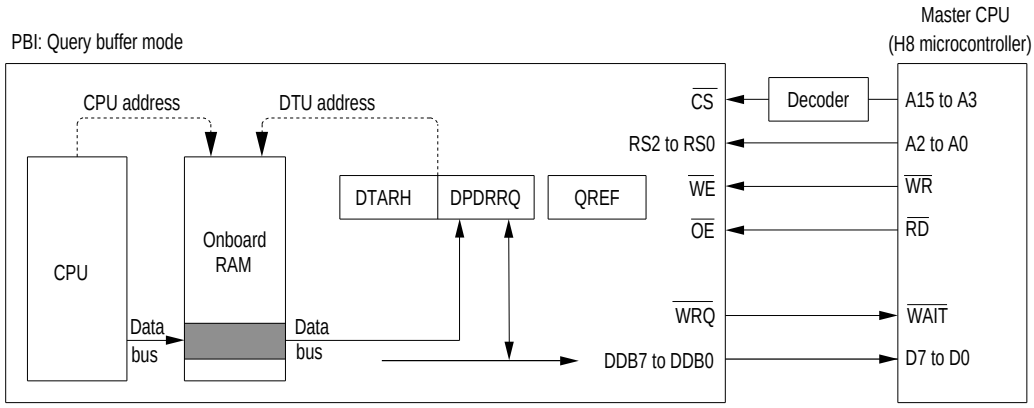
  This parallel interface uses PBI transfer over DTU channels A and B to permit sequential read and write access by the master CPU to up to 128 kbytes of onboard RAM. For a read by the master CPU, the onboard CPU arranges the data sequentially in its onboard RAM, writes the boundary to DTCRA, writes the starting address to DTARA, and clears the MREF flag to `0' to signal to the master CPU that it is ready. The master CPU, when it sees from the MREF flag and the RDY pin that preparations are complete, reads the bytes in sequence from DPDRR. The data bytes move into DPDRR from the onboard RAM via channel A under the control of the PBI controller.

  For a write by the master CPU, the onboard CPU clears the MWEF flag to `0' to signal to the master CPU that it is ready. The master CPU, when it sees from the MWEF flag and the RDY pin that preparations are complete, writes the boundary to DTCRB, writes the starting address to DTARB, and writes the bytes in sequence to DPDRW. The data bytes move from DPDRR to the onboard RAM via channel B under the control of the PBI controller.

- DPRAM direct word mode

  This parallel interface uses register pairs DPDRRH & DPDRRL and DPDRWH & DPDRWL as word-sized (2-byte) onboard dual-port RAM buffers, one each from reads and writes.

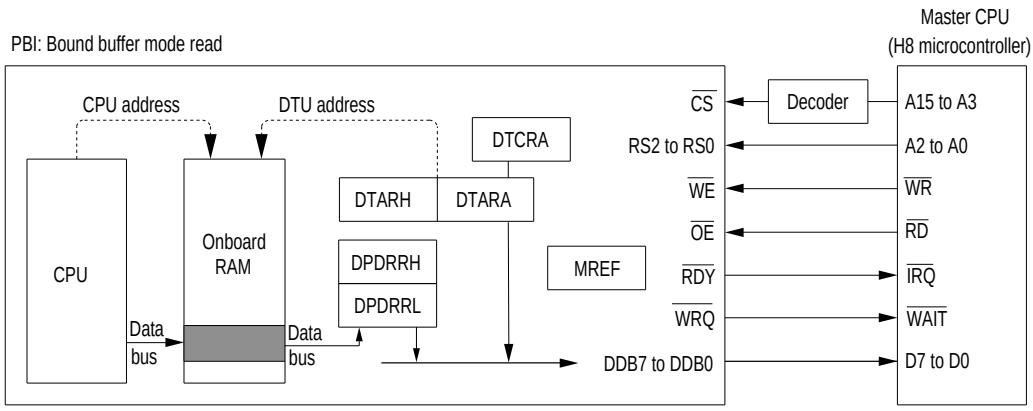
Block Diagram for DPRAM Query Buffer Mode



Legend:

DTARH:	Data transfer address register H
DPDRRQ:	DPRAM data register read Q
QREF:	Query read end flag

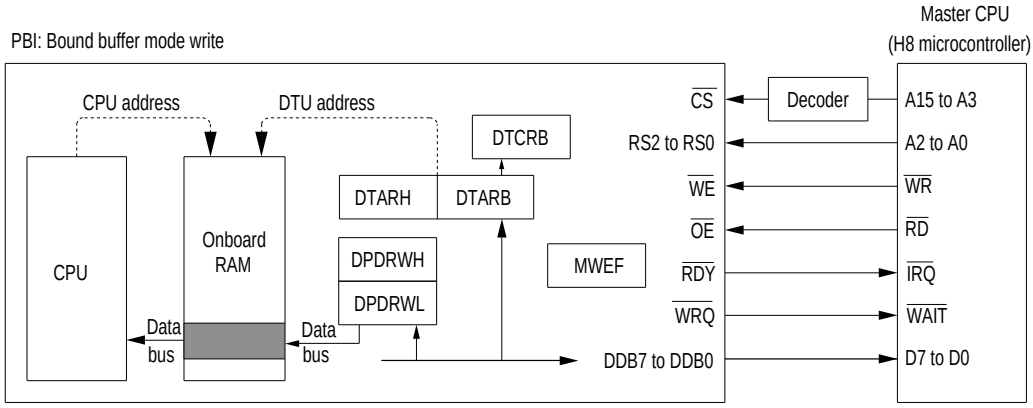
Block Diagram for DPRAM Bound Buffer Mode Read



Legend:

DTCRA:	Data transfer control register A
DTARH:	Data transfer address register H
DTARA:	Data transfer address register A
DPDRRH, DPDRRL:	DPRAM data register read H & L
MREF:	Master read end flag

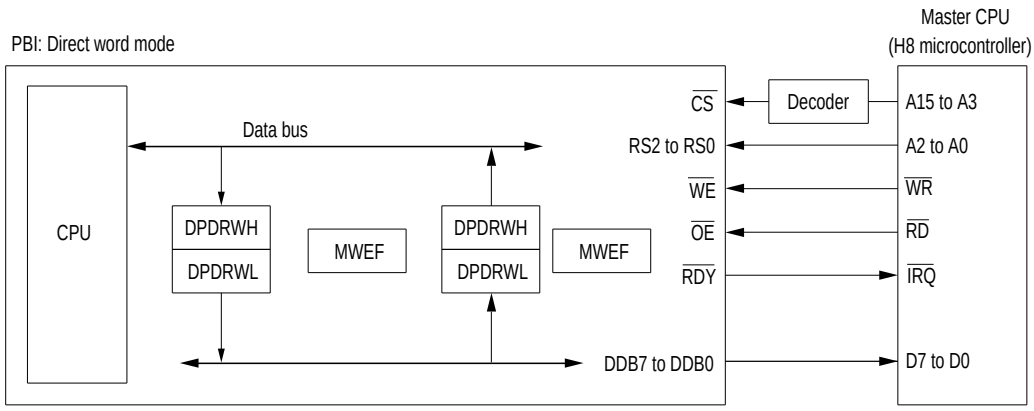
Block Diagram from DPRAM Bound Buffer Mode Write



Legend:

DTCRB:	Data transfer control register B
DTARH:	Data transfer address register H
DTARB:	Data transfer address register B
DPDRWH, DPDRWL:	DPRAM data register write H & L
MWEF:	Master write end flag

Block Diagram for DPRAM Direct Word Mode



Legend:

DPDRRH, DPDRRL:	DPRAM data register read H & L
MREF:	Master read end flag
DPDRWH, DPDRWL:	DPRAM data register write H & L
MWEF:	Master write end flag

4.2 Parallel Handshake Interfaces

The H8/325 Series, in single-chip mode, supports the use of Port 3 as a parallel handshake interface for communications with a master CPU.

The H8/3314 provides a similar parallel handshake interface via its onboard data transfer unit in handshake mode.

4.2.1 H8/325 Onboard Parallel Handshake Interface

Versions with Feature

H8/325 Series

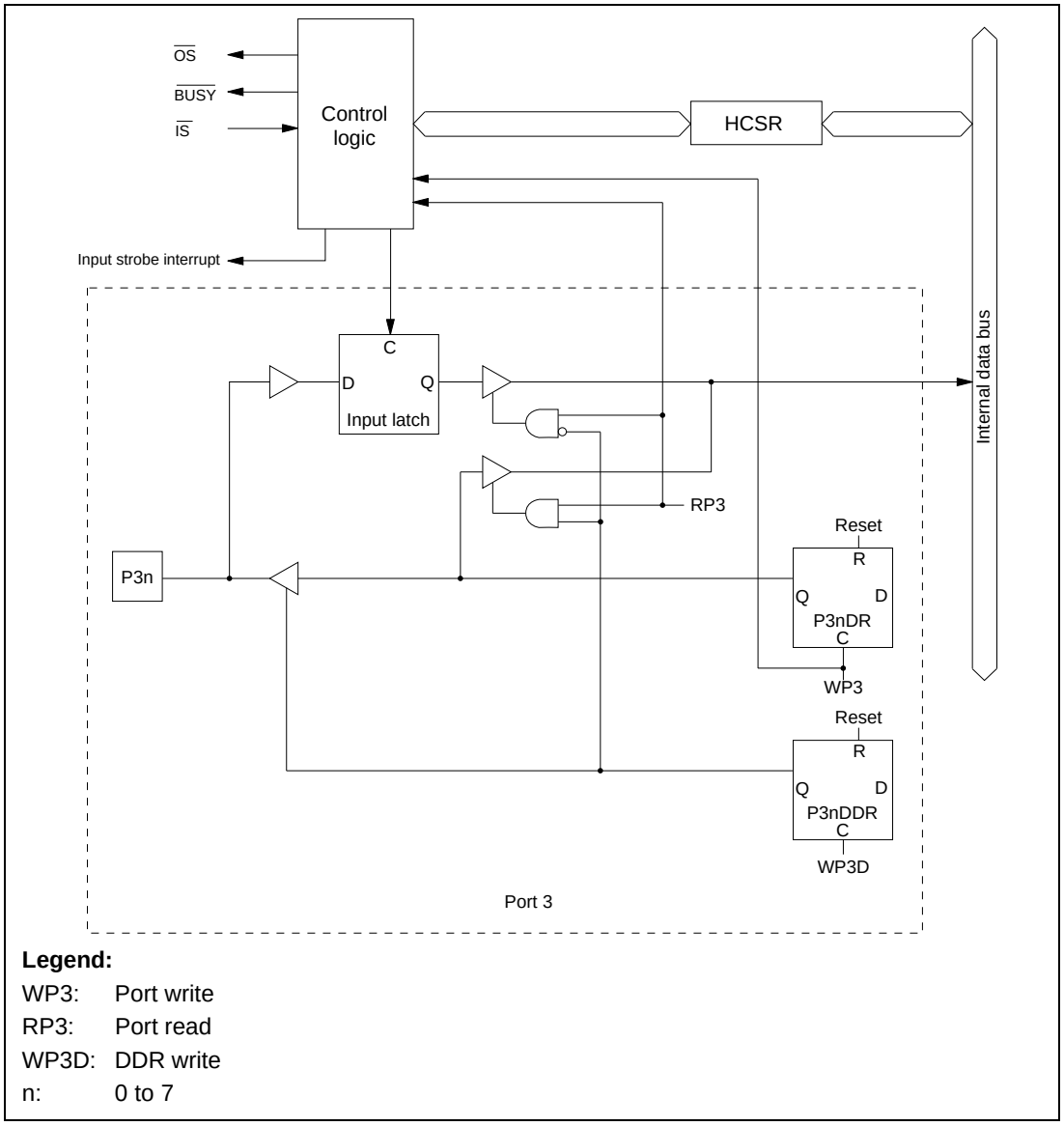
Functions

- In a master-slave configuration with the H8/300 Series member as the slave, this interface provides parallel communications between the two devices over an 8-bit data bus.

Features

- Onboard latch circuit for Port 3
- Communications control with input strobe ($\overline{IS}$) pin, output strobe ($\overline{OS}$) pin, and $\overline{BUSY}$ output pin
  - — At the rising edge of the $\overline{IS}$ signal, the chip latches the Port 3 input data.
  - — A microcomputer read or write operation starts the output strobe from the $\overline{OS}$ pin.
  - — The $\overline{BUSY}$ output pin sends a busy signal as long as the Port 3 data is latched–that is, from the rising edge of the $\overline{IS}$ signal through to the point where the microcomputers reads the latched data and releases the latch.
- Input strobe interrupt (ISI)
  - — The rising edge of the $\overline{IS}$ signal triggers an input strobe interrupt (ISI).
  - — This input strobe interrupt wakes the chip from the software standby mode.

Block Diagram



Legend:

WP3: Port write
RP3: Port read
WP3D: DDR write
n: 0 to 7

4.2.2 Parallel Handshake Interface via DTU/PBI

Version with Feature

H8/3314

Functions

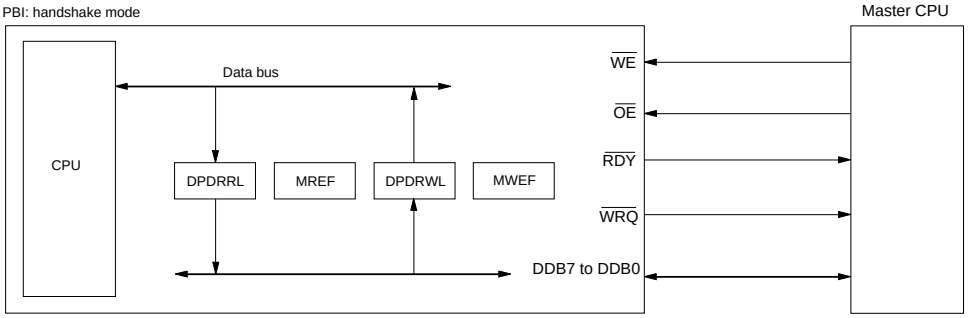
- The handshake mode uses the data transfer unit and parallel buffer interface together to provide a 8-bit parallel interface.
- Communications control is via bus control signals $\overline{\text{WRQ}}$, $\overline{\text{RDY}}$, $\overline{\text{WE}}$, and $\overline{\text{OE}}$.

Features

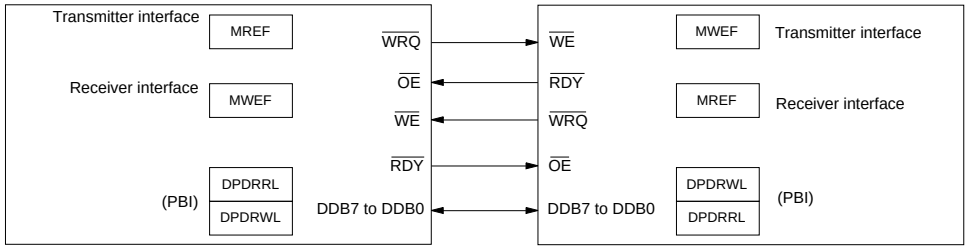
- The transmitter provides latch pulses from its $\overline{\text{WRQ}}$ pin as it sends the data in DPDRRL to the receiver's interface.
- The receiver uses the latch pulses from its $\overline{\text{WE}}$ pin to read the data from the sender's interface into DPDRWL.

Block Diagram

Handshake mode



Wiring example for handshake mode



4.3 Host Interface

H8/300 Series members include a host interface providing two parallel communications channels with a master CPU. This interface consists of seven byte-sized registers (four for data, two for status, and one for control), high-speed GATE A20 logic, and a host interrupt generator. The registers are freely accessible from both the onboard and host CPUs as addresses within the respective address spaces.

Versions with Feature

H8/3334 Series, H8/3337 Series, H8/3437 Series

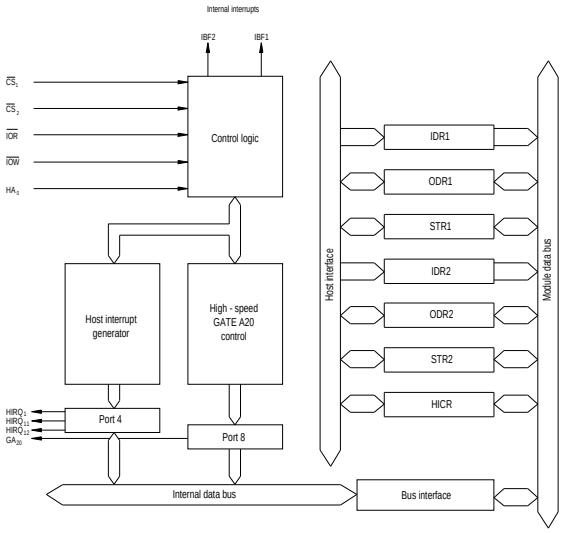
Functions

- In a master-slave configuration with the H8/300 Series member as the slave, this interface provides parallel communications over two channels between the two devices over an 8-bit data bus.

Features

- Two chip select inputs provide independent operation over the two host interface channels.
- A write by the master CPU to an input register triggers an interrupt request to the onboard CPU.
- A write by the onboard CPU to an output register triggers an interrupt request to the master CPU. (Software is also required.)
- The master CPU can control high-speed GATE A20 output with special turn on/turn off data sequences written to an input register.

Block Diagram



Legend:

IDR1: Input data register 1
IDR2: Input data register 2
ODR1: Output data register 1
ODR2: Output data register 2
STR1: Status register 1
STR2: Status register 2
HICR: Host interface control register

4.4 8-Bit Asynchronous/Synchronous Serial Communications Interface

H8/300 Series members include an 8-bit asynchronous/synchronous serial communications interface. The exact interface, Type 1 or Type 2, depends on the version.

Versions with Feature

Type 1: H8/325 Series (2 channels), H8/350 Series (1 channel), H8/330 Series (1 channel)

Type 2: H8/329 Series (1 Channel), H8/3297 Series (1 channel), H8/3314 (2 channels), H8/338 Series (2 channels), H8/3334 Series (1 channel), H8/3337 Series (2 channels), H8/3397 Series (2 channels), H8/3437 Series (2 channels)

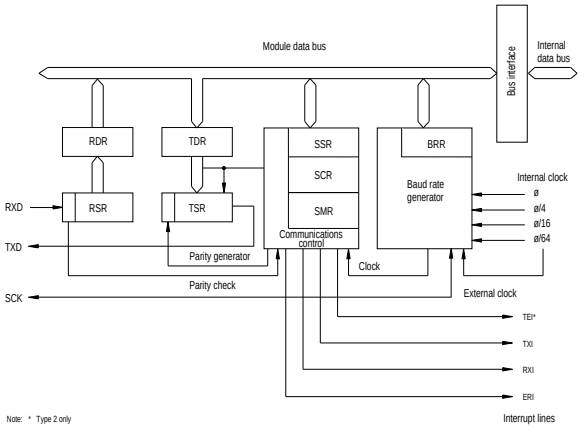
Functions

- Support for both asynchronous and synchronous 8-bit serial communications
- Support for an multiprocessor bit for use in interprocessor serial communications in multiprocessor configurations (Type 2 only)

Features

- Choice of asynchronous for synchronous operation
- Support for full-duplex operation
- Double-buffered data registers for continuous communications
- Onboard baud rate generator providing software control over bit rate
- Choice of clock sources: onboard baud rate generator or external clock (from SCK pin)
- Automatic detection of overrun, framing and parity errors
- LSB-first operation for synchronous operation
- Type 1: Interrupt generator for transmit complete (TXI), receive complete (RXI), and error during receive (ERI) interrupts
- Type 2: Interrupt generator for transmit end (TEI) transmit data empty (TXI), receive data full (RXI), and error during receive (ERI) interrupts

Block Diagram



Legend:

RSR: Receive shift register (8-bit)
RDR: Receive data register (8-bit)
TSR: Transmit shift register (8-bit)
TDR: Transmit data register (8-bit)
SMR: Serial mode register (8-bit)
SCR: Serial control register (8-bit)
SSR: Serial status register (8-bit)
BRR: Bit rate generator (8-bit)

Type 1 vs. Type 2

			Product Versions	
			Type 1	**Type 2**
				H8/329 Series, H8/3297 Series,
				H8/338 Series, H8/3314,
			H8/325 Series, H8/350 Series,	**H8/3334 Series, H8/3337 Series,**
Item			**H8/330 Series**	**H8/3397 Series, H8/3437 Series**
Asynchronous operation	Transmission clock		Onboard baud rate generator or external clock	Onboard baud rate generator or external clock
	Transmission format	World length	7 or 8 bits	7 or 8 bits
		Stop bits	1 or 2 bits	1 or 2 bits

Item			Product Versions	
			Type 1	**Type 2**
				H8/329 Series, H8/3297 Series,
				H8/338 Series, H8/3314,
			H8/325 Series, H8/350 Series,	**H8/3334 Series, H8/3337 Series,**
			H8/330 Series	**H8/3397 Series, H8/3437 Series**
		Parity	Even, odd, none	Even, odd, none
		Multiprocessor bit	--	O
	Error detection	Overrun error detection	O	O
		Parity error detection	O	O
		Framing error detection	O	O
Synchronous operation	Transmission clock		Onboard baud rate generator or external clock	Onboard baud rate generator or external clock
	Transmission format		8 bits per character	8 bits per character
	Transmission order		LSB first	LSB first
	Overrun error detection		O	O
Interrupts	Priority	High	Error during receive (ERI) interrupt	Error during receive (ERI) interrupt
			Receive complete (RXI) interrupt	Receive data full (RXI) interrupt
			Transmit complete (TXI) interrupt	Transmit data empty (TXI) interrupt
		Low	--	Transmit end (TEI) interrupt

4.5 8/16-Bit Synchronous Serial Communications Interface

The H8/350 features a synchronous serial communications interface switchable between 8- and 16-bit operation. The use of separate buffer registers for transmitting and receiving permits continuous communications.

Versions with Feature

H8/350 Series (1 channel)

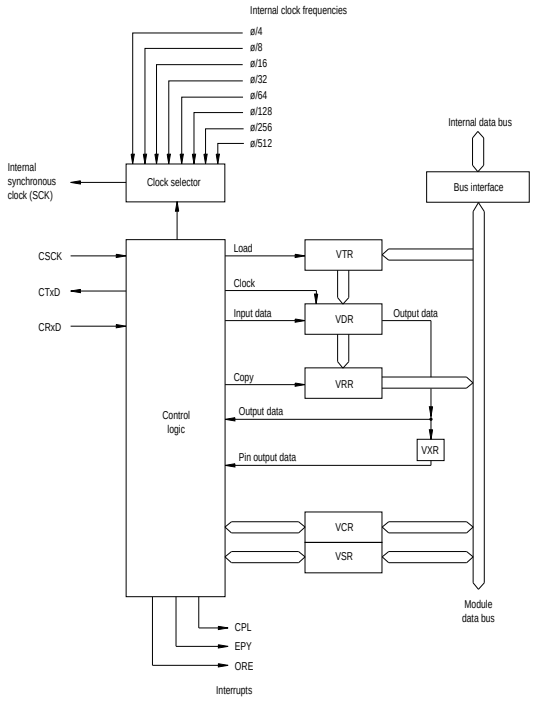
Functions

- This interface supports continuous synchronous 8- or 16-bit serial communications.

Features

- Synchronous interface offering choice of 8- or 16-bit operation
- Continuous communications using buffer registers on the receive and transmit sides of the shift register.
- Support for two-wire interface
  - The chip can be configured to use the high-impedance state for ‘1’ data at I/O pin CTxD.
  - The chip can also be configured to read the level at I/O pin CTxD.
- Choice of nine clock frequencies: external clock frequency or system clock divided by 4, 8, 16, 32, 64, 128, 256, or 512.
- Interrupt generator for transmit complete (EPY), receive complete (CPL), and overrun error (ORE) interrupts.

Block Diagram



Legend:

VSR: VSCI data register (7-bit)
VCR: VSCI control register (8-bit)
VTR: VSCI transmit register (16-bit)
VRR: VSCI receive register (16-bit)
VXR: VSCI expanded data register (1-bit)
VDR: VSCI data shift register (16-bit)

4.6 Inter IC (I^2C) Bus Interface [Option]

The H8/3337 and H8/3437 Series offer, as an option, support for the Philips Inter IC (I^2C) bus interface. This interface economizes on connectors and printed circuit board space by using only one data (SDA) and clock (SCL) line each for data transfers.

Versions Offering Option

H8/3337 Series (option), H8/3437 Series (option)

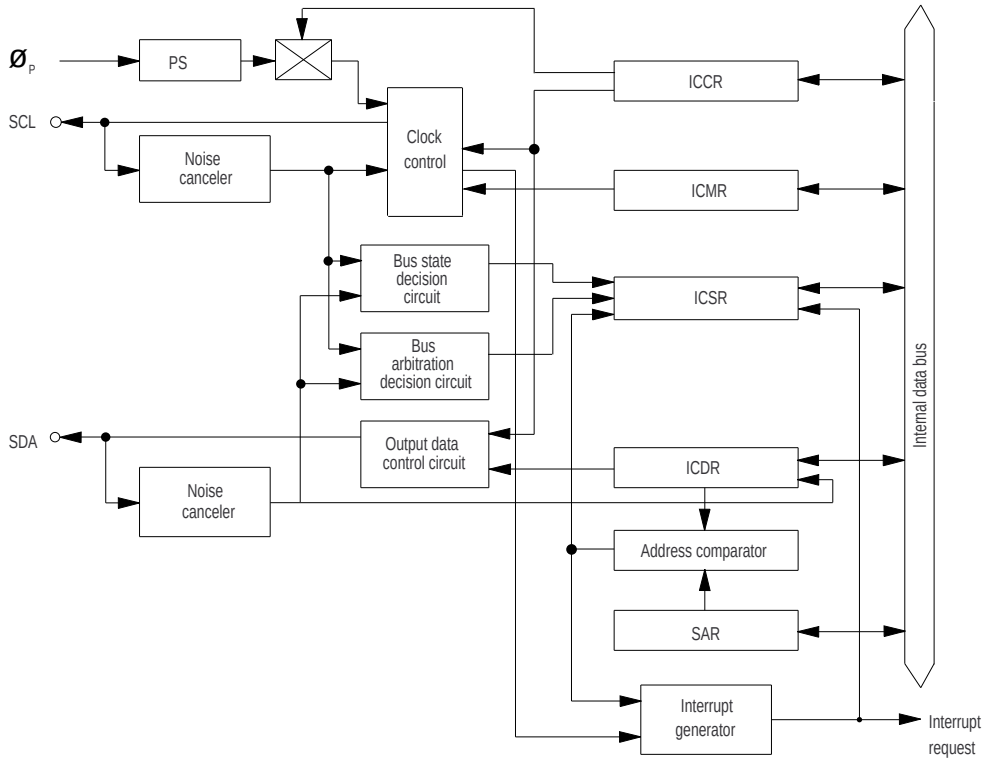
Functions

- In a master-slave configuration, this interface provides serial communications between the two devices.

Features

- Compliance with Philips Inter IC (I^2C) bus interface standard
- Automatic generation of start and stop conditions
- Choice of acknowledge output levels for receiving
- Automatic loading of acknowledge bit for transmitting
- Choice of eight internal clock frequencies in master mode
- Choice of acknowledgment mode or serial mode without acknowledge bit
- Wait state insertion In the acknowledgment mode, the chip automatically pulls the SCL pin low (‘0’) after all data except an acknowledge so as to permit the insertion of wait states.
- Three interrupts generated
  - — At the end of data transmission
  - — In slave receive mode, when the chip receives a slave address matching its own or a general call address
  - — In master transmit mode, when the chip loses bus mastery
- Support for direct bus drive operation

Block Diagram



Legend:

ICCR: I^2C control register
ICMR: I^2C mode register
ICSR: I^2C status register
ICDR: 1^2C data register
SAR: Slave address register
PS: Prescaler

Section 5 Timer

5.1 16-Bit Free-Running Timer

H8/300 Series members include a 16-bit free-running timer for measuring waveform output, pulse width, and frequency. The exact timer, Type 1 or Type 2, depends on the version.

5.1.1 Type 1 16-bit Free-Running Timer

Versions with Feature

H8/325 Series (1 channel), H8/3314 (1 channel)

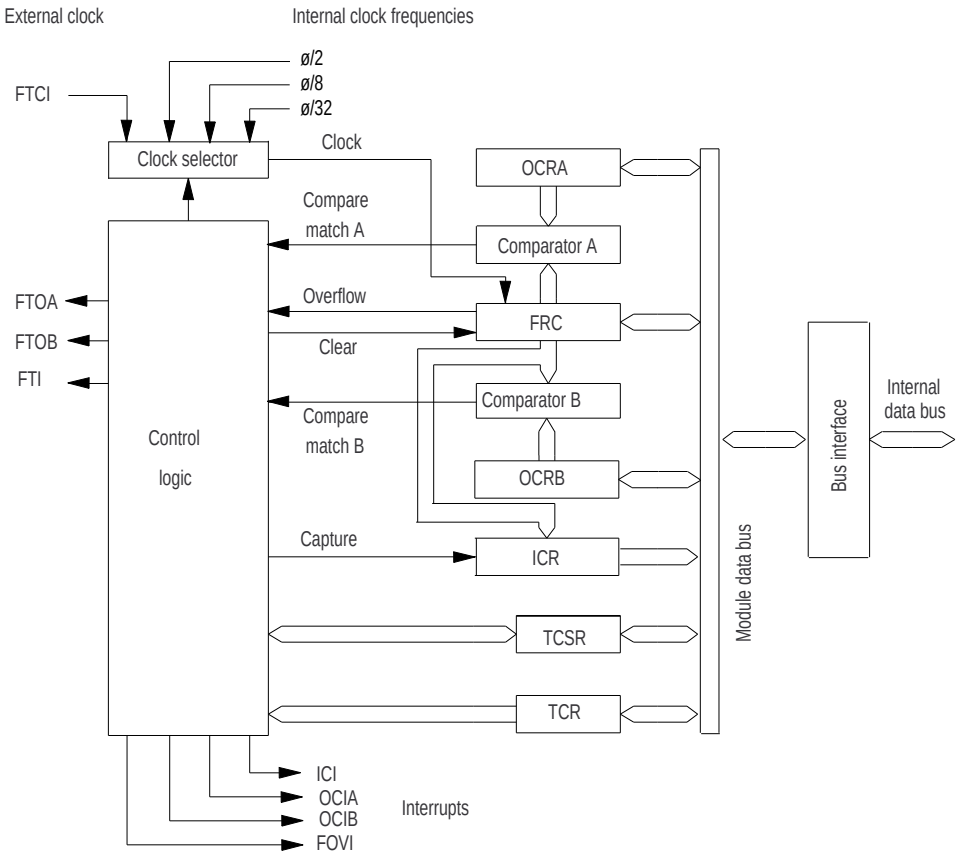
Functions

- This 16-bit free-running timer supports an output compare function using two output compare registers and two output pins and an input capture function using one input capture register and one input pin.

Features

- Choice of four counter input clock frequencies
  - The counter offers a choice of three internal clock frequencies (system clock divided by 4, 8, or 32) and an external clock frequency. The latter permits use as an external event counter, for example.
- Output compare function with two independent comparators
  - The timer is capable of simultaneously producing two different output waveforms.
- Input capture function
  - There is a choice of triggers: rising edge or falling edge.
- Counter clear option
  - The application can specify that a compare match A event clear the value in the free-running counter.
- Interrupt generator for input capture (ICI), compare match A (OCIA and OCIB), and overflow (FOVI) interrupts

Block Diagram



Legend:

TCR: Timer control register (8-bit)
TCSR: Timer control/status register (8-bit)
FRC: Free-running counter (16-bit)
OCRA: Output compare register A (16-bit)
OCRB: Output compare register B (16-bit)
ICR: Input capture register (16-bit)

5.2.1 Type 2 16-bit Free-Running Timer

Versions with Feature

H8/329 Series (1 channel), H8/3297 Series (1 channel), H8/330 Series (1 channel), H8/3314 (1 channel), H8/338 Series (1 channel), H8/3334 Series (1 channel), H8/3337 Series (1 channel), H8/3397 Series (1 channel), H8/3437 Series (1 channel)

Functions

- This 16-bit free-running timer supports an output compare function using two output compare registers and two output pins and an input capture function using four input capture registers, four input pins, and support for buffered operation.

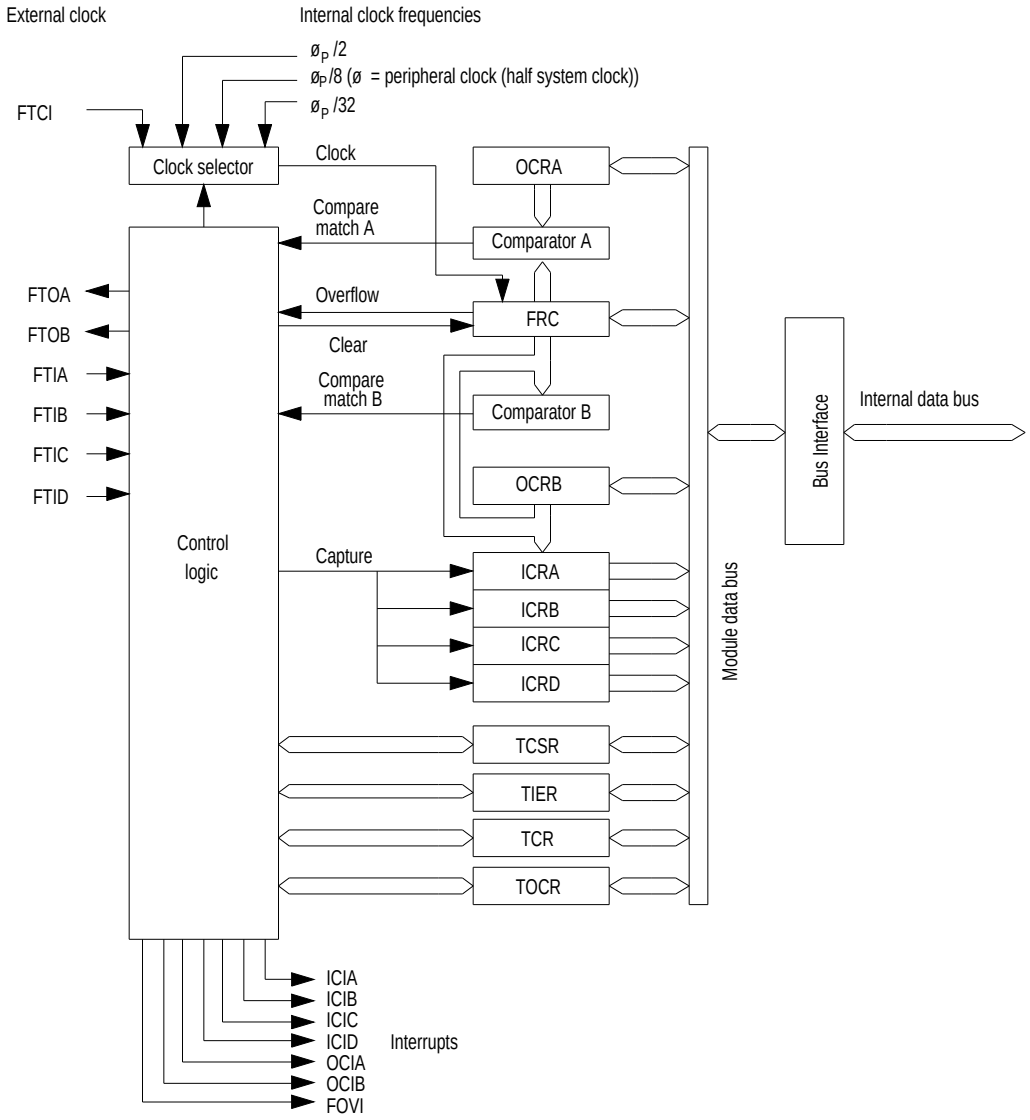
Features

- Choice of four counter input clock frequencies The counter offers a choice of three internal clock frequencies (system clock divided by 4,8, or 32) and an external clock frequency. The latter permits use as an external event counter, for example.
- Output compare function with two independent comparators The timer is capable of simultaneously producing two different output waveforms.
- Input capture function
  - — There is a choice of triggers: rising edge of falling edge. There are four independent input capture registers available and support for buffered operation*.

Note: * Specifying buffered operation divides the four 16-bit input capture registers into two pairs with one member of the pair acting as a buffer for the other.

- Counter clear option
  - — The application can specify that a compare match A event clear the value in the free-running counter.
- Interrupt generator for input capture (ACIA to ICID), compare match (OCIA and OCIB), and overflow (FOVI) interrupts

Block Diagram



Legend:

FRC: Free-running counter (16-bit)

OCRA, OCRB: Output compare registers A and B (16-bit)

ICRA, ICRB, ICRC, ICRD: Input capture registers A, B, C, and D (16-bit)

TCSR: Timer controls/status register (8-bit)

TCR: Timer control register (8-bit)

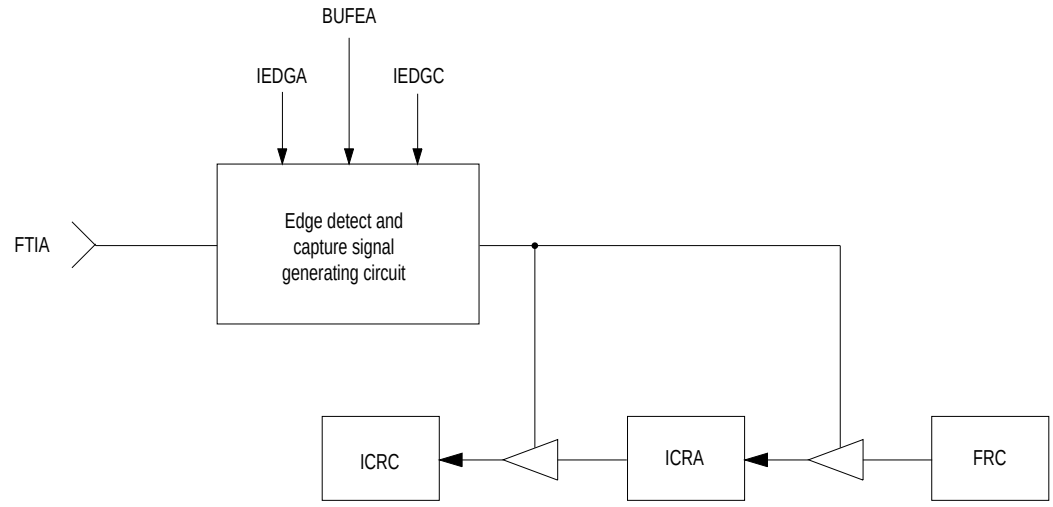
TIER: Timer interrupt enable register (8-bit)

TOCR: TImer output control register (8-bit)

Type 1 vs. Type 2

	Product Versions	
	Type 1	**Type 2**
Item	**H8/325 Series, H8/3314 (FRT Channel 1)**	**H8/329 Series, H8/3297 Series, H8/330 Series, H8/3314 (FRT Channel 0), H8/338 Series, H8/3334 Series, H8/3337 Series, H8/3397 Series, H8/3437 Series**
Output compare registers	2	2
Input capture registers	1	4
Compare match output pins	2	2
Input capture input pins	1	4
External event counter support	O	O
Internal clock frequencies	Three (system clock divided by 2, 8, or 32)	Three (system clock divided by 2, 8 or 32)
Buffered input capture operation	--	O

Input Capture Buffering



Legend:
BUFEA: Buffer enable A
IEDGA: Input edge select A
IEDGC: Input edge select C
ICRC: Input capture register C
ICRA: Input capture register A
FRC: Free-running counter

5.2 8-Bit Multification Timer

H8/300 Series members include an 8-bit multification timer built around an 8-bit counter. This timer has two independent comparators, includes a counter clear function, and is capable of producing output pulses with a wide variety of waveforms.

Versions with Feature

H8/325 Series (2 channels), H8/329 Series (2 channels), H8/3297 Series (2 channels), H8/330 Series (2 channels), H8/3314 (2 channels), H8/338 Series (2 channels), H8/3334 Series (2 channels), H8/3337 Series (2 channels), H8/3397 Series (2 channels), H8/3437 Series (2 channels)

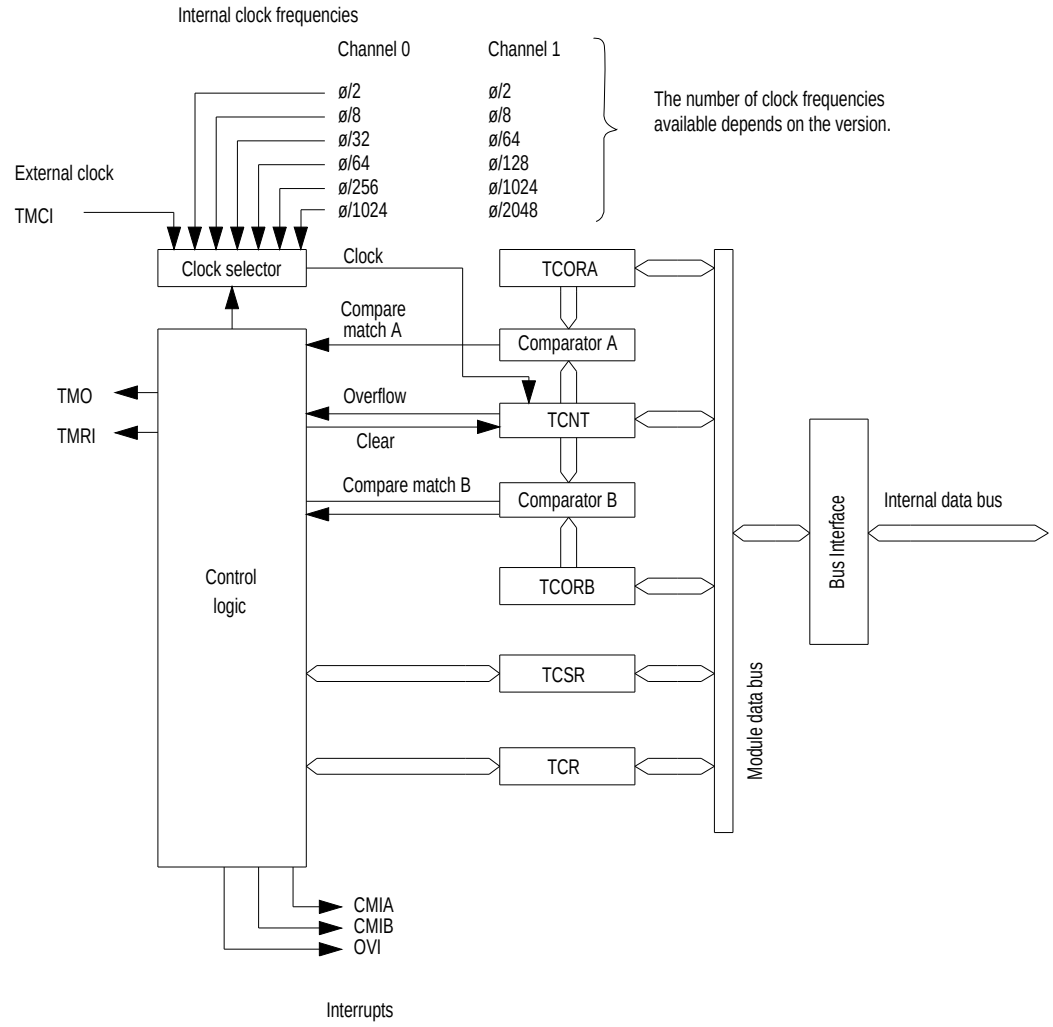
Features

- Choice of at least three internal clock frequencies and an external clock frequency*

Note: * Some versions offer a choice of six internal clock frequencies. (See Table below.)

- Counter clear option
  - — The application can specify that a compare match A event clear the value in the free-running counter.
- Two independent comparators
  - — Timer output may be controlled by the combination of the two independent compare match outputs.
  - — Combination with an external reset signal permits adding delays to an external signal.
- Interrupt generator for compare match (CMIA and CMIB) and overflow (OVI) interrupts

Block Diagram



Legend:

TCR: Timer control register (8-bit)
TCSR: Timer control/status register (8-bit)
TCORA: Timer constant register A (8-bit)
TCORB: Timer constant register B (8-bit)
TCNT: Timer counter (8-bit)

Comparison of Timers

	Product Versions			
	8-Bit Multifunction Timers			
	Channel 0	Channel 1	Channel 0	Channel 1
Item	H8/325 Series, H8/330 Series		H8/329 Series, H8/3297 Series, H8/3314, H8/338 Series, H8-3334 Series, H8/3337 Series, H8/3397 Series, H8/3437 Series	
Comparators	2	2	2	2
Timer output pins	2	2	2	2
External reset support	O	O	O	O
External event counter support	O	O	O	O
Internal clock frequencies	Three: System clock divided by 8, 64, or 1024		Six: System Clock divided by 2, 8, 32, 64, 256, or 1024	Six: System clock divided by 2, 8, 64, 128, 1024, or 2048

5.3 8-Bit Pulse-Width Modulation Timer

H8/300 Series members include a built-in 8-bit pulse width modulation timer. An 8-bit duty register permits selection of a duty ratio for the output pulses anywhere between 0% and 100%.

Versions with Feature

H8/330 Series (2 channels), H8/388 Series (2 channels), H8/3334 Series (2 channels), H8./3337 Series (2 channels), H8/3397 Series (2 channels), H8/3437 Series (2 channels)

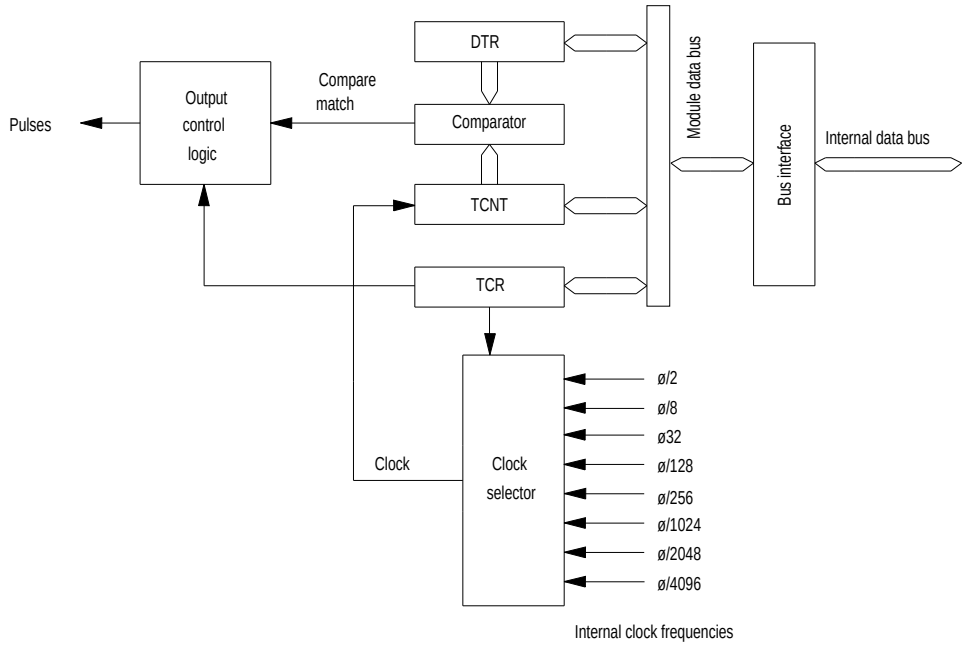
Functions

- Generation of a pulse width modulation waveform with a duty between 0% and 100%

Features

- Choice of eight internal clock frequencies (system clock divided by 2, 8, 32, 128, 256, 1024, 2048, or 4096)
- Resolution of 1/250
  - Duty register values between 0 and 250 (H'00 and H'FA) produce pulses with duty rations between 0% and 100%.
- Choice of direct or inverse output

Block Diagram



Legend:

TCR: Timer control register (8-bit)
DTR: Duty register (8-bit)
TCNT: Timer counter (8-bit)

5.4 14-Bit Pulse-Width Modulation Timer

The H8/350 features a pulse width modualtion D/A converter built around a 14-bit counter. Adding fine-adjustment pulses to the basic carrier pulses yields D/A conversions with low ripple content.

Versions with Feature

H8-350 Series (2 channels)

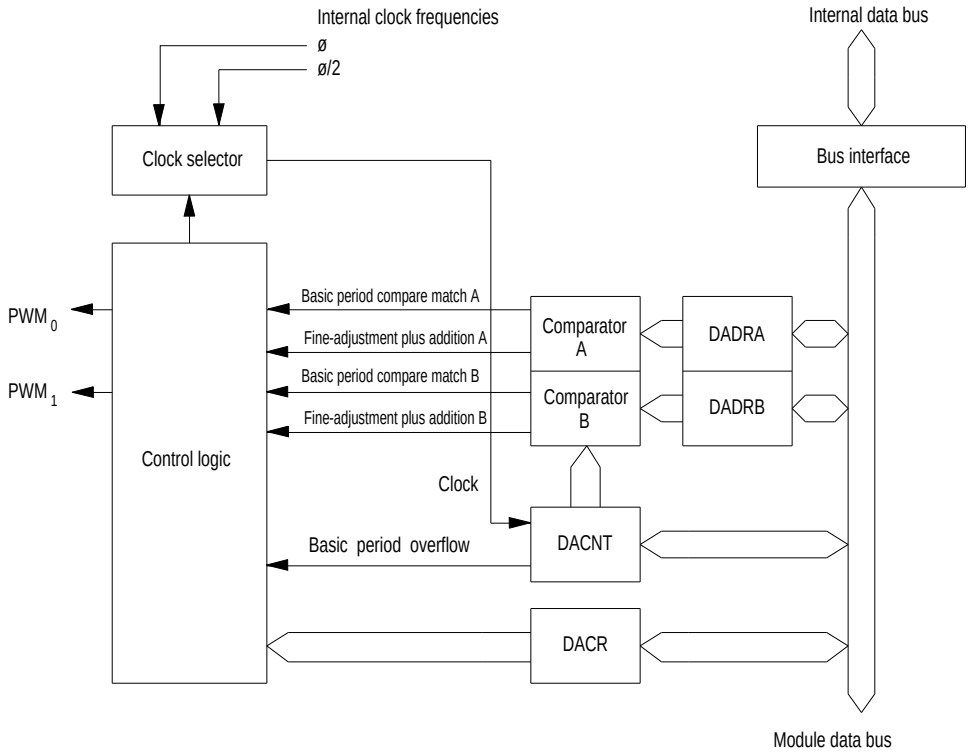
Functions

- Two pulse width modulation output channels sharing a 14-bit counter
- Connection of a low-pass filter enables operation as a D/A converter

Features

- Choice of two internal clock frequencies (system clock or system clock divided by 2) for counter input
- Choice of two basic carrier modulations
  - — Period 64 times that of the input clock with between 0 and 255 fine-adjustment pulses for every 256 basic carrier pulses
  - — Period 256 times that of the input clock with between 0 and 63 fine-adjustment pulses for every 64 basic carrier pulses
- Hardware configuration with two pulse width modulation output channels sharing a counter and control register

Block Diagram



Legend:

DACR: PWM D/A control register (6-bit)
DADRA: PWM D/A data register A (15-bit)
DADRB: PWM D/A data register B(15-bit)
DACNT: PWM D/A counter (14-bit)

5.5 Watchdog Timer

H8/300 Series members include a watchdog timer for monitoring system operation. If the system is unable to reset the timer counter at regular intervals--because it has run out of control, for example--the timer overflows, sending an non-maskable interrupt or reset signals to the CPU.

Versions with Feature

H8/3297 Series (1 channel), H8/3314 (1 channel), H8/3334 Series (1 channel), H8/3337 Series (1 channel), H8/3397 Series (1 channel), H8/3437 Series (1 channel)

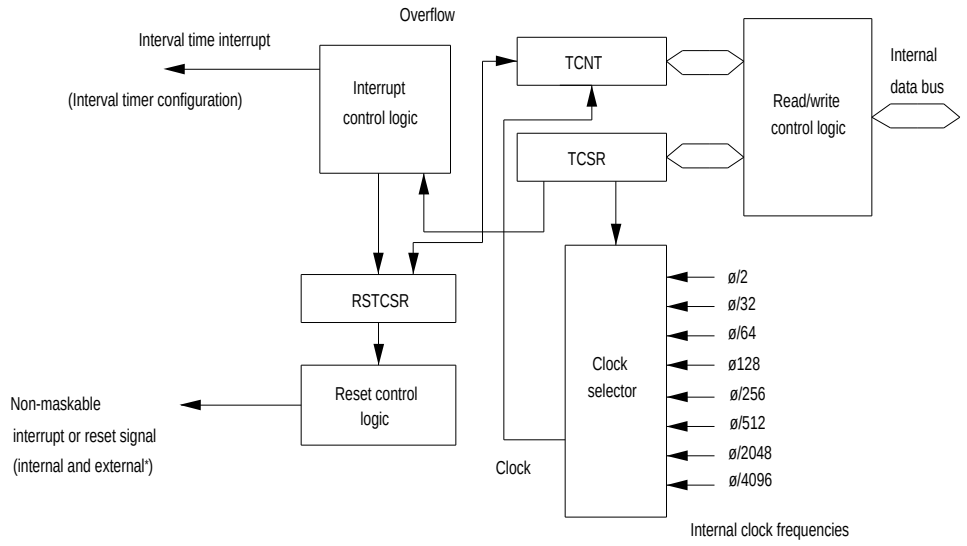
Functions

- Choice of watchdog timer and interval timer operation

Features

- Choice of eight internal clock frequencies (system clock divided by 2, 32, 64, 128, 256, 512, 2048, or 4096)
- Watchdog timer
  - In this configuration, timer overflow produces a non-maskable interrupt or reset signal. This reset signal is available externally for all versions except the H8/3314.
- Interval timer
  - In this configuration, timer overflow produces an interval timer maskable interrupt.

Block Diagram



Note: * The reset signal is not available externally from the H8/3314.

Note: * The reset signal is not available externally from the H8/3314.

Legend:

TCSR: Timer control/status register (8-bit)

TCNT: Timer counter (8-bit)

RSTCSR: Reset control/status register (8-bit)

5.6 H8/350 Built-in Timers and Timer Network

The H8/350 features four timer types, nine timer channels, and a timer network controlling both connections between these channels and I/O.

Versions with Feature

H8/350

5.6.1 H8/350 Built-in Timers

19-bit Free-Running Timer (1 Channel)

- Choice of three internal clock frequencies (system clock divided by 2, 4 or 8) and an external clock frequency for counter input clock
- Four channels each for output compare and input capture
- Choice of edge triggers for input capture: rising, falling, or both
- Counter clear option for compare match and input capture
- Interrupt generator for nine interrupts: four each for compare match and input capture plus one for overflow

  Note: There are, however, only seven interrupt vectors available.

16-Bit Timer/Counters (2 Channels)

- Choice of three internal clock frequencies (system clock divided by 2, 8, or 32) and an external clock frequency for counter input clock.
- Two output compare channels
- Counter clear option for compare match and external reset signal
- Ability to specify minimum counter value for external reset counter clear option
- Interrupt generator for three interrupts: two for compare match plus one for overflow

  Note: There are, however, only two interrupt vectors available.

8-Bit Timer/Counters* (4 Channels)

- Choice of six internal clock frequencies (system clock divided by 8, 16, 32, 64, 256, or 512) and an external clock frequency for counter input clock
- Two output compare channels
- Counter clear option for compare match and external reset signal
- Interrupt generator for three interrupts: two for compare match plus one for overflow

  Note: There are, however, only two interrupt vectors available.

Note: * Except as noted, these timers share the basic functionality as those in Section 5.2 “8-bit Multifunction Timer.”

8-Bit Up/Down Counters (2 Channels)

- Choice of seven internal clock frequencies (system clock divided by 1, 2, 4, 8, 16, 64, or 256) for basic clock
- Choice of seven counter input clock frequencies obtained by dividing the basic clock frequency a number between 1 and 7

  Note: The up and down counters can use different dividers.

- Flexible up/down counter operation through use of two external input pins (TMEI and TMDI) and internal clock
- Tow output compare channels

  Note: The chip supports distinguishing an up counter compare match from a down counter one.

- Counter clear/set options for compare match and external direction signal
- Interrupt generator for six interrupts: four for compare match plus two for overflow/underflow

  Note: There are, however, only four interrupt vectors available.

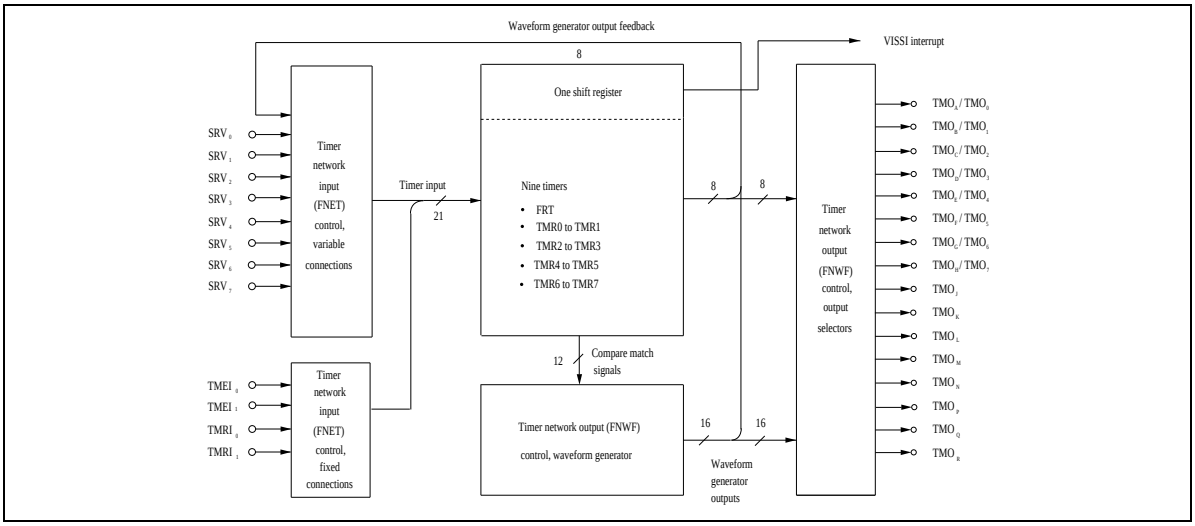
5.6.2 Timer Network

The timer network consists of separate input (FNET) and output (FNWF) control sections determining connections between the nine onboard timers and the I/O pins.

Features

- Input control (FNET)
  This section controls network input from 12 inputs pins and 8 internal feedback lines.
  - — Four input pins (TMEI0, TMEI1, TMRI0, and TMRI1) are connected directly to the timer.
  - — Other timer inputs are the eight input pins (SRV0 through SRV7) and eight feedback lines from the output side of the timer network.
  - — The timer input sources are fixed, selected from pairs, or selected from sets of four.
- Output control (FNWF)
  This section controls the 16 network output lines to produce a variety of waveforms from simple to complex.
  - — There is a choice for these sixteen outputs: 8 waveforms directly from the timers and 16 from the waveform generator alongside the timer network.
  - — The waveform generator alongside the timer network uses 12 compare match signals from the timers as its inputs.
- Shift register
  This circuit samples the timer outputs using the timer inputs. It is thus able to detect duty fluctuations in high-speed timer inputs.

Block Diagram



5.7 Programmable Timing Pattern Controller

H8/300 Series members include a built-in programmable timing pattern controller producing pulse output using a time base from a 16-bit free-running timer. This controller provides four groups of four bits each and supports both independent and joint use of these groups.

Versions with Feature

H8/3314

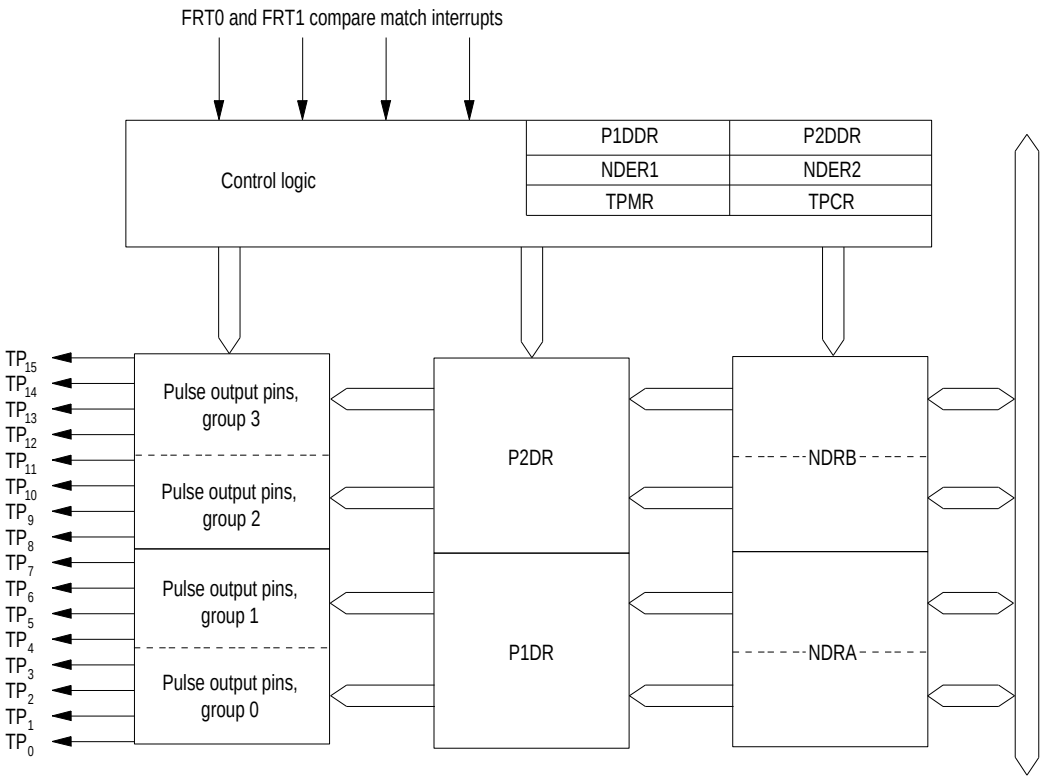
Functions

- The controller uses compare match interrupts A and B from two 16-bit free-running timers (FRT0 and FRT1) as output triggers and is capable of producing up to 16 bits of pulse output simultaneously.

Features

- 16 bits of output data
  - — The controller is capable of producing up to 16 bits of pulse output simultaneously. The output bits can be enabled or disabled individually.
- Four output channels
  - — Each group of four bits may be assigned its own output trigger for a maximum of four 4-bit channels. The groups may also be merged into two 8-bit channels or a single 16-bit channel.
- Choice of output triggers
  - — Each group may be assigned its own output trigger chosen from the four compare match interrupts from FRT0 and FRT1.
- Nonoverlapping operation option
  - — The user can specify a nonoverlapping interval between multiple pulse outputs.
- Coupled operation with data transfer unit
  - — Using the compare match interrupt as the output trigger to drive the data transfer unit permits sequential data transfers that bypass the CPU.

Block Diagram



Legend:

TPMR: TPC output mode register
TPCR: TPC output control register
NDER2: Next data enable register 2
NDER1: Next data enable register 1
P2DDR: Port 2 data direction register
P1DDR: Port 1 data direction register
NDRB: Next data register B
NDRA: Next data register A
P2DR: Port 2 data register
P1DR: Port 1 data register

Section 6 Analog Conversions

6.1 8-Bit A/D Converter

H8/300 Series members include an A/D converter with a precision of 8 bits. Programs are therefore able to simultaneously measure analog inputs on up to 8 channels—16 for the H8/350. The converter also supports the use of an external trigger to initiate processing.

Versions with Features

H8/329 Series (8 channels), H8/350 Series (16 channels), H8/330 Series (8 channels), H8/338 Series (8 channels), H8/3334 Series (8channels)

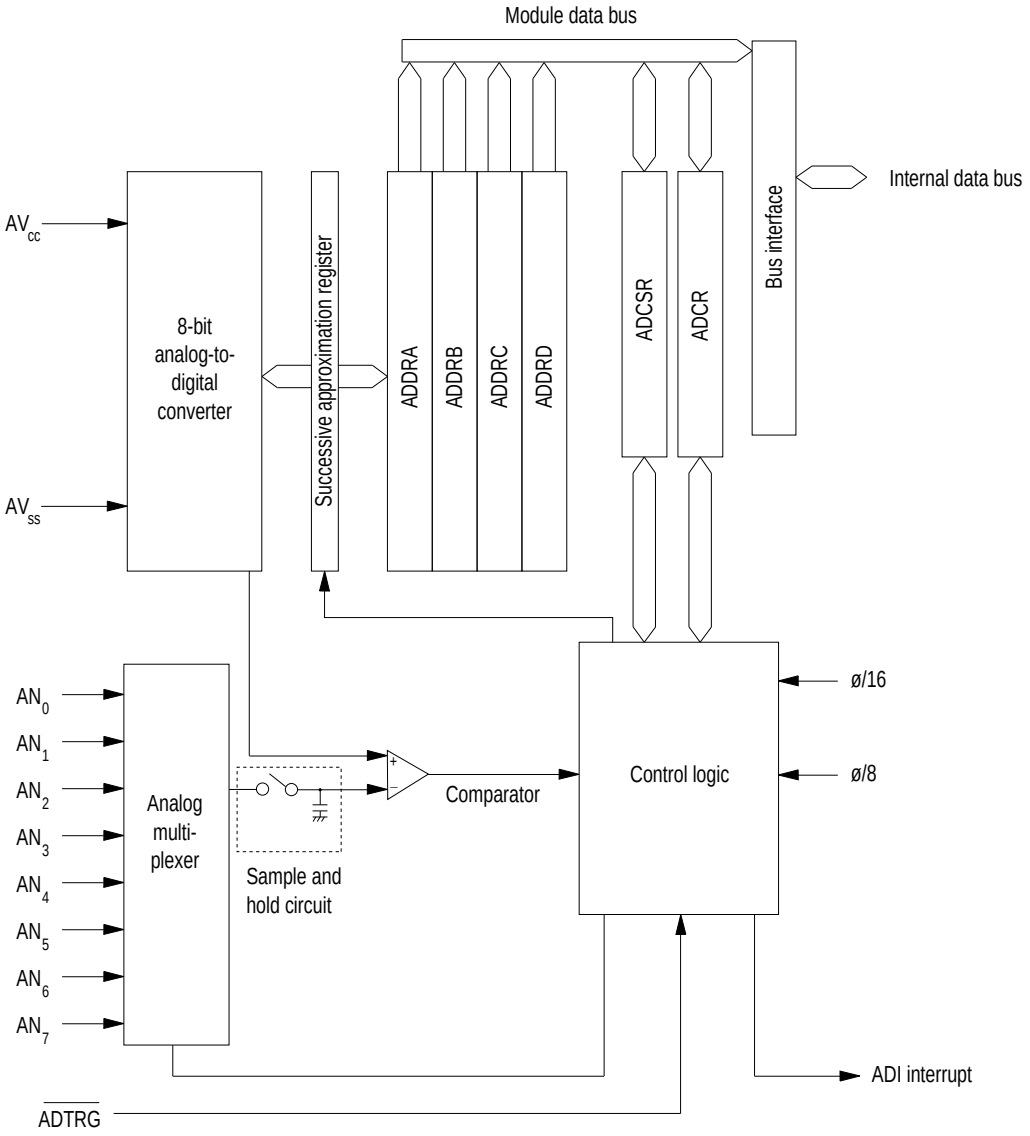
Functions

- 8-bit A/D converter using successive approximation

Features

- Resolution: 8 bits
- Conversion times: 122 or 242 clock cycles
- Four 8-bit data registers
  - The converter stores the results for each channel in a separate register.
- Choice of single-channel and scan modes
  - Single-channel mode: Conversion on a single channel
  - Scan mode: Repeated conversion on one or several channels
- Built-in sample and hold circuit
- Suppot for initiating processing with an external trigger
- Interrupt generator for A/D converter conversion end interrupt (ADI)

Block Diagram (Sample with 8 Analog Inputs)



Legend:

ADCR; A/D control register (8-bit)
ADCSR: A/D control/status register (8-bit)
ADDRA: A/D data register A (16-bit with 8-bit halves ADDRAH & ADDRAL)
ADDRB: A/D data register B (16-bit with 8-bit halves ADDRBH & ADDRBL)
ADDRC: A/D data register C (16-bit with 8-bit halves ADDRCH & ADDRCL)
ADDRD: A/D data register D (16-bit with 8-bit halves ADDRDH & ADDRDL)

6.2 10-bit A/D Converter

H8/300 Series members include an A/D converter with a precision of 10 bits. Programs are therefore able to simultaneously measure analog inputs on up to 8 channels. The converter also supports the use of an external trigger to initiate processing.

Version with Feature

H8/3297 Series (8 channels), H8/3314 (8 channels), H8/3337 Series (8 channels), H8/3397 Series (8 channels), H8/3437 Series (8 channel)

Functions

- 10-bit A/D converter using successive approximation

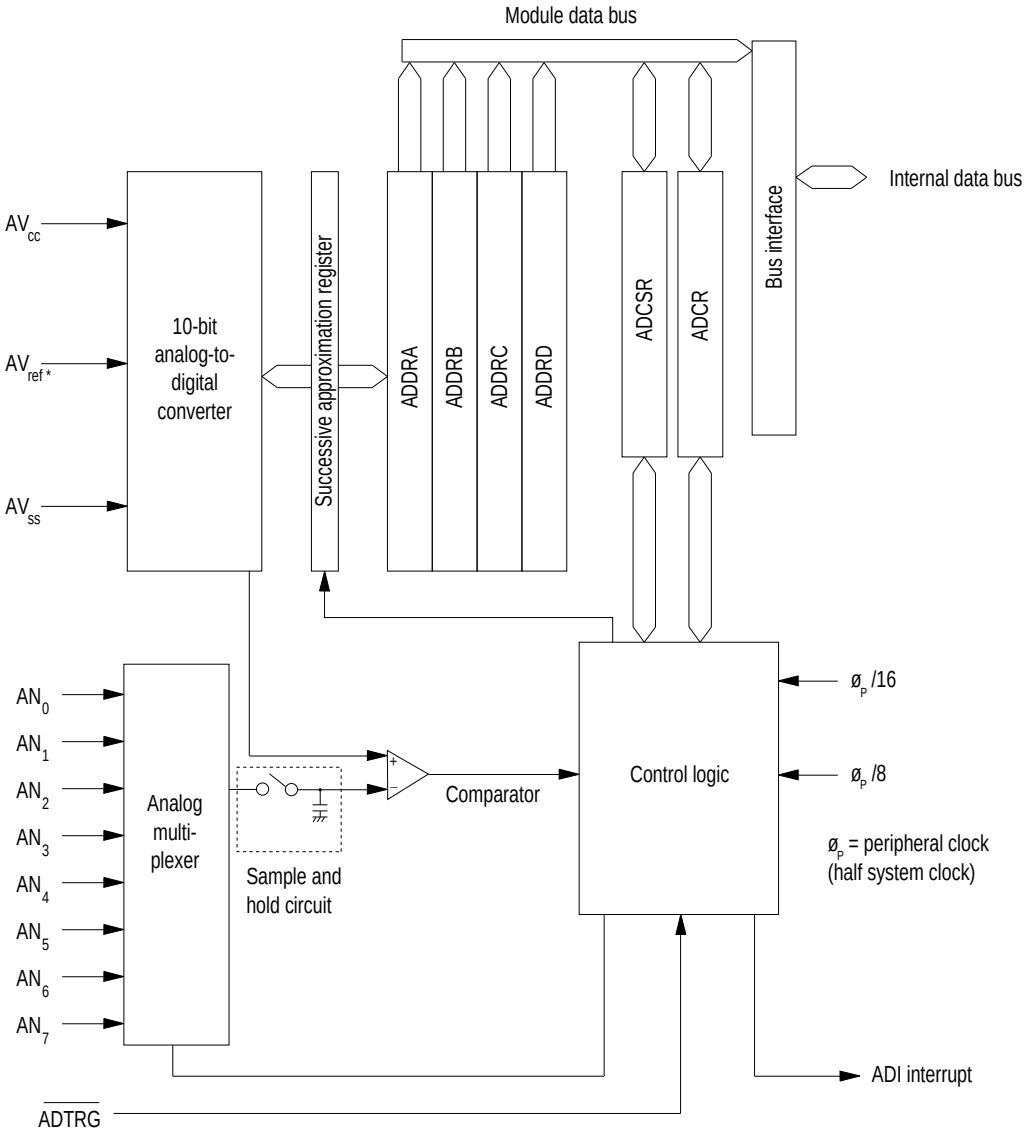
Features

- Resolution: 10 bits
- Conversion times: 134 or 266 clock cycles
- Four 16-bit data registers
  - The converter stores the results for each channel in a separate register.
- Choice of single-channel and scan modes
  - Single-channel mode: Conversion on a single channel
  - Scan mode: Repeated conversion on one or several channels
- Built-in sample and hold circuit
- Support for initiating processing with an external trigger
- External reference (AV_{ref}) pin*

Note: * H8/3437 Series only.

- Interrupt generator for A/D converter conversion end interrupt (ADI)

Block Diagram



Legend:

ADCR: A/D control register (16-bit)
ADCSR: A/D control/statis regoster (16-bit)
ADDRA: A/D data register A (16-bit with 8-bit halves ADDRAH & ADDRAL)
ADDRB: A/D data register B (16-bit with 8-bit halves ADDRBH & ADDRBL)
ADDRC: A/D data register C (16-bit with 8-bit halves ADDRCH & ADDRCL)
ADDRD: A/D data register D (16-bit with 8-bit halves ADDRDH & ADDRDL)

Note: *H8/3437 Series only.

6.3 8-Bit D/A Converter

H8/300 Series members include a digital-to-analog converter with a precision of 8 bits. Programs are therefore able to simultaneously generate analog outputs up to 2 channels.

Versions with Feature

H8/338 Series (2 channels), H8/3337 Series (2 channels), H8/3437 Series (2 channels)

Functions

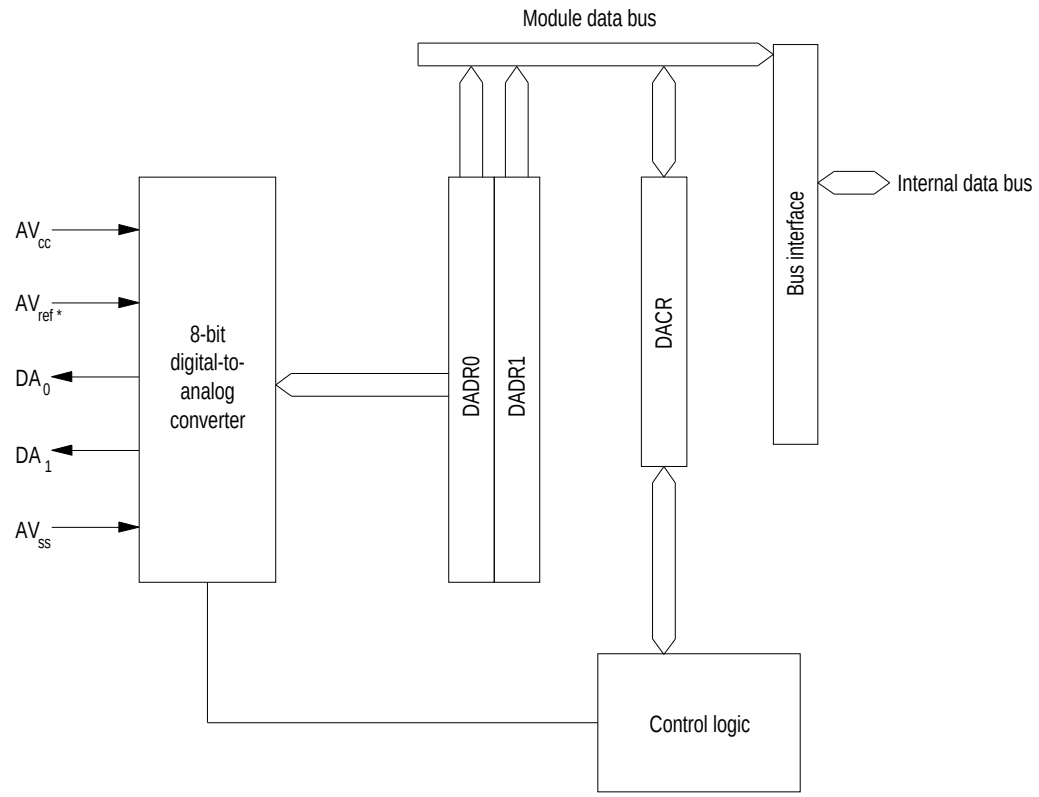
- 8-bit D/A converter driving two analog output pins

Features

- Resolution: 8 bit
- Number of output pins: 2
- Conversion times: max. 10 µs
- Output level: 0 to AV_{CC} for H8/338 and H8/3337 Series; 0 to AV_{ref} for H8/3437 Series

Note: The output level is the full-scale voltage (AV_{CC} or AV_{ref}) multiplied by the contents of the data register (DADR) and divided by 256.

Block Diagram



Legend:
DACR: D/A control register (8-bit)
DADR0: D/A data register 0 (8-bit)
DADR1: D/A data register 1 (8-bit)
Note: * H8/3437 Series only.

Section 7 Product Descriptions

7.1 H8/310 Series

This Series contains H8/300 Series members specifically designed for use as IC card microcomputers. To the H8/300 CPU, they add generous portions of ROM and RAM, an EEPROM that may be electrically written and erased, and I/O ports. Built-in security features protect the contents of the ROM and EEPROM from unauthorized access and alteration.

Series Members

H8/310, H8/3101, H8/3102

Features

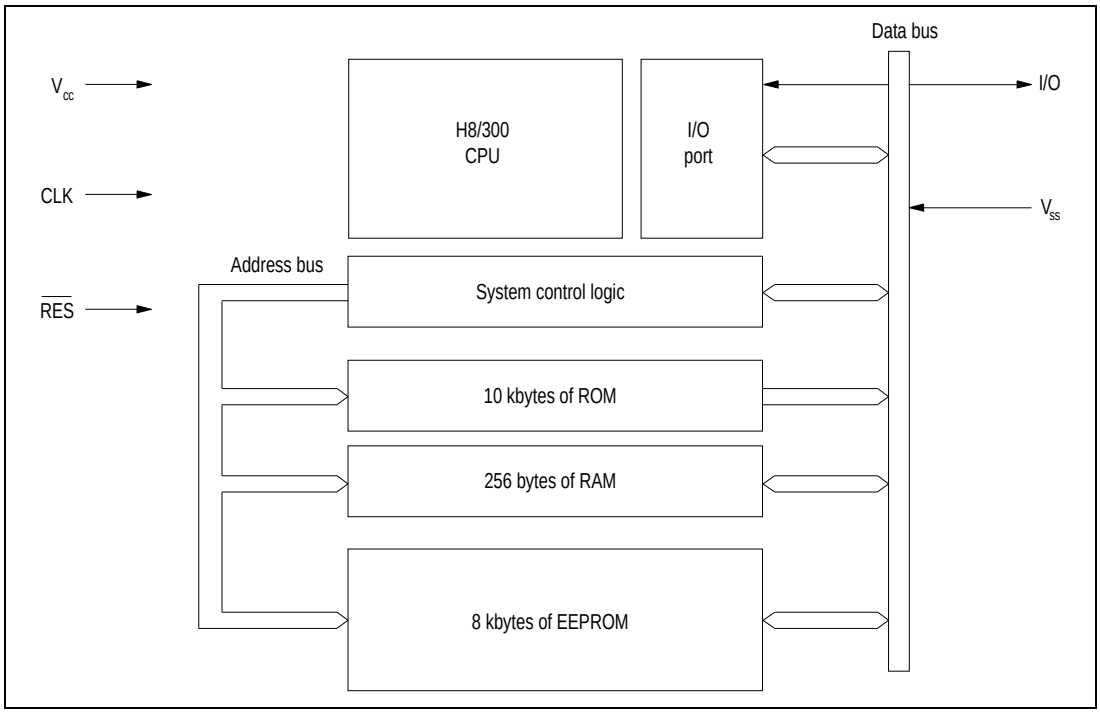
- 8 kbytes of onboard EEPROM
  - CPU instructions for rewriting contents
  - Writing/erasing up to 32 bytes in the same page at a time
  - Data protection facilities
- Onboard memory (unit: bytes)

	H8/310	H8/3101	H8/3102
ROM	10 k	10 k	16 k
RAM	256	256	512
EEPROM	8 k	8 k	8 k

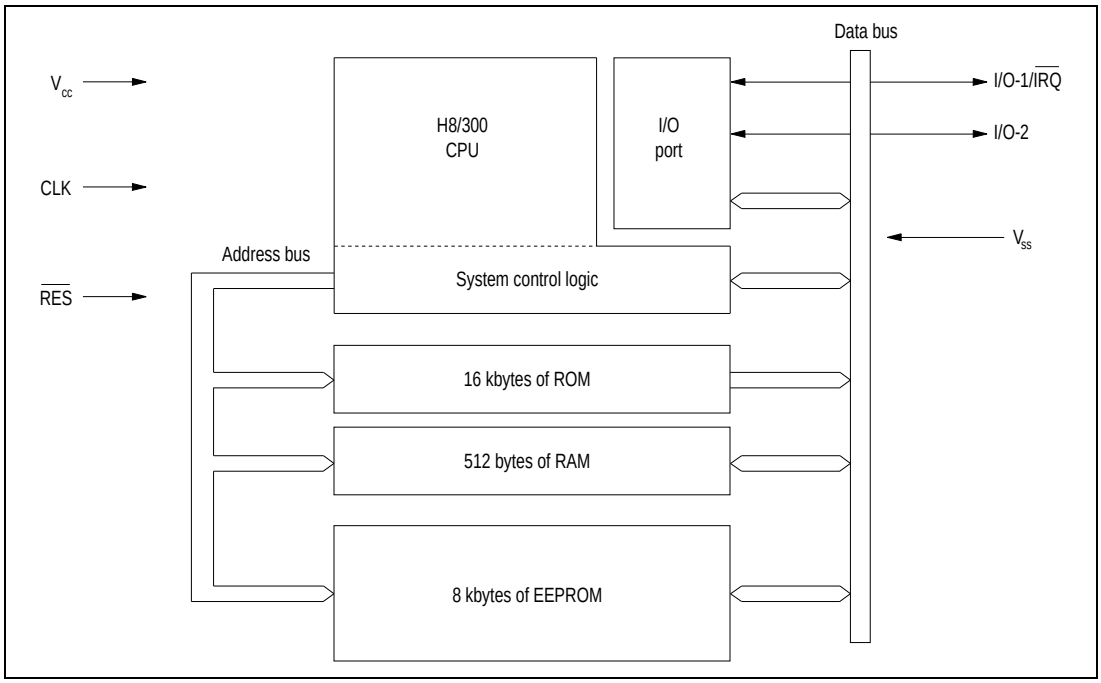
- Bidirectional I/O Pin(s)
  - One on H8/310; two on H8/3101 and H8/3102
- Security
  - ROM data security features
  - Protection against accident writing/erasing of EEPROM
- Operating speed
  - Top operating clock speed of 5 MHz (based on external clock frequency of 10 MHz)
- Low-voltage (3 V) version available
  - H8/3102

- Packages & supply formats
  - COBs
  - Chips
  - SOP-10 (H8/3101 only)
  - Wafers

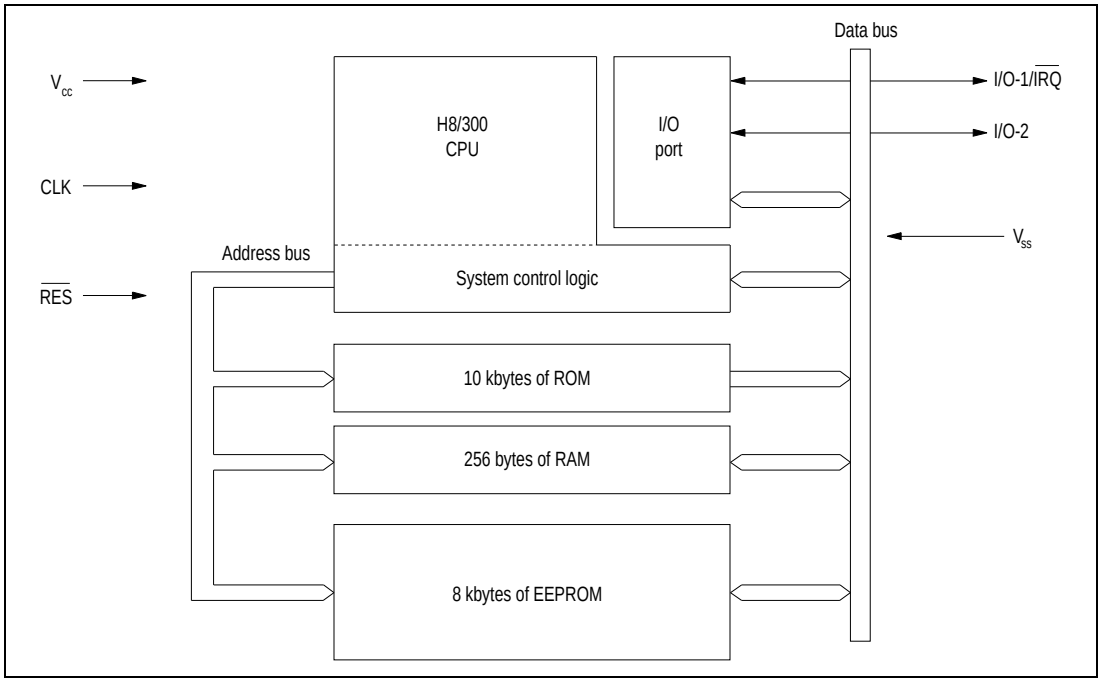
Block Diagram (H8/310)



Block Diagram (H8/3101)



Block Diagram (H8/3102)



7.2 H8/325 Series

This Series, built around the H8/300 CPU, features a choice of six ROM/RAM configurations (60 k/2 k, 48 k/2 k, 32 k/1 k, 24 k/1 k, 16 k/512, and 8 k/256) plus onboard peripherals required by many applications: two different timers, a serial communications interface, seven I/O ports, a parallel handshake interface.

Series Members

H8/3257, H8/3256, H8/325, H8/324, H8/323, H8/322

Features

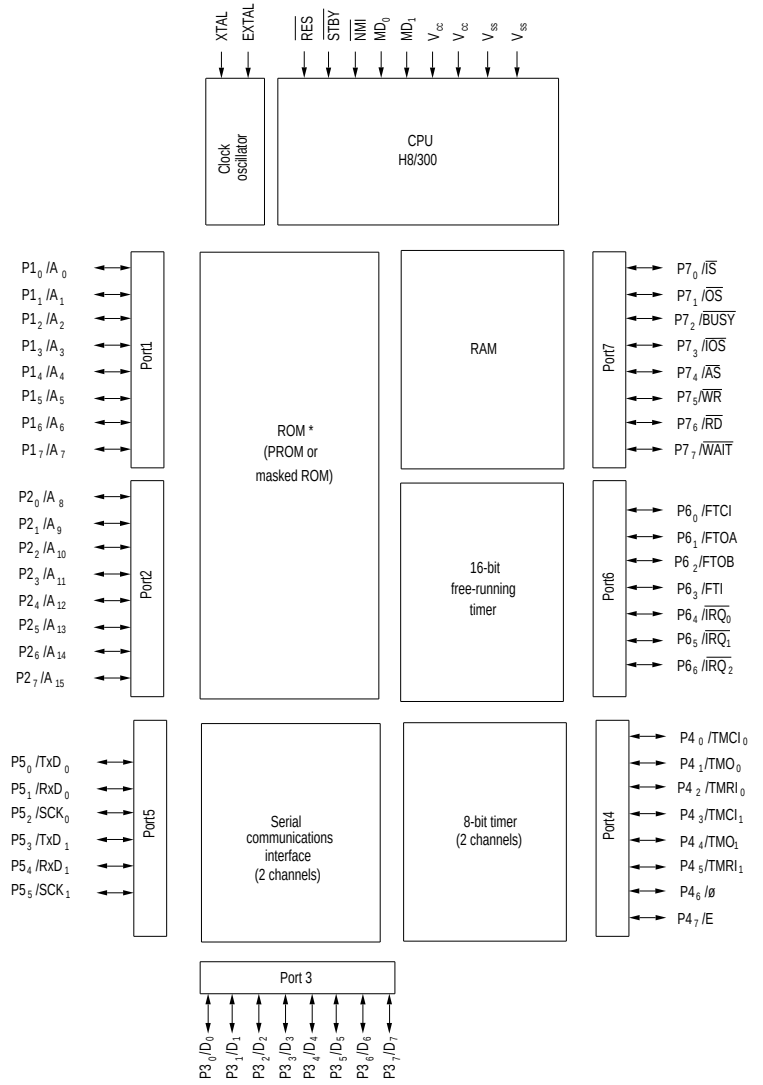
- Onboard memory (unit: bytes)

	H8/3257	H8/3256	H8/325	H8/324	H8/323	H8/322
ROM	60 k	48 k	32 k	24 k	16 k	8 k
RAM	2 k	2 k	1 k	1 k	512	256

- 16-bit free-running timer (1 channel)
  - — One 16-bit free-running timer
    Note: This may be used as an external event counter.
  - — Two output compare output pins
  - — One input capture input pin
- 8-bit multifunction timer (2 channels)
  - — One 8-bit up counter
    Note: This may be used as an external event counter.
  - — Two time constant registers
  - — One timer output
- Serial communications interface (Type 1, 2 channels)
  - — Choice of asynchronous or synchronous operation
  - — Support for full-duplex operation
  - — Onboard baud rate generator

- Seven I/O ports
  - — Parallel handshake interface (Port 3)
  - — 53 bidirectional I/O pins
    - a. 16 pins for driving LEDs
    - b. Software-programmable pull-up resistors on all pins
- Interrupts
  - — 4 external interrupt pins ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)
  - — 17 internal interrupts
- Operating modes
  - — Mode 1: Enhanced mode with onboard ROM disabled
  - — Mode 2: Enhanced mode with onboard ROM enabled
  - — Mode 3: Single-chip mode
- Power conservation modes
  - — Sleep mode
  - — Software standby mode
  - — Hardware standby mode
- Support for output synchronized with E clock
- Clock oscillator
  - — Top operating speed of 10 MHz (based on oscillator frequency of 20 MHz)
- Low-voltage (3 V) versions available
  - — H8/3257, H8/3256
- Packages
  - — 64-pin plastic shrink DIP (DP-64S)
  - — 64-pin ceramic shrink DIP with view port (DC-64S) (H8/3257 and H8/325 only)
  - — 64-pin plastic QFP (FP-64A)
  - — 68-pin PLCC (CP-68)

Block Diagram



Note: * Masked ROM versions only for H8/324.

7.3 H8/329 Series

This Series, built around the H8/300 CPU, features a choice of four ROM/RAM configurations (32 k/1 k, 24 k/1 k, 16 k/512, and 8 k/256) plus onboard peripherals required by many applications: two different timers, a serial communications interface, an A/D converter, and seven I/O ports.

Series Members

H8/329, H8/328, H8/327, H8/326

Features

- Onboard memory (unit: bytes)

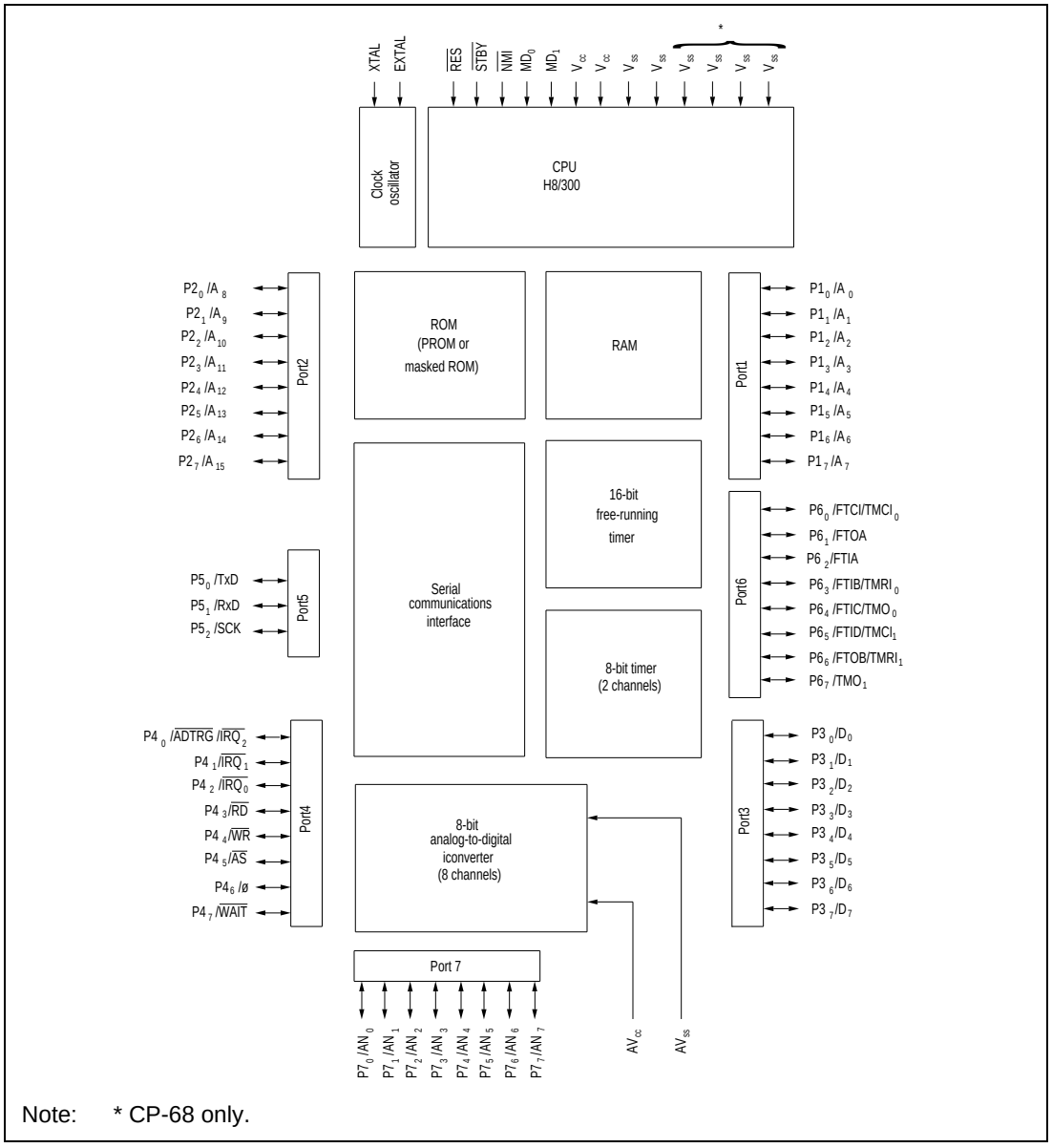
	H8/329	H8/328*	H8/327	H8/326*
ROM	32 k	24 k	16 k	8 k
RAM	1 k	1 k	512	256

Note: * Masked ROM versions only.

- 16-bit free-running timer (1 channel)
  - — One 16-bit free-running timer
    Note: This may be used as an external event counter.
  - — Two output compare output pins
  - — Four input capture input pins (with support for buffered operation)
- 8-bit multifunction timer (2 channels)
  - — One 8-bit up counter
    Note: This may be used as an external event counter.
  - — Two time constant registers
  - — One timer output
- Serial communications interface (Type 2, 2 channels)
  - — Choice of asynchronous or synchronous operation
  - — Support for full-duplex operation
  - — Onboard baud rate generator

- A/D converter
  - — Resolution: 8 bits
  - — 8 channels (Choice of single-channel and scan modes)
  - — Support for initiating processing with an external trigger
  - — Built-in sample and hold circuit
- Seven I/O ports
  - — 43 bidirectional I/0 pins
    - a.16 pins for driving LEDs
    - b.Software-programmable pull-up resistors on 24 pins
  - — 8 unidirectional input pins
- Interrupts
  - — 4 external interrupt pins ($\overline{\text{NMI}}$, $\overline{\text{IRQ}_0}$ to $\overline{\text{IRQ}_2}$)
  - — 18 internal interrupts
- Operating modes
  - — Mode 1: Enhanced mode with onboard ROM disabled
  - — Mode 2: Enhanced mode with onboard ROM enabled
  - — Mode 3: Single-chip mode
- Power conservation modes
  - — Sleep mode
  - — Software standby mode
  - — Hardware standby mode
- Clock oscillator
  - — Maximum clock rate of 10 MHz (based on oscillator frequency of 20 MHz)
- Low-voltage (3 V) versions available
  - — H8/329, H8/328, H8/327, H8/326
- Packages
  - — 64-pin plastic shrink DIP (DP-64S)
  - — 64-pin ceramic shrink DIP with view port (DC-64S) (H8/329 and H8/327 only)
  - — 64-pin plastic QFP (FP-64A)
  - — 64-pin PLCC (CP-68)

Block Diagram



Note: * CP-68 only.

7.4 H8/3297 Series

This Series, built around the H8/300 CPU, features a choice of four ROM/RAM configurations (64 k/2 k, 48 k/2 k, 32 k/1 k, and 16 k/512) plus onboard peripherals required by many applications: three different timers, a serial communications interface, an A/D converter, and seven I/O ports.

Series Members

H8/3297, H8/3296, H8/3294, H8/3292

Features

- Onboard memory (unit: bytes)

	H8/3297	H8/3296*	H8/3294	H8/3292*
ROM	60 k	48 k	32 k	16 k
RAM	2 k	2 k	1 k	512

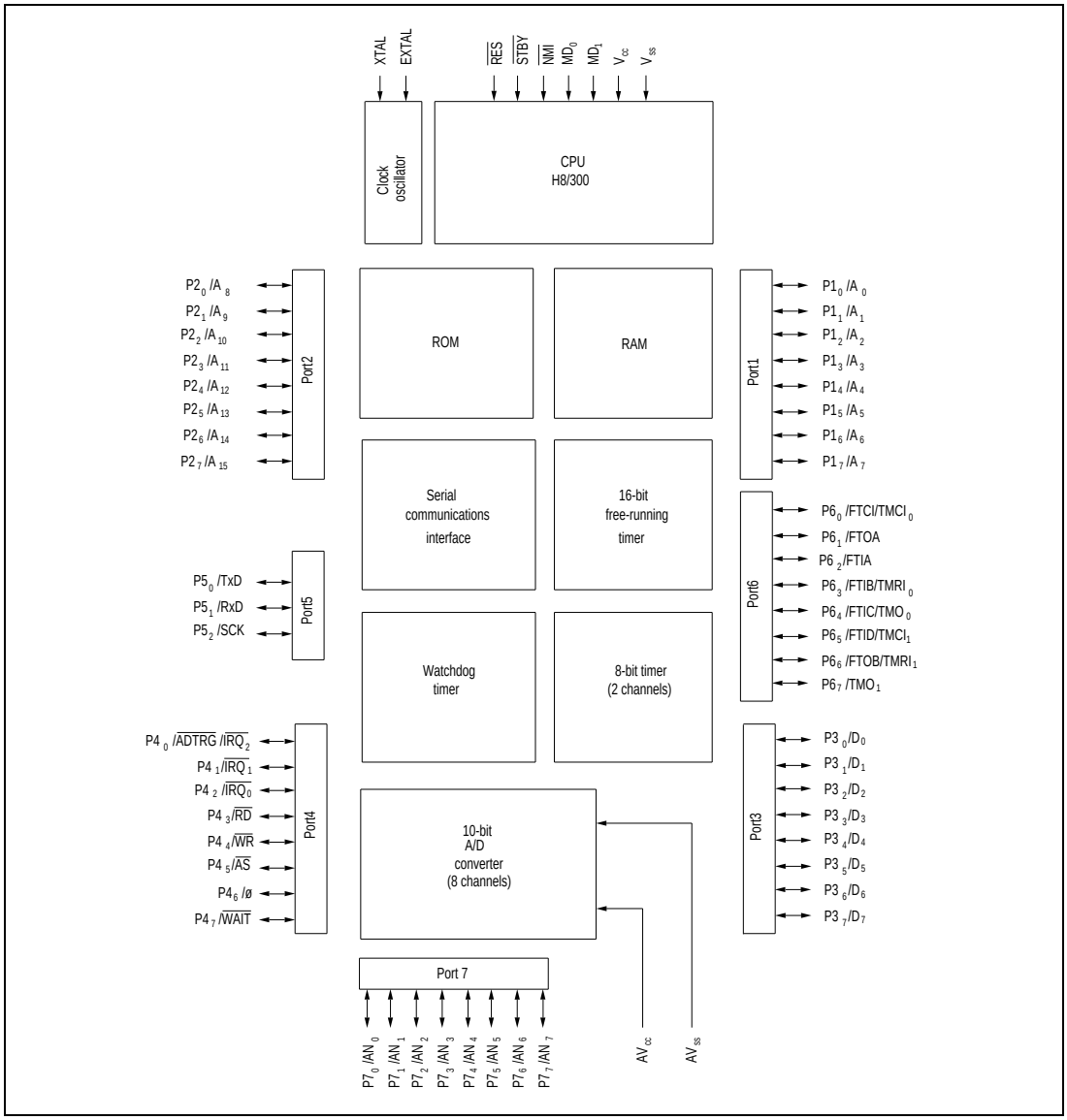
Note: *Masked ROM versions only.

- 16-bit free-running timer (1 channel)
  - — One 16-bit free-running timer
    Note: This may be used as an external event counter.
  - — One output compare output pin
  - — Four input capture input pins (with support for buffered operation)
- 8-bit multifunction timer (2 channels)
  - — One 8-bit up counter
    Note: This may be used as an external event counter.
  - — Two time constant registers
  - — One timer output
- Watchdog timer (1 channel)
  - — Choice of watchdog timer and interval timer operation
- Serial communications interface (Type 2, 1 channel)
  - — Choice of asynchronous or synchronous operation
  - — Support for full-duplex operation
  - — Onboard baud rate generator

- A/D converter
  - — Resolution: 10 bits
  - — 8 channels (Choice of single-channel and scan modes)
  - — Support for initiating processing with an external trigger
  - — Built-in sample and hold circuit
- Wait state controller
  - — Choice of three operating modes: programmable wait mode, pin wait mode, pin auto wait mode
- Seven I/O ports
  - — 43 bidirectional I/O pins
    - a 6 pins for driving LEDs
    - b Software-programmable pull-up resistors on 24 pins
  - — 8 unidirectional input pins
- Interrupts
  - — 4 external interrupt pins ($\overline{\text{NMI}}$, $\overline{\text{IRQ}_0}$ to $\overline{\text{IRQ}_2}$)
  - — 19 internal interrupts
- Operating modes
  - — Mode 1: Enhanced mode with onboard ROM disabled
  - — Mode 2: Enhanced mode with onboard ROM enabled
  - — Mode 3: Single-chip mode
- Power conservation modes
  - — Sleep mode
  - — Software standby mode
  - — Hardware standby mode
- Clock oscillator
  - — Maximum clock rate of 16 MHz for 5-V operation and 10 MHz for 3-V operation (based on oscillator frequencies of 16 MHz and 10 MHz respectively)
- Low-voltage (3 V) versions available
  - — H8/3297, H8/3296, H8/3294, H8/3292

- Packages
  - — 64-pin plastic shrink DIP (DP-64S)
  - — 64-pin ceramic shrink DIP with view port (DC-64S) (H8/3297 only)
  - — 64-pin plastic QFP (FP-64A)
  - — 80-pin TQFP (TFP-80)

Block Diagram



7.5 H8/350

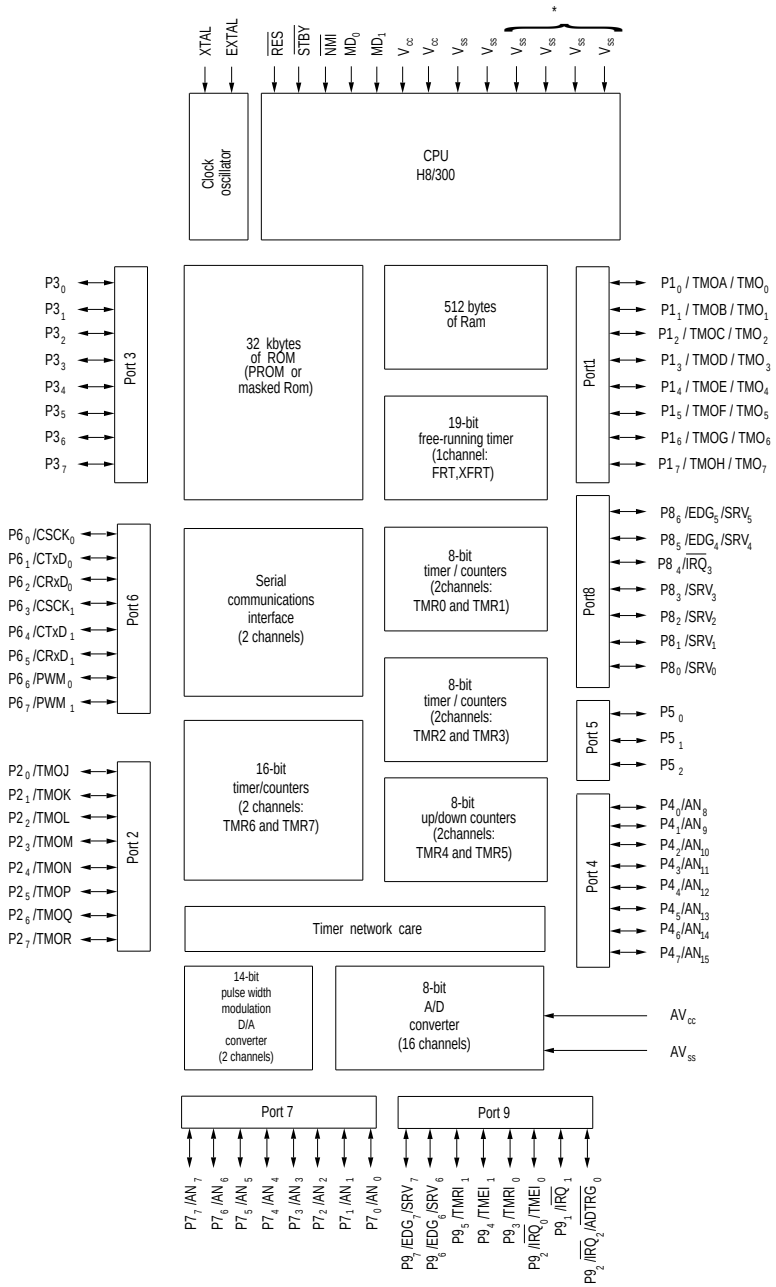
This version, built around the H8/300 CPU, features 32 kbytes of ROM, 512 bytes of RAM, and such onboard peripherals as nine timers, a timer network, a pulse width modulation D/A converter, a serial communications interface, an A/D converter, and nine I/O ports.

Features

- Onboard Memory
  - — 32 kbytes of ROM (PROM or masked ROM)
  - — 512 bytes of RAM
- Nine timers and timer network
  - — 19-bit free-running timer (1 channel)
    - a. Four output compare output pins
    - b. Four input compare input pins
  - — 16-bit timer/counters (2 channels)
    - a. Two output compare output pins
  - — 8-bit up/down counters (2 channels)
    - a. Two output compare output pins
  - — 8-bit timer/counters (4 channels)
    - a. Two output compare output pins
  - — Timer network shift registers: One (8-bit)
  - — Timer network inputs: 12
  - — Timer network outputs: 16
- 14-bit pulse-width modulation D/A converter (2 channels)
  - — Basic carrier pulses plus fine-adjustment pulses
  - — Resolution: 1/16384
  - — Maximum carrier frequency: system clock divided by 500

- Serial communications interface (Type 1, 2 channels)
  - — One 8-bit interface with choice of asynchronous or synchronous operation
    - a. Support for full-duplex operation
    - b. Onboard baud rate generator
  - — One 8/16-bit interface supporting synchronous operation
- A/D converter
  - — Resolution: 8 bits
  - — 16 channels (Choice of single-channel, and scan modes)
  - — Support for initiating processing with an external trigger
  - — Built-in sample and hold circuit
- Nine I/O ports
  - — 50 bidirectional I/O pins
    - a. 16 pins for driving LEDs
    - b. Software-programmable pull-up resistors on all pins
  - — 16 unidirectional input pins
- Interrupts
  - — 9 external interrupt pins ($\overline{\text{NMI}}$, $\overline{\text{IRQ}_0}$ to $\overline{\text{IRQ}_3}$, EDG4 to EDG7)
  - — 19 internal interrupts
- Operating modes
  - — Mode 3: Single-chip mode
- Power conservation modes
  - — Sleep mode
  - — Software standby mode
  - — Hardware standby mode
- Clock oscillator
  - — Top operating clock speed of 10 MHz (based on oscillator frequency of 20 MHz)
- Packages
  - — 80-pin plastic QFP (FP-80A)
  - — 84-pin PLCC (CP-84)
  - — 84-pin LCC with view port (CG-84)

Block Diagram



Note: * CP-84 and CG-84 versions only.

7.6 H8/330

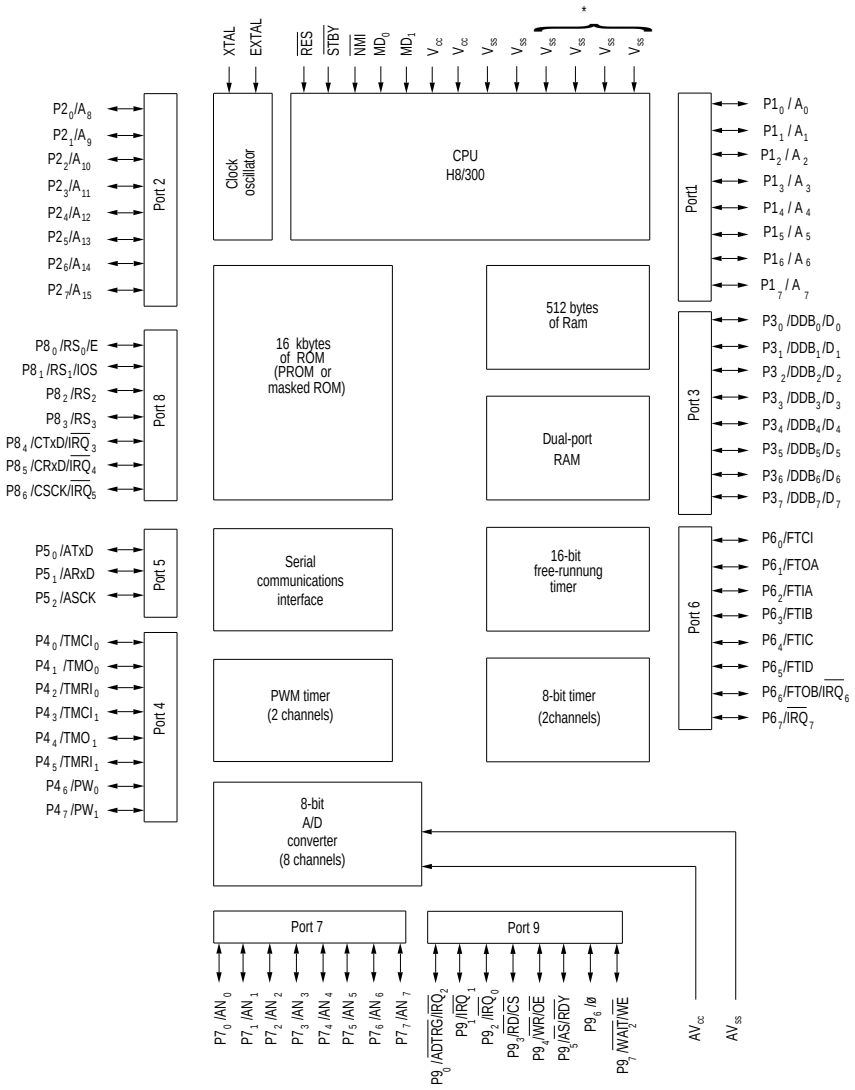
This version, built around the H8/300 CPU, features 16 kbytes of ROM, 512 bytes of RAM, and onboard peripherals required by many applications: three different timers, a serial communications interface, dual-port RAM, an A/D converter, and nine I/O ports.

Features

- Onboard Memory
  - — 16 kbytes of PROM
  - — 512 bytes of RAM
  - — Onboard dual-port RAM
    - a. One byte as a control register plus 15 bytes as data registers
    - b. Simple protocol for managing communications between the master and slave
- 16-bit free-running timer (1 channel)
  - — One 16-bit free-running timer
    - Note: This may be used as an external event counter.
  - — Two output compare output pins
  - — Four input capture input pins (with support for buffered operation)
- 8-bit multifunction timer (2 channels)
  - — One 8-bit up counter
    - Note: This may be used as an external event counter.
  - — Two time constant registers
  - — One timer output
- 8-bit pulse-width modulation timer (2 channels)
  - — Duty: 0% to 100%
  - — Resolution: 1/250
  - — Maximum carrier frequency: system clock divided by 500
- Serial communications interface (Type 1, 1 channel)
  - — Choice of asynchronous or synchronous operation
  - — Support for full-duplex operation
  - — Onboard baud rate generator

- A/D converter
  - Resolution: 8 bits
  - 8 channels (Choice of single-channel and scan modes)
  - Support for initiating processing with an external trigger
  - Built-in sample and hold circuit
- Nine I/O ports
  - 58 bidirectional I/O pins
    a. 16 pins for driving LEDs
    b. Software-programmable pull-up resistors on all pins
  - 8 unidirectional input pins
- Interrupts
  - 9 external interrupt pins ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)
  - 19 internal interrupts
- Operating modes
  - Mode 1: Enhanced mode with onboard ROM disabled
  - Mode 2: Enhanced mode with onboard ROM enabled
  - Mode 3: Single-chip mode
- Power conservation modes
  - Sleep mode
  - Software standby mode
  - Hardware standby mode
- Support for output synchronized with E clock
- Clock oscillator
  - Maximum clock rate of 10 MHz (based on oscillator frequency of 20 MHz)
- Packages
  - 80-pin plastic QFP (FP-80A)
  - 84-pin PLCC (CP-84)
  - 84-pin LCC with view port (CG-84)

Block Diagram



Note * CP-84 and CG-84 versions only.

7.7 H8/3314

This version, built around the H8/300 CPU, features 32 kbytes of ROM, 1 kbyte of RAM, and onboard peripherals required by many applications: three different timers, a serial communications interface, a data transfer unit (DTU/PBI) supporting 256 bytes of dual-port RAM, an A/D converter, and nine I/O ports.

Features

- Onboard Memory
  - 32 kbytes of PROM
  - 1 kilobyte of RAM
- Data transfer unit (4 channels)
  - Single-address PBI transfers over the R channel
  - Choice of PBI or I/O transfers over channels A and B
  - Dual-address I/O transfers over the C channel

Note: PBI stands for parallel buffer interface.

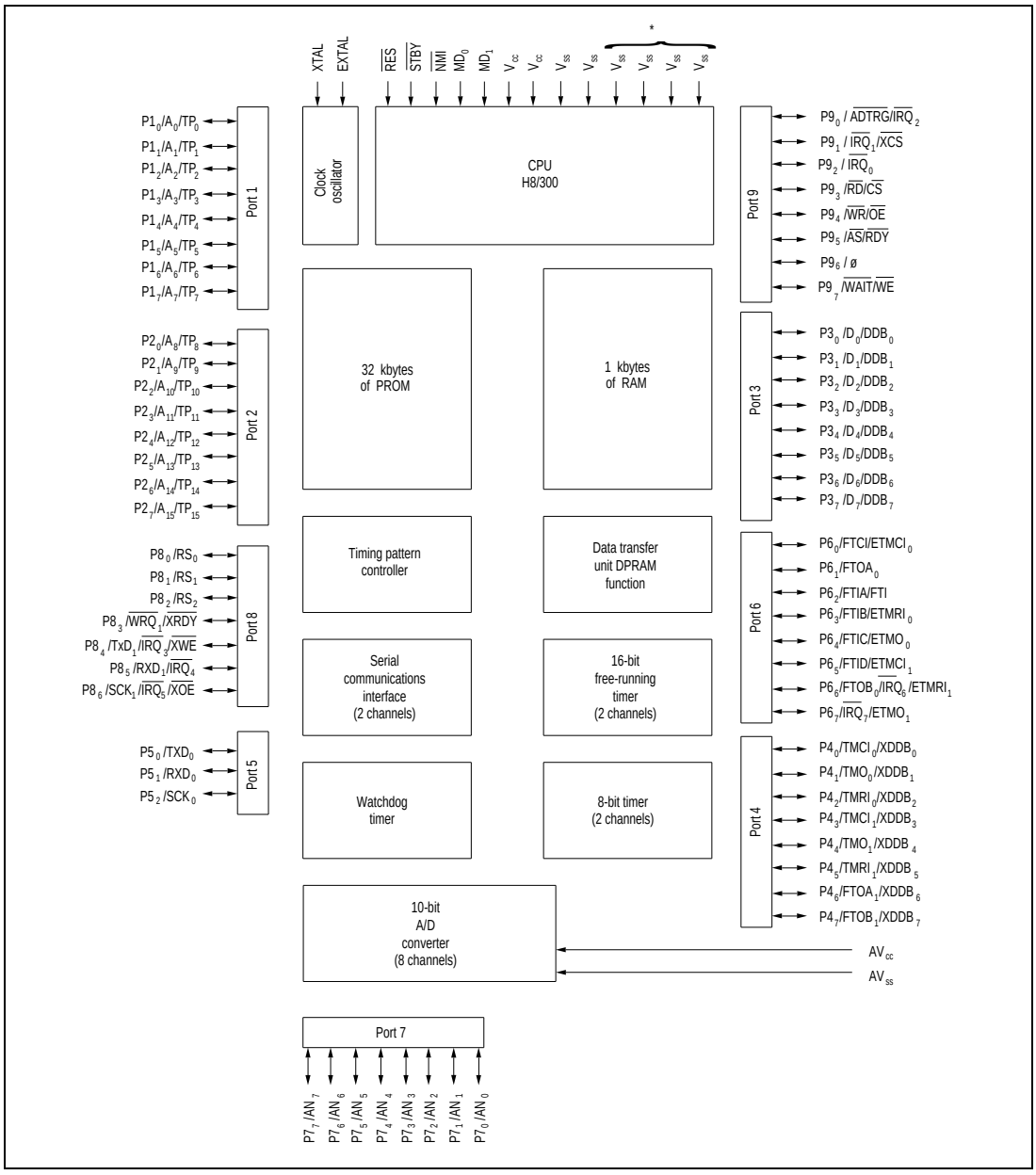
- Together, the data transfer unit and parallel buffer interface provide external devices easy read/write access to up to 256 bytes of onboard RAM as dual-port RAM.
- 16-bit free-running timer (2 channels)
  - One 16-bit free-running timer
    Note: This may be used as an external event counter.
  - Two output compare output pins
  - Channel 0: Four input capture input pins (with support for buffered operation)
  - Channel 1: One input capture input pin
- 8-bit multifunction timer (2 channels)
  - One 8-bit up counter
    Note: This may be used as an external event counter.
  - Two time constant registers
  - One timer output
- Programmable timing pattern controller
  - Up to 16 bits of data output using a time base from a 16-bit free-running timer

— Maximum of four groups of four bits each (support for one 16-bit group, two 8-bit groups, etc.)
— Nonoverlapping operation option
— Support for data output via data transfer unit

- Watchdog timer (1 channel)
  — Choice of watchdog timer and interval timer operation
- Serial communications interface (Type 2, 2 channels)
  — Choice of asynchronous or synchronous operation
  — Support for full-duplex operation
  — Onboard baud rate generator
- A/D converter
  — Resolution: 10 bits
  — 8 channels (Choice of single-channel and scan modes)
  — Support for initiating processing with an external trigger
  — Built-in sample and hold circuit
- Nine I/O ports
  — 58 bidirectional I/O pins
    a. 16 pins for driving LEDs
    b. Software-programmable pull-up resistors on 24 pins
  — 8 unidirectional input pins
- Interrupts
  — 9 external interrupt pins $\overline{\text{NMI}}$, $\overline{\text{IRQ}_0}$ to $\overline{\text{IRQ}_7}$)
  — 33 Internal interrupts
- Operating modes
  — Mode 1: Enhanced mode with onboard ROM disabled
  — Mode 2: Enhanced mode with onboard ROM enabled
  — Mode 3: Single-chip mode
- Power conservation modes
  — Sleep mode
  — Software standby mode
  — Hardware standby mode

- Clock oscillator
  - Maximum clock rate speed of 10 MHz (based on oscillator frequency of 20 MHz)
- Packages
  - 80-pin plastic QFP (FP-80A)
  - 84-pin PLCC (CP-84)

Block Diagram



7.8 H8/338 Series

This Series, built around the H8/300 CPU, features a choice of three ROM/RAM configurations (48 k/2 k, 32 k/1 k, and 24 k/1 k) plus onboard peripherals required by many applications: three different timers, a serial communications interface, an A/D converter, a D/A converter, and seven I/O ports.

Series Members

H8/338, H8/337, H8/336

Features

- Onboard memory (unit: bytes)

	H8/338	H8/337	H8/336*
ROM	48 k	32 k	24 k
RAM	2 k	1 k	1 k

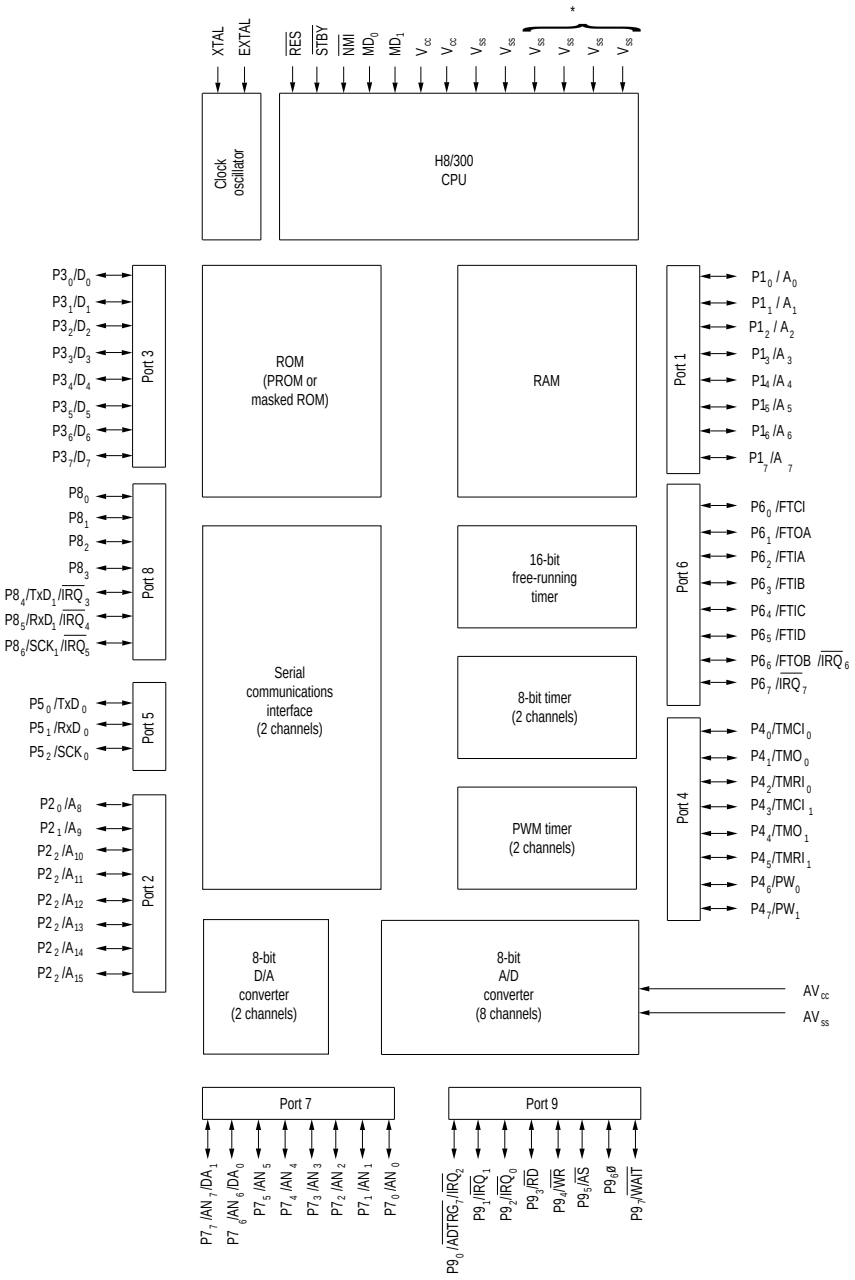
Note: * Masked ROM versions only.

- 16-bit free-running timer (1 channel)
  - — One 16-bit free-running timer
    Note: This may be used as an external event counter.
  - — Two output compare output pins
  - — Four input capture input pins (with support for buffered operation)
- 8-bit multifunction timer (2 channels)
  - — One 8-bit up counter
    Note: This may be used as an external event counter.
  - — Two time constant registers
  - — One timer output
- 8-bit pulse-width modulation timer (2 channels)
  - — Duty: 0% to 100%
  - — Resolution: 1/250
  - — Maximum carrier frequency: system clock divided by 500

- Serial communications interface (Type 2, 2 channels)
  - — Choice of asynchronous or synchronous operation
  - — Support for full-duplex operation
  - — Onboard baud rate generator
- A/D converter
  - — Resolution: 8 bits
  - — 8 channels (Choice of single-channel and scan modes)
  - — Support for initiating processing with an external trigger
  - — Built-in sample and hold circuit
- D/A converter
  - — Resolution: 8 bits
  - — Two channels of analog output
- Seven I/O ports
  - — 58 bidirectional I/O pins
    - a. 16 pins for driving LEDs
    - b. Software-programmable pull-up resistors on 24 pins
  - — 8 unidirectional input pins
- Interrupts
  - — 9 external interrupt pins ($\overline{\text{NMI}}$, $\overline{\text{IRQ}_0}$ to $\overline{\text{IRQ}_7}$)
  - — 22 internal interrupts
- Operating modes
  - — Mode 1: Enhanced mode with onboard ROM disabled
  - — Mode 2: Enhanced mode with onboard ROM enabled
  - — Mode 3: Single-chip mode
- Power conservation modes
  - — Sleep mode
  - — Software standby mode
  - — Hardware standby mode
- Clock oscillator
  - — Maximum clock rate of 10 MHz (based on oscillator frequency of 20 MHz)

- Low-voltage (3 V) versions available
  - H8/338, H8/337, H8/336
- Packages
  - 80-pin plastic QFP (FP-80A)
  - 84-pin PLCC (CP-84)
  - 84-pin LCC with view port (CG-84) (H8/338 and H8/337 only)

Block Diagram



Note: * CP-84 and CG-84 versions only.

7.9 H8/3334 Series

This Series, built around the H8/300 CPU, features a choice of two ROM/RAM configurations (32 k/1 k and 16 k/512) plus onboard peripherals required by many applications: four different timers, a serial communications interface, an A/D converter, a host interface, and nine I/O ports.

Series Members

H8/3334, H8/3332

Features

- Onboard memory (unit: bytes)

	H8/3334	H8/3332
ROM	32 k	16 k
RAM	1 k	512

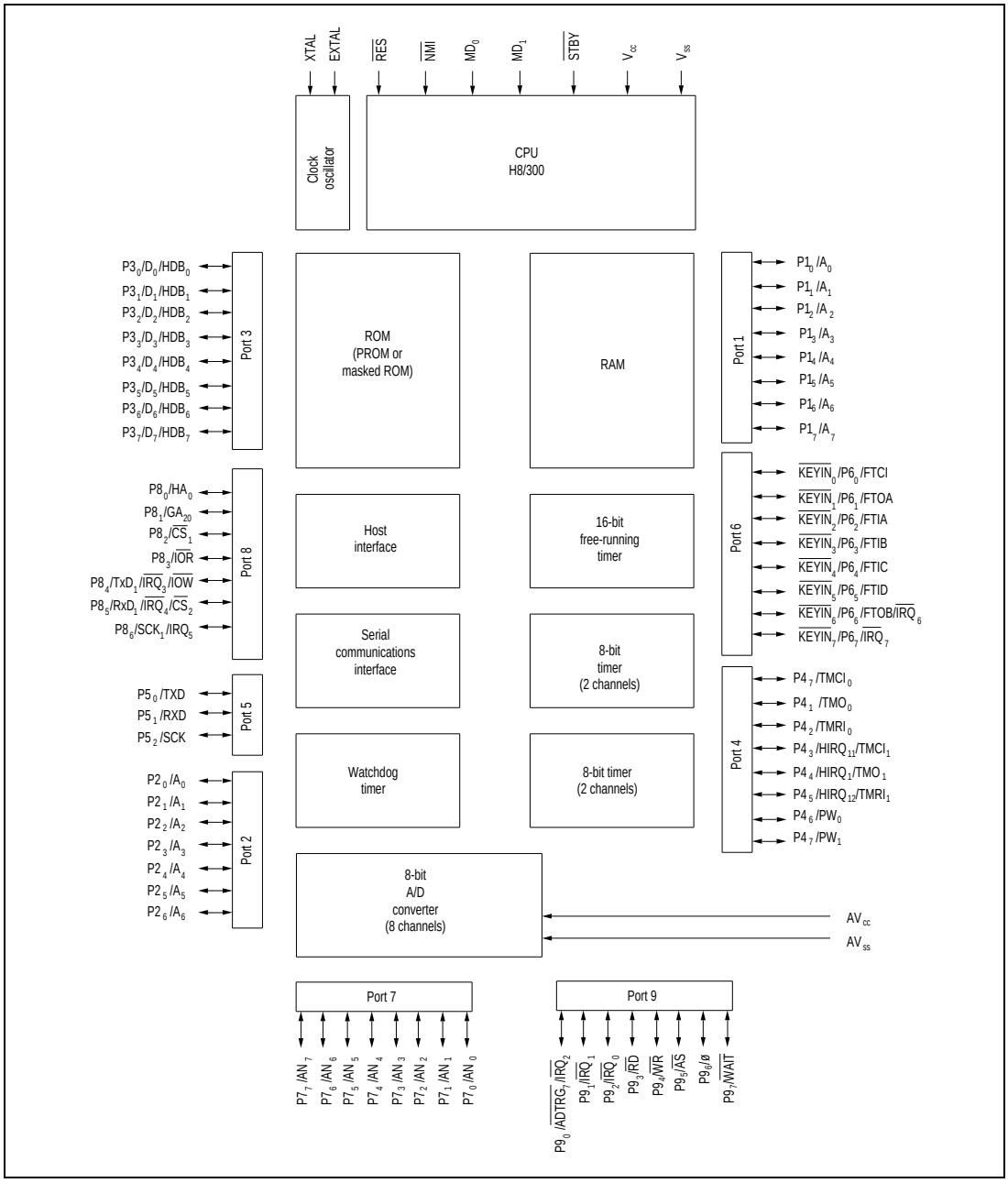
- 16-bit free-running timer (1 channel)
  - — One 16-bit free-running timer
    Note: This may be used as an external event counter.
  - — Two output compare output pins
  - — Four input capture input pins (with support for buffered operation)
- 8-bit multifunction timer (2 channels)
  - — One 8-bit up counter
    Note: This may be used as an external event counter.
  - — Two time constant registers
  - — One timer output
- 8-bit pulse-width modulation timer (2 channels)
  - — Duty: 0% to 100%
  - — Resolution: 1/250
  - — Maximum carrier frequency: system clock divided by 500
- Watchdog timer (1 channel)
  - — Choice of watchdog timer and interval timer operation

- Serial communications interface (Type 2, 1 channel)
  - — Choice of asynchronous or synchronous operation
  - — Support for full-duplex operation
  - — Onboard baud rate generator
- A/D converter
  - — Resolution: 8 bits
  - — 8 channels (Choice of single-channel and scan modes)
  - — Support for initiating processing with an external trigger
  - — Built-in sample and hold circuit
- Host interface
  - — 8-bit host interface port
  - — Three host interrupts (HIRQ1, HIRQ2, HIRQ3)
  - — Choice of normal and high-speed GATE A20 output
- Keyboard controller
  - — Controls matrix keyboard with configuration supporting keyboard scan with both wake-up and sense port interrupts
- Nine I/O ports
  - — 58 bidirectional I/O pins
    - a. 16 pins for driving LEDs
    - b. Software-programmable pull-up resistors on 25 pins
  - — 8 unidirectional input pins
- Interrupts
  - — 9 external interrupt pins ($\overline{\text{NMI}}$, $\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_7$)
  - — 21 internal interrupts
  - — 8 key sense interrupts pins

    Note: These share the $\overline{\text{IRQ}}_6$ interrupt vector and wake the chip from the software standby mode.
- Operating modes
  - — Mode 1: Enhanced mode with onboard ROM disabled
  - — Mode 2: Enhanced mode with onboard ROM enabled
  - — Mode 3: Single-chip mode

- Power conservation modes
  - Sleep mode
  - Software standby mode
  - Hardware standby mode
- Clock oscillator
  - Maximum clock rate of 10 MHz (based on oscillator frequency of 20 MHz)
- Low-voltage (3 V) versions available
  - H8/3334, H8/3332
- Packages
  - 80-pin TQFP (TFP-80C)
  - 80-pin plastic QFP (FP-80A)
  - 84-pin PLCC (CP-84)
  - 84-pin LCC with view port (CG-84) (H8/3334 only)

Block Diagram



7.10 H8/3337 Series

This Series, built around the H8/300 CPU, features a choice of three ROM/RAM configurations (60 k/2 k, 48 k/2 k, and 32k/1 k) plus onboard peripherals required by many applications: four different timers, a serial communications interface, an A/D converter, a D/A converter, a host interface, and nine I/O ports.

Also available is an F-ZTAT™ version with onboard flash memory that the application system can rewrite.

Series Members

H8/3337Y, H8/3336Y, H8/3334Y

Features

- Onboard memory (unit: bytes)

	H8/3337Y	H8/3336Y*[1]	H8/3334Y*[2]
ROM	60 k	48 k	32 k
RAM	2 k	2 k	1 k

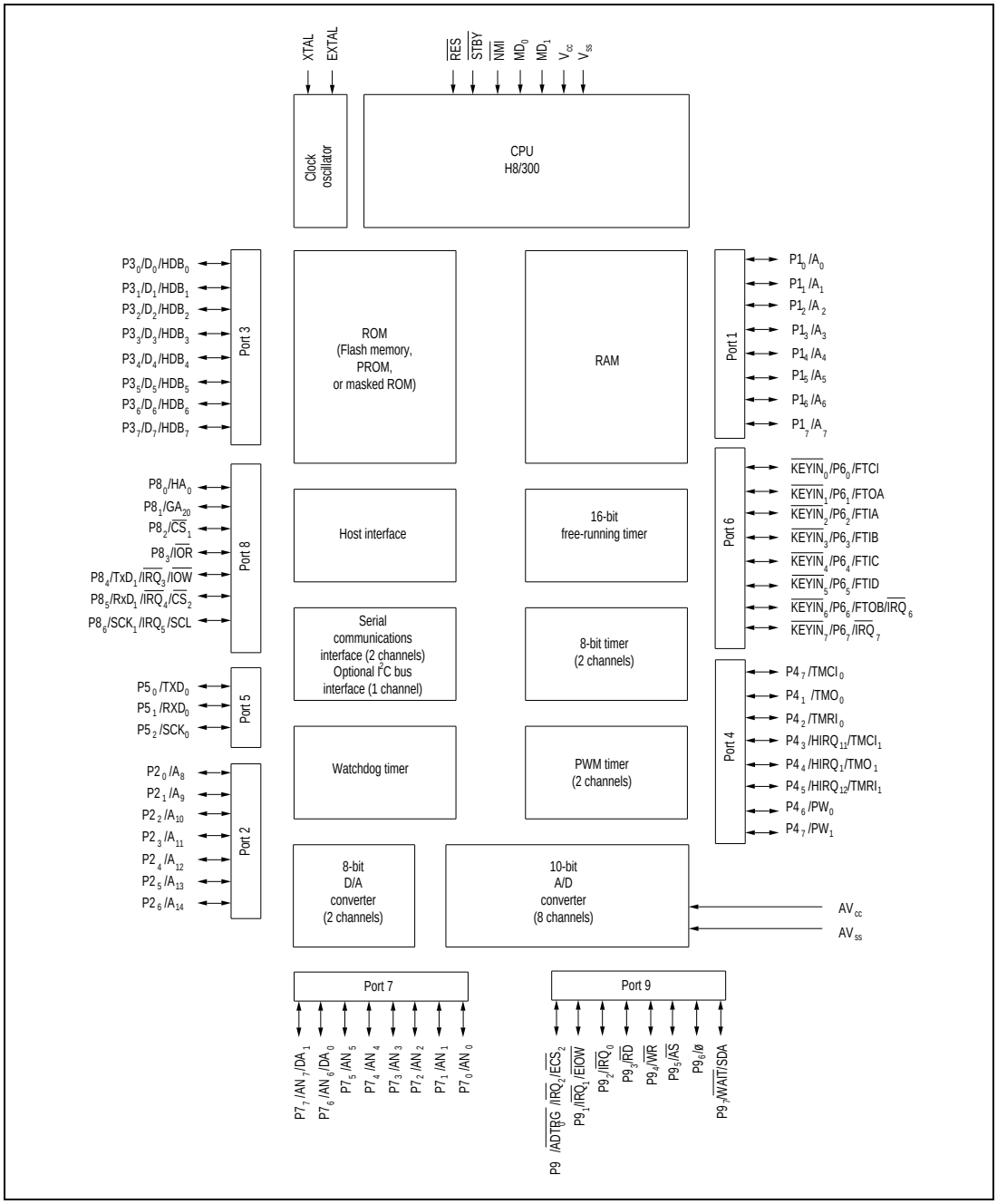
Notes: 1. Masked ROM version only.
2. F-ZTAT™ version also available.

- 16-bit free-running timer (1 channel)
  - — One 16-bit free-running timer
    Note: This may be used as an external event counter.
  - — Two output compare output pins
  - — Four input capture input pins (with support for buffered operation)
- 8-bit multifunction timer (2 channels)
  - — One 8-bit up counter
    Note: This may be used as an external event counter.
  - — Two time constant registers
  - — One timer output
- 8-bit pulse-width modulation timer (2 channels)
  - — Duty: 0% to 100%
  - — Resolution: 1/250
  - — Maximum carrier frequency: system clock divided by 500

- Watchdog timer (1 channel)
  - Choice of watchdog timer and interval timer operation
- Serial communications interface (Type 2, 2 channels)
  - Choice of asynchronous or synchronous operation
  - Support for full-duplex operation
  - Onboard baud rate generator
- Optional I^2C bus interface (1 channel)
  - Compatible with the Philips Inter IC (I2C) bus interface
  - Choice of single master and slave modes
- A/D converter
  - Resolution: 10 bits
  - 8 channels (Choice of single-channel and scan modes)
  - Support for initiating processing with an external trigger
  - Built-in sample and hold circuit
- D/A converter
  - Resolution: 8 bits
  - Two channels of analog output
- Host interface
  - 8-bit host interface port
  - Three host interrupts (HIRQ1, HIRQ2, HIRQ3)
  - Choice of normal and high-speed GATE A20 output
- Keyboard controller
  - Controls matrix keyboard with configuration supporting keyboard scan with both wake-up and sense port interrupts
- Wait state controller
  - Choice of three operating modes: programmable wait mode, pin wait mode, pin auto wait mode

- Nine I/O ports
  - 58 bidirectional I/O pins
    a. 16 pins for driving LEDs
    b. Software-programmable pull-up resistors on 32 pins
  - 8 unidirectional input pins
- Interrupts
  - 9 external interrupt pins ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)
  - 26 internal interrupts
  - 8 key sense interrupt pins
    Note: These share the $\overline{IRQ_6}$ interrupt vector and wake the chip from the software standby mode.
- Operating modes
  - Mode 1: Enhanced mode with onboard ROM disabled
  - Mode 2: Enhanced mode with onboard ROM enabled
  - Mode 3: Single-chip mode
- Power conservation modes
  - Sleep mode
  - Software standby mode
  - Hardware standby mode
- Clock oscillator
  - Maximum clock rate of 16 MHz for 5-V operation and 10 MHz for 3-V operation (based on oscillator frequencies of 16 MHz and 10 MHz respectively)
- Low-voltage (3 V) versions available
  - H8/3337Y, H8/3336Y, H8/3334Y
- Packages
  - 80-pin plastic QFP (FP-80A)
  - 80-pin TQFP (TFP-80C)
  - 84-pin PLCC (CP-84)
  - 84-pin LCC with view port (CG-84) (H8/3337Y only)

Block Diagram



7.11 H8/3397 Series

This Series, built around the H8/300 CPU, features a choice of three ROM/RAM configurations (60 k/2 k, 48 k/2 k, and 32 k/1 k) plus onboard peripherals required by many applications: four different timers, a serial communications interface, an A/D converter, and nine I/O ports.

Series Members

H8/3397, H8/3396, H8/3394

Features

- Onboard memory (unit: bytes)

	H8/3397	H8/3396	H8/3394
ROM	60 k	48 k	32 k
RAM	2k	2 k	1k

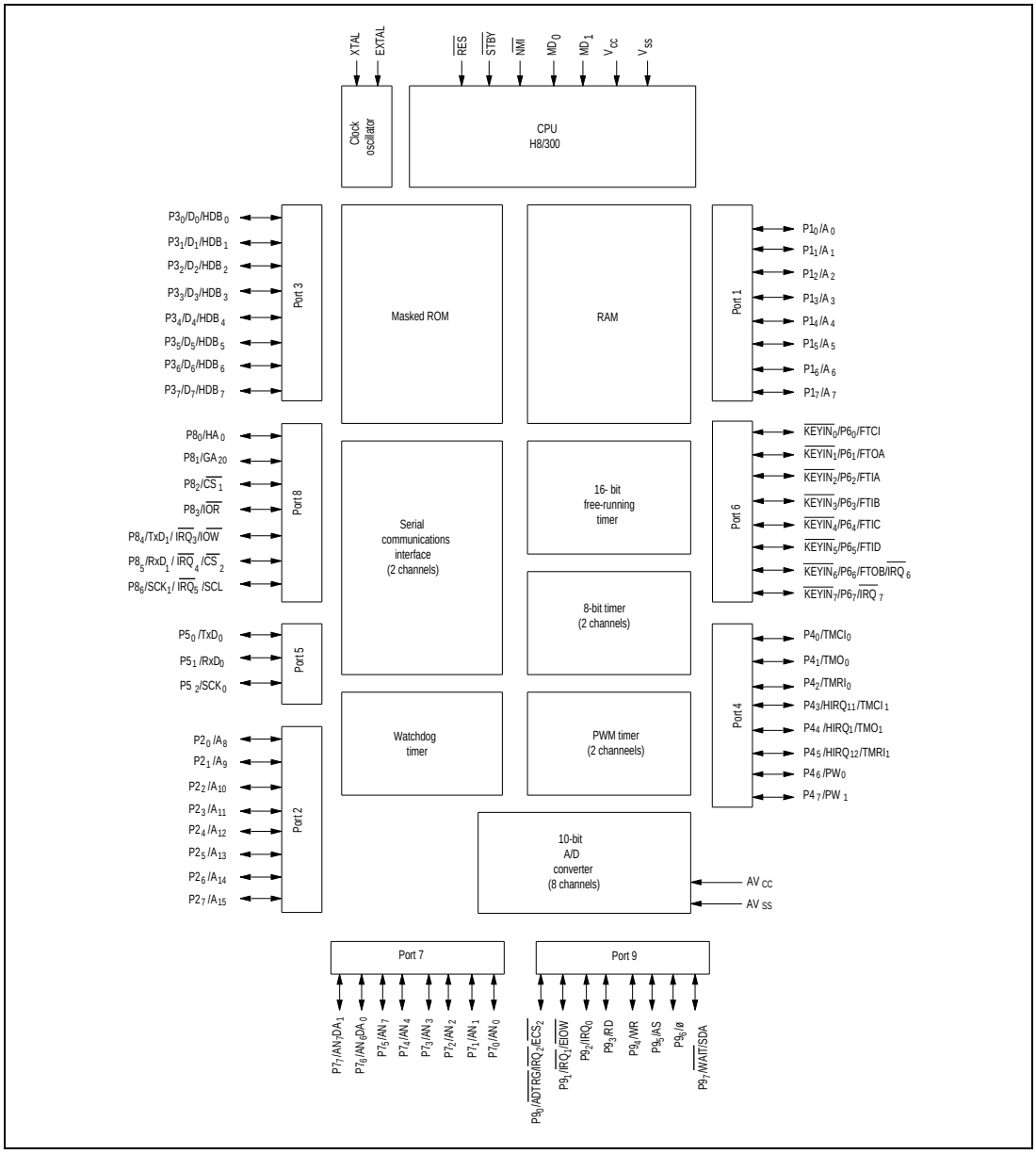
- 16-bit free-running timer (1 channel)
  - — One 16-bit free-running timer
    Note: This may be used as an external event counter.
  - — Two output compare output pins
  - — Four input capture input pins (with support for buffered operation)
- 8-bit multifunction timer (2 channels)
  - — One 8-bit up counter
    Note: This may be used as an external event counter.
  - — Two time constant registers
  - — One timer output
- 8-bit pulse-width modulation timer (2 channels)
  - — Duty: 0% to 100%
  - — Resolution: 1/250
  - — Maximum carrier frequency: system clock divided by 500
- Watchdog timer (1 channel)
  - — Choice of watchdog timer and interval timer operation

- Serial communications interface (Type 2, 2 channels)
  - — Choice of asynchronous or synchronous operation
  - — Support for full-duplex operation
  - — Onboard baud rate generator
- A/D converter
  - — Resolution: 10 bits
  - — 8 channels (Choice of single-channel and scan modes)
  - — Support for initiating processing with an external trigger
  - — Built-in sample and hold circuit
- Keyboard controller
  - — Controls matrix keyboard with configuration supporting keyboard scan with both wake-up sense port interrupts
- Wait state controller
  - — Choice of three operating modes: programmable wait mode, pin wait mode, pin auto wait mode
- Nine I/O ports
  - — 58 bidirectional I/O pins
    - a. 16 pins for driving LEDs
    - b. Software-programmable pull-up resistors on 32 pins
  - — 8 unidirectional input pins
- Interrupts
  - — 9 external interrupt pins ($\overline{\text{NMI}}$, $\overline{\text{IRQ}_0}$ to $\overline{\text{IRQ}_7}$)
  - — 26 internal interrupts
  - — 8 key sense interrupt pins

    Note: These share the $\overline{\text{IRQ}_6}$ interrupt vector and wake the chip from the software standby mode.
- Operating modes
  - — Mode 1: Enhanced mode with onboard ROM disabled
  - — Mode 2: Enhanced mode with onboard ROM enabled
  - — Mode 3: Single-chip mode

- Power conservation modes
  - Sleep mode
  - Software standby mode
  - Hardware standby mode
- Clock oscillator
  - Maximum clock rate of 16 MHz for 5-V operation and 10 MHz for 3-V operation (based on oscillator frequencies of 16 MHz and 10 MHz respectively)
- Low-voltage (3 V) versions available
  - H8/3397, H8/3396, H8/3395
- Packages
  - 80-pin plastic QFP (FP-80A)
  - 80-pin TQFP (TFP-80C)
  - 80-pin PLCC (CP-84)

Block Diagram



7.12 H8/3437 Series

This Series, built around the H8/300 CPU, features a choice of three ROM/RAM configurations (60 k/2 k, 48 k/2 k, and 32 k/ 1 k) plus onboard peripherals required by many applications: four different timers, a serial communications interface, an A/D converter, a D/A converter, a host interface, and nine I/O ports.

Also available is an F-ZTAT™ version with onboard flash memory that the application system can rewrite.

Series Members

H8/3437, H8/3436, H8/3434

Features

- Onboard memory (unit: bytes)

	H8/3437	H8/3436*[1]	H8/3434*[2]
ROM	60 k	48 k	32 k
RAM	2 k	2 k	1 k

Notes: 1. Masked ROM version only.
2. F-ZTAT™ version also available.

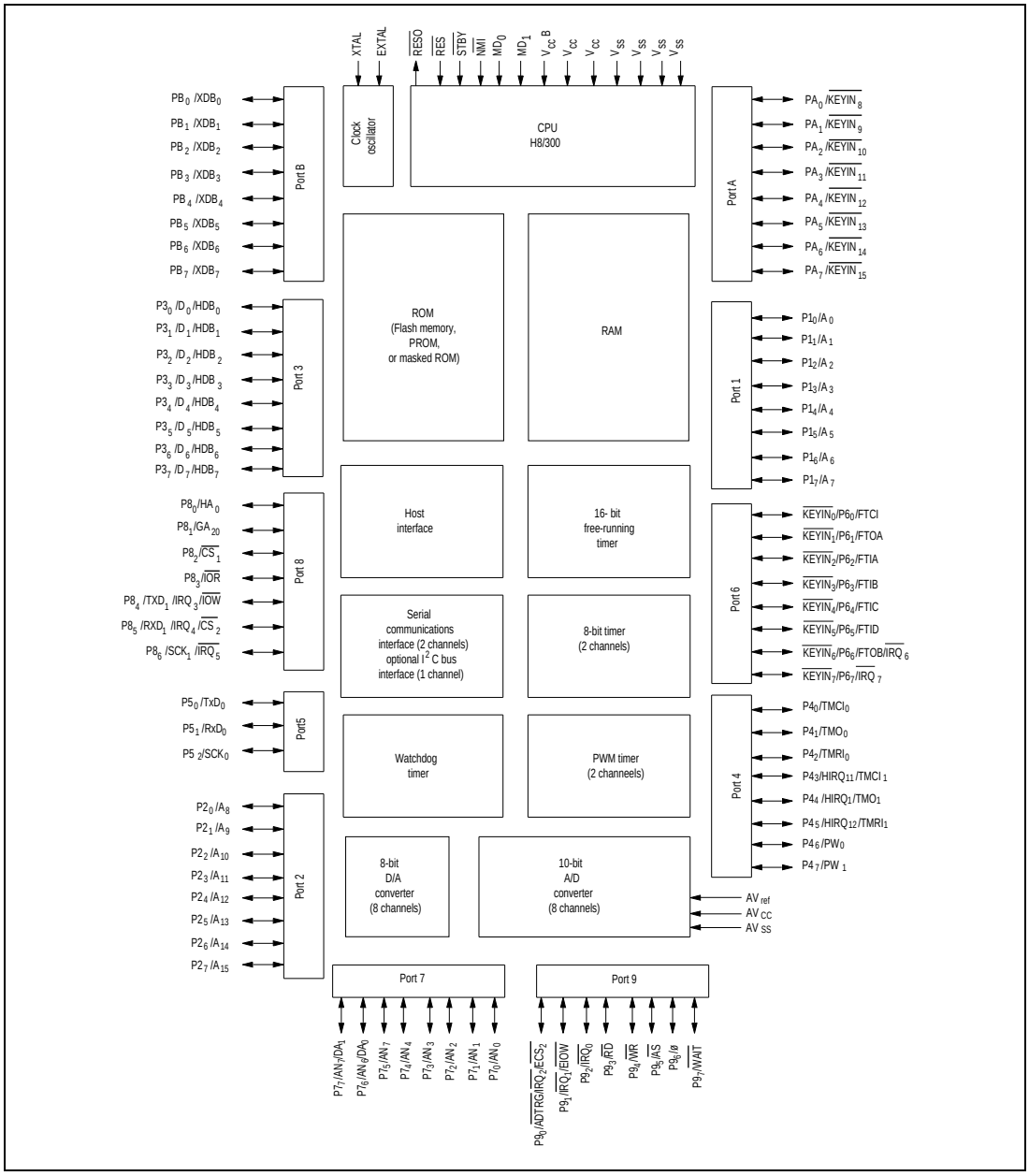
- 16-bit free-running timer (1 channel)
  - — One 16-bit free-running timer
    Note: This may be used as an external event counter.
  - — Two output compare output pins
  - — Four input capture input pins (with support for buffered operation)
- 8-bit multifunction timer (2 channels)
  - — One 8-bit up counter
    Note: This may be used as an external event counter.
  - — Two time constant registers
  - — One timer output
- 8-bit pulse-which modulation timer (2 channels)
  - — Duty: 0% to 100%
  - — Resolution: 1/250
  - — Maximum carrier frequency: system clock divided by 500

- Watchdog timer (1 channel)
  - — Choice of watchdog timer and interval timer operation
- Serial communications interface (Type 2, 1 channel)
  - — Choice of asynchronous or synchronous operation
  - — Support for full-duplex operation
  - — Onboard baud rate generator
- Optional I^2C bus interface (1 channel)
  - — Compatible with the Philips Inter IC (I^2C) bus interface
  - — Choice of single master and slave modes
- A/D converter
  - — Resolution: 10 bits
  - — 8 channels (Choice of single-channel and scan modes)
  - — Support for initiating processing with an external trigger
  - — Built-in sample and hold circuit
- D/A converter
  - — Resolution: 8 bits
  - — Two channels of analog output
- Host interface
  - — 8-bit host interface port
  - — Three host interrupts (HIRQ1, HIRQ2, HIRQ3)
  - — Choice of normal and high-speed GATE A20 output
- Keyboard controller
  - — Controls matrix keyboard with configuration supporting keyboard scan with both wake-up and sense port interrupts
- Nine I/O ports
  - — 74 bidirectional I/O pins
    - a. 16 pins for driving LEDs
    - b. Software-programmable pull-up resistors on 48 pins
  - — 8 unidirectional input pins

- Interrupts
  - 9 external interrupt pins ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)
  - 26 internal interrupts
  - 16 key sense interrupt pins

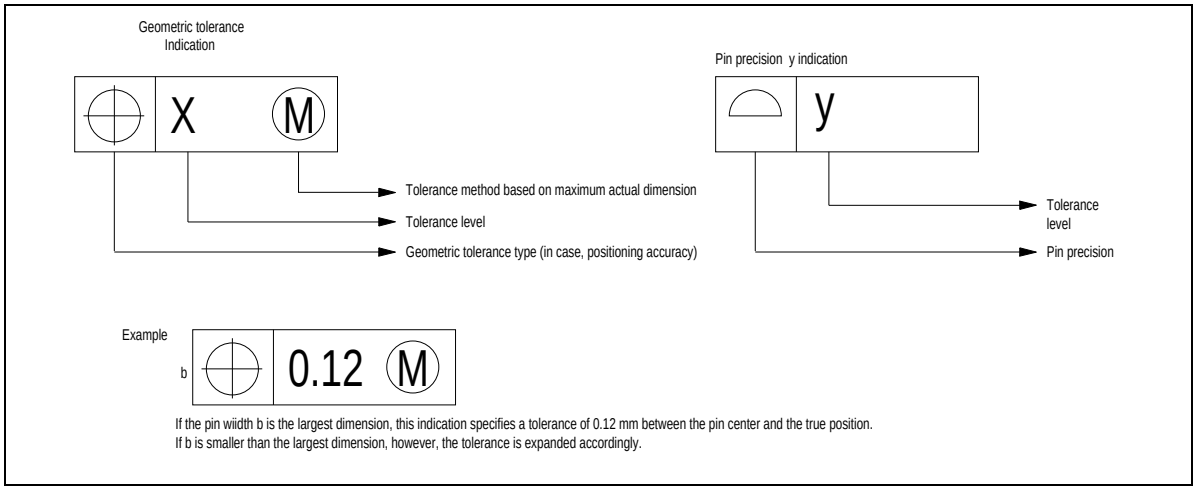
    Note: These share the $\overline{IRQ_6}$ interrupt vector and wake the chip from the software standby mode.
- Operating modes
  - Mode 1: Enhanced mode with onboard ROM disabled
  - Mode 2: Enhanced mode with onboard ROM enabled
  - Mode 3: Single-chip mode
- Power conservation modes
  - Sleep mode
  - Software standby mode
  - Hardware standby mode
- Clock oscillator
  - Maximum clock rate of 16 MHz for 5-V operation and 10 MHz for 3-V operation (based on oscillator frequencies of 16 MHz and 10 MHz respectively)
- Low-voltage (3 V) versions available
  - H8/3437, H8/3436, H8/3434
- Packages
  - 100-pin TQFP (TFP-100B)
  - 100-pin plastic QFP (FP-100B)

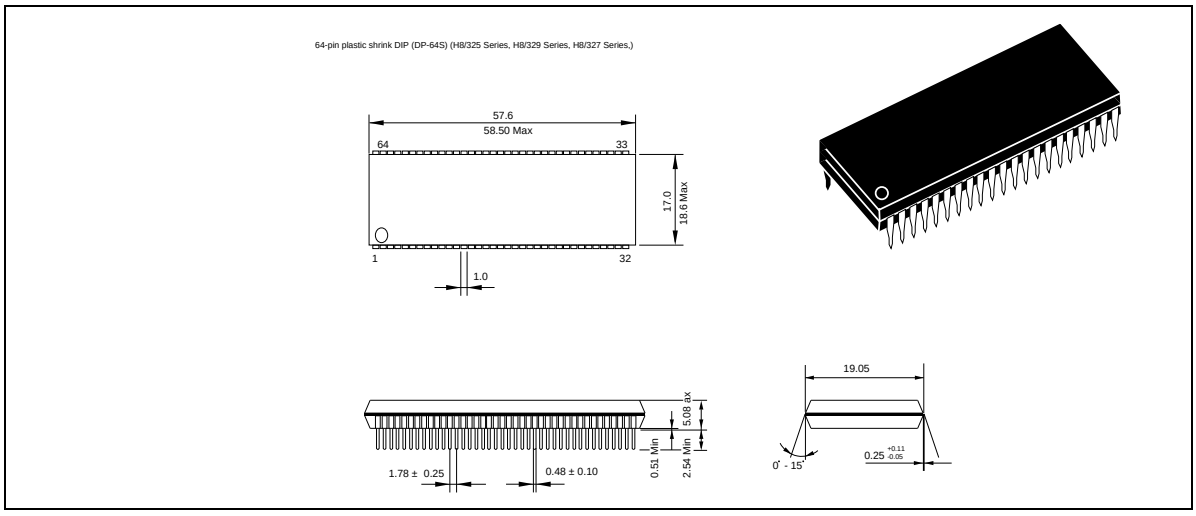
Block Diagram



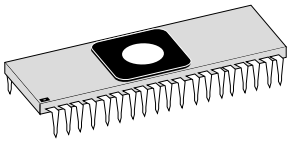
Appendix A Packages

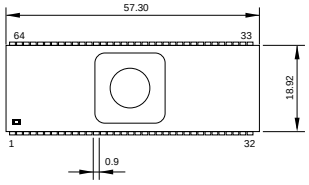
External Dimension Drawings (Unit: mm)

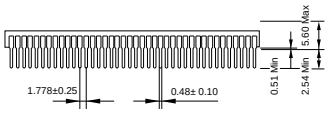


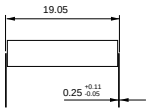


64-pin ceramic shrink DIP with view port (DP-64S) (H8/325 Series, H8/3257 Series, H8/327 Series, H8/329 Series, H8/3297 Series)

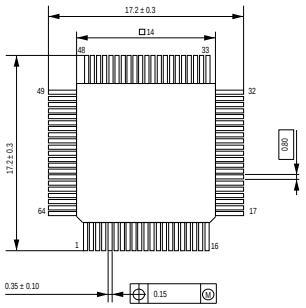


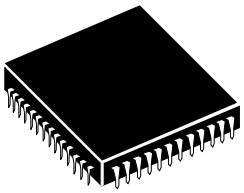


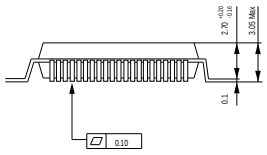


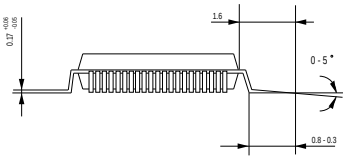


64-pin plastic QFP (FP-64A) (H8/325 Series, H8/329 Series, H8/3297 Series)

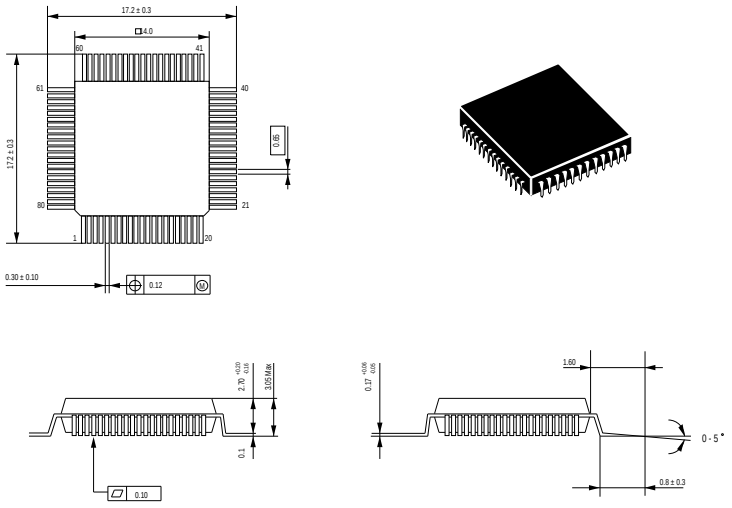




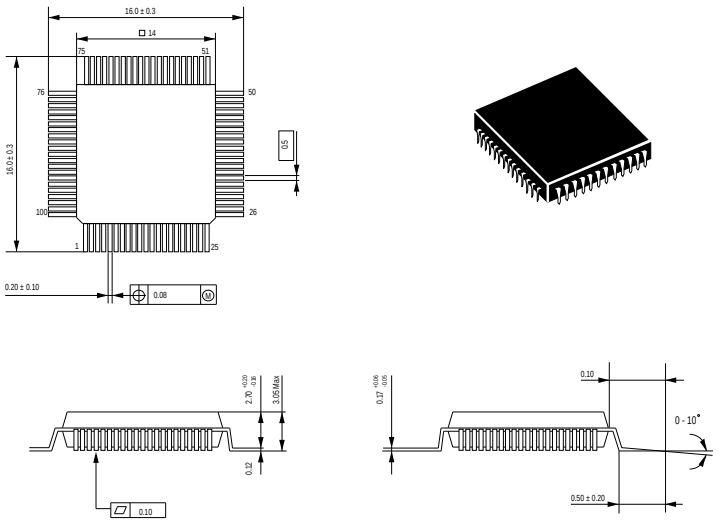




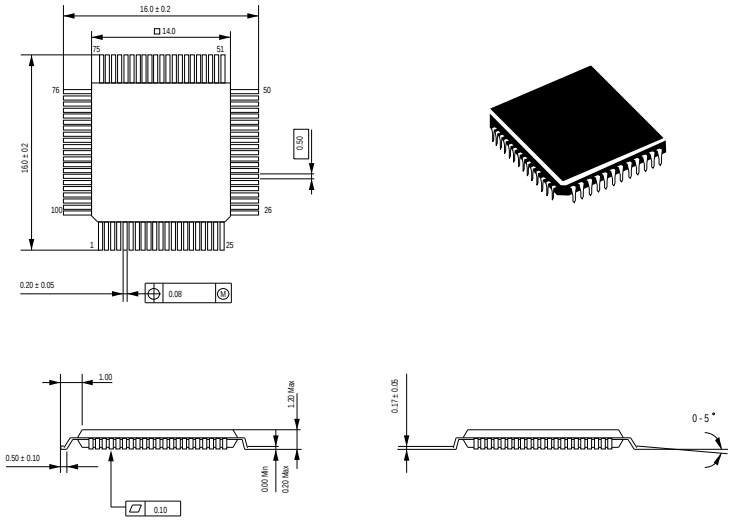
80-pin plastic QFP (FP-80A) (H8/350 Series, H8/330 Series, H8/3314 Series, H8/338 Series, H8/3334 Series, H8/3337 Series, H8/3397 Series)



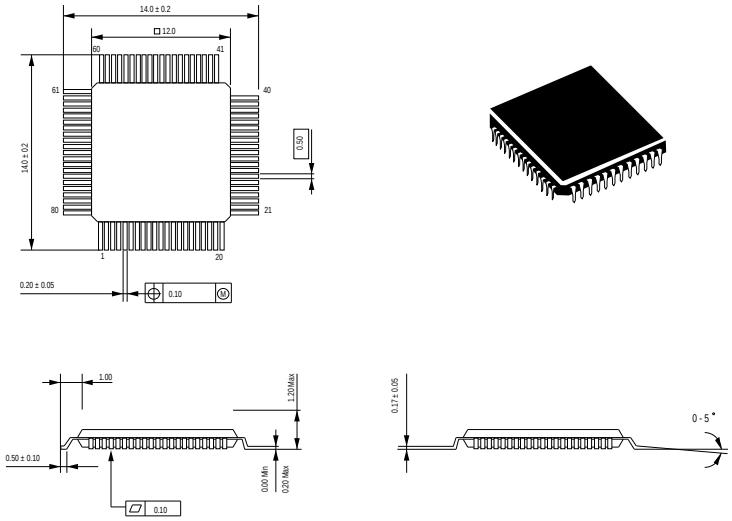
100-pin plastic QFP (FP-100B) (H8/3437 Series)



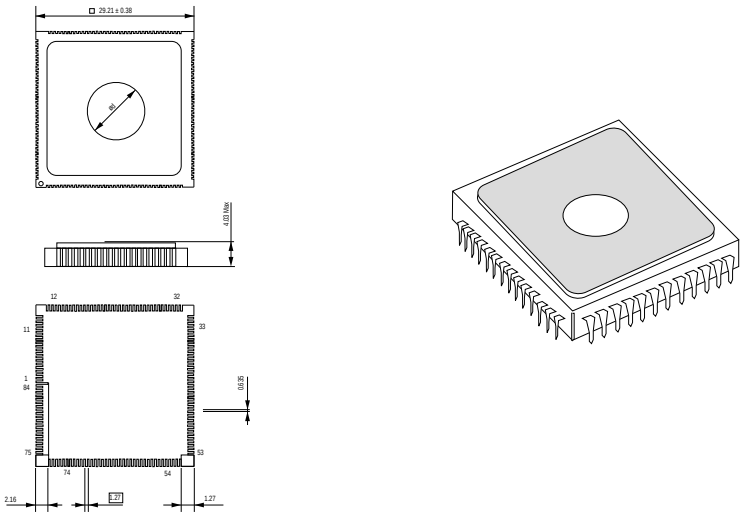
100-pin TQFP (TFP-100B) (H8/3437 Series)



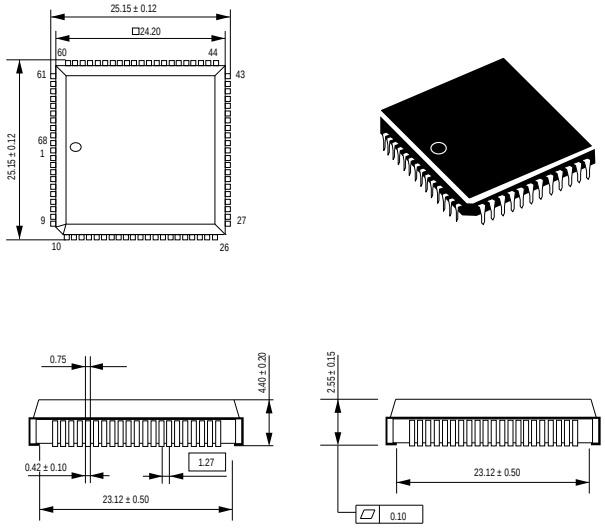
80-pin TQFP (TFP-80C) (H8/3297 Series, H8/3334 Series, H8/3337 Series, H8/3397 Series)



80-pin LCC with view port (CG-84) (H8/350, H8/330, H8/337, H8/338, H8/3334, H8/3337Y)

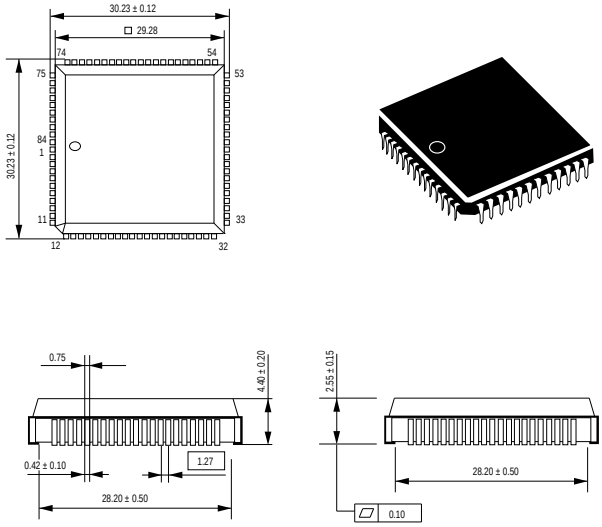


68-pin PLCC (CP-68) (H8/325 Series, H8/329 Series)



SOP-10 (H8/3101)

84-pin PLCC (CP-84) (H8/350 Series, H8/330 Series, H8/3314 Series, H8/3381 Series, H8/3334 Series, H8/3337 Series, H8/3397 Series)



84-pin PLCC (CP-84) (H8/350 Series, H8/330 Series, H8/3314 Series, H8/3381 Series, H8/3334 Series, H8/3337 Series, H8/3397 Series)