# Hitachi America, Ltd.

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## Application Engineering
## TechNote


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# CMOS Design Tips for H8/53x Devices

The purpose of this technote is to provide design tips for the hardware engineer that intends to design the H8/53x CMOS microcontroller into an embedded system. Although this technote will focus on the H8/53x, by no means is the discussion limited to this device.

**Design Tip 1**

The Reset and Hardware Standby Mode are of importance to the hardware design engineer. Operating in either mode will cause certain pins to float to unknown voltage levels. This condition is highly undesirable especially if the floating output pins are tied to the inputs of other CMOS devices. Please refer to figure 1 to see which pins will float.

**Part**
**H8/532/534/536/538**

| MODE | ZTAT | MASK ROM |
|---|---|---|
| 1 | **A,B** | **A,B** |
| 2 | **A,B,C** | **A,B,C** |
| 3 | **A,B** | **A,B** |
| 4 | **A,B,C,D** | **A,B,C,D** |
| 7 | **A** | **A** |

Symbol Table

**A** = I/O ports initialized to input state ( Tri-State )
**B** = Data Bus (D7-DO) is placed in Tri-State
**C** = Port 5 initialized to input state ( Tri-State )
**D** = Port 6.0 - 6.3 initalized to input state (Tri-state)

**Figure 1:** Hardware Standby and Reset Mode: Pins that Tri-State

Excessive current draw from the power supply may result even if the device enters the **Reset** or **Hardware Standby Mode** for a short time. To prevent this unwanted condition from occurring, all pins shown in figure 1 that tri-state should be terminated via a pull-up resistor to Vcc or a pull-down resistor to ground. The resistor is typical chosen to be between 3.5k and 1 M ohms. Choosing a large resistor value will lower the power dissipation at the expense of a longer rise and fall time(slower bus) for the output signal. Likewise, a small resistor value will increase the power dissipation while shortening the output signal's rise and fall time (faster bus). A typical value chosen for the pull-up or pull-down resistor is 10k ohm.

**Design Tip 2**

For CMOS devices, the practical limitation of fanout is due to the input rise time. The output driver must be able to switch from a low to a high within the maximum permissible rise time specified by EIA/JEDEC specifications. For Hitachi's CMOS logic family, the maximum permissible rise time (tr) is 500ns at Vcc=4.5v. Lets determine the maximum number of CMOS inputs that can be driven by a single standard CMOS output. Please refer to Figure 2 for the worst case input model of a CMOS gate.

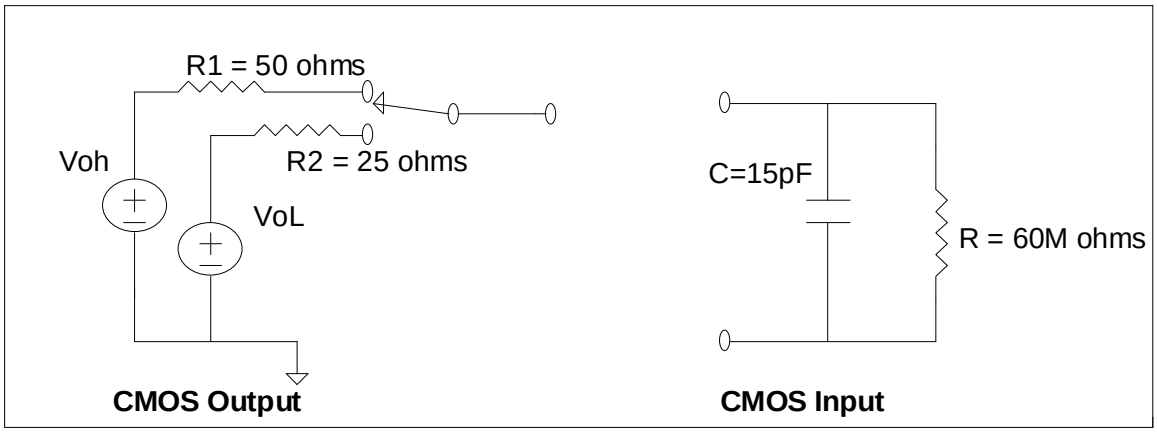


**Figure 2:** Worst Case Input/Output Models

For a fan-out of 'n' high-speed CMOS devices, the input capacitance will be (nx15)pF. As mentioned earlier, when the driving device switches its output from the low level to the high level, the input capacitance off all devices in the fanout must be charged up and reach Vih(min) within 500ns. The equation below is used to determine the maximum fanout (n).

$$Vih(min) = Voh(typ) \times (1-e^{-t/RC})$$

Soving for the fanout "n",

$$n = \frac{-t/RC}{15(1X10exp-12)\ln[1- Vih(min)/Voh(typ)]}$$

R= 50 ohms
C= (15Xn)pF
t = 500ns
n = number of fanout

It is determined that a single CMOS output can safely drive 505 CMOS loads. We can see from this calculation that the AC and not DC characteristics is the limiting factor in determining fanout.

Unlike standard CMOS logic, there is a limitation imposed on the H8/53x data lines (PORT 3) fanout capacity. Port 3 can safely drive a maximum capacitive load of 90 pF. For standard CMOS devices connected to the data bus, this means that 6 CMOS devices could be safely driven without the need to buffer the data bus.





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