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Application Engineering
TechNote

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H8/300 Mask ROM Content Verification

The H8/300 family of microcontrollers share many similar features, and among those is an internal Read-Only Memory (ROM) block of varying size. Based upon the internal ROM type, each member of the H8/300 family can either be programmed by the user on a general-purpose PROM writer (such as the Data I/O 200-series), or can only be programmed at the factory. The ROM contents of the user-programmable parts (ZTATs, OTPs, and EPROMs) can be verified for accuracy by using the PROM writer *Verify* function by comparing the data in the device with the data read into the programmer's memory during the preceding load or download operation. If the contents match, the checksum of the data is displayed; if the contents do not match, the programmer will successively indicate the address location(s) where incorrect data has been detected. However, the ROM contents of the factory-programmed parts (Mask ROMs) cannot be verified by using a PROM writer. Even if the master data was previously loaded into the programmer's memory, the ROM contents cannot be read and verified by the programmer since the device cannot be set into the programming mode (by pulling low the 2 mode pins, MD2 and MD1).

One way in which the user can verify that the proper data has been programmed into the device is by executing a software routine within the loaded ROM program that reads each ROM memory location and performs successive additions of the data contained at each location. The final result of all additions will represent the checksum of the ROM contents, and will be stored in a 16-bit general purpose register. This process could be initiated right after reset as a result of a software check of an arbitrarily chosen input port pin; if a high level is detected at this pin, then the content verification routine will be executed, but if the state of the pin is low (its initial state), then the routine will be skipped. The ROM data 16-bit checksum can be loaded into 2 arbitrarily chosen 8-bit I/O Port Data Registers (DRs). A logic analyzer can be used to read the contents of the 2 I/O Data Registers through a connected pod (or 16 probe leads). An additional I/O Port bit can be used by the software to output a high-to-low (or low-to-high) strobe signal in order to trigger the logic analyzer to load the contents of the DRs into its memory buffer. Hence, the user can easily find the ROM data checksum by reading the contents of the logic analyzer memory buffer.