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Application Engineering
TechNote

Ron Schreck

Memory Bank Switching Considerations for the H8/3XX

There are some applications of the H8/300 family of microprocessors that require more than the 64K of memory space that the chip normally addresses. These system designs can be facilitated by use of bank switching for the applications program. Generally the memory space has four unique areas or map zones. The first area is that reserved for the Vector Table and usually resides at locations H'0000 thru H'003D. The second area is the internal RAM which on the H8/330 resides at H'FD80 thru H'FF7F. The third area is reserved for the on chip register fields from H'FF90 to H'FFA7 and H'FFB0 to H'FFFF. Depending on the specific member of the H8/300 family and the mode of operation some of these areas may be moved in the 64K memory map.

The fourth area of the memory map (i.e. all other memory space not covered above) is used for external address space or the on chip ROM (EPROM, MASK ROM, OTP ROM). It is in this area that memory paging is usually done. There are two commonly used paging schemes, perhaps the most common is through the use of just software to control memory allocation. Another method uses both software and hardware to control multiple pages.

The use of the port lines as additional address lines has certain restrictions but these can be minimized by careful consideration of the user code implementation. Another consideration is that the vector table, RAM and register fields should be common to any selected page thus minimizing page switching latency time. When using an I/O port line as an A16 address line to swap to another memory map the port should be configured as an input port upon power up/reset and tied through a resistor to + 5 volts. This will define the exact page that the system will boot up from before the actual operating system takes over page management. Using the single I/O port pin gives the user the ability to switch almost the entire 64K memory space (from H'003E to H'FF8F) when operating in Mode 1 with the RAME bit in SYSCR set to "0". This will allow a large program to operate and swap into another large program area. Depending on the application this might provide a the fastest operation as if the code can run in these large blocks it would minimize the page switching overhead. The problem with this mode is that you do not have a common RAM block to store variables that might be required in both pages of the program and may need to be stored in registers between page switching. Switching between pages could be as simple as a bit test or bit set of the I/O port pin used for the A16 address bit. Care must be used to insure all variables are set as the program requires before switching between the pages.

Another configuration would allow page switching without loosing any of the on chip ROM or RAM. This would be used in the Mode 2 chip configuration. A15 can be NOR'd in conjunction with A14 and A15 and port lines to generate multiple pages that start at H'4000. Thus allowing the use of the standard vector tables, the standard on-chip ROM, the standard on-chip RAM and register locations. This requires an external bit of hardware (probably a PAL) to do the page switching but it allows various software programs to be "loaded" into the H8/300 memory space at H'4000 with a minimal amount of overhead. Using this configuration allows each "page" to be configured as a specific subroutine as features are changed in the target system.

A key item to ether design is to install all software switching routines in a common area. This requires the sub-routine for page switching be placed in an area of the overall memory map that is not switched; as on-chip ROM/RAM in application two or as an identical program on each page if the entire memory area is swapped as in application one. Using application one requires additional overhead to monitor the page swapping software to insure that the switching routines are identical before switching. This precaution is just in case something was changed by some sub routine that the original system design did not take into account.

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Hitachi America, Ltd. • San Francisco Center • 2000 Sierra Point Parkway • Brisbane, CA 94005-1819 • (415) 589-8300