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Application Engineering
TechNote

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Multiplexed I/O Functions on the H8/3003 and H8/304X

The H8/300H microcontroller family combines a 32-bit register architecture CPU with high peripheral function integration in a small, 112-pin QFP package. Consequently, the need of multiplexing signals belonging to various on-chip modules arises. Virtually all I/O Port Pins are multiplexed with 1, 2, or 3 other input/output signals that control various peripheral and CPU functions. The H8/3003 has 9 I/O Ports with a total of 58 I/O pins, and the H8/3042 has 11 I/O Ports with a total of 78 I/O pins. All but 2 I/O bits are multiplexed on the H8/3003, and all I/O lines of the H8/3042 have at least dual functions. Although the distribution of peripheral function signals among the available I/O pins has been carefully optimized, the high degree of pin function-sharing poses some constraints on the operation conditions of the chip. This technote will elucidate these constraints for each I/O Port. Also refer to Appendix C - I/O Port Block Diagrams in the Hardware Manuals for more information on the I/O Ports structure.

Port 8 (lines 0-3): P80 / RFSH- / IRQ0-
P81 / CS3- / IRQ1-
P82 / CS2- / IRQ2-
P83 / CS1- / IRQ3-

If the corresponding interrupt enable bit for IRQ1, IRQ2, and/or IRQ3 in the Interrupt Enable Register (IER) is set (and the corresponding I-bit in CCR is cleared) while the microcontroller is interfaced to external devices mapped in memory areas 3, 2, and/or 1 respectively, an interrupt request will occur every time the corresponding chip select signal is asserted. The reason is that the output chip select signal is fed back to the interrupt controller inputs through a non-tristatable buffer and an inverter, as illustrated in the Port 8 Block Diagram of Appendix C in the Hardware Manual. Since in most cases this situation is undesirable, a user cannot employ an external interrupt signal if it is multiplexed with a chip select signal used to address an external device. Similarly, IRQ0- cannot be used if the microcontroller is interfaced to PSRAM or DRAM devices that uses the RFSH- line for its refresh cycle.

Port 9 (lines 4 and 5): P94 / SCK0 / IRQ4-
P95 / SCK1 / IRQ5-

If the corresponding interrupt enable bit for IRQ4 and/or IRQ5 in IER is set (and the I-bit in CCR is cleared) while the SCI is driven from an external serial clock or outputs the internal serial clock, an interrupt request will occur on each falling edge or low level at the SCK0 and/or SCK1 pins respectively (and regardless of the DDR-bits settings). In order to avoid these occurrences, an external interrupt cannot be used if it is multiplexed with an I/O pin used for the SCI serial clock.

Port A (lines 0-7): PA0 / TP0 / TEND0- / TCLKA
PA1 / TP1 / TEND1- / TCLKB
PA2 / TP2 / TIOCA0 / TCLKC
PA3 / TP3 / TIOCB0 / TCLKD
PA4 / TP4 / TIOCA1 / A23 (only for H8/304X in modes 3 and 4)
PA5 / TP5 / TIOCB1 / A22 (only for H8/304X in modes 3 and 4)
PA6 / TP6 / TIOCA2 / A21 (only for H8/304X in modes 3 and 4)
PA7 / TP7 / TIOCB2 / A20 (only for H8/304X in modes 3 and 4)

If the Integrated Timer Unit (ITU) is configured for external clock input via TCLKA or TCLKB, and the DMA module is activated by external request and uses signals TEND0 or TEND1 as end-of-DMA cycle flags, the ITU will be driven from the corresponding TEND signal (and regardless of the DDR-bits settings). Since this situation is not desirable in most

applications, the ITU should not be driven by an external clock if it is multiplexed with an I/O pin used by the DMA controller to provide an end-of-cycle flag.

The ITU should not be set to use TCLKC or TCLKD as external clock inputs while using TIOCA0, or TIOCB0 respectively, as compare-match outputs since the corresponding I/O Port outputs are fed back to the counter clock inputs (see Appendix C in the Hardware Manuals). If the ITU is configured to use TCLKC or TCLKD while set up for input-capture trigger action at TIOCA0 or TIOCB0 respectively, an input-capture event will occur on the selected external clock transitions. Unless this particular situation is needed, do not set up the ITU to be driven from an external clock input pin that is multiplexed with an input-capture pin used by the timer network.

The Timing Pattern Controller (TPC) cannot use outputs TP2-3 to be triggered by an ITU input-capture event at pins TIOCA0 or TIOCB0 (if TPC is operating in the non-overlapping mode) since TP2 and TP3 are function multiplexed with TIOCA0 and TIOCB0 respectively. Likewise, outputs TP4 and TP6 cannot be triggered by input-capture action at pins TIOCA1 and TIOCA2 respectively because they are function-multiplexed on the same I/O pins. Also, outputs TP5 and TP7 cannot be utilized if input-capture occurs at TIOCB1 and TIOCB2 respectively, if TPC is operating in the non-overlapping mode.

Also, the ITU cannot be driven from an external clock via TCLKD, TCLKC, TCLKB, or TCLKA if TPC outputs are desired from TP3, TP2, TP1, or TP0 respectively.

Port B (lines 0-3, 6-7):
PB0 / TP8 / TIOCA3
PB1 / TP9 / TIOCB3
PB2 / TP10 / TIOCA4
PB3 / TP11 / TIOCB4
PB6 / TP14 / DREQ0-
PB7 / TP15 / DREQ1- / ADTRG-

The TPC cannot use outputs TP8 or TP10 if they are triggered by an input-capture action via TIOCA3 or TIOCA4 respectively, since the same pins are used for both functions. Similarly, outputs TP9 or TP11 cannot be used if they are triggered by an input-capture action via TIOCB3 or TIOCB4 respectively (and if the TPC is operating in the non-overlapping mode).

If the TPC is configured to use outputs TP14 and/or TP15 while the DMA controller is set up to be activated upon an external trigger at DREQ0- or DREQ1-, DMA transfer operations will occur every time a high-to-low transition happens at the corresponding TP outputs (since the I/O port output is fed back to the input line (see Appendix C in the Hardware Manual).

If the DMA controller is configured to perform transfers upon a falling edge at DREQ1- while the A/D converter is setup to accept start-of-conversion upon a falling edge at ADTRG-, both operations will start simultaneously since they are triggered at the same pin (PB7).

Port C (lines 2-5):
PC2 / TEND2- / CS4- (and only for H8/3003)
PC3 / DREQ2- / CS5-
PC4 / TEND3- / CS6-
PC5 / DREQ3- / CS7-

If the DMA controller is set up to be activated upon an external trigger at the DREQ2- or DREQ3- pins while the microcontroller is interfaced to external devices mapped in memory areas 5 or 7 respectively, DMA transfers will occur every time the corresponding multiplexed chip select signal (CS_5- or CS_7-) is asserted. This situation can be avoided by using only one of the pin functions. Similarly, if the DMA uses the $TEND_2$- or $TEND_3$- pins to signal end-of-transfer, the microcontroller should not be interfaced to external devices mapped in memory areas 4 and 6, and viceversa.

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