Hitachi America, Ltd.

Application Note

H8/3003

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Memory Interface to the H8/3003

INTRODUCTION

The H8/3003, a member of the H8/300H family, is a powerful microcontroller that brings major enhancements to the H8/300 series devices while maintaing downward compatibility with them. Among its remarkable attributes is a 32-bit CPU structure, faster internal clock rate, and additional and enhanced on-chip peripherals. However, the H8/3003 does not contain any internal memory except for 512 bytes of RAM. Therefore, the user's program must reside in an external ROM. Also, in many applications, 512 bytes of RAM are not sufficient for temporary data storage, so the need to utilize external random access memory chips such as SRAMs, DRAMs, and/or PSRAMs arises quite often. In light of these aspects, the H8/3003 has been designed to facilitate interface to a variety of external memory devices by including a bus controller and a DRAM refresh controller in its architecture. In addition, the width of the external data bus has been expanded to 16 bits, and the maximum addressability range has been extended to a whole 16MBytes, via a 24-bit address bus.

GENERAL CONSIDERATIONS

The H8/3003 has 4 normal operation modes that mainly determine the communication path between the chip and the external devices to which it is interfaced. The microcontroller is configured into any one of these modes by setting the MD2 - 0 input pins to the appropriate level. Table 1 below shows the MD pin settings and describes each mode of operation.

Mode	Pin Settings	Description
1	MD2-0 = 001	8-bit Data Bus 1 MByte Addressability
2	MD2-0 = 010	16-bit Data Bus 1MByte Addressability
3	MD2-0 = 011	8-bit Data Bus 16MByte Addressability
4	MD2-0 = 100	16-bit Data Bus 16MByte Addressability

Table 1. Mode Selections

For the byte transfer modes 1 and 3, only lines D15 - 8 are utilized, and for the word transfer modes 2 and 4, the whole data bus D15 - 0 is employed. For the 1MByte modes 1 and 2, the valid address lines are A19 - 0, while for the 16MByte modes, all the address lines are employed (A23 - 0).

The on-chip bus controller partitions the memory space into eight consecutive areas. This translates into eight 128KByte areas for the 1MByte modes, and 8 2MByte areas for the 16MByte modes. Each area is correlated to one chip select output signal (CS7- to CS0-) that changes state from initial high to low when any address within the corresponding memory space is accessed, hence providing full area decoding. Since the chip select lines are multiplexed with I/O port bits and/or various control signals, their function is selected when their corresponding port bits are configured to outputs. In addition, to utilize CS_1 - CS_3, external interrupts IRQ_1 - IRQ_3 cannot be used, and if the user needs CS_4 - CS_7, external DMA requests on channels 2 and 3 are not possible. These conditions are illustrated in table 2 below. Normally after reset, the CS_0- pin is an output pin, while the CS_1 - CS_7 lines are configured to be input pins. Therefore, to decode memory areas 1-7, the user must program a 1 into the corresponding I/O port DDR bit.

The on-chip bus controller module offers some more options for interfacing to external memory devices. One option is to control the external data transfer bus size regardless of the level on the MD2 - 0 pins. This is achieved by programming the corresponding control bits for each memory partition area in the Bus Width Control Register (ABWCR). If the chip is configured for either mode 2 or 4 and only byte transfers are desired during accesses to external devices mapped in a particular memory area, the corresponding ABW bit of the ABWCR register must be set to 1. Vice versa, if the microcontroller is configured for either mode 1 or 3 and word accesses are needed into a particular memory area, the corresponding ABW bit must be cleared to 0.

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Area 7							0
7	6	5	4	3	2	1	0
ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0

Figure 1. Bus Width Control Register (ABWCR)

The other option allows the user to set the number of T-states for a read or write external memory cycle into any memory partition. This option is exercised by programming the control bit (ASTn) for the corresponding memory area in the Access State Control Register (ASTCR) as desired. Writing a zero into the ASTn bit selects 2 clock cycle access, while a one forces a 3 clock cycle access.

Area 7							0
7	6	5	4	3	2	1	0
AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0

Figure 2. Access State Control Register (ASTCR)

Furthermore, in order to accommodate for low-speed memory devices, the bus controller allows insertion of wait states (Tw) into memory cycles for any memory area that has been configured for 3 T-state access. The H8/3003 offers 4 possible wait-state generation modes that are selected by programming the wait mode select (WMS) bits 3 and 2 in the Wait Control Register (WCR). The number of wait states inserted for some of those modes are set by the wait count (WC) bits 1 and 0 in the WCR register as well. Wait states for any memory access area can be enabled (or disabled) by writing a 1 (or 0) into the corresponding wait state control enable (WCE) bit in the Wait State Control Enable Register (WCER).

7	6	5	4	3	2	1	0
-	-	-	-	WMS1	WMS2	WC1	WC0

Figure 3. Wait Control Register (WCR)

Area 7							0
7	6	5	4	3	2	1	0
WCE7	WCE6	WCE5	WCE4	WCE3	WCE2	WCE1	WCE0

Figure 4. Wait State Control Enable Register

For a complete description of each wait state mode, please refer to section 6.3.5 in the H8/3003 hardware manual.

Pin number	Function	CSn- function selection
104	CS_0-/$P8_4$	$P8_4$ DDR = 1
103	CS_1-/$P8_3$/IRQ3-	$P8_3$ DDR = 1 and IER_3 = 0
102	CS_2-/$P8_2$/IRQ2-	$P8_2$ DDR = 1 and IER_2 = 0
101	CS_3-/$P8_1$/IRQ1-	$P8_1$ DDR = 1 and IER_1 = 0
13	CS_4-/PC_2/$TEND_2$-	PC_2 DDR = 1 and no external DMA request on channel 2
14	CS_5-/PC_3/$DREQ_2$-	PC_3 DDR = 1 and no external DMA request on channel 2
15	CS_6-/PC_4/$TEND_3$-	PC_4 DDR = 1 and no external DMA request on channel 3
16	CS_7-/PC_5/$DREQ_3$-	PC_5 DDR = 1 and no external DMA request on channel 3

Table 2. Chip Select Function Selection

EPROM CONNECTION

Since EPROMs are directly addressed, their interface to the H8/3003 is fairly straight forward. However, two main factors must be taken into consideration before interfacing any EPROM to the microcontroller:

1. **The type of access**. As was discussed previously, any memory partition area can be configured individually for either 8-bit or 16-bit access. If byte access is required, an 8-bit EPROM is the logical choice, and byte reads will occur on the D15 - 8 data lines. The address lines from the H8/3003 can be directly connected to the address pins of the EPROM in an equal correspondence (i.e. A0 - A0, A1 - A1, etc.). If word access is needed, a 16-bit EPROM is the easiest solution, and word reads will take place through all data bus lines D15 - 0. In this case, the H8/3003 assumes that the upper byte (D15 - 8) of a word resides at an even address with A0 = 0, and the lower byte (D7 - 0) occupies an odd address with A0 = 1. Therefore, 2 consecutive 16-bit word locations are differentiated by A1 only, and A0 will always be low during a word access cycle. As a result, the EPROM memory pins MA_n - MA_0 must be tied to the microcontroller address lines SA_1 - SA_{n+1}.
   If the H8/3003 interface to the EPROM is designed for word accesses, and the user reconfigures it for byte accesses (by setting the corresponding bit in the ABWCR), the microcontroller will perform reads only through the upper data byte D15 - 8, and the

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odd address locations will be skipped. Figures 5 and 6 depict 2 generic EPROM connections for both byte and word access areas. The RD- line of the H8/3003 must be connected to the OE- pin of the EPROM(s).

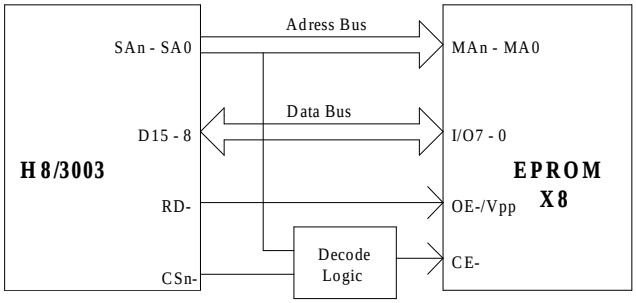

Figure 5. EPROM connection to a byte access area.

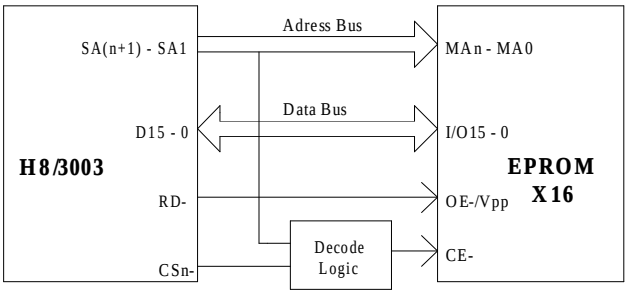

Figure 6. EPROM connection to a word access area.

2. **The size of the EPROM.** If the memory size of the device is equal to the memory partition area(s), only the CS_n lines(s) of the microcontroller are needed for decoding. If the EPROM's memory size is different from the size of a memory partition area (or an even multiple of it), additional address lines will be needed for decoding.

SRAM CONNECTION

When board space, cost, and power consumption requirements are not as important as speed, a variety of SRAM devices can be interfaced to the microcontroller. The bus controller module of the H8/3003 provides all memory transfer control signals, and allows for direct or simplified device(s) decoding. As for the EPROM case, the access mode (8 or 16-bit) is a factor in determining how to interface the memory device(s) to the microcontroller. Figures 7 and 8 show a generic SRAM interface to a byte access and to a word access area. For 16-bit interfaces, the H8/3003 provides 2 active low write-enable signals, HWR- and LWR-; HWR- goes low for accesses on the high byte (D15 - 8), and LWR- indicates accesses on the low byte (D7 - 0) upon a falling edge. Since for packaging reasons there are few SRAMs on the market that use 16 I/O lines, figure 8 shows a connection to 2 X8 SRAMs. In addition, as explained in the EPROM section, the memory size of the devices contribute to the simplicity of the decode logic. Also, in areas designed for 16-bit accesses that are reconfigured by software to 8-bit accesses, only the upper data bus D15 - 8 is employed and every other address location will be skipped.

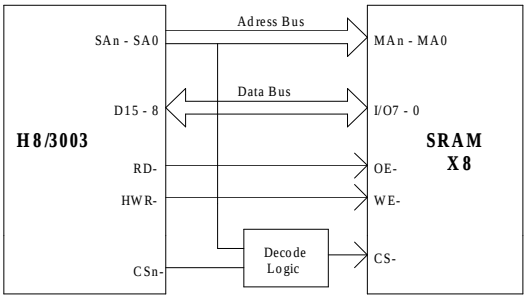

Figure 7. SRAM connection to a byte access area.

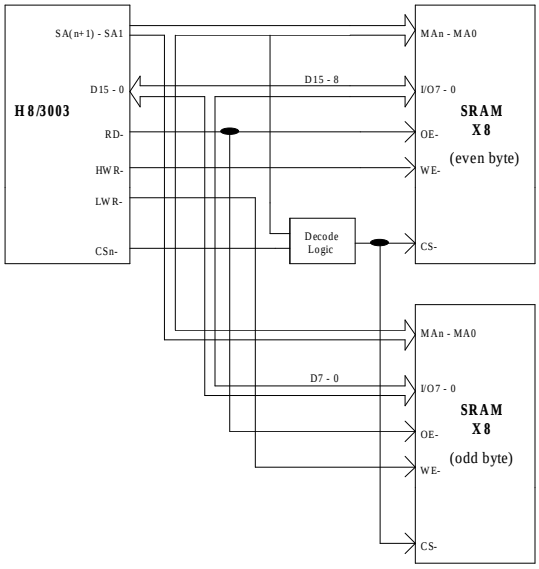

Figure 8. SRAM connection to a word access area.

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DRAM CONNECTION

When minimal board real-estate, cost, and power consumption are essential design features, the user has the option of directly connecting 16-bit wide DRAM devices to the H8/3003. Since the chip select signal CS3- is multiplexed with the RAS- signal onto the same pin, direct connection is only possible if the DRAM unit(s) is mapped within memory partition area 3. Therefore, a maximum of 128KBytes memory locations (in the 1MByte modes 1 and 2), and 2MBytes memory locations (in the 16MByte modes 3 and 4) can be mapped in DRAM devices. The refresh controller module within the H8/3003 provides all the necessary DRAM control signals (such as RAS-, CAS-, WE-), and performs periodic CAS-before-RAS refresh cycles. DRAMs that use either 2 CAS- lines or 2 WE- lines for byte control can be used. Please note that only page-mode DRAMs can be interfaced to the H8/3003, and not static-column devices (since they are not using the CAS- signal to latch the column address).

In order to be able to perform accesses to the DRAM, the 4 control registers in the refresh controller unit must be properly initialized. The type of DRAM used must be conveyed to the microcontroller by setting bits 6 - 3 of the Refresh Control Register (RFSHCR) shown below appropriately.

7	6	5	4	3	2	1	0
SRFMD	PSRAME	DRAME	CAS/WE	M9/M8	RFSHE	Res	RCYCE
X	0	1	X	X	X	1	X

Bits 6 (PSRAME) and 5 (DRAME) enable the microcontroller for DRAM interface, and must be set to 0 and 1 respectively. Bit 4 (CAS/WE-) indicates if the DRAM uses 2 CAS or 2 WE lines for byte control. Bit 3 (M9/M8-) indicates the address multiplexing mode of the DRAM (only for 4Mbit - 256K x 16 DRAMs) as follows: if the chip uses the 9 rows x 9 columns addressing scheme, it should be set to 1, while for the 10 rows x 8 columns addressing method, it should be cleared to 0. The refresh conditions must be specified by programming bits 7, 2, and 0 of the RFSHCR. Bit 0 (RCYCE),when set , allows the refresh process through insertion of refresh cycles. Bit 2 (RFSHE) enables the refresh signal to be output via the RFSH- pin of the H8/3003, and bit 7 (SRFMD) enables the self-refresh feature in the software standby mode for DRAMs that possess this capability. Please consult the H8/3003 Hardware Manual for a detailed explanation on this feature, and also on the refresh process in general. Bits 5 (CKS2), 4 (CKS1), and 3 (CKS0) of the Refresh Timer Control/Status Register (RTMCSR) allows for 7 possible refresh clock frequencies; for each refresh clock period, the Refresh Timer Counter Register (RTCNT) is incremented by 1. Finally, the time interval between refresh cycles is further precised by loading the Refresh Time Constant Register (RTCOR) with the desired compare-match value upon which RTCNT is cleared and counting resumes again. In addition, the DDR bit corresponding to bit 1 of I/O port 8 must be set to 1 in order to enable the microcontroller to output the CS3-/RAS- signal. Also, bit 3 in the ABWCR must be cleared since only 16-bit DRAM accesses are possible. Figure 9 below shows the precise order a programmer must follow in order to setup memory area 3 for DRAM interface.

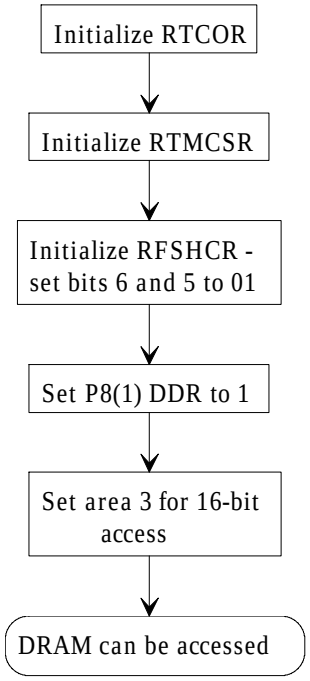

Figure 9. DRAM setup sequence.

Either 1 Mbit (64K x 16) or 4 Mbit (256K x 16) DRAM devices can be interfaced to the H8/3003 that use either 2 CAS or 2 WE lines for byte control, and address the memory array via a 9 rows x 9 columns or a 10 rows x 8 columns matrix scheme. Figure 10, 11, and 12 show generic connections to the H8/3003 of 3 types of DRAM devices.

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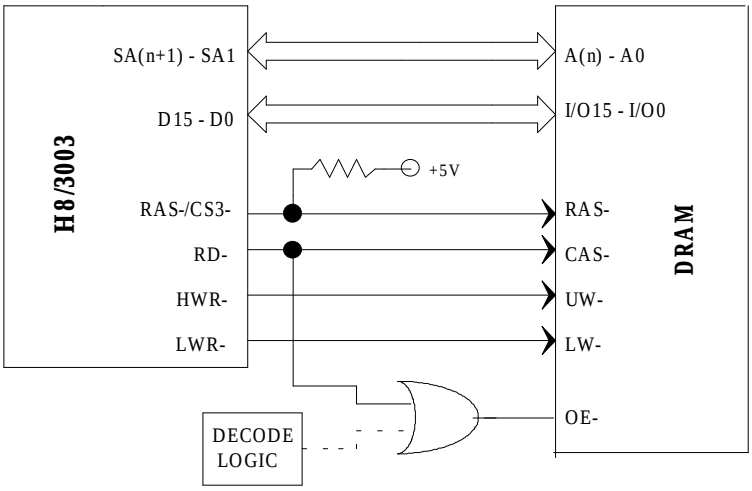

Figure 10. 1 and 4 Mbit (9 x 9 addresssing) 2WE DRAM connection.

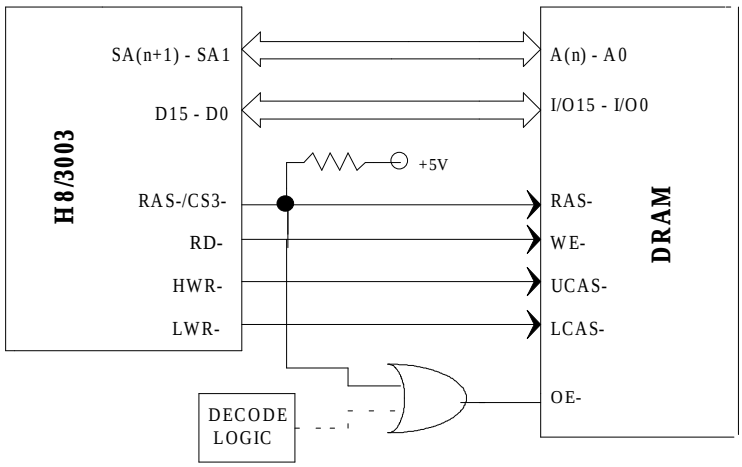

Figure 11. 1 and 4 Mbit (9 x 9 addressing) 2CAS DRAM connection.

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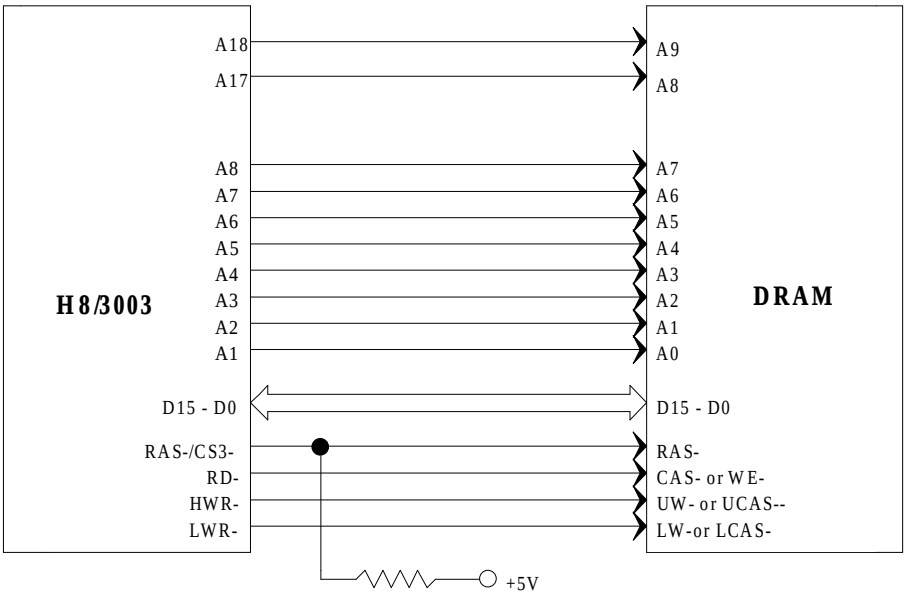

Figure 12. 4 Mbit (10 x 8 addressing) DRAM connection.

Note that for 10 x 8 addressing mode 4Mbit DRAMs, the upper 2 bits of the 10-bit row address are sent via address lines A18 and A17 of the microcontroller. If a 4Mbit DRAM with a 9 x 9 addressing mode is utilized, the row and column address are sent through lines A1-A9. The RD- pin acts as the single CAS- line for 2WE DRAMs, and as the single WE- line for 2CAS devices. Similarly, the UW- and LW- signals (for 2WE DRAMs) and the UCAS- and LCAS- signals (for 2CAS- devices) are sent via microcontroller pins HWR- and LWR- respectively. Also observe that the DRAM is enabled if the CS3- line and the additional decode logic output (for the 2 CAS devices), and the RD- line plus the additional decode logic output (for the 2 WE- devices) are both valid low. Additional decode logic is only needed if only a segment within memory area 3 needs to be decoded.

DESIGN EXAMPLE

In this example, several memory devices of various sizes are connected to the H8/3003 microcontroller. Figure 13 on the next page shows the memory map assignments of each memory device for the 1MByte modes as well as for the 16MByte modes. In addition, the transfer type (8- or 16-bit) and the access cycle size (3 or 2-state) are also indicated. Figures 14 - 17 on pages 11 - 14 depict the interface schematics. The table below shows the devices being connected to the H8/3003:

Device	Qty	Size	Access Type
HN27C1024H EPROM	1	64Kx16	16-bit, 3-state
HN27512 EPROM	1	64Kx8	8-bit, 3-state
HM514260 DRAM	1	256Kx16	16-bit, 2-state
HM628128 SRAM	2	128Kx8	16-bit, 3-state
HM628128 SRAM	1	128Kx8	8-bit, 2-state

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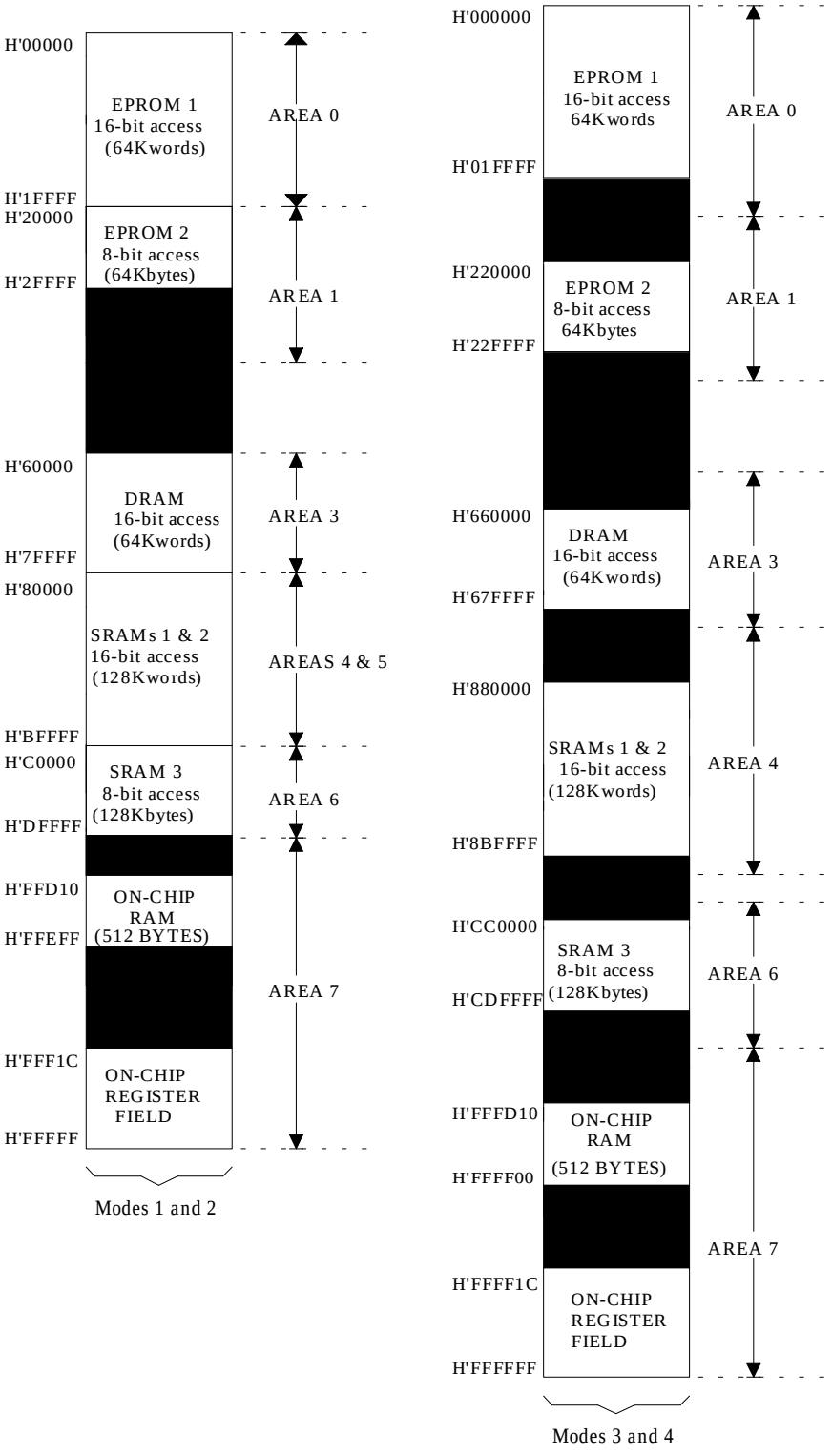

Figure 13. External Memory Map Assignments.

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EPROM INTERFACE

The H8/3003 interfaces to 2 EPROM devices: the 64K x 16 27C1024H (U2) and the 64K x 8 27512 (U3). Figure 15 on page 12 shows the interface schematic.

U2 is configured for 16-bit access (bit 0 of ABWCR is cleared) and 3-state read cycles (bit 0 of ASTCR is set to 1). The device occupies a memory block of 64Kwords (or 128KBytes) in memory area 0. For modes 1 and 2, only CS0- is necessary for address decoding. Since only a portion of memory area 0 is occupied in the 16MByte modes (3 and 4), address lines A20 - 17 are needed in addition to CS0- to assign the memory space between H'000000 - H'01FFFF to the EPROM. Hence, the following conditions have to be met in order to select the EPROM: CS0- low, A20 low, and A19-17 low. A 74HC138 3 x 8 decoder (U8), shown in figure 14 on page 11, is employed to output the appropriate active-low enable signal (ENABLE0-) corresponding to A19-17 = 000. Therefore, a triple-input OR-gate is used to satisfy these conditions, and to provide the chip enable signal. 16 address lines are needed to address 64 Kwords of EPROM. Since the device is configured for word accesses, lines A16 - A1 are wired to pins A15 - A0 of U2.

U3 is configured for 8-bit access (bit 0 of ABWCR is set) and 3-state read cycles (bit 0 of ASTCR is set). The EPROM occupies a memory block of 64KBytes in memory area 1. For the 1Mbyte modes, CS1- and A16 have to be low, and for the 16MByte modes, A17-19 should be 001 and A20 should be low. Decoder U8 provides the active low signal ENABLE 1- corresponding to A19 - 17 = 001. Both conditions are implemented via a 3-input and a 2-input OR-gate. Since the EPROM is configured for byte accesses, direct connection between pins A15 - A0 of both devices is adequate. Figures 14 and 15 on pages 11 - 12 show the connections between the H8/3003 and the EPROM in detail.

Note that A20 is multiplexed with bit 4 of I/O port 5, and A20 must be low in all modes in order to enable the EPROM; therefore, this port bit must not be used as such in modes 1 and 2, since a high would disable the EPROM.

DRAM INTERFACE

The H8/3003 is connected to a HM514260 DRAM (U7). Figure 16 on page 13 shows the interface schematic. This device uses 2 CAS lines for byte control, and a 9 rows x 9 columns address multiplexing scheme. Since memory area 3 is configured for word accesses (bit 3 of ABWCR is 0), and address lines A9 - A1 from the microcontroller are connected to pins A8 - A0 of the device. Bit 3 of ASTCR is cleared, indicating 2-state access cycle length. A 74HC245 bi-directional buffer (U6) is installed onto the lower data lines D7 - D0, and is used to isolate the DRAM lower I/O lines (I/O7 - I/O0) from the data bus when the microcontroller is set into the byte transfer modes 1 and 3. A 74HC138 decoder (U9) is used to output a low control signal corresponding to the 4 different modes of operation settings of lines MD2 - 0. The Y4- and Y6- outputs correspond to modes 1 and 3 respectively, and a XOR-gate is used to clear pin OE- of U6 when these modes are selected, hence isolating the lower DRAM I/O lines from the data bus. The appropriate lower byte data flow direction is selected by connecting the WE- line to the DIR pin of U6. The DRAM occupies a 64Kword (or 128Kbyte) block in memory area 3. For the 1Mbyte modes, only CS3- is necessary for address decoding; for the 16Mbyte modes, A19 - A17 need to be 011 (via decoder U8 output ENABLE3-) and A20 has to be low. Hence, a triple-input OR gate is sufficient to select the chip.

Again, since A20 must be low for all modes of operation in order to select DRAM operation, the corresponding I/O port bit ($P5_4$) should not be used in the 1Mbyte modes.

SRAM INTERFACE

The H8/3003 is connected to 3 128K x 8 SRAMs. Figure 17 on page 14 shows the interface schematic. Two of them (U4 and U5) are configured for 16-bit access (bits 4 and 5 of ABWCR are cleared), and for 3-state access (bits 4 and 5 of ASTCR are set). U4 will store the upper byte and U5 will contain the lower data byte. Since they occupy a 128Kword (or 256 Kbyte) memory block, they are mapped into memory areas 4 and 5 (for the 1Mbyte modes) and only in memory area 4 (for the 16Mbyte modes). The remaining SRAM (U6) is configured for 8-bit and 2-state access, and occupies a 128Kbyte block into memory area 6.

The first 2 SRAMs are selected under the following minimum conditions:

1. For modes 1 and 2, either CS4- or CS5- must be low.
2. For modes 3 and 4, CS4-, A18, and A20 must be low, and A19 must be high.

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For the sake of simplifying the decode logic, A18 = A20 = low and A19 = high is a select condition in all modes of operation, and is implemented by an inverter and a triple-input OR gate connected to CS1- of both devices. Decoder U9 is used to provide active-low control outputs for each mode selection (via MD2 - 0). A XOR gate is used to output a high signal when either mode 1 or 2 are selected, and another XOR gate is used to provide a high output when either CS4- or CS5- are low; both outputs are driven through an AND gate since they need to be valid high in order to select the first condition stated on the previous page. A similar approach is taken to meet the second condition. A XOR gate is used to output a high signal when either mode 3 or 4 are selected, and an inverter is used to switch the CS4- level. When the second condition is met, the output of the AND-gate is high. Since both conditions cannot occur at the same time, the outputs from both AND gates are driven into another XOR gate that provides the second select signal to the SRAMs. 17 address lines are needed to address the whole 128Kword (or 256Kbyte) SRAM space; since the devices are configured for word access, lines A17 - A1 from the H8/3003 are connected to pins A16 - A0 of both U4 and U5. The WE- pin of U4 is connected to the HWR- line of the H8/3003, while the WE- pin of U5 is wired to the LWR- line.

The third SRAM (U6) is selected under the following minimum conditions:

1. For modes 1 and 2, CS6- must be low.
2. For modes 3 and 4, CS6- and A20 must be low, and A19 -A17 have to be 110.

Decoder U8 provides an active-low control signal (ENABLE2-) corresponding to the above settings of A19 - A17. Therefore, a triple-input OR gate is sufficient to satisfy all above conditions. The output of the OR-gate is connected to pin CS1- of U6, and pin CS2 is tied high. Since the SRAM is configured for byte accesses, lines A16 - A0 are directly connected to pins A16 - A0 of U6. The write-enable signal is provided via line HWR- of the H8/3003.

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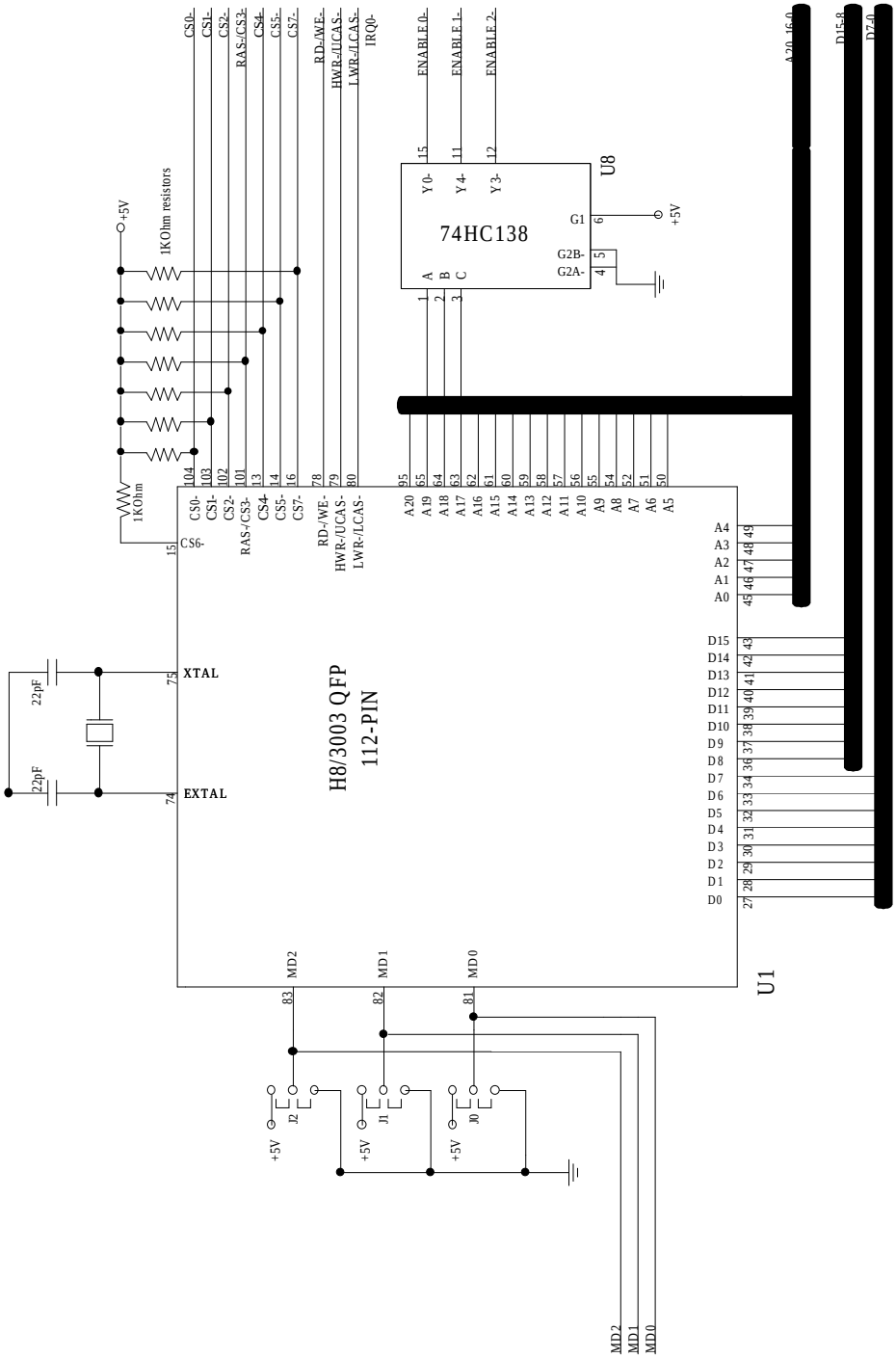

Figure 14. H8/3003 and address decoder.

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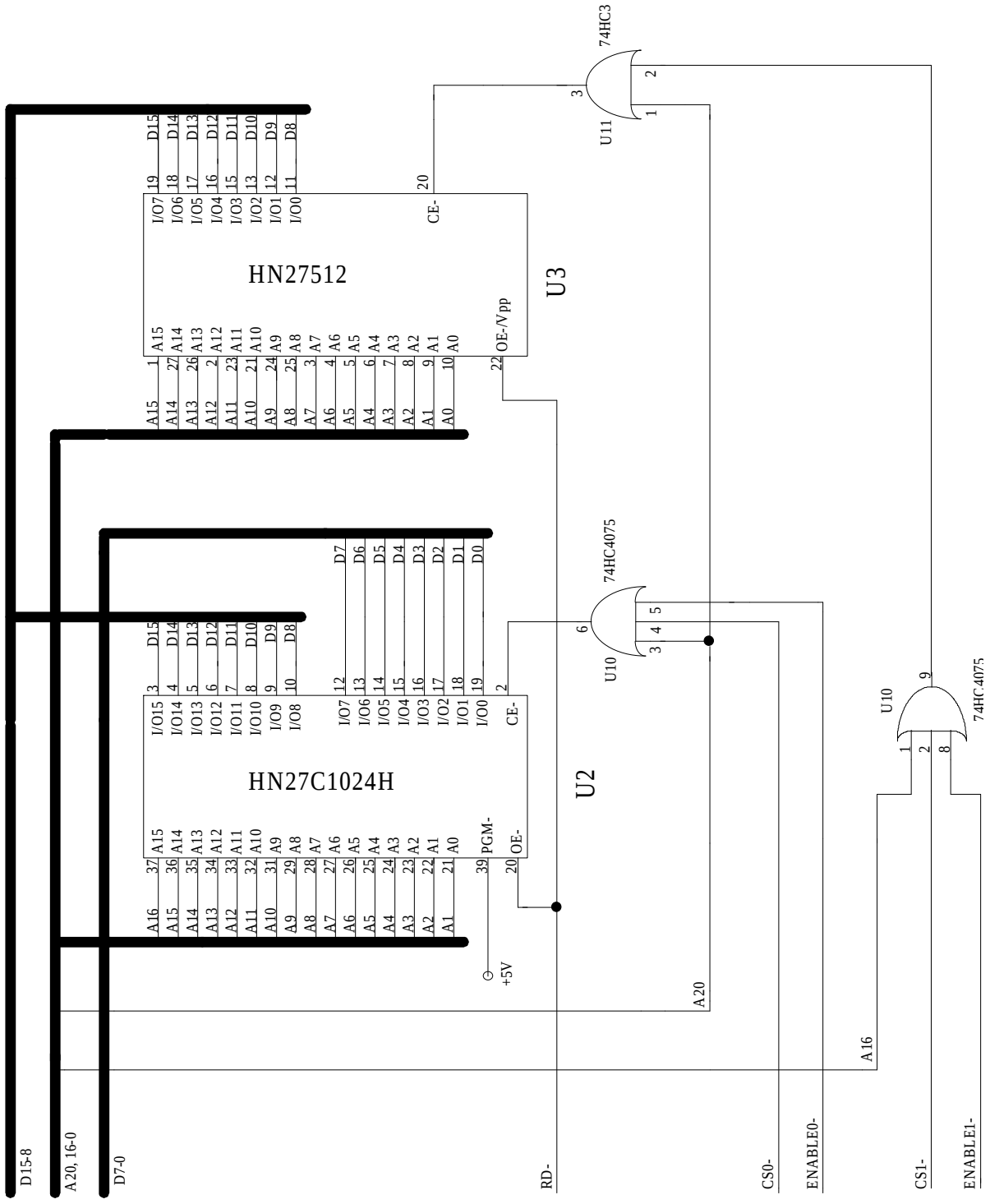

Figure 15. EPROM connection.

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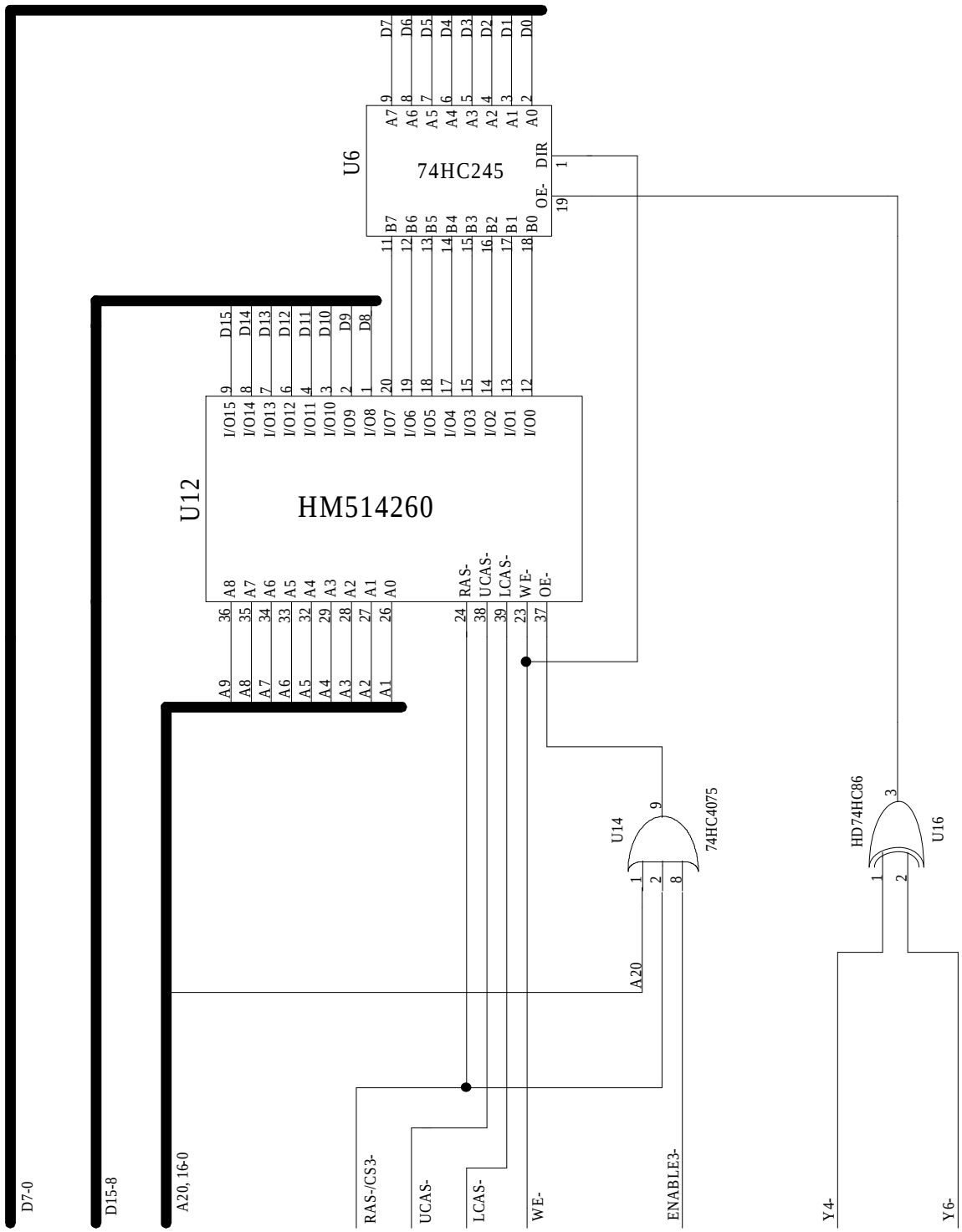

Figure 16. DRAM connection.

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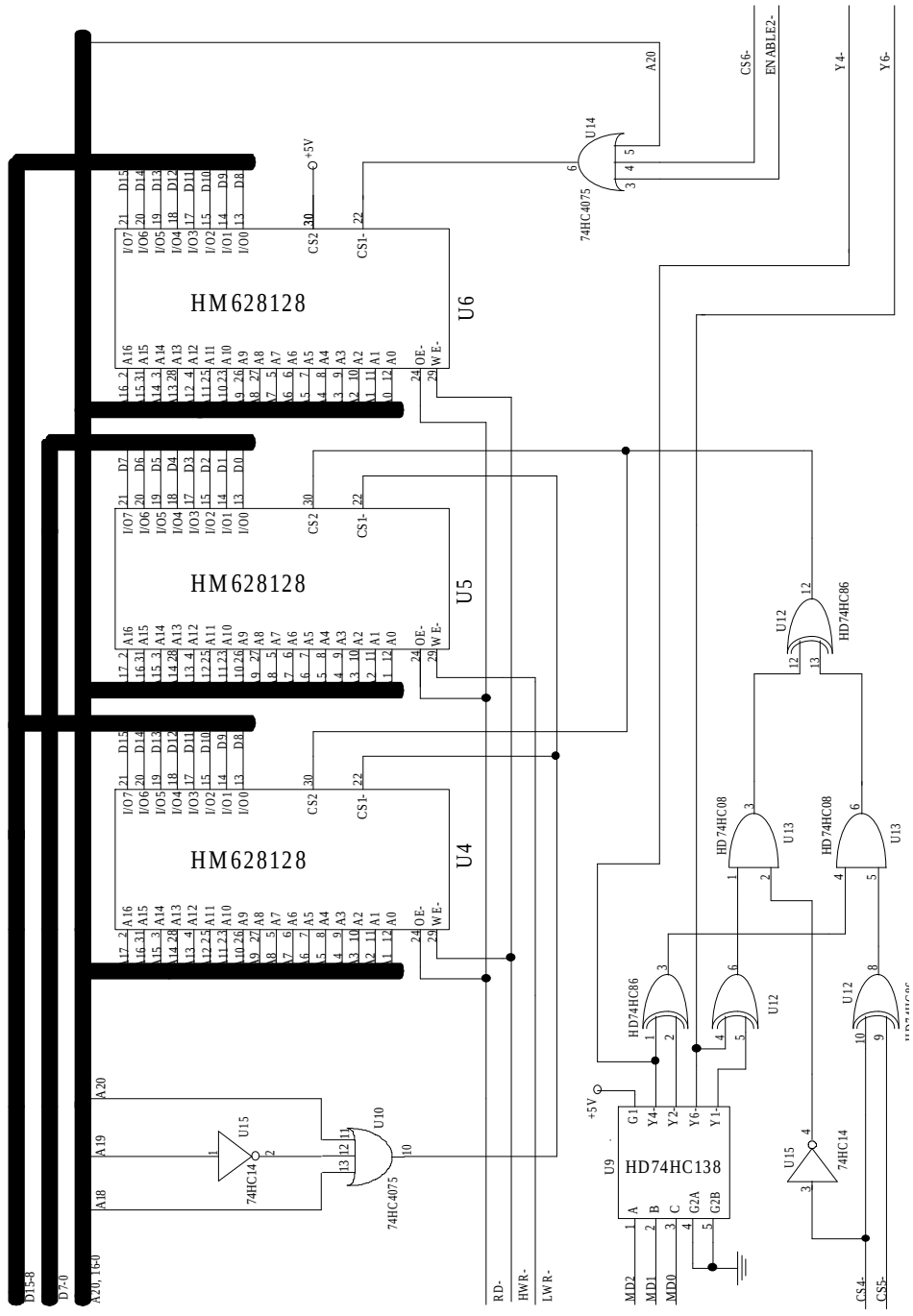

Figure 17. SRAM connection.

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