Hitachi Microcomputer

H8/3003 Interface

Application Note

HITACHI

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Introduction

The H8/300H series are Hitachi-designed high-performance 16-bit single-chip microcomputers incorporating peripheral functions that are optimal for embedded industrial applications. The H8/300H CPU is upward compatible with the H8/300 CPU.

The devices incorporate a CPU, RAM, DMA controller (DMAC), bus controller, timers, serial communication interface (SCI), and other functions that make them suitable for a broad range of applications in small to large systems.

The H8/3003 Interface Application Note gives examples of interfacing between the H8/3003 and peripheral LSIs, and is intended as a helpful reference for users during hardware design.

Although the sample tasks described in this application note have been checked for operation, it is recommended that users carry out their own operational checks before actual use.

Contents

Figures

Tables

Section 1 Manual Organization

This *H8/3003 Interface Application Note* describes methods of interfacing the H8/3003 with peripheral devices (ROM, RAM, timers LSIs etc.). The information for each example in section 3 is organized as shown in figure 1.1.

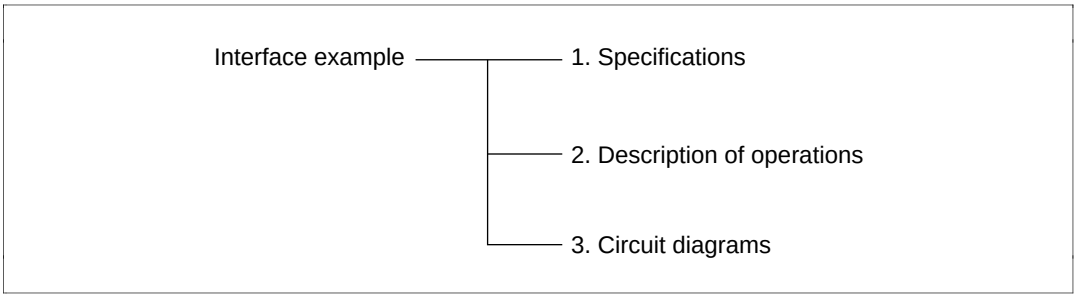


Figure 1.1 Organization of the Information in Interface Examples

1.1 Specifications

The specifications section describes the interconnected peripheral device names, circuit specifications of memory maps, etc.

1.2 Operation

The operation section describes circuit operation using timing charts.

1.3 Circuit Diagrams

The circuit diagram section shows the circuitry of interfaces with peripheral devices.

Section 2 Bus Control Functions

2.1 Bus Controller

Depending on the operation mode, the H8/3003 can be set for a maximum address space of 16 Mbytes (modes 3 and 4) or maximum of 1 Mbyte (modes 1 and 2). The maximum address space in the set mode is divided into 8 equal parts, ranging in order from the lower address area 0 through area 7. The access data bus width and number of access states can be set for each area using the bus controller. Wait states can be inserted automatically for interfacing with a slow external device, and the bus cycle can also be extended.

Register setting examples for area settings used in the interface examples are described in this application note. The following registers are used:

- Bus controller's bus width control register (ABWCR)
- Access state control register (ASTCR)
- Wait control register (WCR)
- Wait controller enable register (WCER)

Setting these registers sets the access bus width, number of access states, and presence of wait states for each area. The register functions are described in the following sections.

2.1.1 Area Byte/Word Control Register (ABWCR)

An 8-bit register that sets an 8-bit or 16-bit data bus access space for each area (figure 2.1). Bit 0 corresponds with area 0, and areas 0–7 are controlled by bits 0–7. Setting a bit value to 0 gives a 16-bit data bus access space, and setting to 1 gives an 8-bit data bus access space.

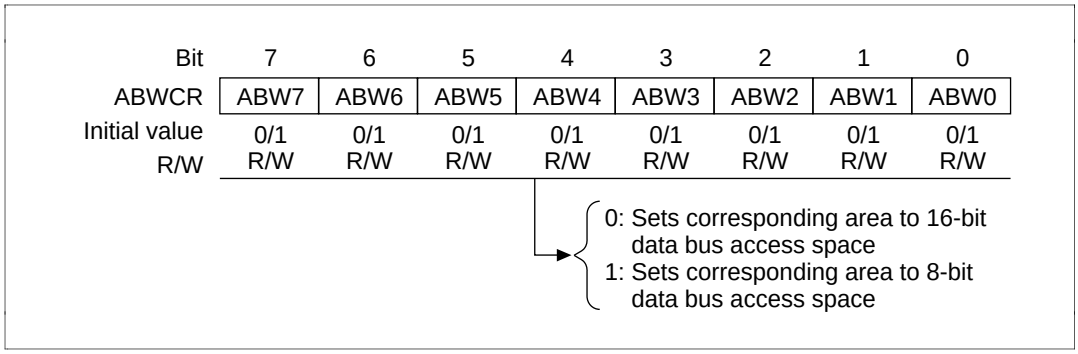


Figure 2.1 Area Byte/Word Control Register (ABWCR)

2.1.2 Area 2-State/3-State Control Register (ASTCR)

An 8-bit register that sets a 2-state or 3-state access space for each area (figure 2.2). Areas 0–7 are controlled by bits 0–7. Setting a bit value to 0 gives a 2-state access space, and a setting of 1 gives a 3-state access space.

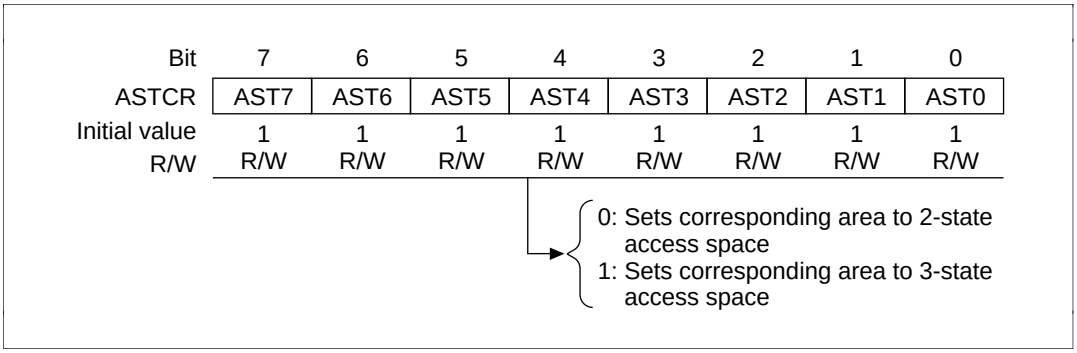


Figure 2.2 Area 2-State/3-State Control Register (ASTCR)

2.1.3 Wait Controller Enable Register (WCER)

An 8-bit register that enables/disables WSC operation for external 3-state access space (figure 2.3).

Areas 7–0 are controlled by bits 7–0. Setting a bit value to 0 disables the WSC, and a setting of 1 enables the WSC.

Wait states cannot be inserted for an area set to 2-state access. Therefore, the WCER bits corresponding to a 2-state access space set by the ASTCR have no meaning.

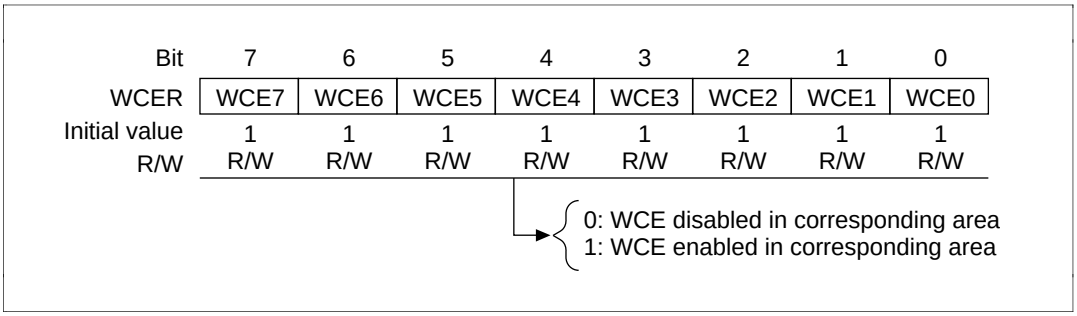


Figure 2.3 Wait Controller Enable Register (WCER)

2.1.4 Wait Control Register (WCR)

The wait control register (figure 2.4) is an 8-bit register that selects the number of wait states and the wait mode. Bits 1 and 0 (WC0 and WC1) specify the number of waits, bits 3 and 2 (WMS1 and WMS0) set wait mode (tables 2.1 and 2.2). Bits 7–4 are reserved bits and are not used.

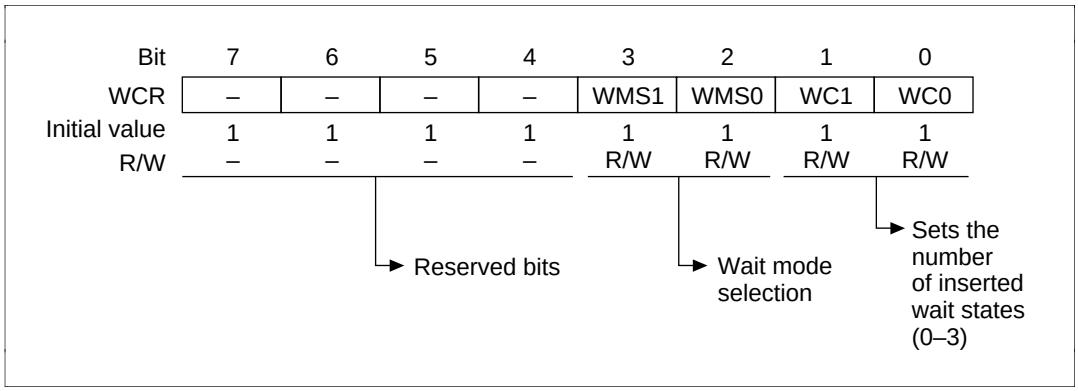


Figure 2.4 Wait Control Register (WCR)

Table 2.1 Wait Mode Selection

ASTCR	WCER	WCR		
ASTn	WCEn	WMS1	WMS0	Wait Mode
0	—	—	—	Disable
1	0	—	—	Pin wait mode 0
1	1	0	0	Programmable wait mode
		0	1	Disable
		1	0	Pin wait mode 1
		1	1	Pin auto-wait mode

Table 2.2 Wait Modes

Wait Mode	Description
Pin wait mode 0	Wait state can be inserted only by WAIT pin.
Pin wait mode 1	Normally, the wait state set by WC1/WC0 bits is inserted. Wait state due to WAIT pin can also be inserted.
Pin auto-wait mode	Insertion of wait states set by WAIT pin and WC1/WC0.
Programmable wait mode	Wait state set by WC0/WC1 always inserted. Wait state insertion by WAIT pin disabled.

2.2 Refresh Controller

The H8/3003 has a built-in refresh controller that can be connected directly to a ×16-bit configured DRAM. The refresh controller can also be connected to a PSRAM instead of a DRAM.

The address space that the refresh controller can control is area 3. Modes 1 and 2 (1-Mbyte mode) use a maximum of 128 kbytes, modes 3 and 4 (16-Mbyte mode) use a maximum of 2 Mbytes.

2.2.1 Refresh Control Register (RFSHCR)

RFSHCR is an 8-bit register (figure 2.5) that selects the refresh controller's operation mode. Setting this register enables selection of connecting device (DRAM/PSRAM), use or non-use of refresh, and the selection of access method.

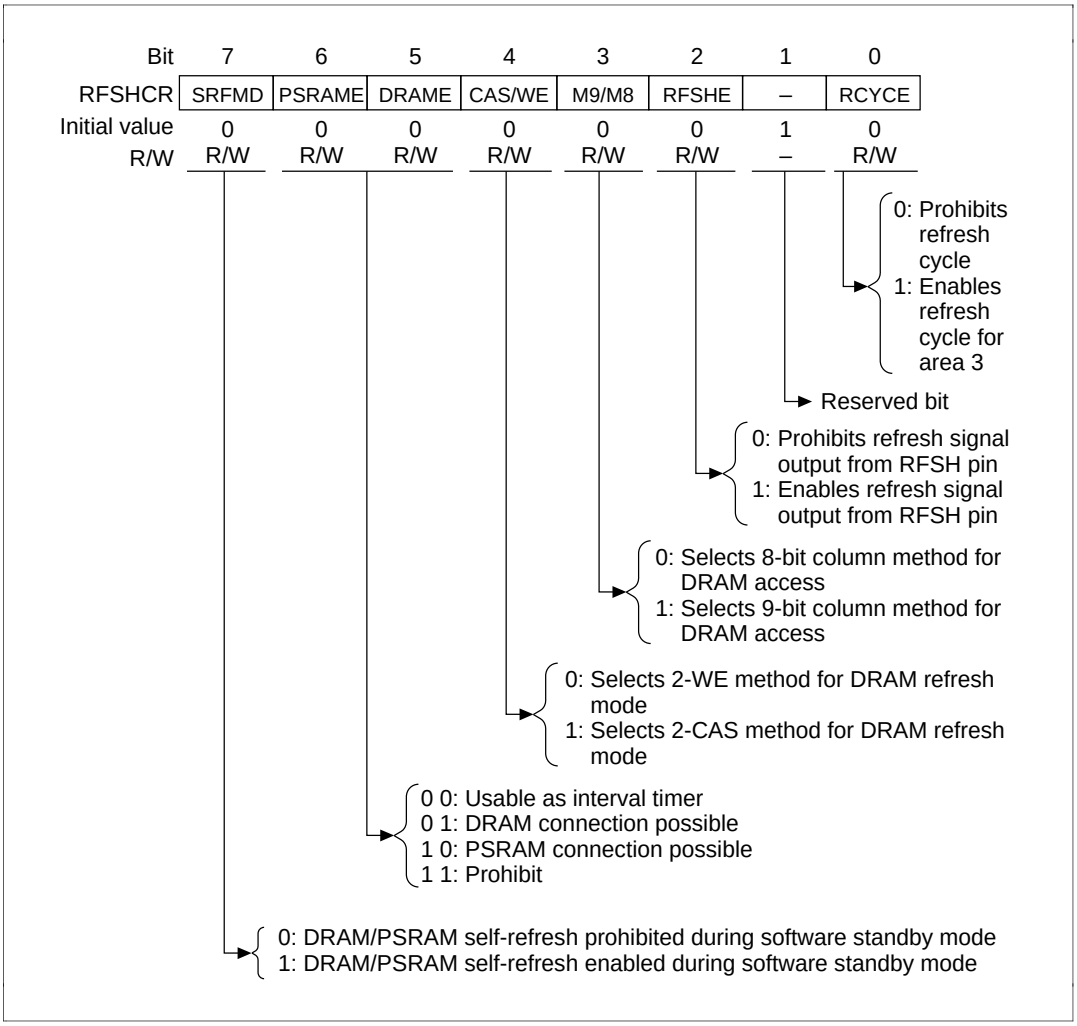


Figure 2.5 Refresh Control Register (RFSHCR)

2.2.2 Refresh Timer Control Status Register (RTMCSR)

RTMCSR is an 8-bit register (figure 2.6) that selects the refresh timer counter input clock.

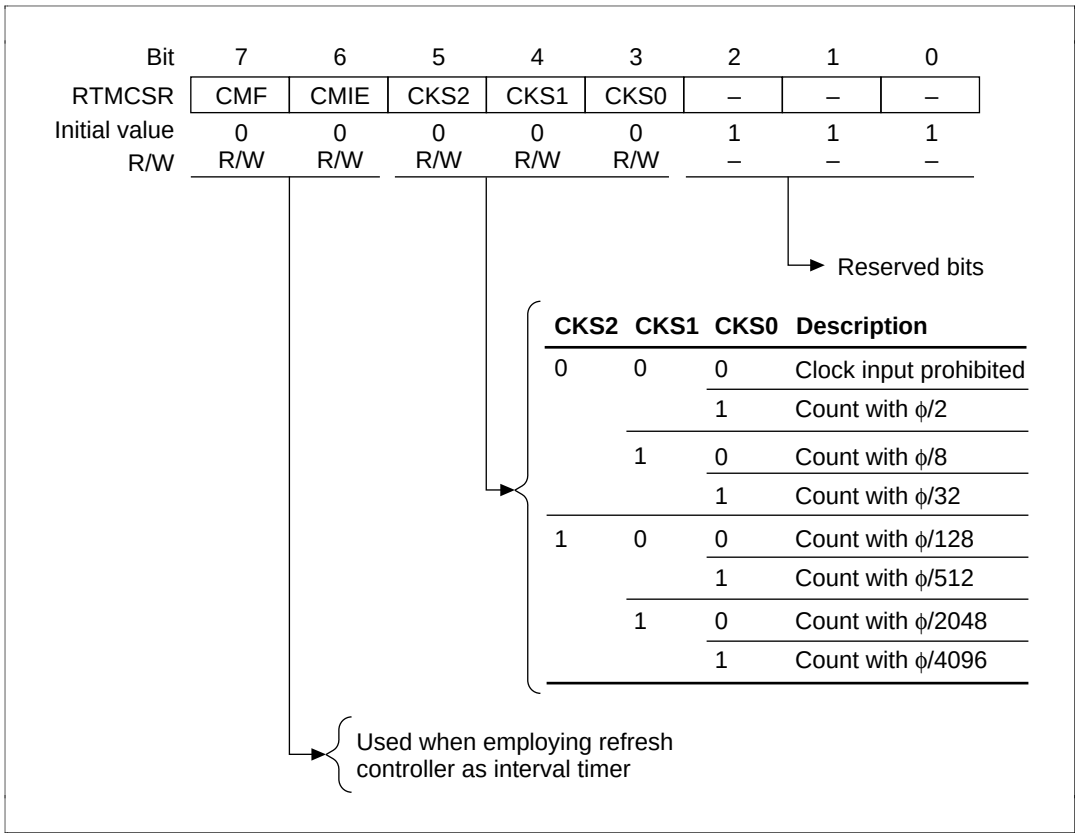


Figure 2.6 Refresh Timer Control Status Register (RTMCSR)

2.2.3 Refresh Timer Constant Register (RTCOR)

RTCOR is an 8-bit register (figure 2.7) that sets the refresh timer counter's clear cycle.

Refresh timer counter and refresh timer constant register values are continually compared, and the refresh timer counter is cleared when the two values match.

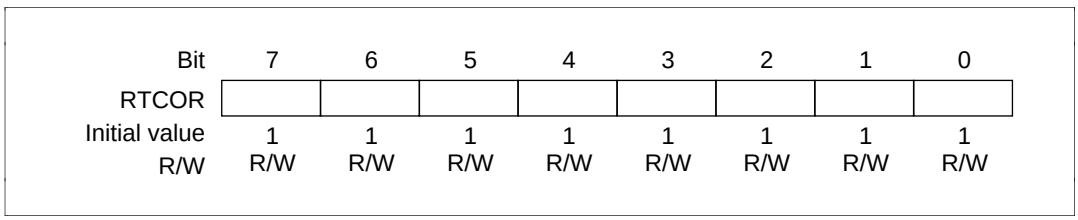


Figure 2.7 Refresh Timer Constant Register (RTCOR)

2.3 Bus Controller and Refresh Controller Setting Examples

Figure 2.8 shows the area map for the interface examples provided in this document.

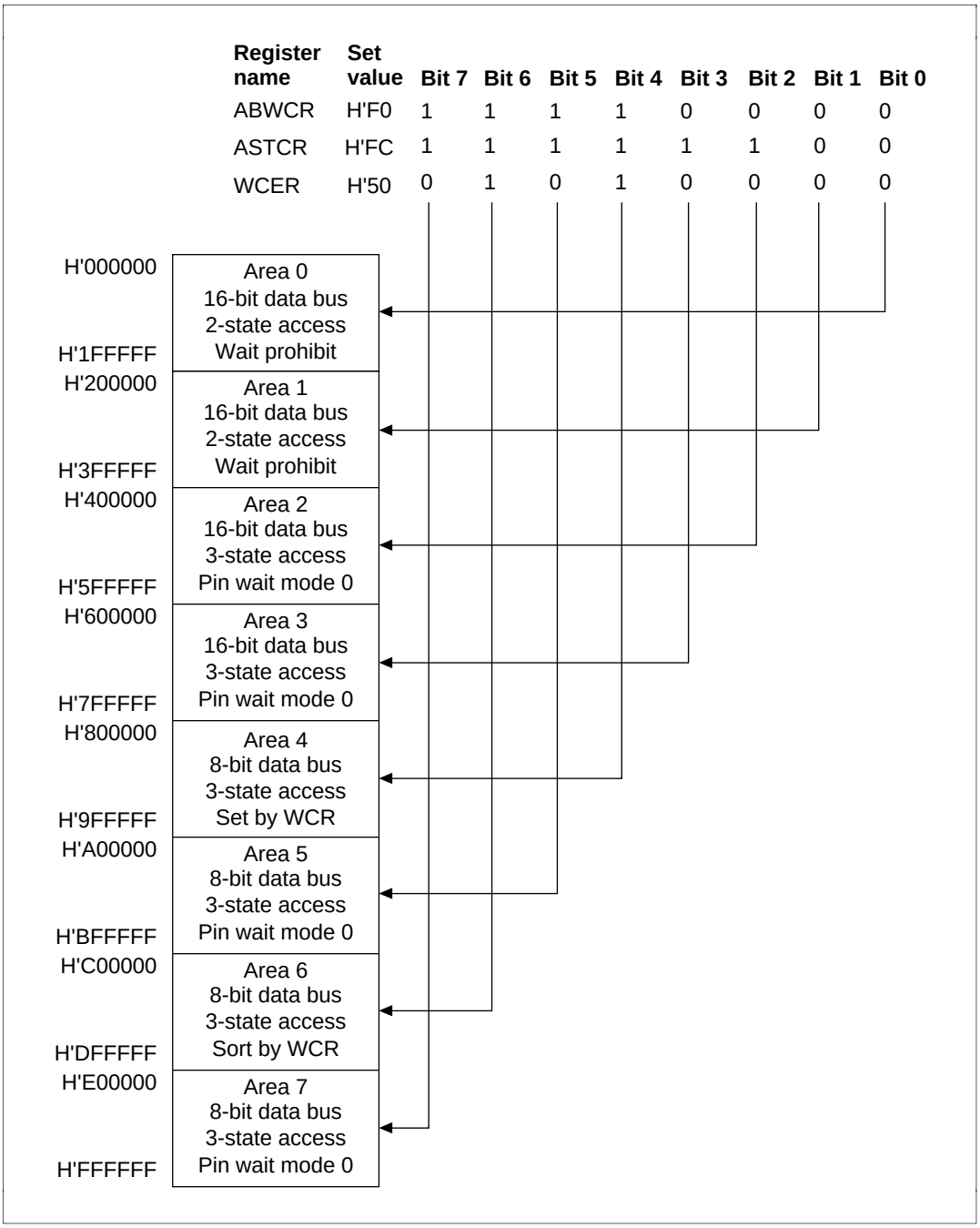


Figure 2.8 Area Map

The WCR (wait control register) setting differs depending on the connecting device. Table 2.3 lists settings for various devices used with the examples provided in this document.

Table 2.3 WCR Settings

Connecting Device	Wait Mode	Number of Waits	WCR
DPRAM	Pin wait mode	2 states	H'FA
LCD			H'FA
UPP		1 state	H'F9
PIO	Programmable wait mode		H'F1

Figure 2.9 shows register settings to set the areas for the interface examples covered by this application note.

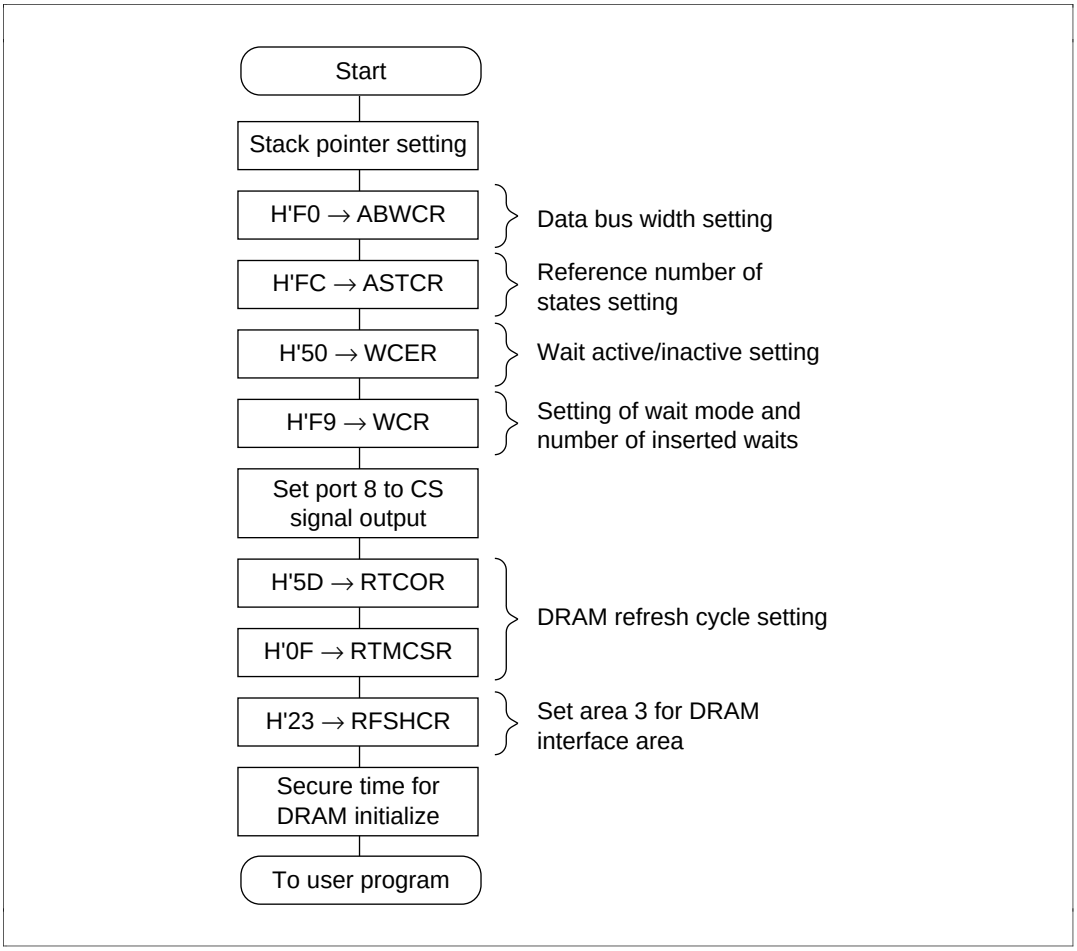


Figure 2.9 Register Settings

Section 3 Interface Examples

3.1 SRAM (HM62832H-45) Interface

MCU: H8/3003

Function: Mode 4 (16-bit data bus, 16-Mbyte address space)

3.1.1 Specifications

The H8/3003 mode 4 (16-bit data bus, 16-Mbyte address space) interface with an SRAM (HM62832H-45) is shown in figure 3.1.

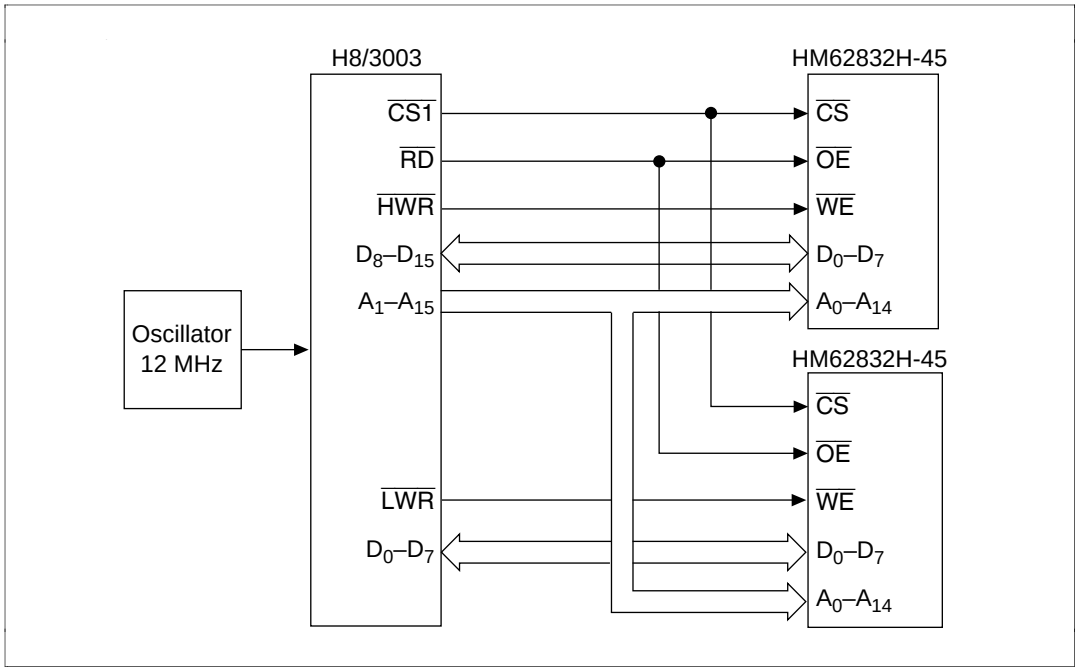


Figure 3.1 Block Diagram of H8/3003 and HM62832H-45 Interface

As shown in figure 3.2, area 1 (H'200000–H'3FFFFF) of the 16-Mbyte memory space is allotted. The area 1 bus controller settings are as follows:

- Data bus width: 16 bit bus
- Number of states: 2 states
- Wait mode: wait disabled

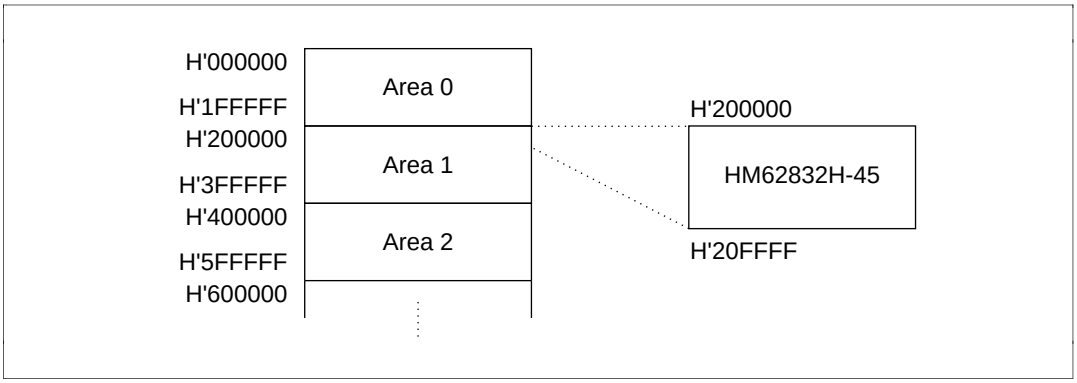


Figure 3.2 Memory Map

3.1.2 Operation

Data Read/Write: Figure 3.3 shows the read/write timing chart. When directly connecting the H8/3003 and HM62832H-45, check whether the following timing conditions are satisfied:

- H8/3003:
  - — t_{ACC1} and t_{ACC3} (read data access times)
  - — t_{RDH} (read data hold time)
- HM62832H-45:
  - — t_{DW} (data setup time)
  - — t_{DH} (data hold time)
  - — t_{CW} (chip select time)
  - — t_{WP} (write pulse width)

Figure 3.3 shows the timing as follows:

- H8/3003:
  - — t_{ACC1} and t_{ACC3}

    t_{ACC1} = t_{ACS} (max)
    = 45 ns ≤ 80 ns (H8/3003 t_{ACC1})

    t_{ACC3} = t_{OE} (max)
    = 20 ns ≤ 40 ns (H8/3003 t_{ACC3})

  - — t_{RDH}

    t_{RDH} = t_{CHZ} (min)
    = 0 ns ≥ 0 ns (H8/3003 t_{RDH})
- HM62832H-45:
  - — t_{DW} and t_{DH}

    t_{DW} = t_{WDS1} (min)
    = 60 ns ≥ 20 ns (HM62832H-45 t_{DW})

    t_{DH} = t_{WDH} (min)
    = 20 ns ≥ 0 ns (HM62832H-45 t_{DH})

  - — t_{CW} and t_{WP}

    t_{CW} = $T_1 + T_2 + t_{AD}$ (min) – t_{AD} (max)
    = 83.3 + 83.3 + 0 – 35
    = 131.6 ns ≥ 25 ns (HM62832H-45 t_{CW})

    t_{WP} = t_{WSW1} (min)
    = 55 ns ≥ 25 ns (HM62832H-45 t_{WP})

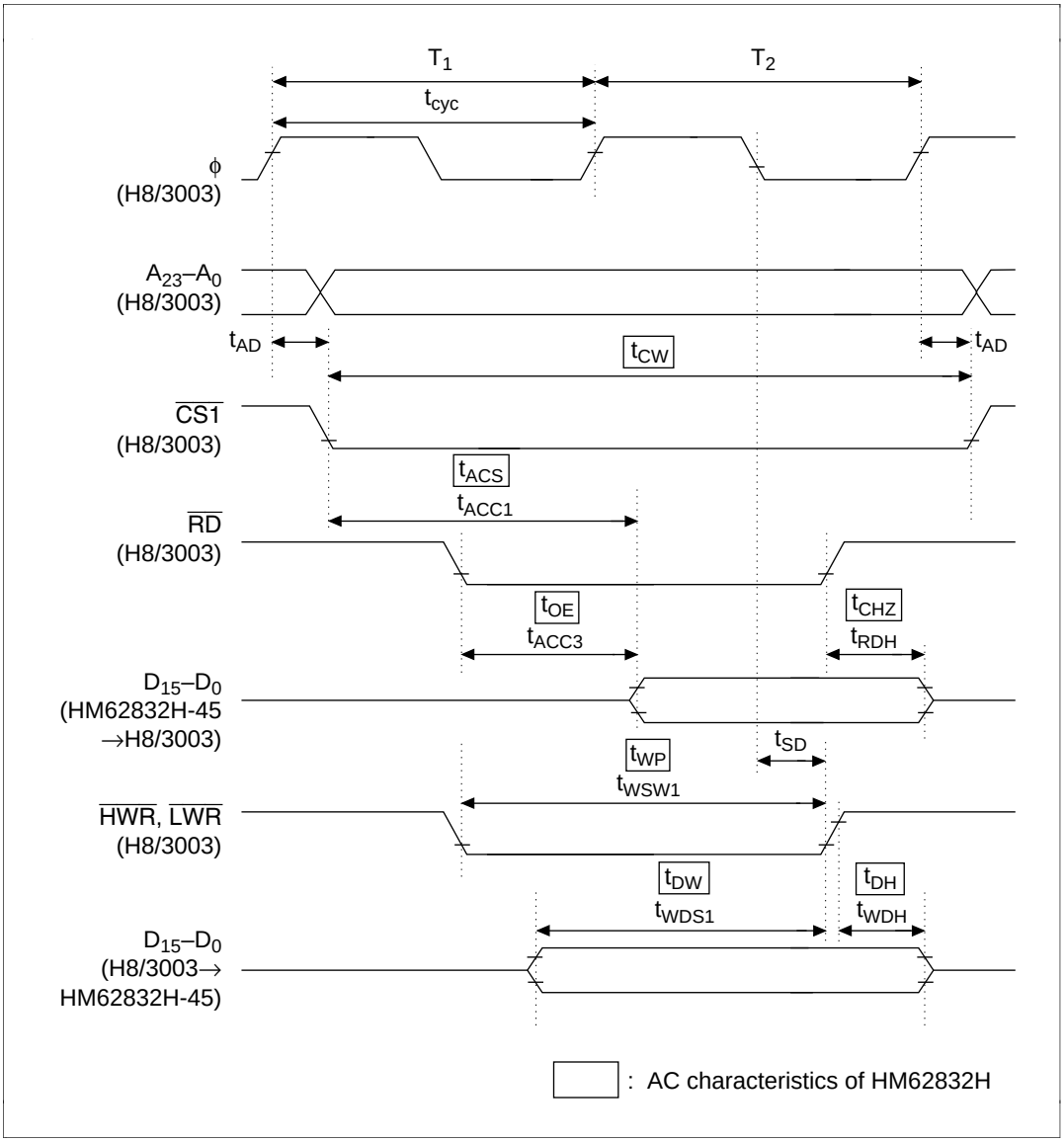


Figure 3.3 Read/Write Timing Chart

3.1.3 Circuit Diagram

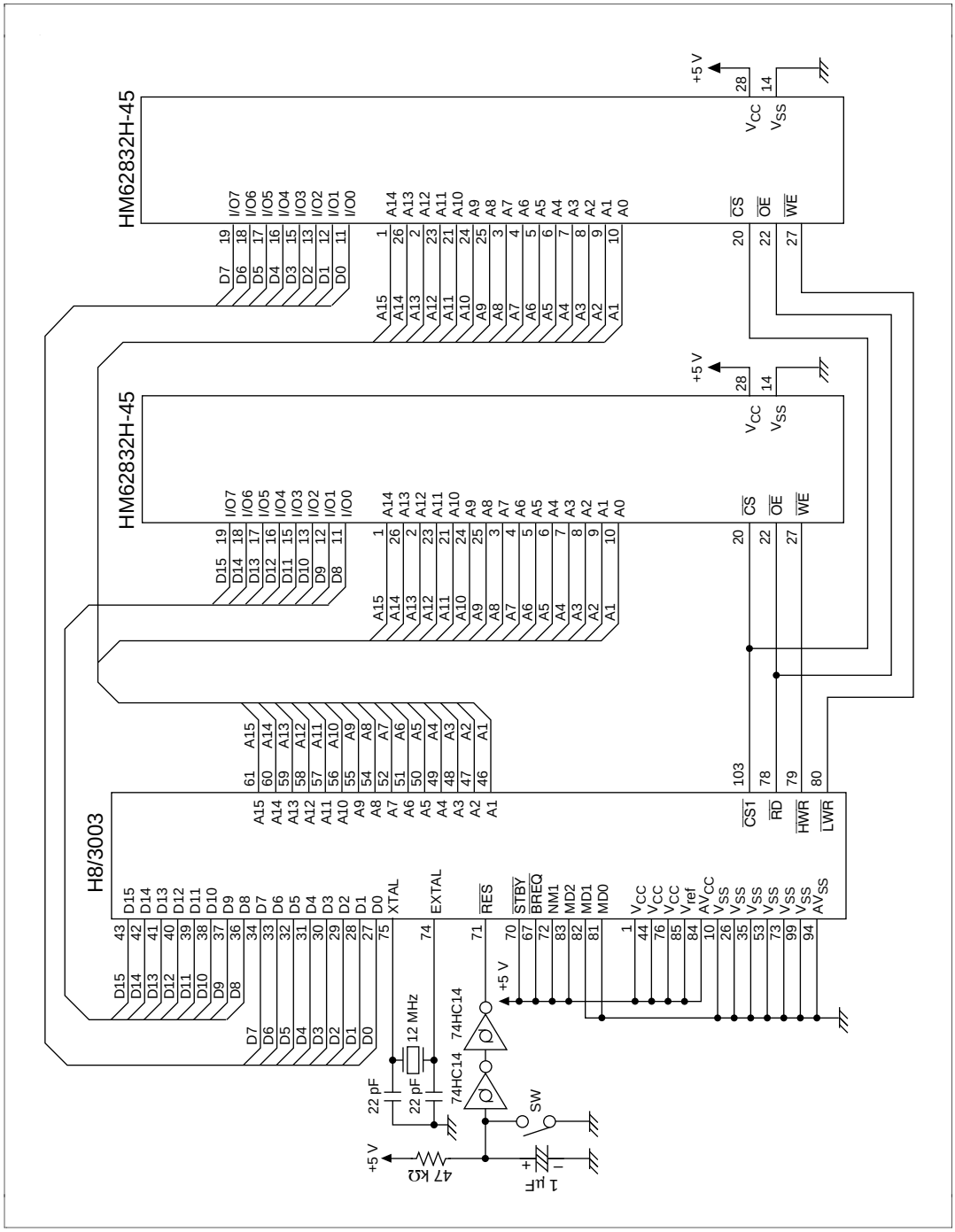


Figure 3.4 Circuit Diagram

3.2 EPROM (HN27C256-70) Interface

MCU: H8/3003

Function: Mode 4 (16-bit data bus, 16-Mbyte address space)

3.2.1 Specifications

The H8/3003 mode 4 (16-bit data bus, 16-Mbyte address space) interface with an EPROM (HN27C256-70) is shown in figure 3.5.

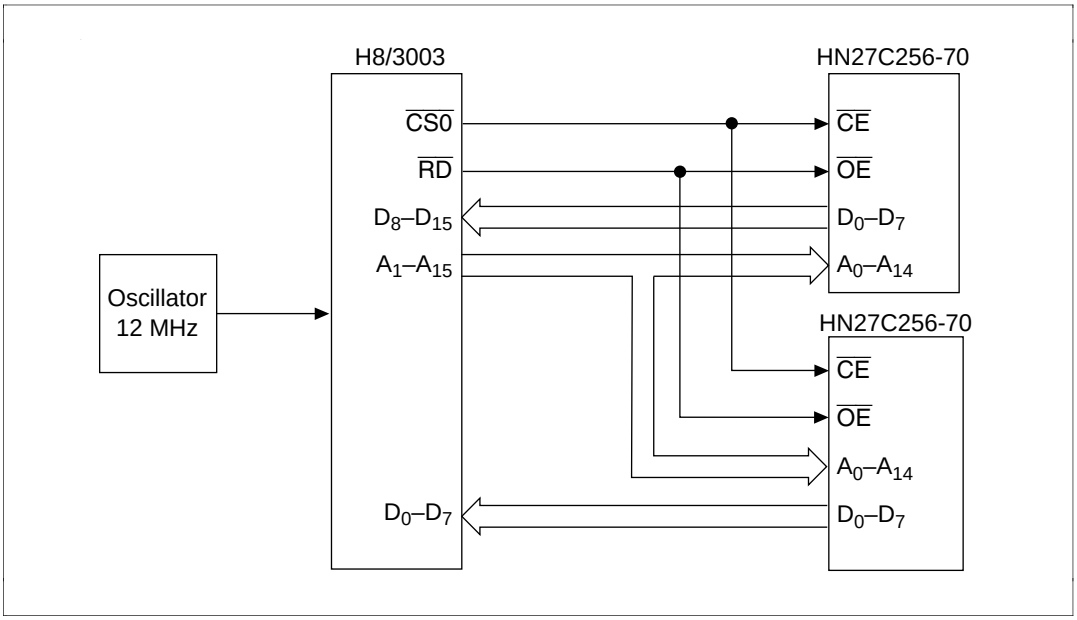


Figure 3.5 Block Diagram of H8/3003 and HN27C256-70 Interface

As shown in figure 3.6, area 0 (H'000000–H'1FFFFF) of the 16-Mbyte memory space is allotted. The area 0 bus controller settings are as follows:

- Data bus width: 16 bit bus
- Number of states: 2 states
- Wait mode: wait disabled

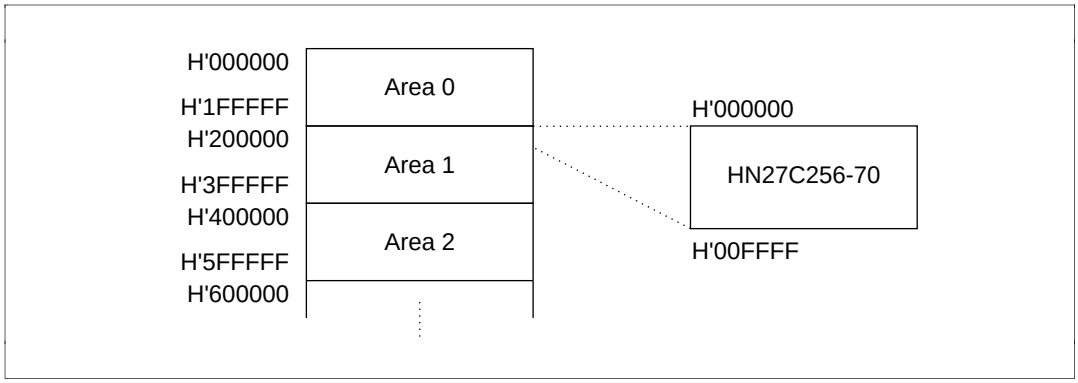


Figure 3.6 Memory Map

3.2.2 Data Read

Figure 3.7 shows the data read timing chart. When directly connecting the H8/3003 and HN27C256-70, check whether the following timing conditions are satisfied:

- H8/3003:
  - — t_{ACC1} and t_{ACC3} (read data access times)
  - — t_{RDH} (read data hold time)

Figure 3.7 shows the timing as follows:

- H8/3003:
  - — t_{ACC1} and t_{ACC3}

    t_{ACC1} = t_{CE} (max)
    = 70 ns ≤ 80 ns (H8/3003 t_{ACC1})

    t_{ACC3} = t_{OE} (max)
    = 40 ns ≤ 40 ns (H8/3003 t_{ACC3})

  - — t_{RDH}

    t_{RDH} = t_{DOH} (min)
    = 5 ns ≥ 0 ns (H8/3003 t_{RDH})

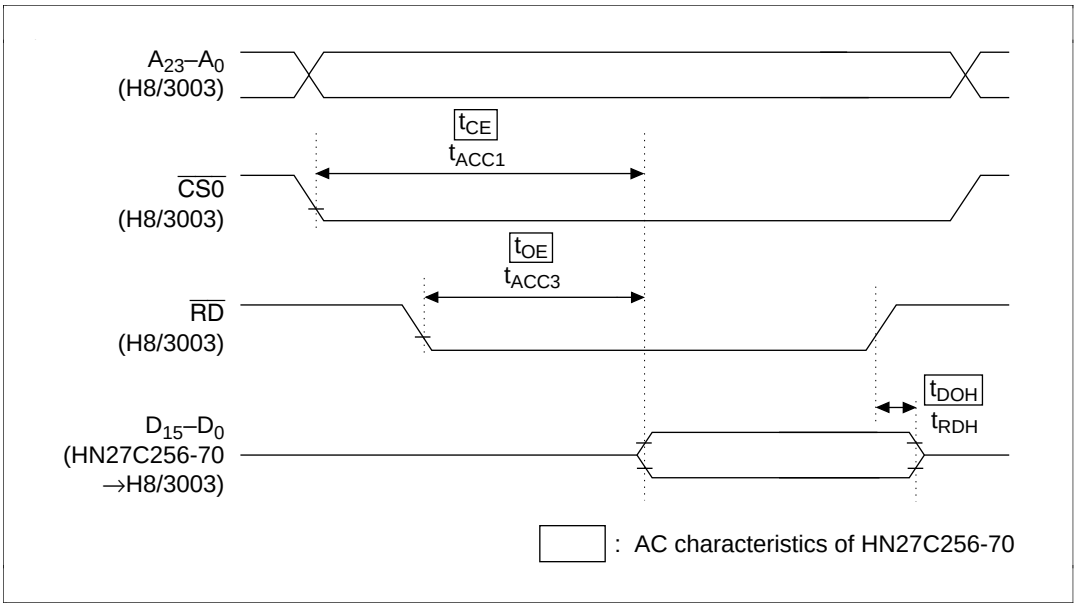


Figure 3.7 Read Timing Chart

3.2.3 Circuit Diagram

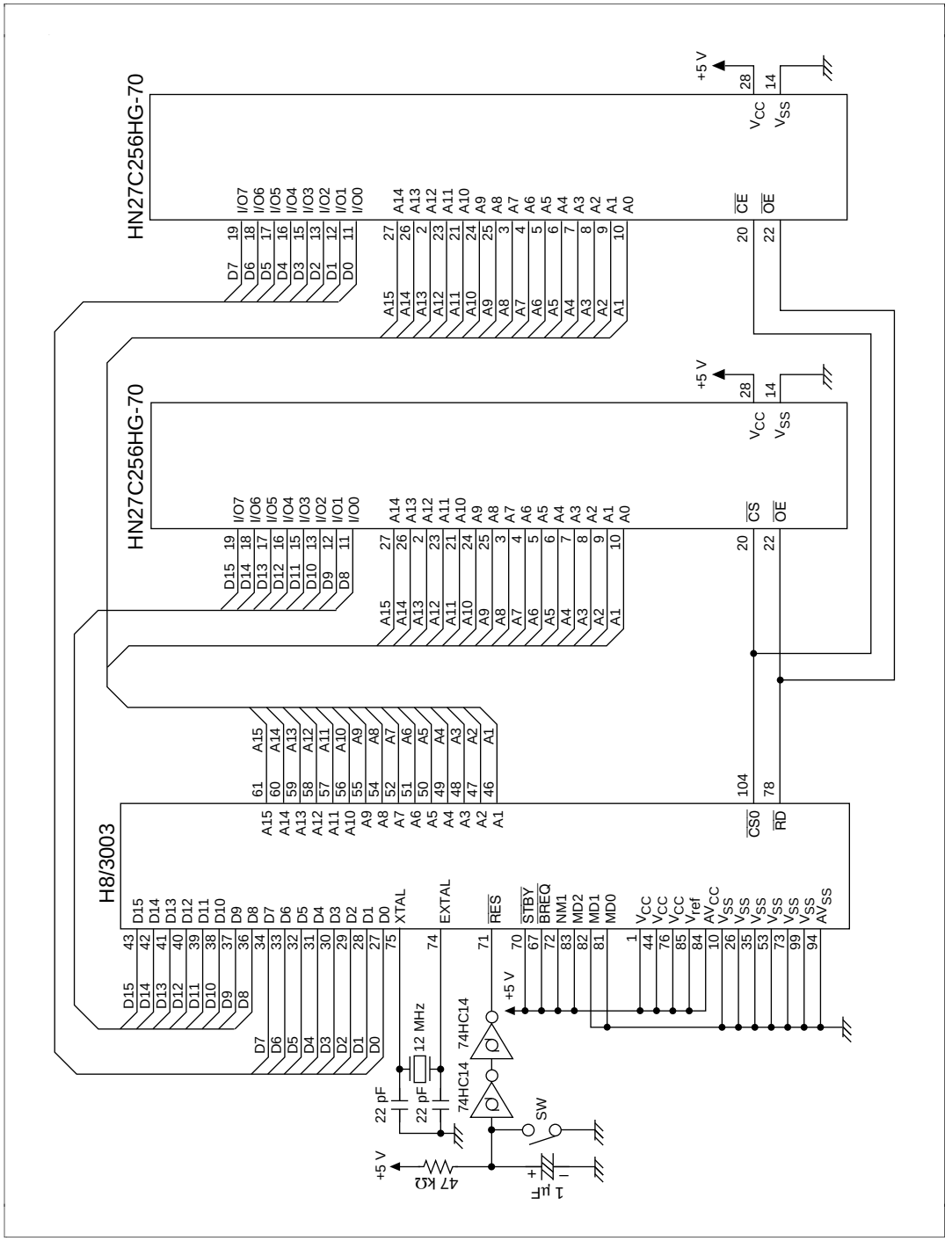


Figure 3.8 HN27C256-70 Interface

3.3 DPRAM (HD63310RP20) Interface

MCU: H8/3003

Function: Mode 4 (16-bit data bus, 16-Mbyte address space)

3.3.1 Specifications

The H8/3003 mode 4 (16-bit data bus, 16-Mbyte address space) interface with a DPRAM (HD63310RP20) is shown in figure 3.9.

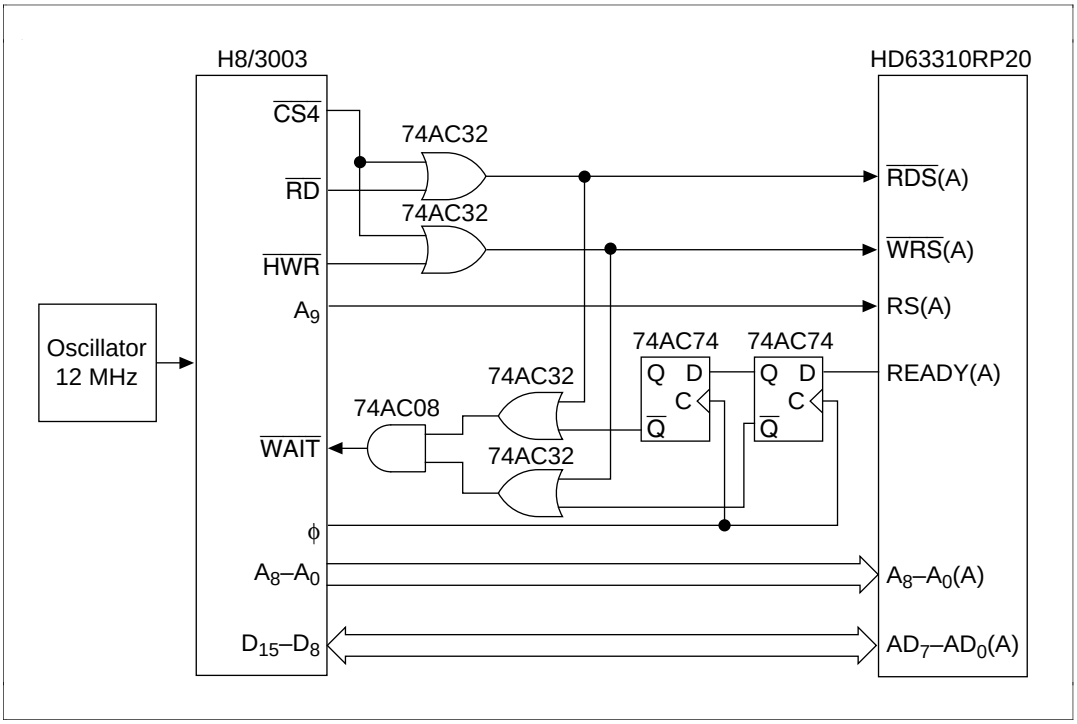


Figure 3.9 Block Diagram of the H8/3003 and HD63320RP20 Interface

As shown in figure 3.10, area 4 (H'800000–H'9FFFFF) of the 16-Mbyte memory space is allotted. The area 4 bus controller settings are as follows:

- Data bus width: 8 bit bus
- Number of states: 3 states
- Wait mode: pin wait mode 1
- Number of waits: 2 states

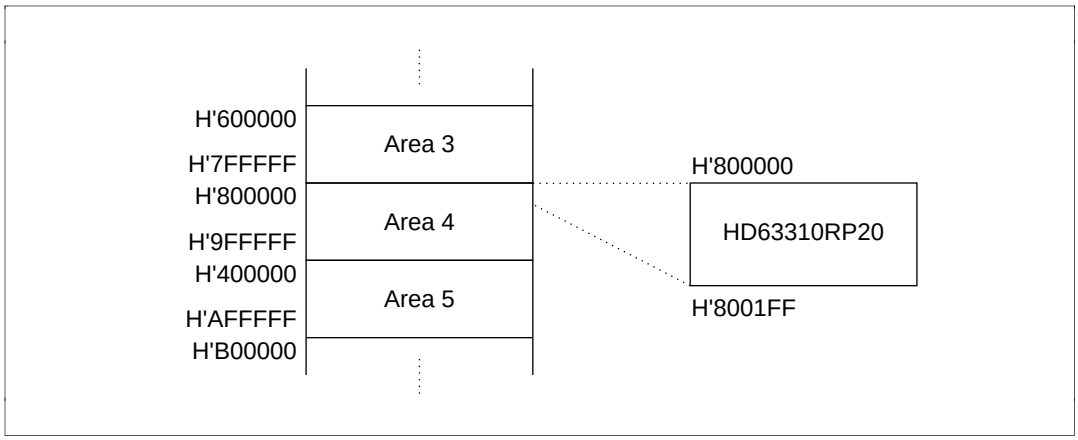


Figure 3.10 Memory Map

3.3.2 Wait Signal Generator

Figure 3.11 shows the wait signal generator circuit. Figure 3.12 shows the wait timing chart. When the H8/3003 and HD63310RP20 are connected, read/write from the H8/3003 is not conducted correctly while the HD63310RP20 is performing other processes. Therefore, a wait cycle is inserted in the read/write cycle until the HD63310RP20's READY signal falling edge, effecting a wait period to the end of HD63310RP20 processing.

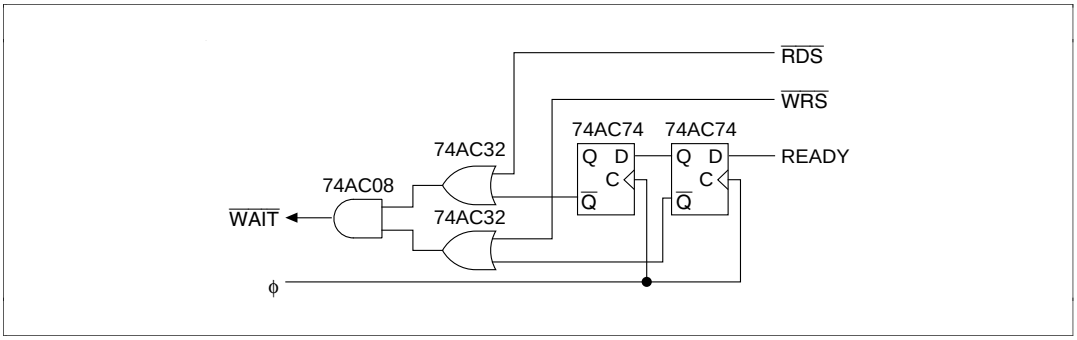


Figure 3.11 Wait Signal Generator

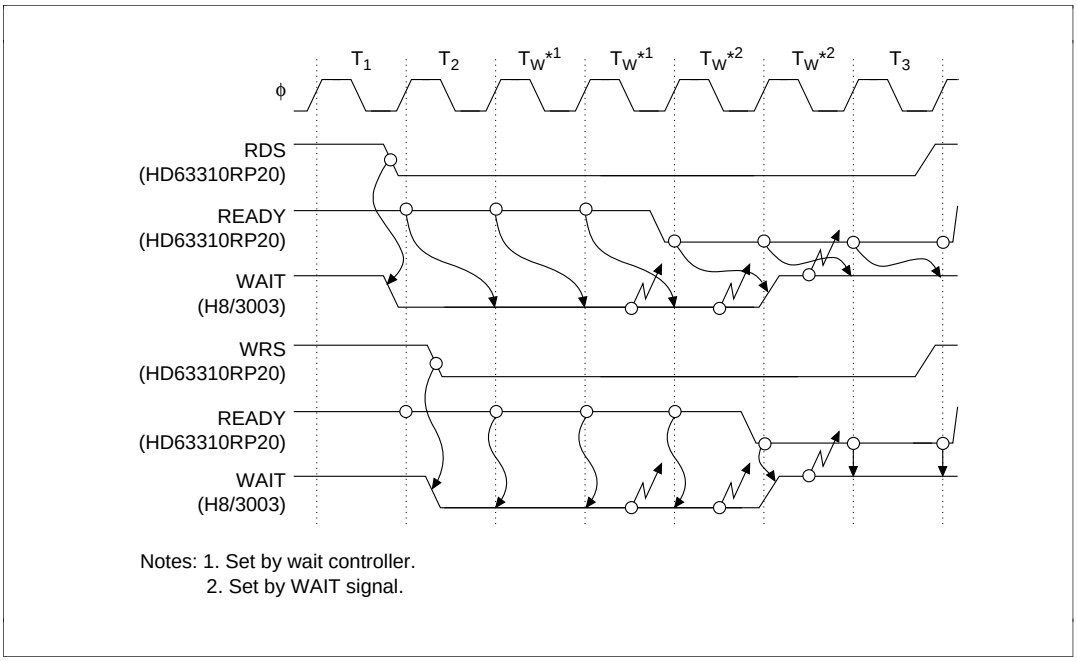


Figure 3.12 Wait Timing Chart

The WAIT signal is driven low at the falling edge of RDS and WRS. The READY signal is detected at the ϕ clock rising edge, and after detection of low level, the read cycle time is delayed by one clock, the write cycle follows immediately, and the WAIT signal is driven high.

3.3.3 Data Read/Write

Figure 3.13 shows the data read timing chart and figure 3.14 the write timing chart. When connecting the H8/3003 and HD63310RP20, check whether the following timing conditions are satisfied:

- H8/3003:
  - — t_{RDS} (read data setup time)
  - — t_{RDH} (read data hold time)
- HD63310RP20:
  - — t_{DSW} (data input setup time)
  - — t_{DHW} (data input hold time)

During the read cycle, HD63310RP20 data output timing is dependent on the READY signal falling edge. When calculating t_{RDS}, the READY signal falling edge timing becomes important, but as this timing varies widely due to HD63310RP20 operating conditions, t_{RDS} calculation has been performed using α to indicate the time from the READY signal falling edge to the next clock rising edge.

Figure 3.13 shows the timings as follows:

- H8/3003:
  - — t_{RDS} and t_{RDH}

$$t_{RDS} = \alpha\,(\text{min}) + T_W + T_W + t_{CH}\,(\text{min}) - t_{DDR}\,(\text{max})$$
$$= 0 + 83.3 + 83.3 + 30 - 120$$
$$= 76.6\ \text{ns} \geq 20\ \text{ns}\ (\text{H8/3003}\ t_{RDS})$$

$$t_{RDH} = t_{DHR}\,(\text{min}) + t_{DEL1}\,(\text{min})$$
$$= 10 + 0$$
$$= 10\ \text{ns} \geq 0\ \text{ns}\ (\text{H8/3003}\ t_{RDH})$$

- HD63310RP20:
  - — t_{DSW} and t_{DHW}

$$t_{DSW} = T_2 + T_W \times 2 + t_{CH}\,(\text{min}) + t_{SD}\,(\text{min}) + t_{DEL2}\,(\text{min}) - t_{WSD}\,(\text{max}) + t_{WDS2}\,(\text{min})$$
$$= 83.3 + 83.3 \times 2 + 30 + 0 + 0 - 35 + 10$$
$$= 254.9\ \text{ns} \geq 60\ \text{ns}\ (\text{HD63310RP20}\ t_{DSW})$$

$$t_{DHW} = t_{WDH}\,(\text{min}) - t_{DEL2}\,(\text{max})$$
$$= 20 - 8.5$$
$$= 11.5\ \text{ns} \geq 0\ \text{ns}\ (\text{HD63310RP20}\ t_{DHW})$$

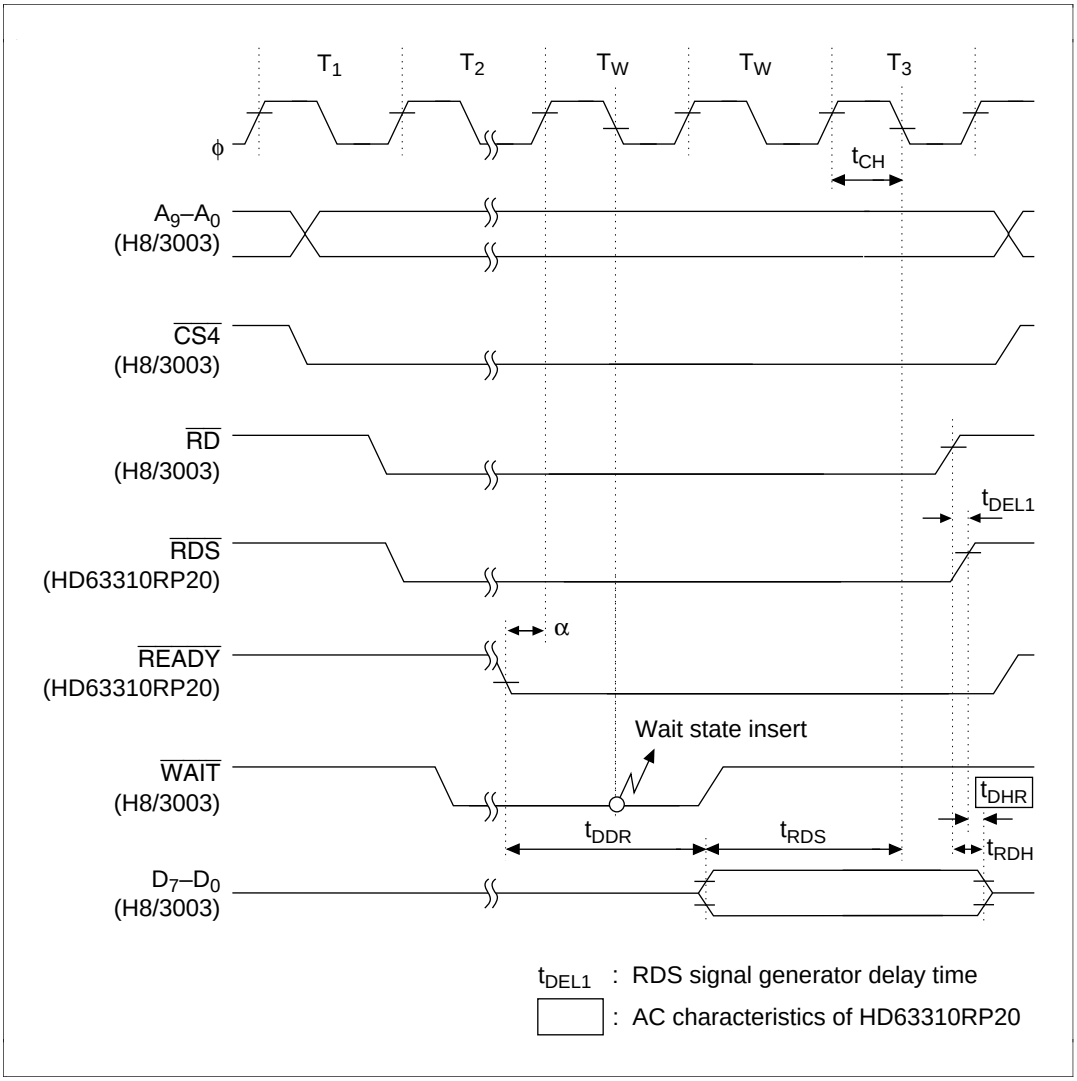


Figure 3.13 Read Timing Chart

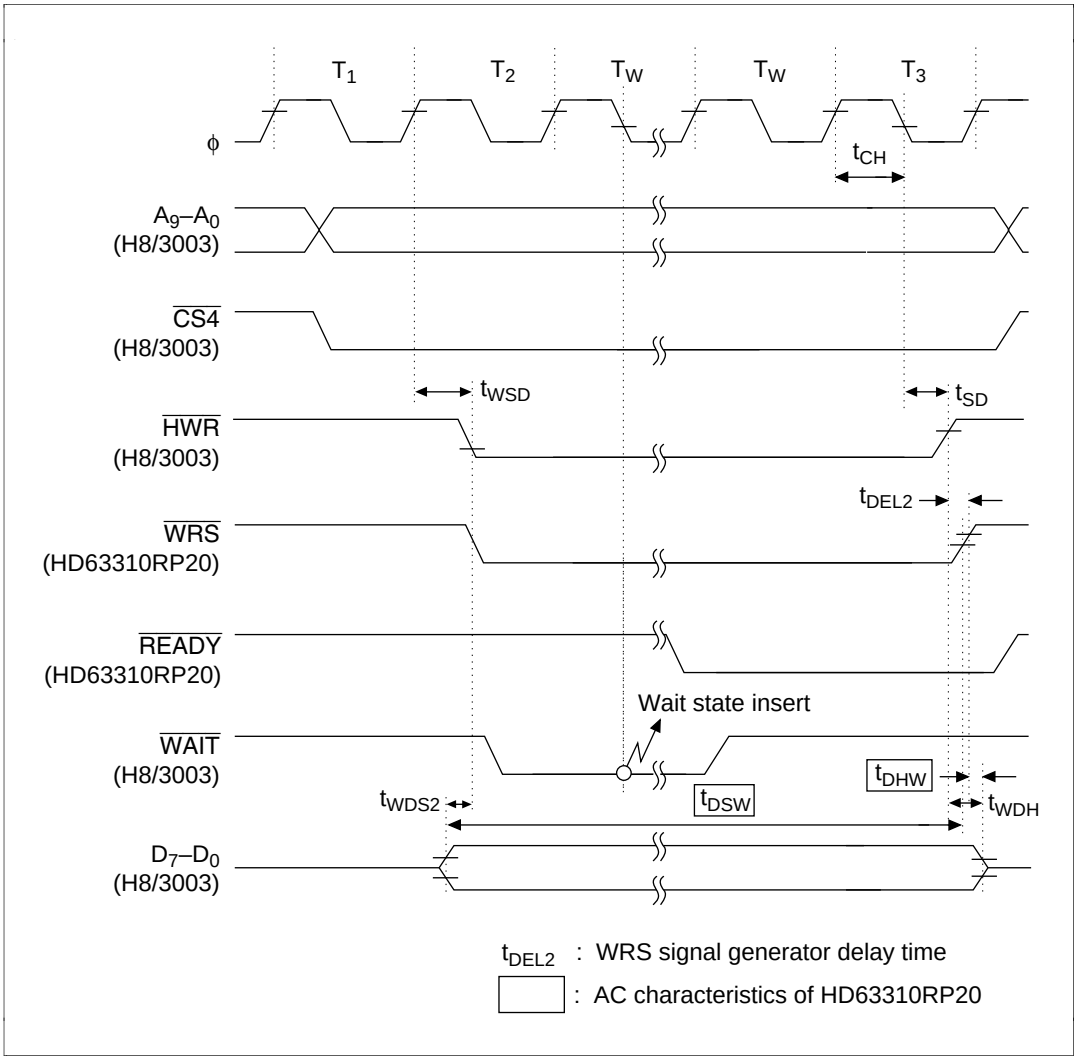


Figure 3.14 Write Timing Chart

3.3.4 Circuit Diagram

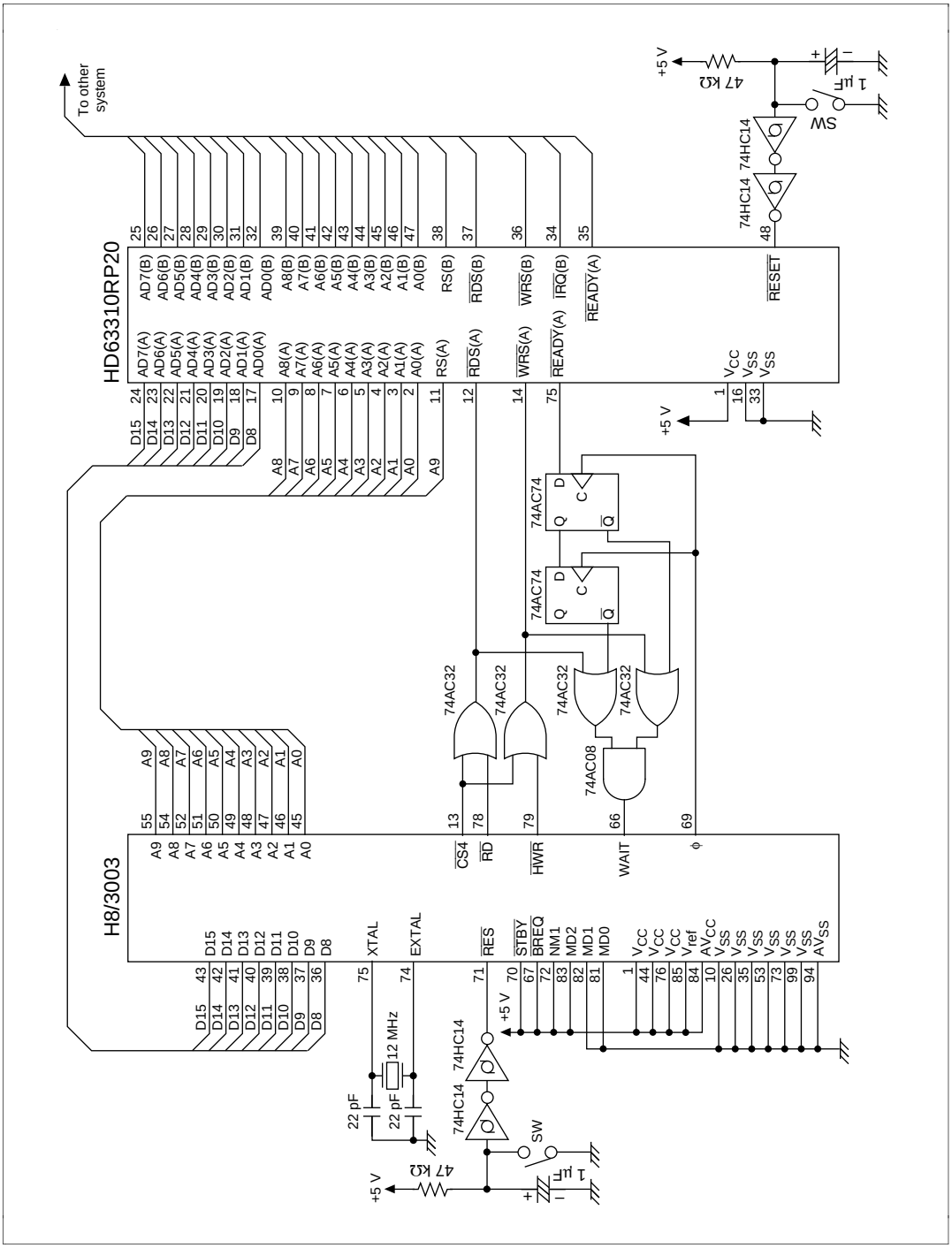


Figure 3.15 Circuit Diagram

3.4 Mask ROM (HN62444BNP) Interface

MCU: H8/3003

Function: Mode 4 (16-bit data bus, 16-Mbyte address space)

3.4.1 Specifications

The H8/3003 mode 4 (16-bit data bus, 16-Mbyte address space) interface with a mask ROM (HN62444BNP) is shown in figure 3.16.

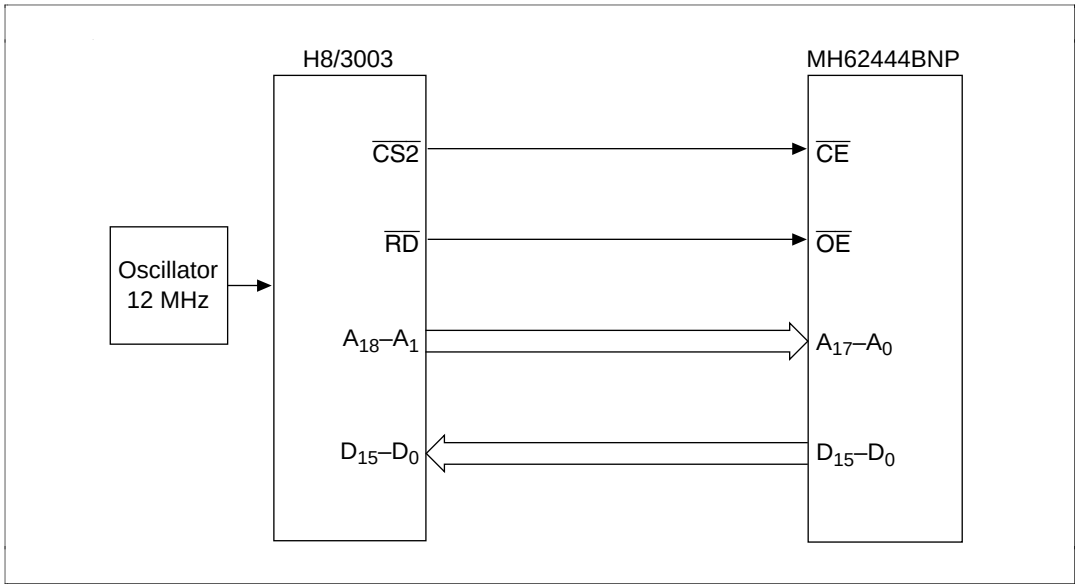


Figure 3.16 Block Diagram of H8/3003 and HN62444BNP Interface

As shown in figure 3.17, area 2 (H'400000–H'5FFFFF) of the 16-Mbyte memory space is allotted. The area 2 bus controller settings are as follows:

- Data bus width: 16 bit bus
- Number of states: 3 states
- Wait mode: pin wait mode 0

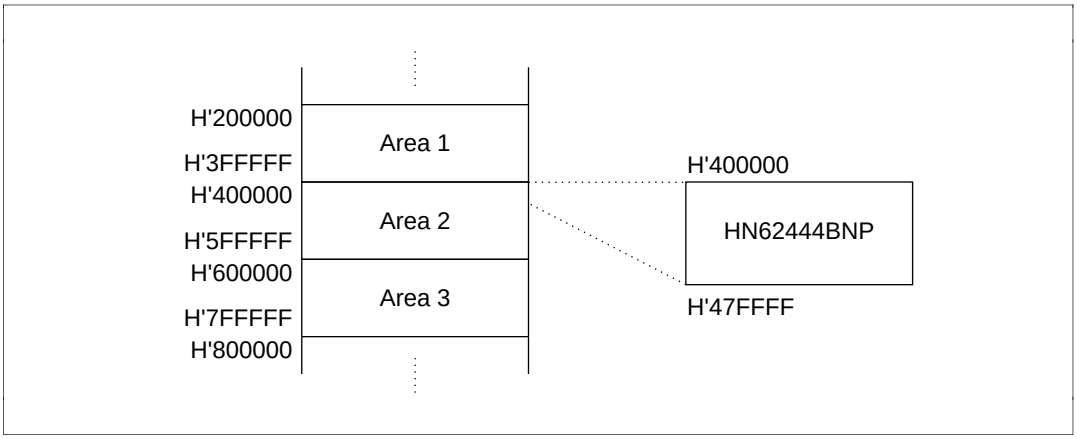


Figure 3.17 Memory Map

3.4.2 Data Read

Figure 3.18 shows the read timing chart. When directly connecting the H8/3003 and HN62444BNP, check whether the following timing conditions are satisfied:

- H8/3003:
  - — t_{ACC2} and t_{ACC4} (read data access times)
  - — t_{RDH} (read data hold time)

From figure 3.18, the timings are as follows:

- H8/3003:
  - — t_{ACC2} and t_{ACC4}

    t_{ACC2} = t_{ACE} (max)
    = 120 ns ≤ 160 ns (H8/3003 t_{ACC2})

    t_{ACC4} = t_{OE} (max)
    = 55 ns ≤ 120 ns (H8/3003 t_{ACC4})

  - — t_{RDH}

    t_{RDH} = t_{DHO} (min)
    = 0 ns ≥ 0 ns (H8/3003 t_{RDH})

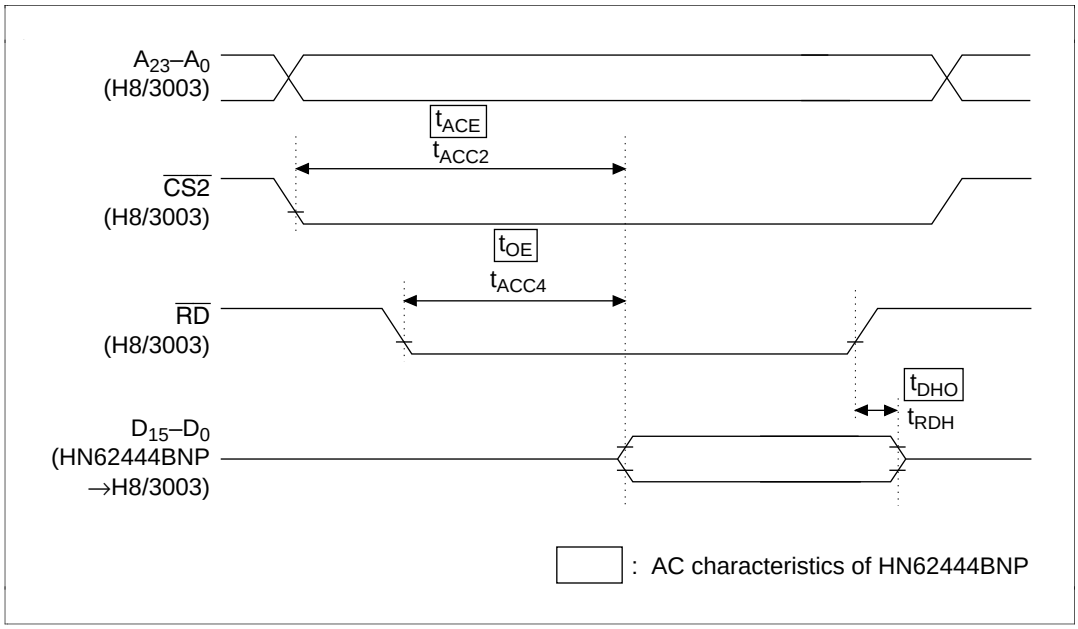


Figure 3.18 Read Timing Chart

3.4.3 Circuit Diagram

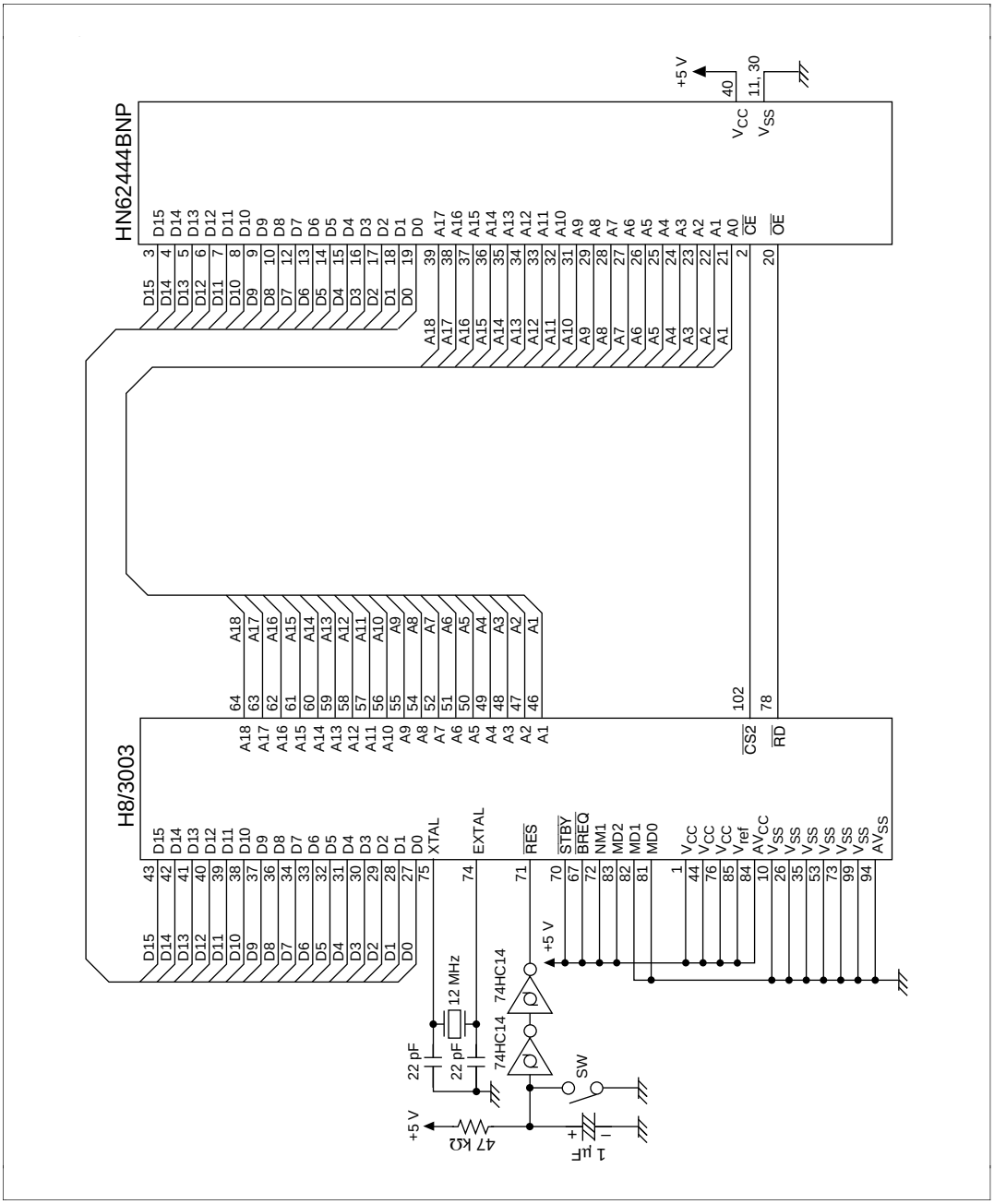


Figure 3.19 Circuit Diagram

3.5 Dummy SRAM (HM65256B-10) Interface

MCU: H8/3003

Function: Mode 4 (16-bit data bus, 16-Mbyte address space)

3.5.1 Specifications

The H8/3003 mode 4 (16-bit data bus, 16-Mbyte address space) interface with a dummy SRAM (HM65256B-10) is shown in figure 3.20.

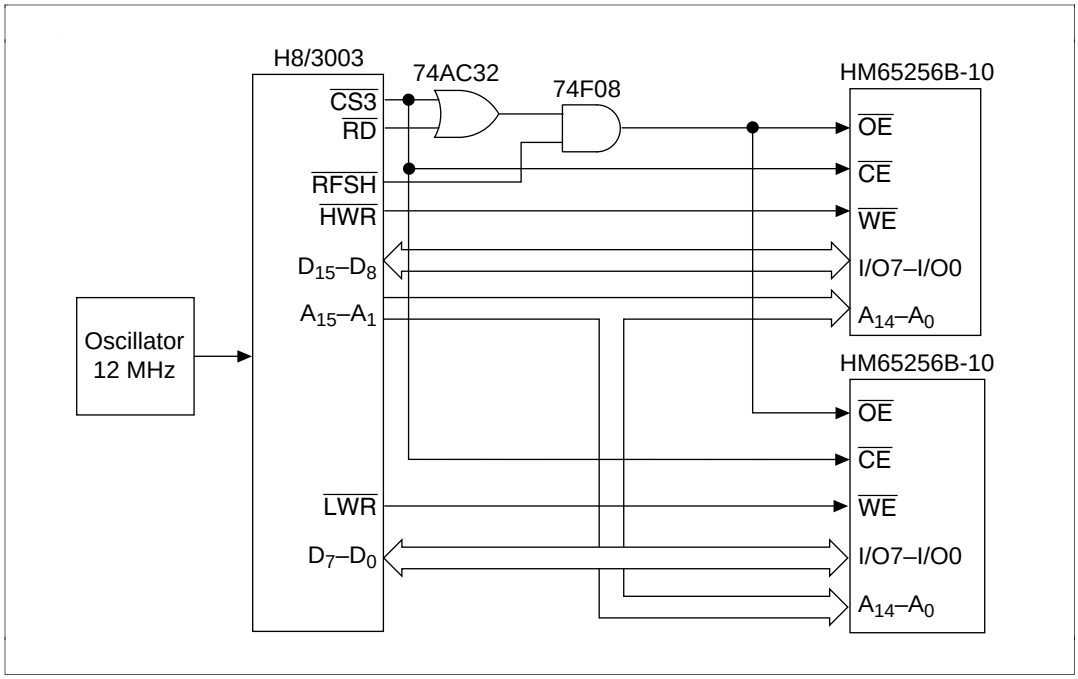


Figure 3.20 Block Diagram of H8/3003 and HM65256B Interface

As shown in figure 3.21, area 3 (H'600000–H'7FFFFF) of the 16-Mbyte memory space is allotted. The area 3 bus controller settings are as follows:

- Data bus width: 16 bit bus
- Number of states: 3 states
- Wait mode: pin wait mode 0
- Refresh controller: dummy SRAM mode

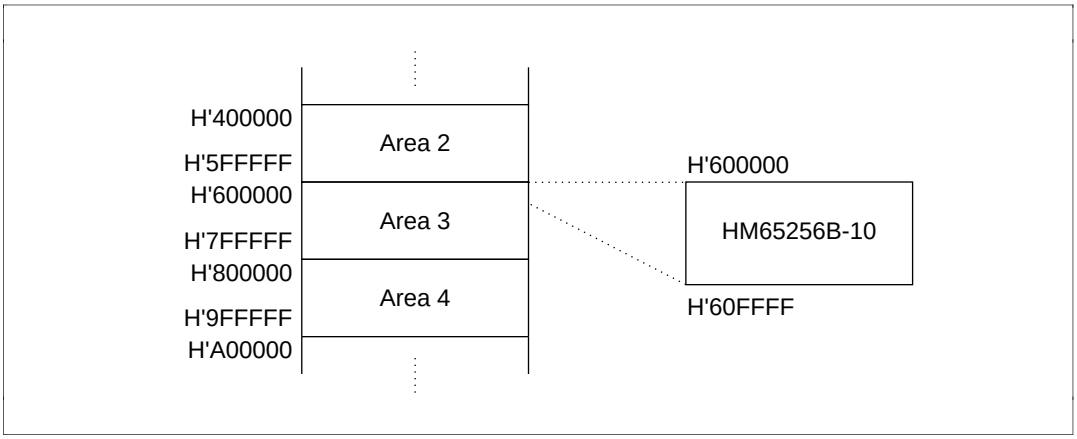


Figure 3.21 Memory Map

3.5.2 Data Read/Write

Figure 3.22 shows the read/write timing chart. When connecting the H8/3003 and HM65256B-10, confirm whether the following are satisfied:

- H8/3003:
  - t_{RDS} (read data setup time)
  - t_{RDH} (read data hold time)
- HM65256B-10:
  - t_{DW} (data input setup time)
  - t_{DH} (data input hold time)
  - t_P (chip enable pre-charge time)
  - t_{CE} (chip enable pulse width)
  - t_{RC} (random read/write cycle time)

Figure 3.22 shows the timing as follows:

- H8/3003:
  - t_{RDS} and t_{RDH}

$$t_{RDS} = T_2 + t_{CH}\,(\min) - t_{ASD}\,(\max) - t_{DEL}\,(\max) - t_{OEA}\,(\max)$$
$$= 83.3 + 30 - 35 - 14.8 - 40$$
$$= 23.5\ \text{ns} \geq 10\ \text{ns}\ (\text{H8/3003}\ t_{RDS})$$

$$t_{RDH} = t_{OHZ}\,(\min) + t_{DEH}\,(\min)$$
$$= 25 + 4$$
$$= 29\ \text{ns} \geq 0\ \text{ns}\ (\text{H8/3003}\ t_{RDH})$$

- HM65256B-10:
  - t_{DW} and t_{DH}

$$t_{DW} = T_2 + t_{CH}\,(\min) - t_{WSD}\,(\max) + t_{WDS2}\,(\min)$$
$$= 83.3 + 30 - 35 + 10$$
$$= 88.3\ \text{ns} \geq 20\ \text{ns}\ (\text{HM65256B-10}\ t_{DW})$$

$$t_{DH} = t_{WDH}\,(\min)$$
$$= 20\ \text{ns} \geq 5\ \text{ns}\ (\text{HM65256B-10}\ t_{DH})$$

— t_P, t_{CE}, and t_{RC}

t_P = t_{RP} (min)
= 55 ns ≥ 50 ns (HM65256B-10 t_P)

t_{CE} = t_{CL} (min) + T_2 + t_{CH} (min) + t_{RAD3} (min) – t_{RAD1} (max)
= 30 + 83.3 + 30 + 0 – 30
= 113.3 ns ≥ 100 ns (HM65256B-10 t_{CE})

t_{RC} = t_{CL} (min) + T_2 + t_{CH} (min) + t_{RAD3} (min) – t_{RAD1} (max) + t_{RP} (min)
= 30 + 83.3 + 30 + 0 – 30 + 55
= 168.3 ns ≥ 160 ns (HM65256B-10 t_{RC})

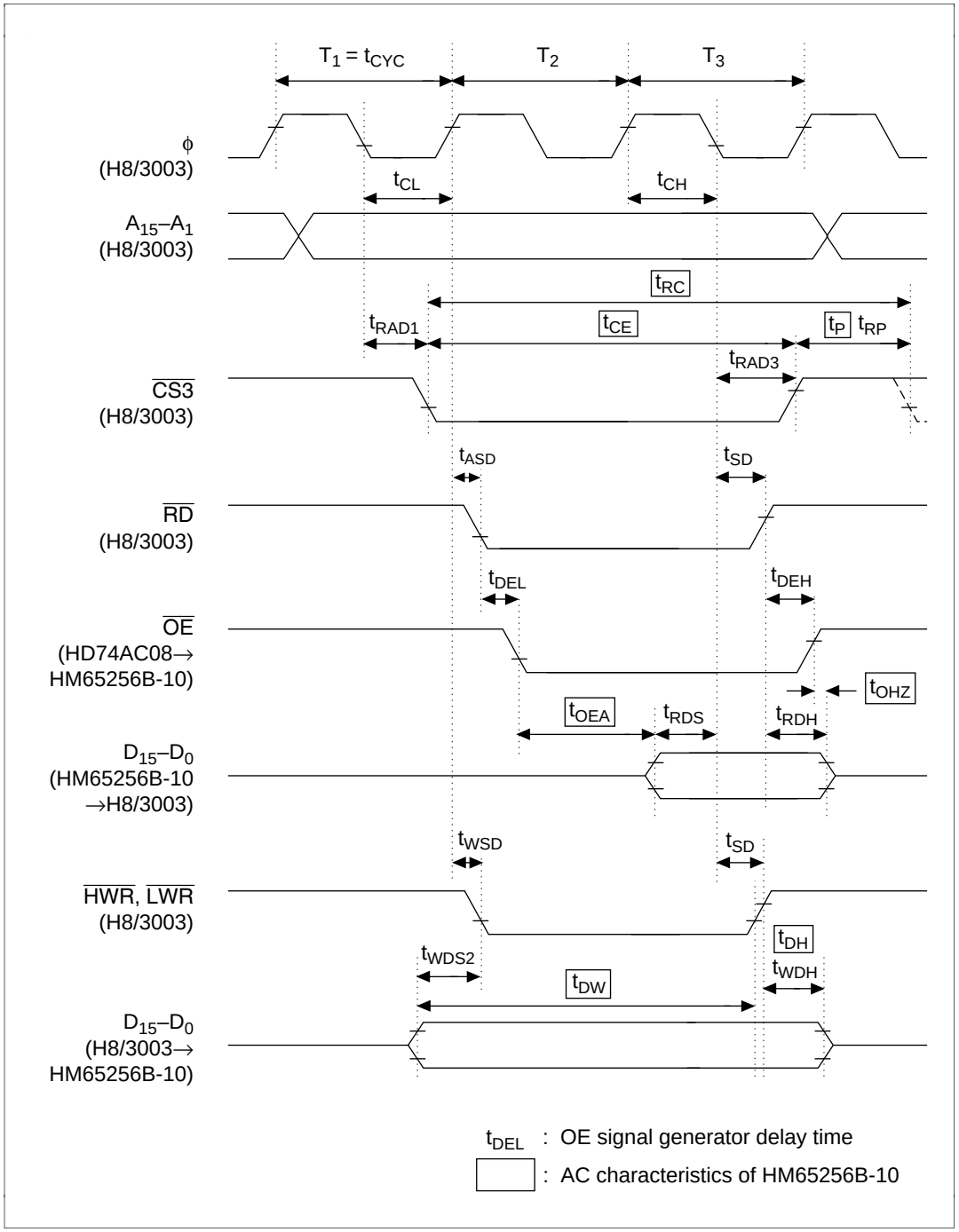


Figure 3.22 Read/Write Timing Chart

3.5.3 Refresh Timing

Figure 3.23 shows the refresh timing. The HM65256B-10 refresh is conducted by the HM65256B-10's auto-refresh function using the H8/3003's refresh controller. The HM65256B-10 refresh runs at 256 cycles/4 ms, therefore the refresh cycle is 4 ms/256 = 15.625 µs.

To satisfy this refresh cycle, the refresh controller drives the REFS signal low every 15.5 µs (12 MHz/2 × 93).

Check that the following conditions are satisfied for timing design during refresh:

- HM65256B-10:
  - — t_{FP} (refresh pre-charge time)

$$t_{FP} = t_{CL}\,(\min) + T_1 + t_{RAD2}\,(\min) + t_{DEL}\,(\min) - t_{RAD3}\,(\max) - t_{DEH}\,(\max)$$
$$= 30 + 83.3 + 0 + 2.5 - 30 - 6.6$$
$$= 79.2\ \text{ns} \geq 30\ \text{ns}\ (\text{HM65256B-10}\ t_{FP})$$

  - — t_{FAP} (refresh command pulse width).

$$t_{FAP} = T_1 + t_{CH}\,(\min) + t_{RAD3}\,(\min) + t_{DEH}\,(\min) - t_{RAD2}\,(\max) - t_{DEL}\,(\max)$$
$$= 83.3 + 30 + 0 + 3 - 30 - 6.3$$
$$= 80\ \text{ns} \geq 80\ \text{ns}\ (\text{HM65256B-10}\ t_{FAP})$$

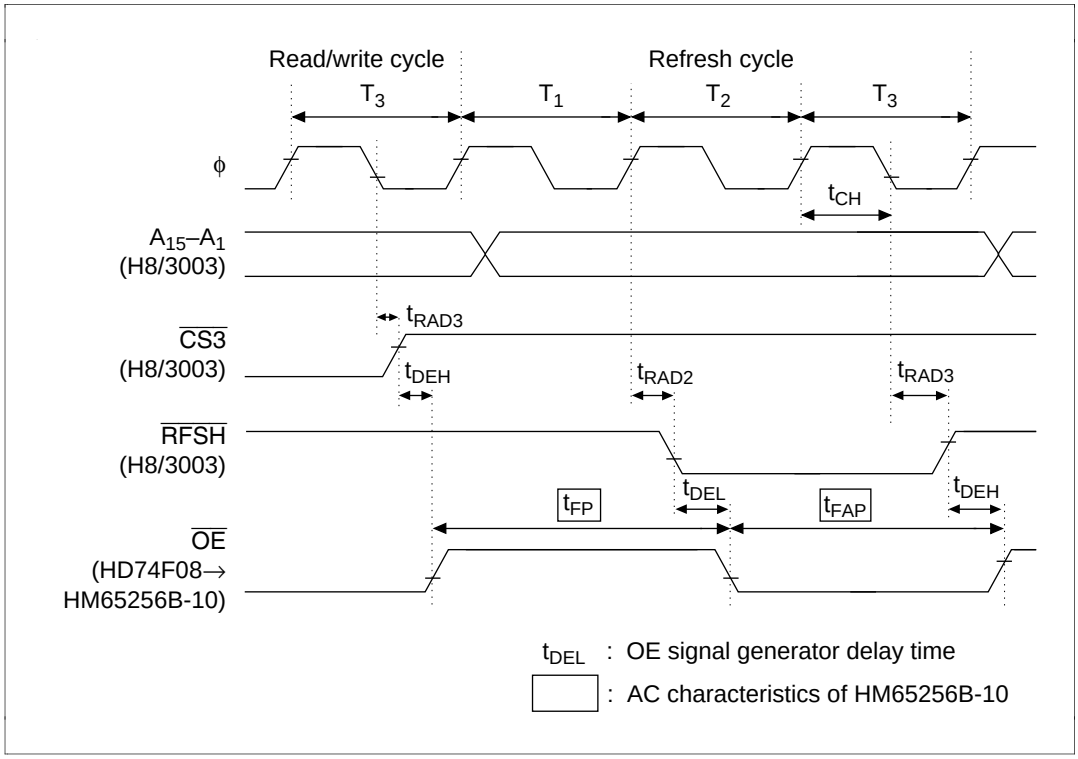


Figure 3.23 Refresh Timing

3.5.4 Circuit Diagram

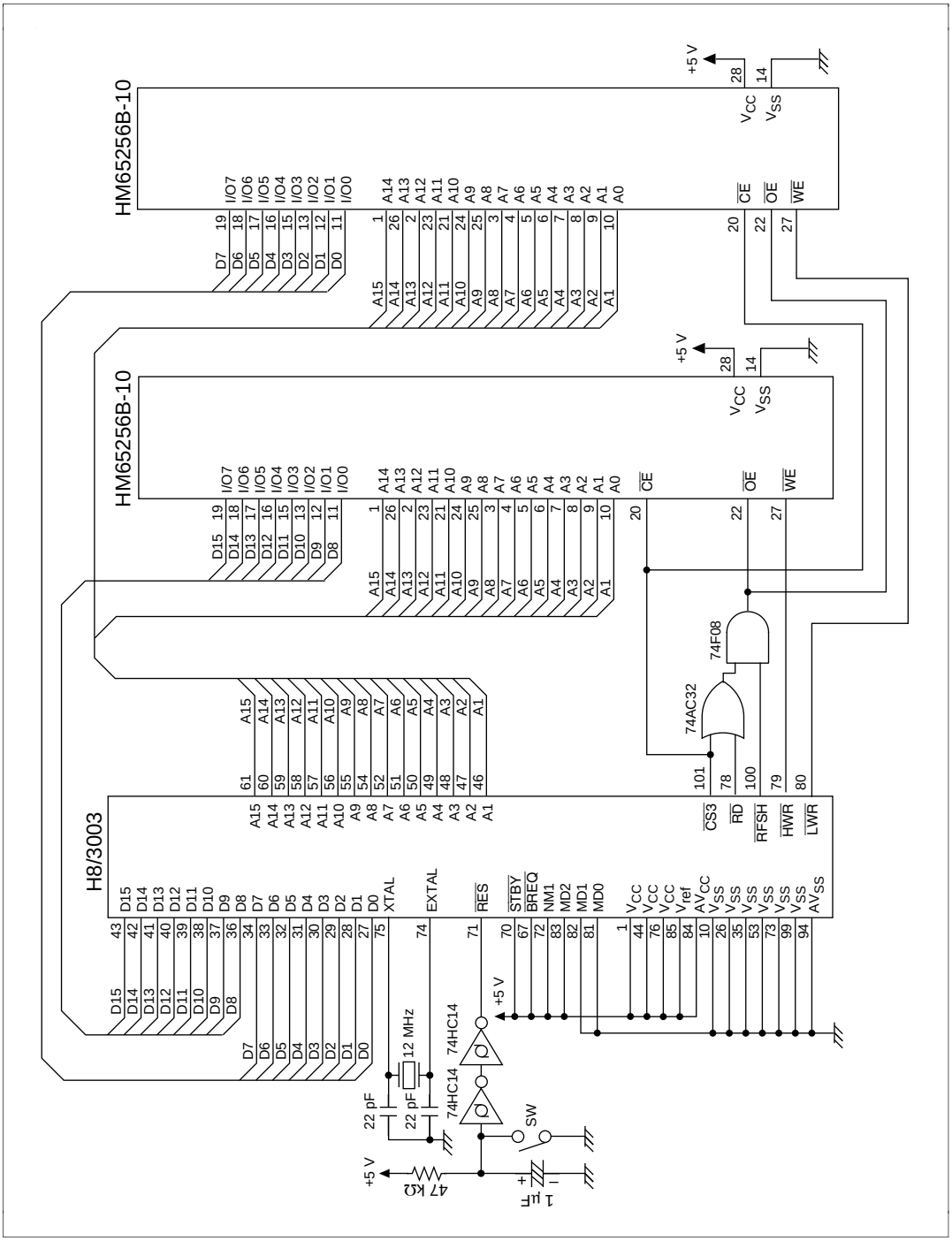


Figure 3.24 Circuit Diagram

3.6 DRAM (HM514260-7) Interface

MCU: H8/3003

Function: Mode 4 (16-bit data bus, 16-Mbyte address space)

3.6.1 Specifications

The H8/3003 mode 4 (16-bit data bus, 16-Mbyte address space) interface with a DRAM (HM514260-7) is shown in figure 3.25.

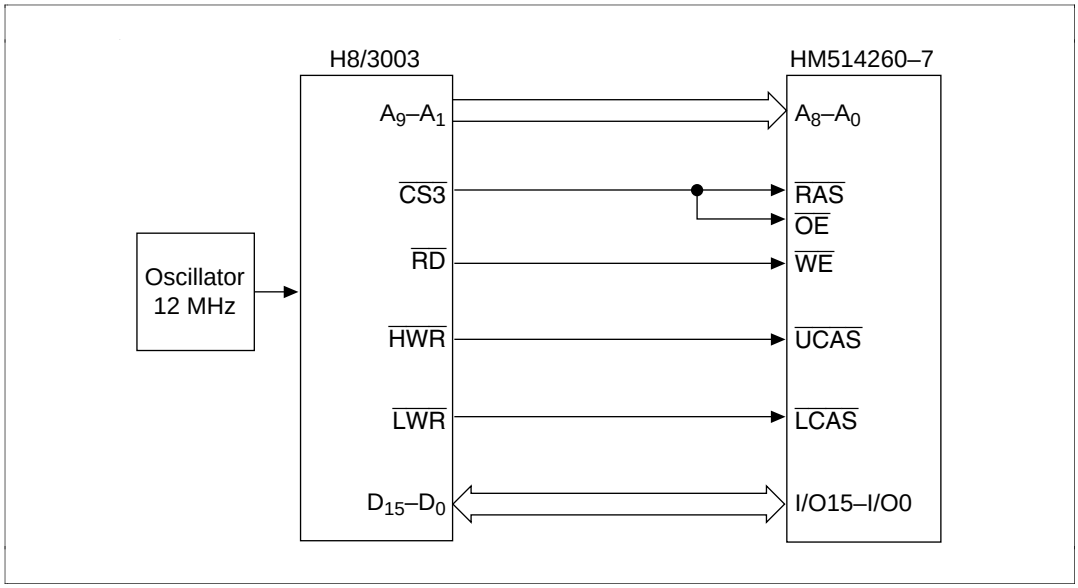


Figure 3.25 Block Diagram of H8/3003 and HM514260-7 Interface

As shown in figure 3.26, area 3 (H'600000-H'7FFFFF) of the 16-Mbyte address space is allotted. The area 3 bus controller settings are as follows:

- Data bus width: 16 bit bus
- Number of states: 3 states
- Wait mode: Pin wait mode 0
- Refresh controller: 2CAS method, 4-Mbit DRAM

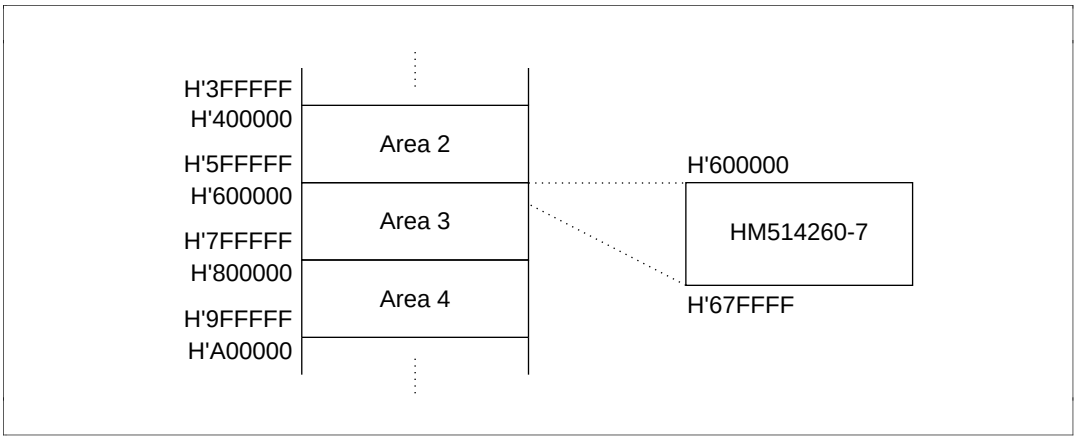


Figure 3.26 Memory Map

3.6.2 Data Read/Write

Figure 3.27 shows the read/write timing chart. When directly connecting the H8/3003 and HM514260-7, check that the following are satisfied:

- H8/3003:
  - t_{CAC} (CAS access time)
  - t_{AA} (address access time)
  - t_{RAC} (RAS access time)
  - t_{RDH} (read data hold time)
- HM514260-7:
  - t_{DS} (data input setup time)
  - t_{DH} (data input hold time)
  - t_{RC} (random read/write cycle time)
  - t_{RP} (RAS pre-charge time)

Since the DRAM uses an address multiplex system, confirm that the following conditions are satisfied:

- HM514260-7:
  - t_{ASR} (row address setup time)
  - t_{RAH} (row address hold time)
  - t_{ASC} (column address setup time)
  - t_{CAH} (column address hold time)

Figure 3.27 shows the timing as follows:

- H8/3003:
  - t_{CAC}, t_{AA}, t_{RAC}, and t_{RDH}

    $t_{CAC} = t_{CAC\ (max)}$
    $= 20\ ns \leq 40\ ns$ (H8/3003 t_{CAC})

    $t_{AA} = t_{AA\ (max)}$
    $= 35\ ns \leq 55\ ns$ (H8/3003 t_{AA})

    $t_{RAC} = t_{RAC\ (max)}$
    $= 70\ ns \leq 120\ ns$ (H8/3003 t_{RAC})

    $t_{RDH} = t_{OFF1\ (min)}$
    $= 0\ ns \geq 0\ ns$ (H8/3003 t_{RDH})

- HM514260-7:
  - t_{DS}, t_{DH}, t_{RC}, and t_{RP}

    $t_{DS} = t_{WDS3\ (min)}$
    $= 40\ ns \geq 0\ ns$ (HM514260-7 t_{DS})

    $t_{DH} = t_{CL\ (min)} + t_{CH\ (min)} + t_{SD\ (min)} + t_{WDH\ (min)} - t_{ASD\ (max)}$
    $= 30 + 30 + 0 + 20 - 30$
    $= 50\ ns \geq 15\ ns$ (HM514260-7 t_{DH})

    $t_{RC} = t_{CL\ (min)} + T2 + T3 + t_{CH\ (min)} + t_{ASD\ (min)} - t_{ASD\ (max)}$
    $= 30 + 83.3 + 83.3 + 30 + 0 - 30$
    $= 196.6\ ns \geq 130\ ns$ (HM514260-7 t_{RC})

    $t_{RP} = t_{RP\ (min)}$
    $= 55\ ns \geq 50\ ns$ (HM514260-7 t_{DS})

- HM514260-7:
  - t_{ASR}, t_{RAH}, t_{ASC}, and t_{CAH}

    $t_{ASR} = t_{AS1\ (min)}$
    $= 10\ ns \geq 0\ ns$ (HM514260-7 t_{ASR})

    $t_{RAH} = t_{RAH\ (min)}$
    $= 15\ ns \geq 10\ ns$ (HM514260-7 t_{RAH})

    $t_{ASC} = t_{AS1\ (min)}$
    $= 10\ ns \geq 10\ ns$ (HM514260-7 t_{ASC})

    $t_{CAH} = T2 + T3 + t_{AD\ (min)} - t_{AD\ (max)}$
    $= 83.3 + 83.3 + 0 - 35$
    $= 131.6\ ns \geq 15\ ns$ (HM514260-7 t_{CAH})

- HM514260-7:
  - t_{RAS}, t_{CAS}, t_{CSH}, and t_{RSH}

    $t_{RAS} = t_{CL\ (min)} + T2 + t_{CH\ (min)} + t_{RAD3\ (min)} - t_{ASD\ (max)}$
    $= 30 + 83.3 + 30 + 0 - 35$
    $= 108.3\ ns \geq 70\ ns$ (HM514260-7 t_{RAS})

    $t_{CAS} = t_{CL\ (min)} + t_{CH\ (min)} + t_{SD\ (min)} - t_{ASD\ (max)}$
    $= 30 + 30 + 0 - 35$
    $= 25\ ns \geq 20\ ns$ (HM514260-7 t_{CAS})

    $t_{CSH} = t_{CL\ (min)} + T2 + t_{CH\ (min)} + t_{SD\ (min)} - t_{ASD\ (max)}$
    $= 30 + 83.3 + 30 + 0 - 35$
    $= 108.3\ ns \geq 70\ ns$ (HM514260-7 t_{CSH})

    $t_{RSH} = t_{CL\ (min)} + t_{CH\ (min)} + t_{RAD3\ (min)} - t_{ASD\ (max)}$
    $= 30 + 30 + 0 - 35$
    $= 25\ ns \geq 20\ ns$ (HM514260-7 t_{RSH})

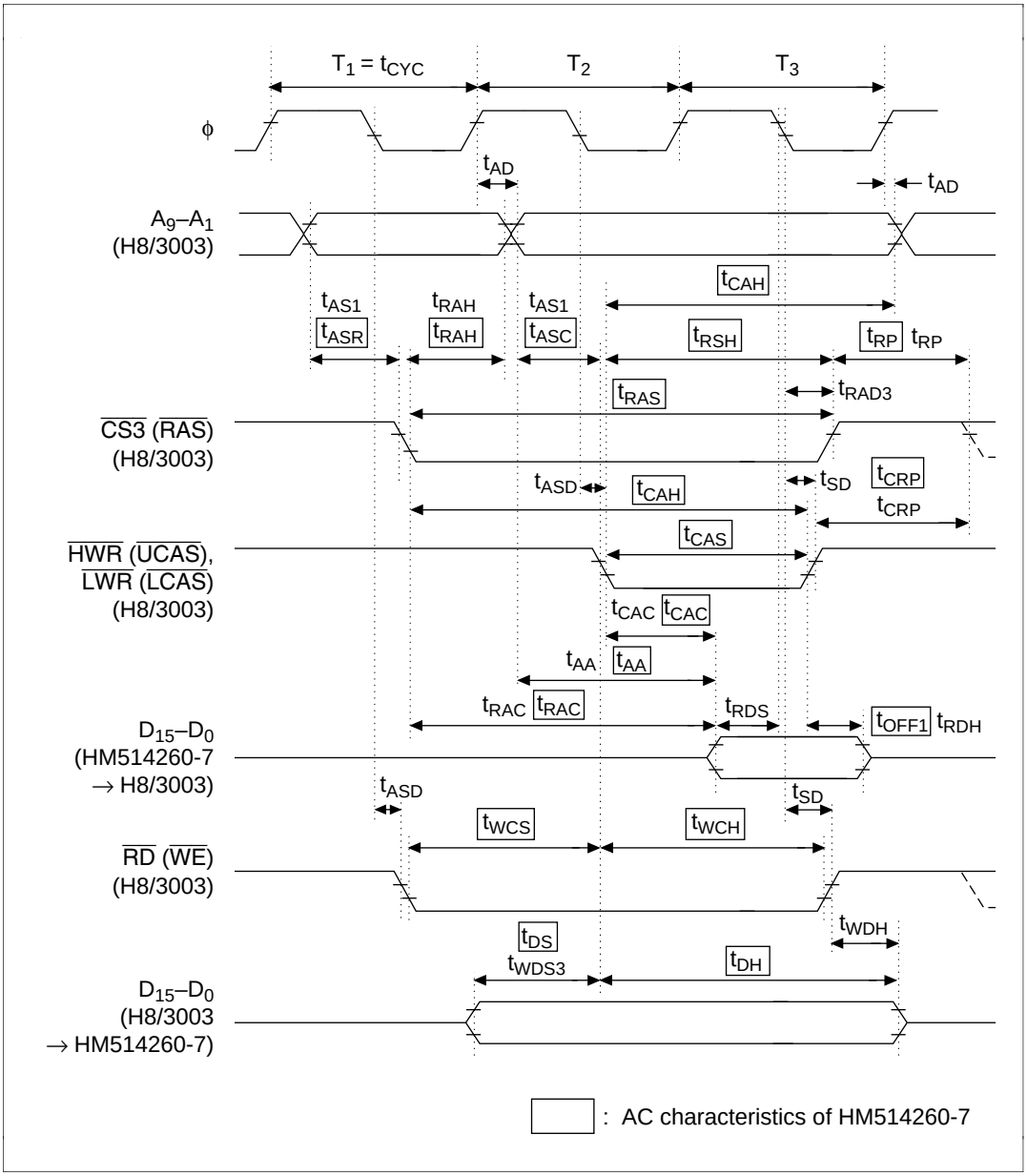


Figure 3.27 Read/Write Timing

3.6.3 Refresh

Figure 3.28 shows the CAS before RAS timing chart. When directly connecting the H8/3003 to the HM514260-7, check that the following are satisfied.

- HM514260-7:
  - t_{CSR} (CAS setup time)
  - t_{CHR} (CAS hold time)
  - t_{CPN} (CAS pre-charge time)
  - t_{RC} (random read/write cycle)
  - t_{RAS} (RAS pulse width)

Figure 3.28 shows the timing as follows:

- HM514260-7:
  - t_{CSR}, t_{CHR}, t_{CPN}, t_{RC}, and t_{RAS}

$$t_{CSR} = t_{CSR\,(min)}$$
$$= 15\text{ ns} \geq 10\text{ ns (HM514260-7 } t_{CSR})$$

$$t_{CHR} = T2 + t_{CH\,(min)} + t_{SD\,(min)} - t_{RAD2\,(max)}$$
$$= 83.3 + 30 + 0 - 30$$
$$= 83.3\text{ ns} \geq 10\text{ ns (HM514260-7 } t_{CHR})$$

$$t_{CPN} = t_{CL\,(min)} + T2 + t_{CH\,(min)} + t_{ASD\,(min)} - t_{SD\,(min)}$$
$$= 30 + 83.3 + 30 + 0 - 30$$
$$= 113.3\text{ ns} \geq 10\text{ ns (HM514260-7 } t_{CPN})$$

$$t_{RC} = T2 + T3 + t_{CH\,(min)} + t_{RAD1\,(min)} - t_{RAD2\,(max)}$$
$$= 83.3 + 83.3 + 30 + 0 - 30$$
$$= 166.6\text{ ns} \geq 130\text{ ns (HM514260-7 } t_{RC})$$

$$t_{RAS} = T2 + t_{CH\,(min)} + t_{RAD3\,(min)} - t_{RAD2\,(max)}$$
$$= 83.3 + 30 + 0 - 30$$
$$= 83.3\text{ ns} \geq 70\text{ ns (HM514260-7 } t_{RAS})$$

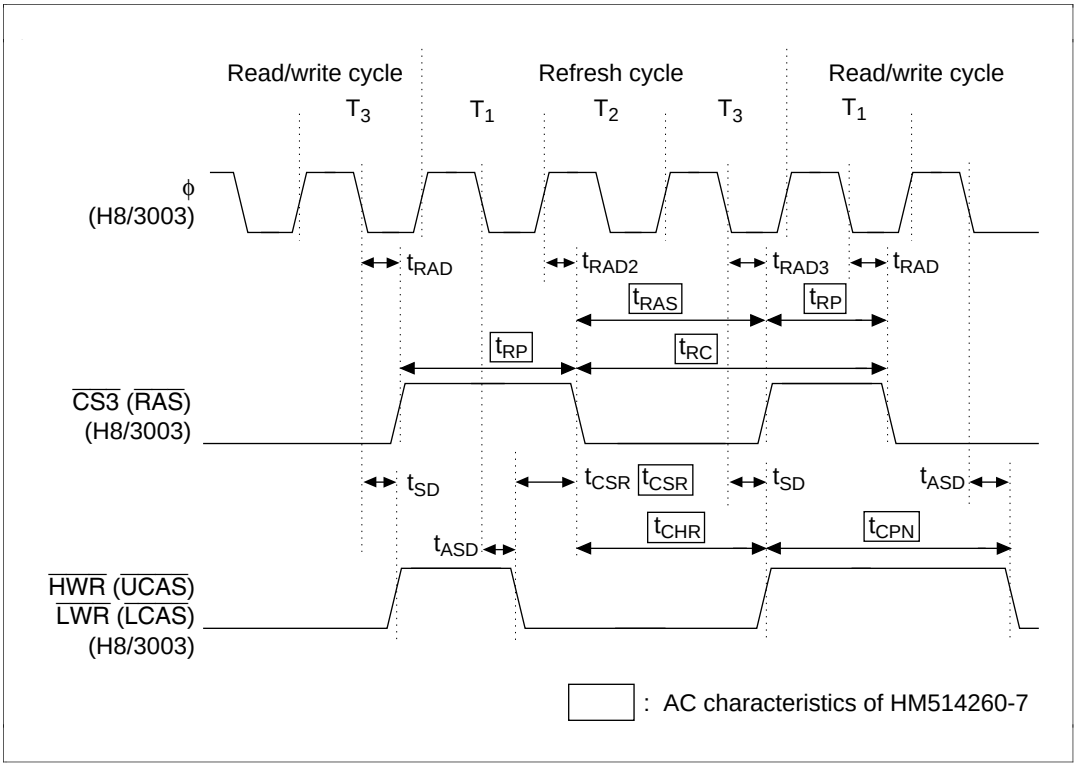


Figure 3.28 Refresh Timing

3.6.4 Circuit Diagram

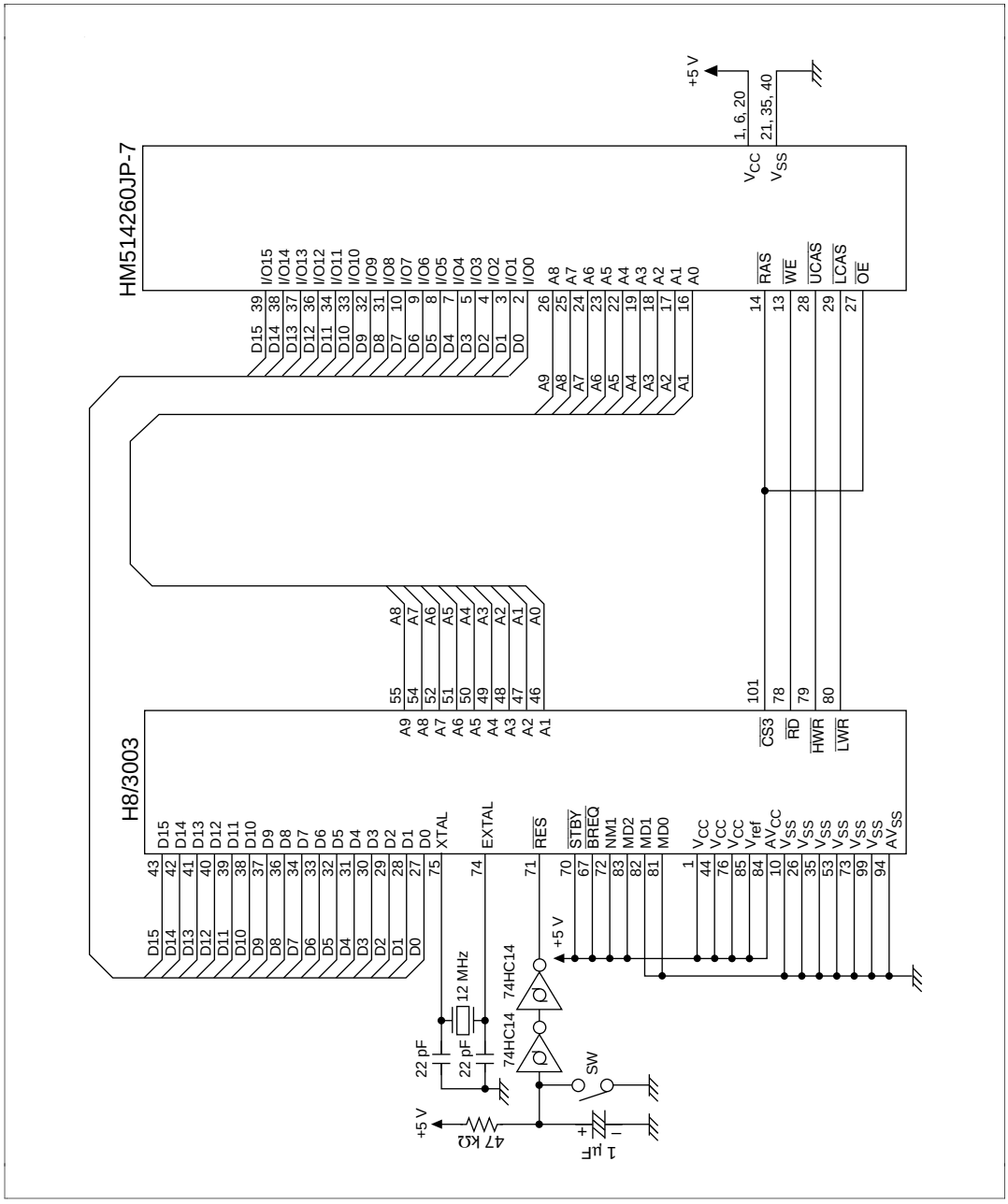


Figure 3.29 Circuit Diagram

3.7 UPP (HD63143) Interface

MCU: H8/3003

Function: Mode 4 (16-bit data bus, 16-Mbyte address space)

3.7.1 Specifications

The H8/3003 mode 4 (16-bit data bus, 16-Mbyte address space) interface with the UPP (HD63143) is shown in figure 3.30.

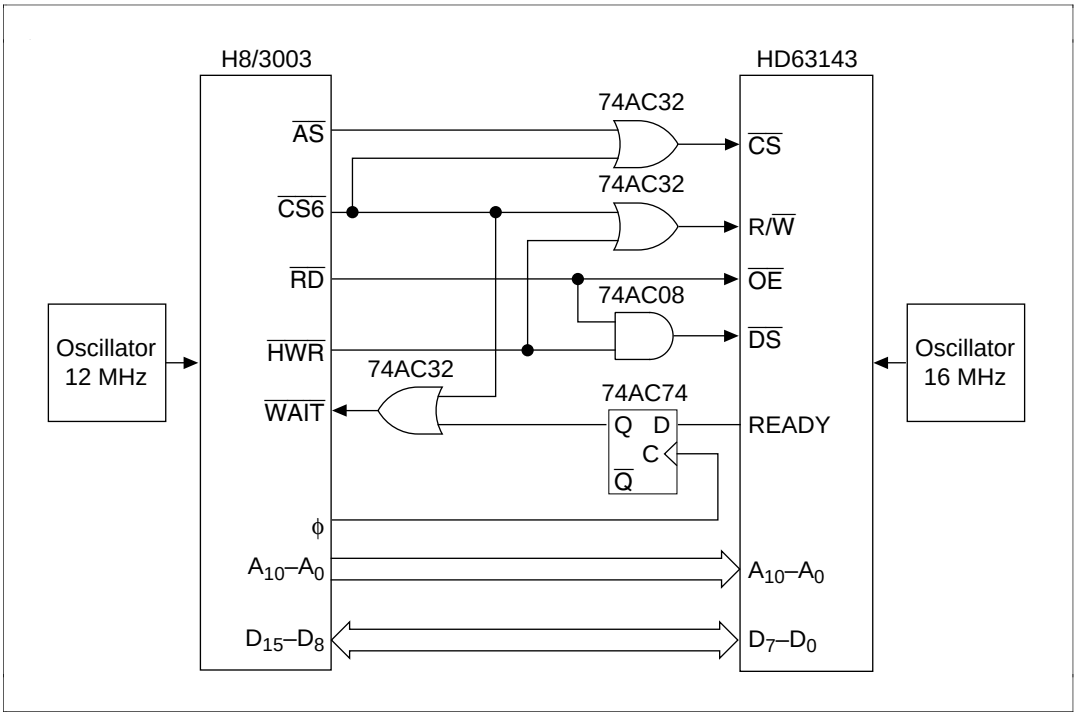


Figure 3.30 Block Diagram of H8/3003 and HD63143 Interface

As shown in figure 3.31, area 6 (H'C00000–H'DFFFFF) of the 16-Mbyte memory space is allotted. The area 6 bus controller settings are as follows:

- Data bus width: 8 bit bus
- Number of states: 3 states
- Wait mode: pin wait mode 1
- Number of waits: 1 state

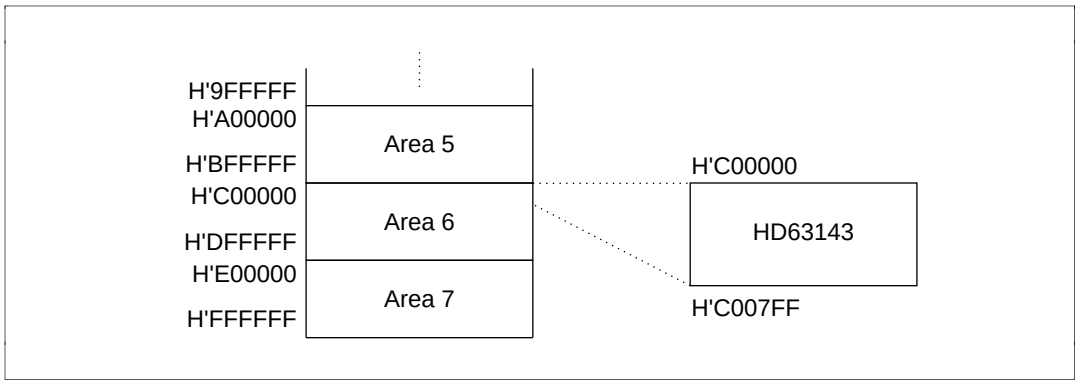


Figure 3.31 Memory Map

3.7.2 Wait Signal Generator

Figure 3.32 shows the wait signal generator and figure 3.33 the wait timing chart. When the H8/3003 and HD63143 are directly connected, read/write from the H8/3003 is not conducted correctly while the HD63143 is performing other processes. Therefore, a wait cycle is inserted in the read/write cycle until the HD63143's READY signal rising edge, effecting a wait period to the end of HD63143 processing.

The READY signal's level is detected and a WAIT signal generated.

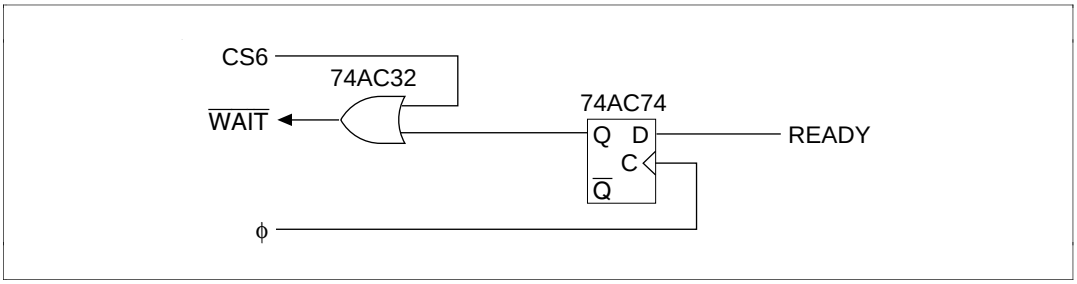


Figure 3.32 Wait Signal Generator Circuit

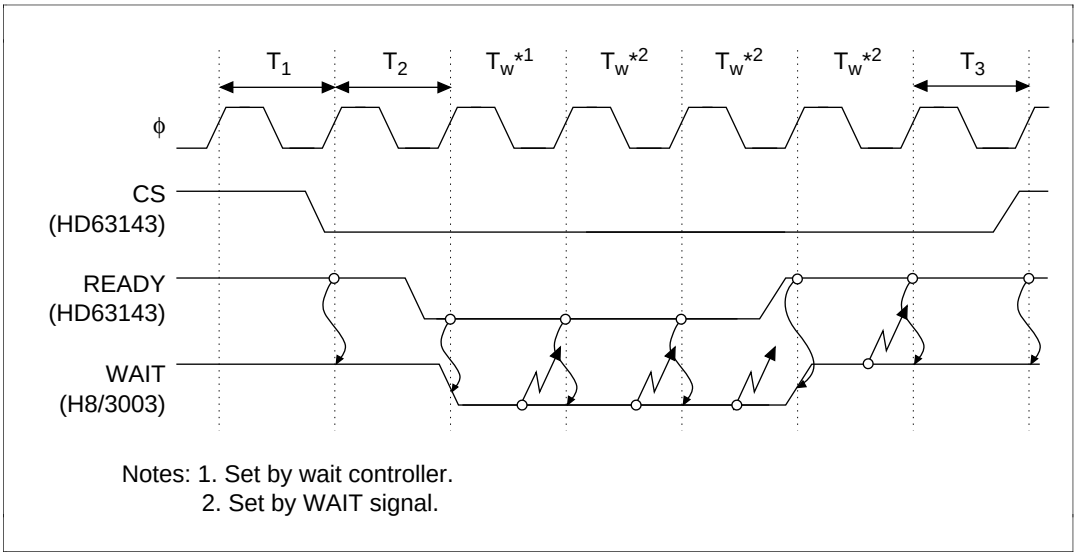


Figure 3.33 Wait Timing Chart

3.7.3 Data Read/Write

Figure 3.34 shows the read/write timing chart and figure 3.35 shows read/write timing for other than RAM. When connecting the H8/3003 and HD63143, check that the following are satisfied:

- H8/3003:
  - — t_{RDS} (read data setup time)
  - — t_{RDH} (read date hold time)
- HD63143:
  - — t_{WDS} (write data setup time)
  - — t_{WDH} (write data hold time)
  - — t_{WDD} (write data delay time).

During read cycles other than RAM, the HD63143's data output timing depends on the READY signal falling edge. READY signal falling edge timing is important when computing t_{RDS}. However, READY signal timing differs greatly depending on the operating state of HD63143. Because of this, t_{RDS} calculation is conducted using the time (α) from the READY signal falling edge to the rising edge of next clock.

Figures 3.34 and 3.35, show the timing as follows:

- H8/3003:
  - — t_{RDS} and t_{RDH} during RAM read cycle

$$t_{RDS} = t_{CL}\ (\text{min}) + T_2 + T_W + t_{CH}\ (\text{min}) - t_{ASD}\ (\text{max}) - t_{ORDD}\ (\text{max})$$
$$= 30 + 83.3 + 30 - 35 - 80$$
$$= 111.6\ \text{ns} \geq 20\ \text{ns}\ (\text{H8/3003}\ t_{RDS})$$

$$t_{RDH} = t_{ORDH}\ (\text{min})$$
$$= 10\ \text{ns} \geq 0\ \text{ns}\ (\text{H8/3003}\ t_{RDH})$$

  - — t_{RDS} and t_{RDH} at times other than RAM read cycle

$$t_{RDS} = \alpha\ (\text{min}) + T_W + t_{CH}\ (\text{min}) - t_{RRDD}\ (\text{max})$$
$$= 0 + 83.3 + 30 - 60$$
$$= 53.3\ \text{ns} \geq 20\ \text{ns}\ (\text{H8/3003}\ t_{RDS})$$

$$t_{RDH} = t_{ORDH}\ (\text{min})$$
$$= 10\ \text{ns} \geq 0\ \text{ns}\ (\ t_{RDH})$$

- HD63143:
  - — t_{WDS} and t_{WDH}

    $t_{WDS} = T_2 + T_W + t_{CH}$ (min) + t_{SD} (min) – t_{WSD} (max) + t_{WDS2} (min)
    $= 83.3 + 83.3 + 30 + 0 – 35 + 10$
    $= 171.6$ ns ≥ 100 ns (HD63143 t_{WDS})

    $t_{WDH} = t_{WDH}$ (min) – t_{DELH} (max)
    $= 20 – 8.5$
    $= 11.5$ ns ≥ 5 ns (HD63143 t_{WDH})

  - — t_{WDD}

    $t_{WDD} = –t_{DELL}$ (min) – t_{WDS2} (min)
    $= –0 – 10$
    $= –10$ ns ≤ 120 ns (HD63143 t_{WDD})

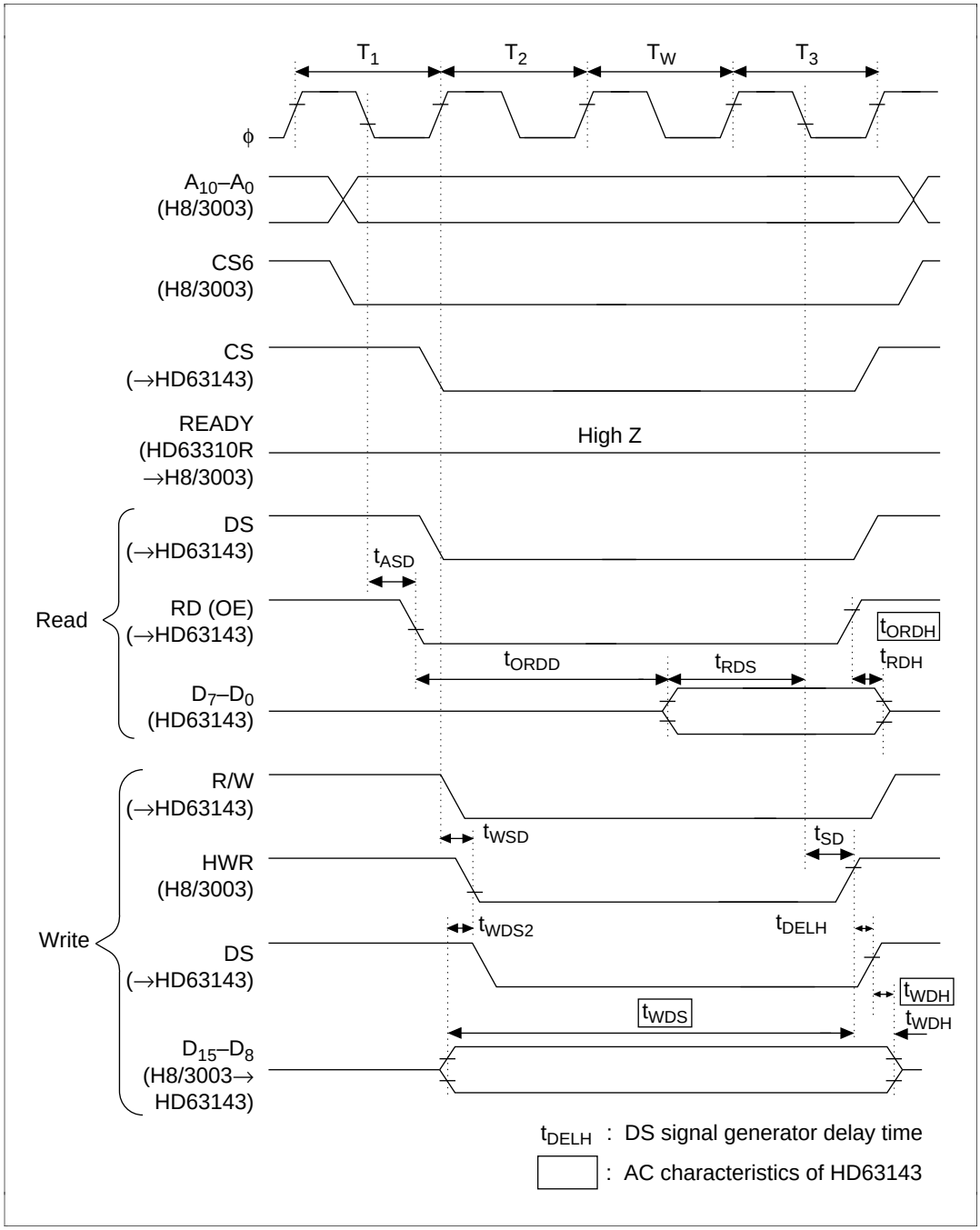


Figure 3.34 Read/Write Timing Chart (RAM)

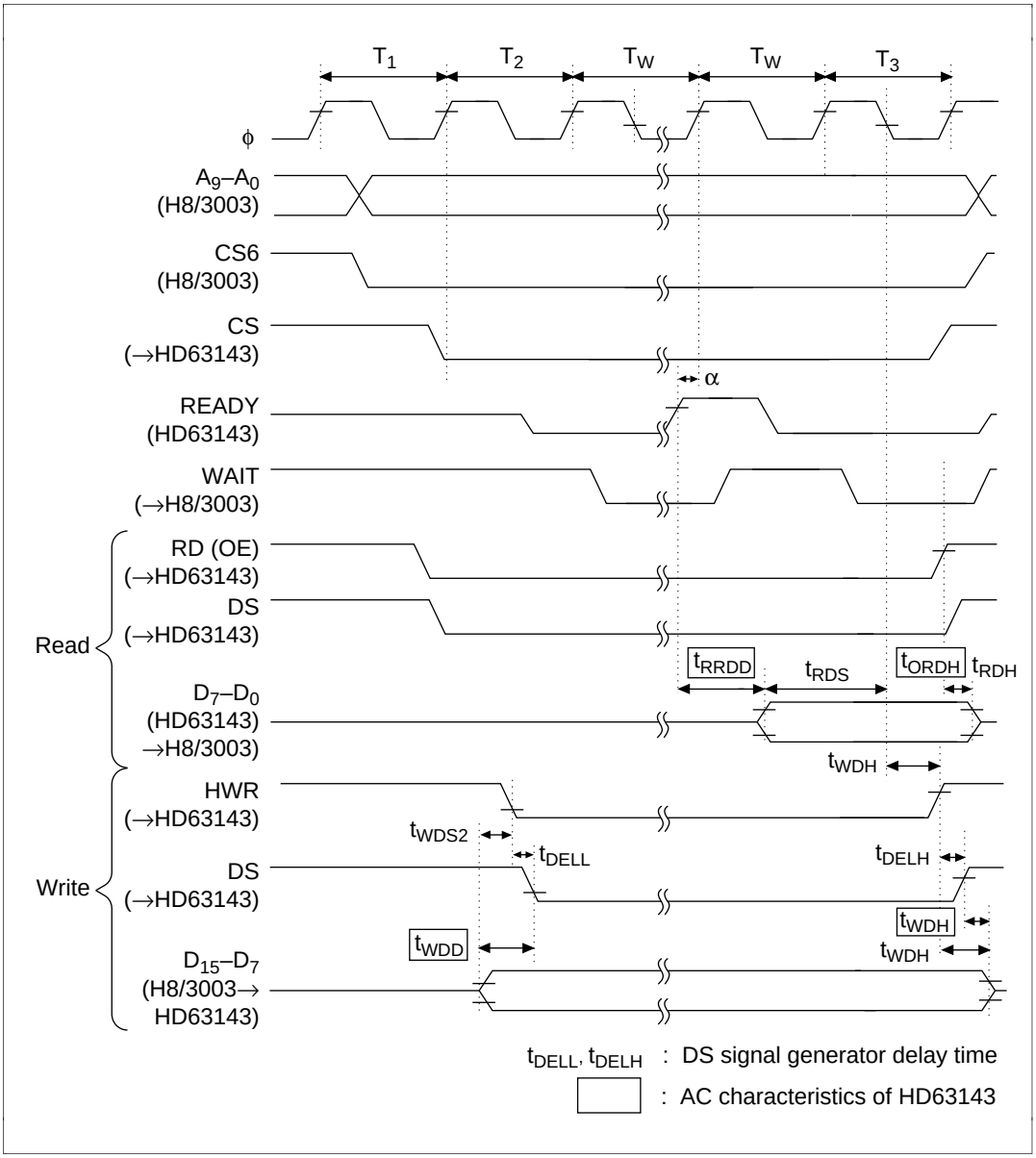


Figure 3.35 Read/Write Timing Chart (non-RAM)

3.7.4 Circuit Diagram

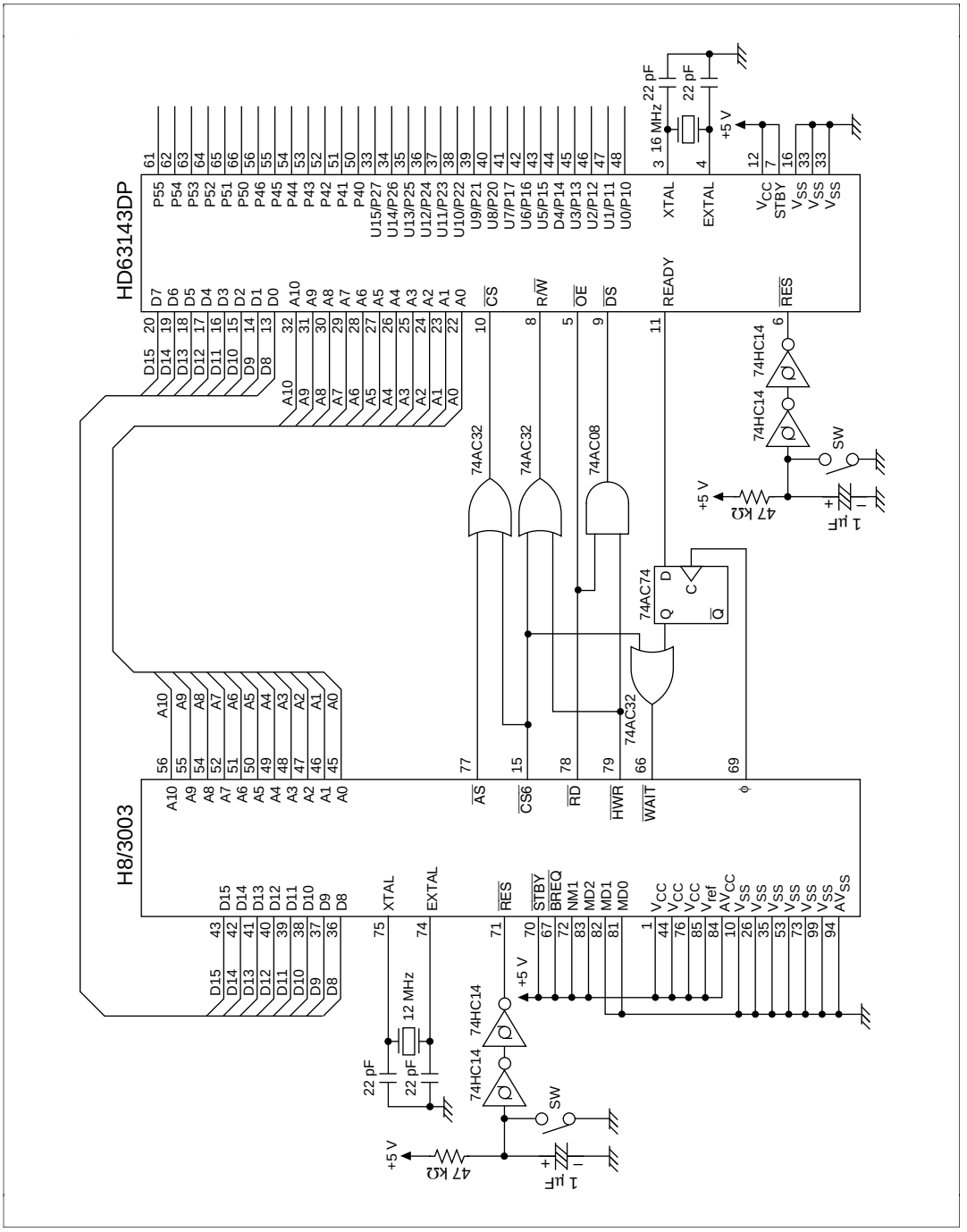


Figure 3.36 Circuit Diagram

3.8 PIO (TMP82C55AP-10) Interface

MCU: H8/3003

Function: Mode 4 (16-bit data bus, 16-Mbyte address space)

3.8.1 Specifications

The H8/3003 mode 4 (16-bit data bus, 16-Mbyte address space) interface with PIO (TMP82C55AP-10) is shown in figure 3.37.

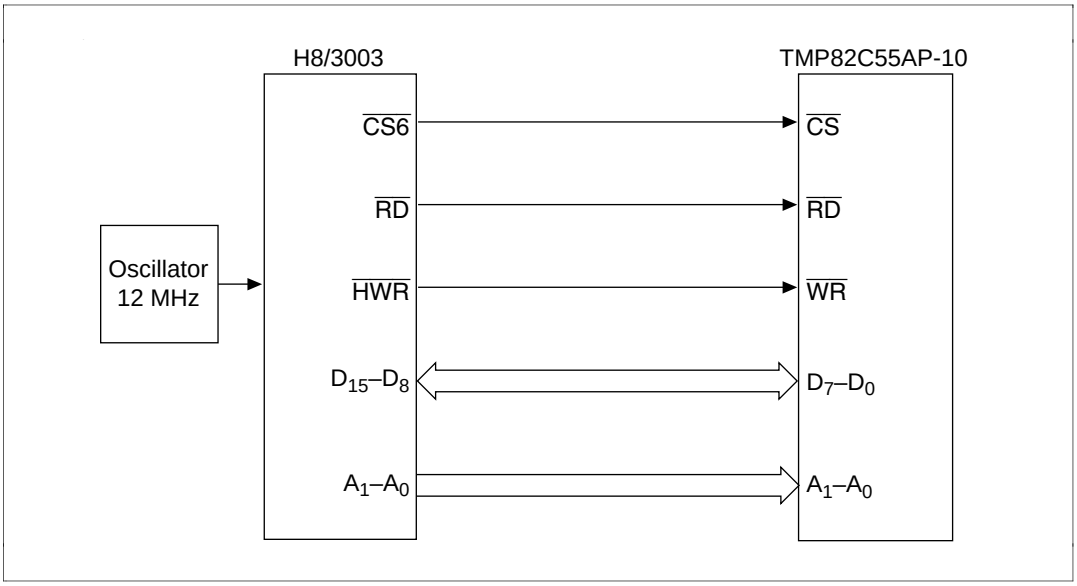


Figure 3.37 Block Diagram of H8/3003 and TMP82C55AP Interface

As shown in figure 3.38, area 6 (H'C00000–H'DFFFFF) of the 16-Mbyte memory space is allotted. The area 6 bus controller settings are as follows:

- Data bus width: 8 bit bus
- Number of states: 3 states
- Wait mode: programmable wait mode
- Number of waits: 1 state

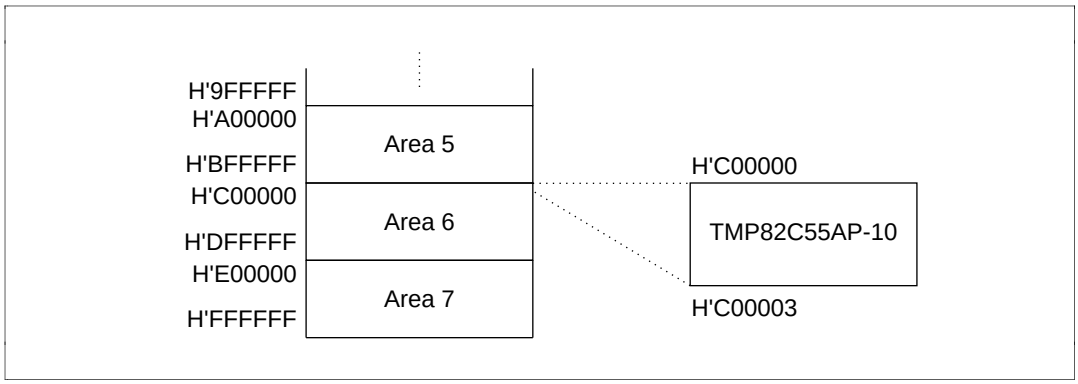


Figure 3.38 Memory Map

3.8.2 Data Read/Write

Figure 3.39 shows the read/write timing chart. When directly connecting the H8/3003 and TMP82C55AP-10, check whether the following timing conditions are satisfied:

- H8/3003:
  - — t_{ACC4} (read data access time)
  - — t_{RDH} (read data hold time)
- TMP82C55AP-10:
  - — t_{DW} (input data setup time)
  - — t_{WD} (input data hold time)
  - — t_{AR} (address setup time during read)
  - — t_{AW} (address setup time during write)

From figure 3.39, the timings are as follows:

- H8/3003:
  - — t_{ACC4} and t_{RDH}

$$t_{ACC4} = t_{RD}\ (max) - T_W$$
$$= 100 - 83.3$$
$$= 16.7\ ns \leq 120\ ns\ (H8/3003\ t_{ACC4})$$

$$t_{RDH} = t_{DF}\ (min)$$
$$= 0\ ns \leq 0\ ns\ (H8/3003\ t_{RDH})$$

- TMP82C55AP-10:
  - — t_{DW} and t_{WD}

$$t_{DW} = T_2 + T_W + t_{CH}\ (min) + t_{SD}\ (min) - t_{WSD}\ (max) + t_{WDS2}\ (min)$$
$$= 83.3 + 83.3 + 30 + 0 - 35 + 10$$
$$= 171.6\ ns \geq 100\ ns\ \ (TMP82C55AP\text{-}10\ t_{DW})$$

$$t_{WD} = t_{WDH}\ (min)$$
$$= 20\ ns \geq 0\ ns\ (TMP82C55AP\text{-}10\ t_{WD})$$

  - — t_{AR} and t_{AW}

$$t_{AR} = t_{AS1}\ (min)$$
$$= 10\ ns \geq 0\ ns\ (TMP82C55AP\text{-}10\ t_{AR})$$

$$t_{AW} = t_{AS2}\ (min)$$
$$= 50\ ns \geq 0\ ns\ (TMP82C55AP\text{-}10\ t_{AW})$$

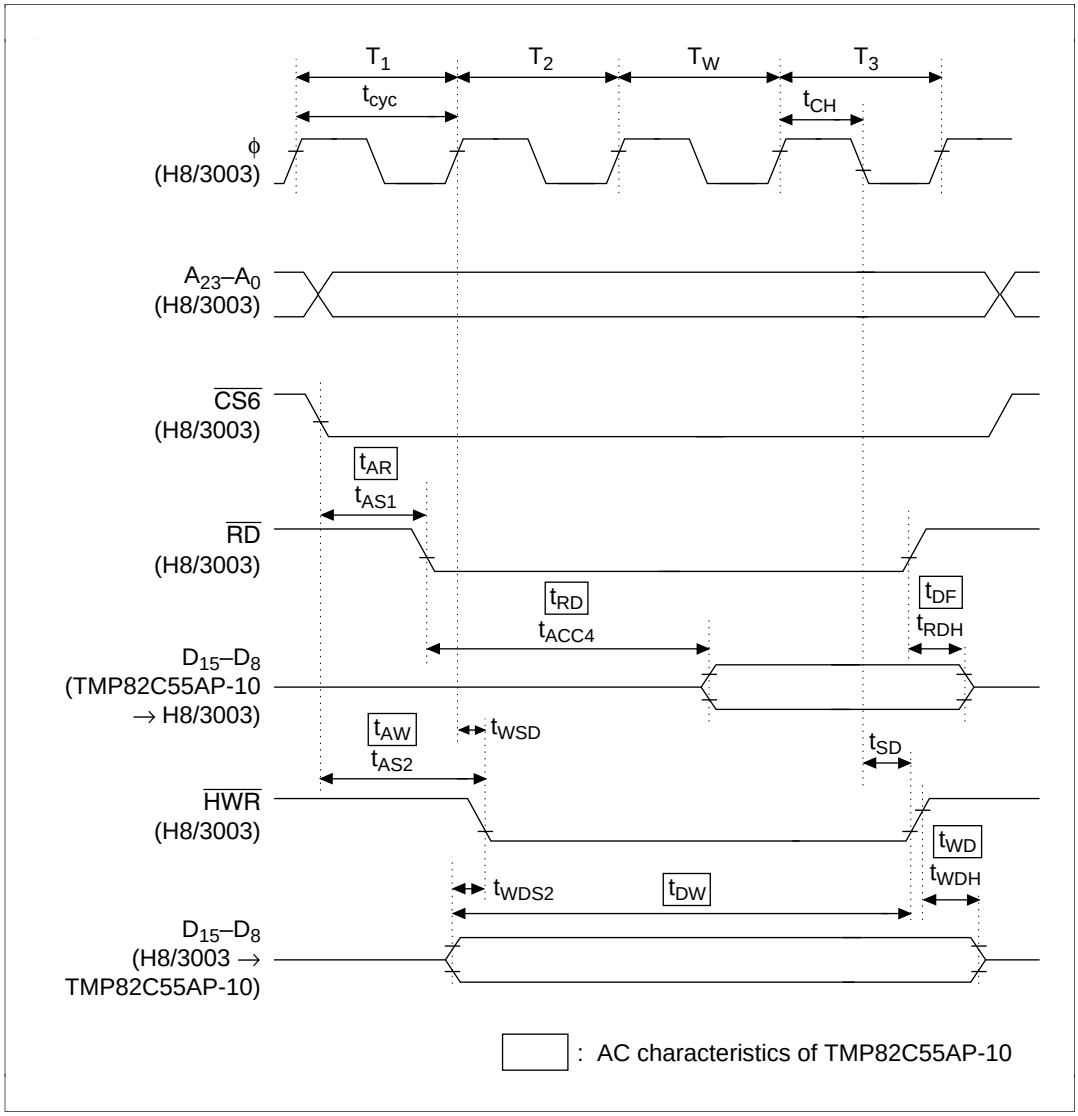


Figure 3.39 Read/Write Timing Chart

3.8.3 Circuit Diagram

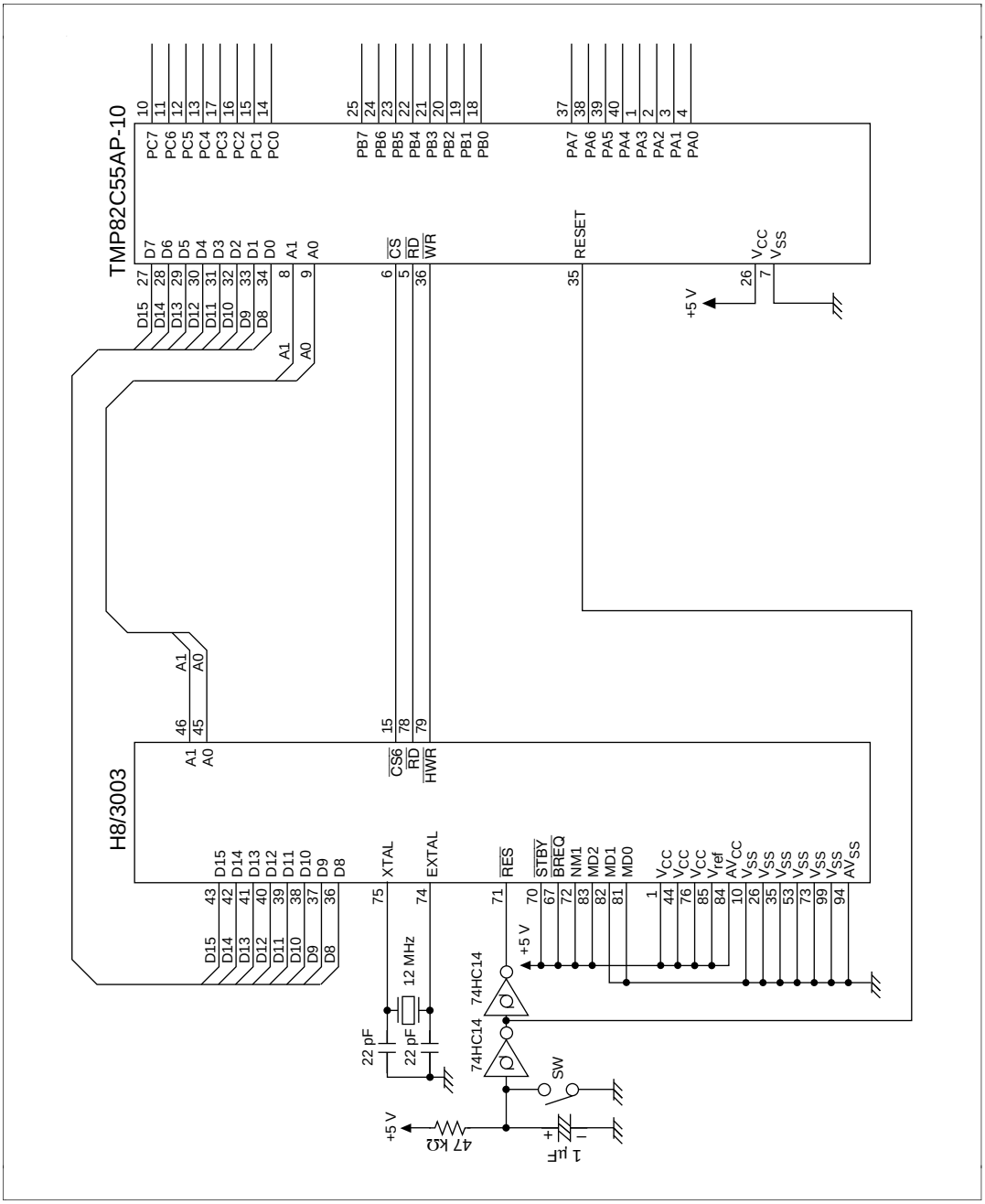


Figure 3.40 Circuit Diagram

3.9 RTC (HD64610) Interface

MCU: H8/3003

Function: Mode 4 (16-bit data bus, 16-Mbyte address space)

3.9.1 Specifications

The H8/3003 mode 4 (16-bit data bus, 16-Mbyte address space) interface with a calendar-clock usage device (HD64610) is shown in figure 3.41.

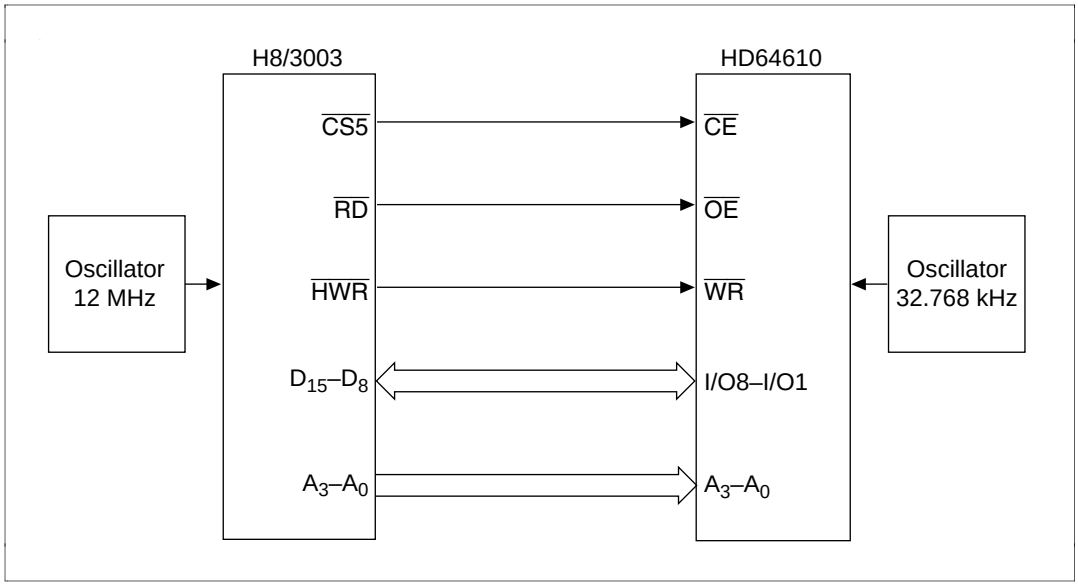


Figure 3.41 Block Diagram of H8/3003 and HD64610 Interface

As shown in figure 3.42, area 5 (H'A00000–H'BFFFFF) of the 16-Mbyte memory space is allotted. The area 5 bus controller settings are as follows:

- Data bus width: 8 bit bus
- Number of states: 3 states
- Wait mode: pin wait mode 0

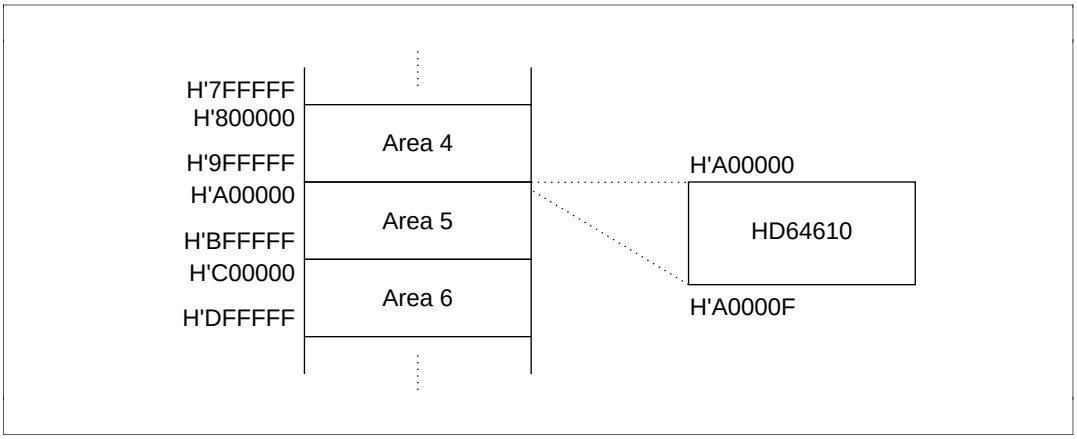


Figure 3.42 Memory Map

3.9.2 Data Read/Write

Figure 3.43 shows the read/write timing chart. When directly connecting the H8/3003 and HD64610, check whether the following timing conditions are satisfied:

- H8/3003:
  - — t_{ACC4} (read data access time)
  - — t_{RDH} (read data hold time)
- HD64610:
  - — t_{DW} (input data set time)
  - — t_{DH} (input data hold time)

Figure 3.43 shows the timing as follows:

- H8/3003:
  - — t_{ACC4} and t_{RDH}

$$t_{ACC4} = t_{OE} \text{ (max)}$$
$$= 45 \text{ ns} \leq 120 \text{ ns (H8/3003 } t_{ACC4})$$

$$t_{RDH} = t_{OHZ} \text{ (min)}$$
$$= 0 \text{ ns} \geq 0 \text{ ns (H8/3003 } t_{RDH})$$

- HD64610:
  - — t_{DW} and t_{DH}

$$t_{DW} = T_2 + t_{CH} \text{ (min)} + t_{SD} \text{ (min)} - t_{WSD} \text{ (max)} + t_{WDS2} \text{ (min)}$$
$$= 83.3 + 30 + 0 - 35 + 10$$
$$= 88.3 \text{ ns} \geq 40 \text{ ns (HD64610 } t_{DW})$$

$$t_{DH} = t_{WDH} \text{ (min)}$$
$$= 20 \text{ ns} \geq 0 \text{ ns (HD64610 } t_{DH})$$

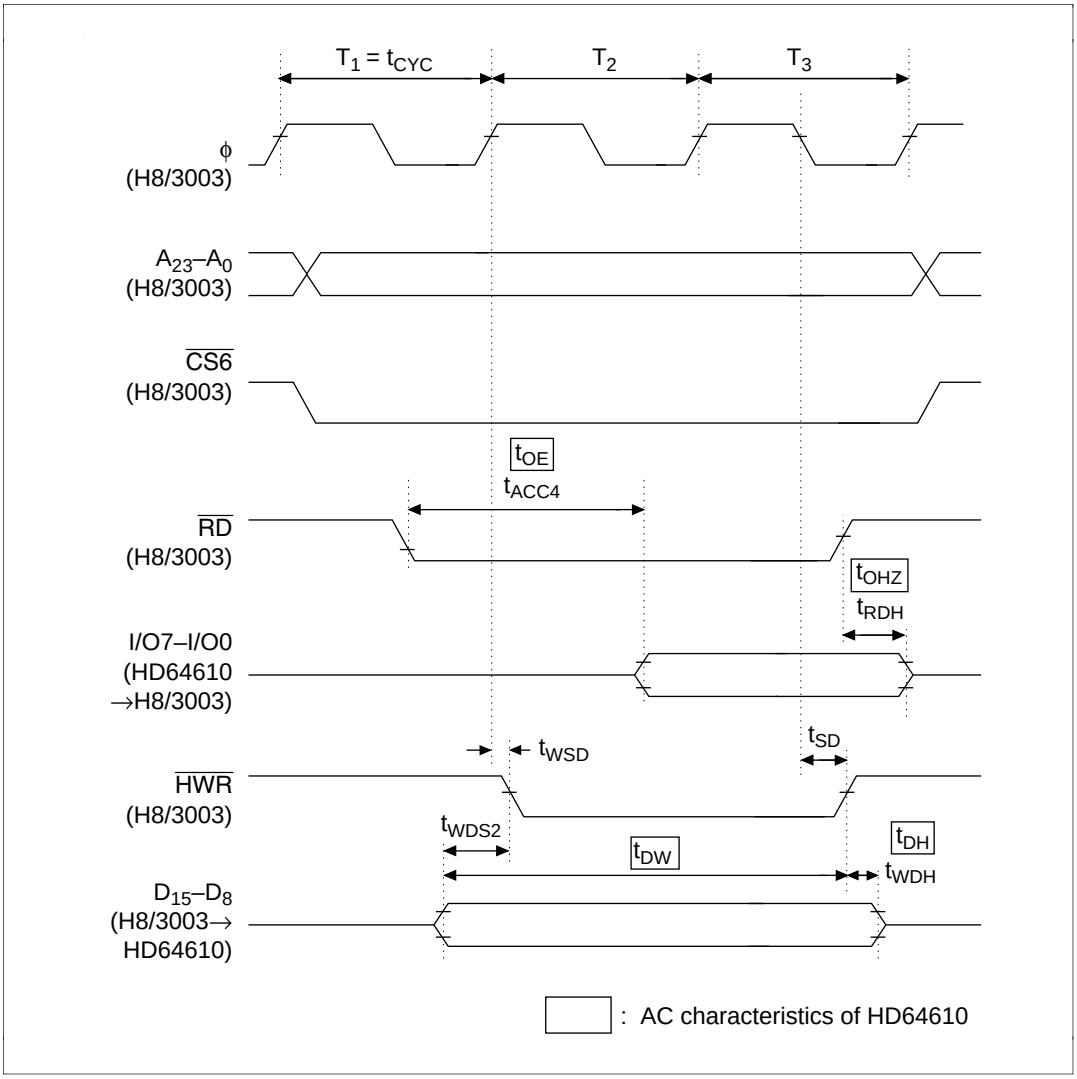


Figure 3.43 Read/Write Timing Chart

3.9.3 Circuit Diagram

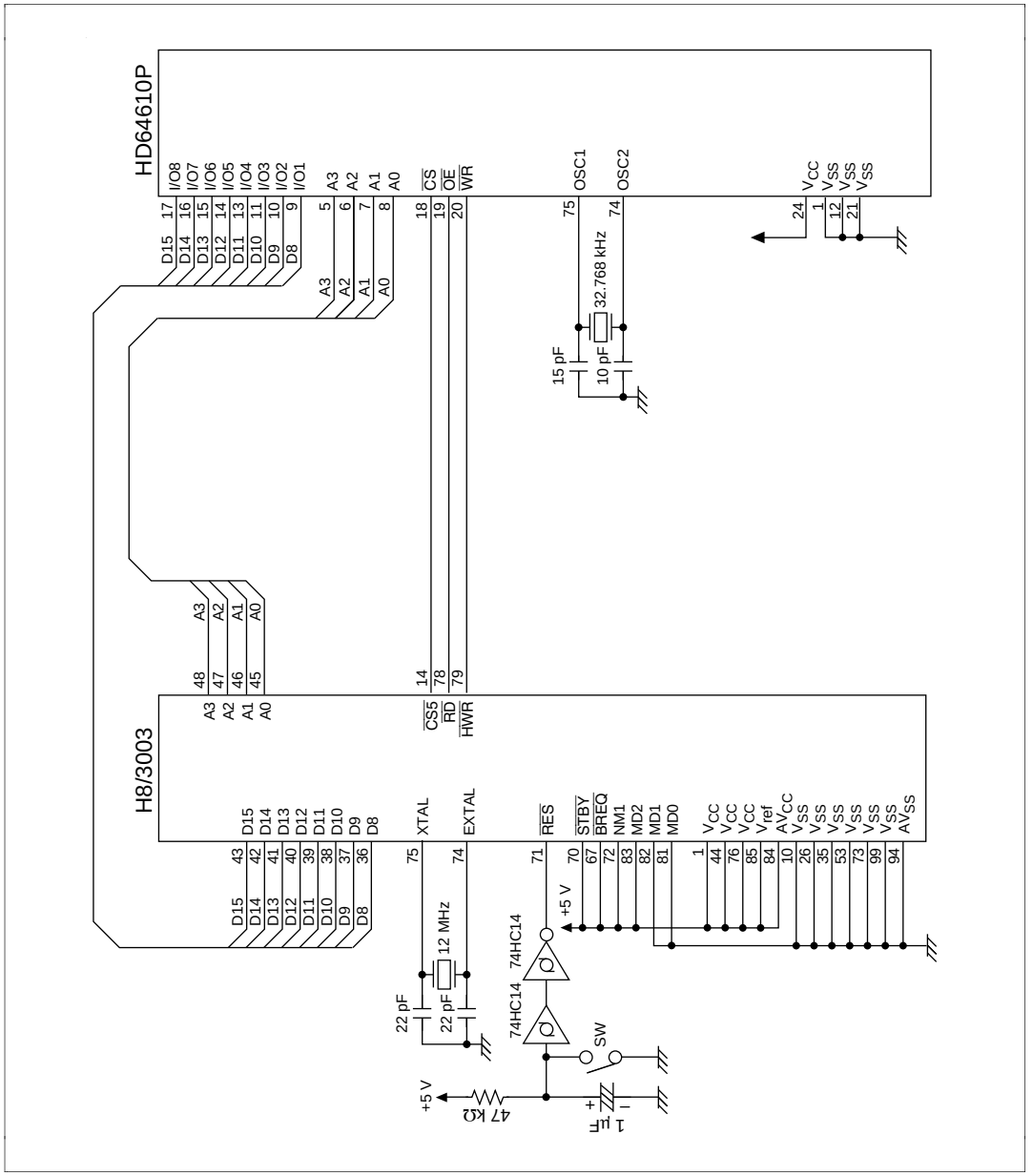


Figure 3.44 Circuit Diagram

3.10 LCD (LM032L) Interface

MCU: H8/3003

Function: Mode 4 (16-bit data bus, 16-Mbyte address space)

3.10.1 Specifications

The H8/3003 mode 4 (16-bit data bus, 16-Mbyte address space) interface with LCD (LM032L) is shown in figure 3.45.

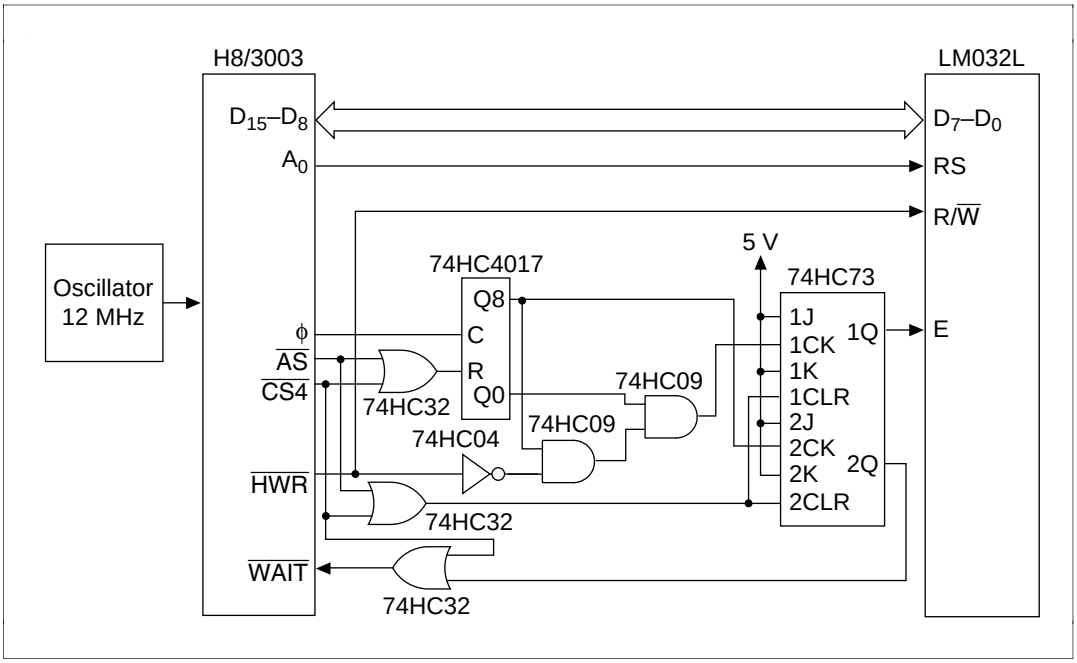


Figure 3.45 Block Diagram of H8/3003 and LM032L Interface

As shown in figure 3.46, area 4 (H'800000–H'9FFFFF) of the 16-Mbyte memory space is allotted. The area 4 bus controller settings are as follows:

- Data bus width: 8 bit bus
- Number of states: 3 states
- Wait mode: pin wait mode 1
- Number of waits: 2 states

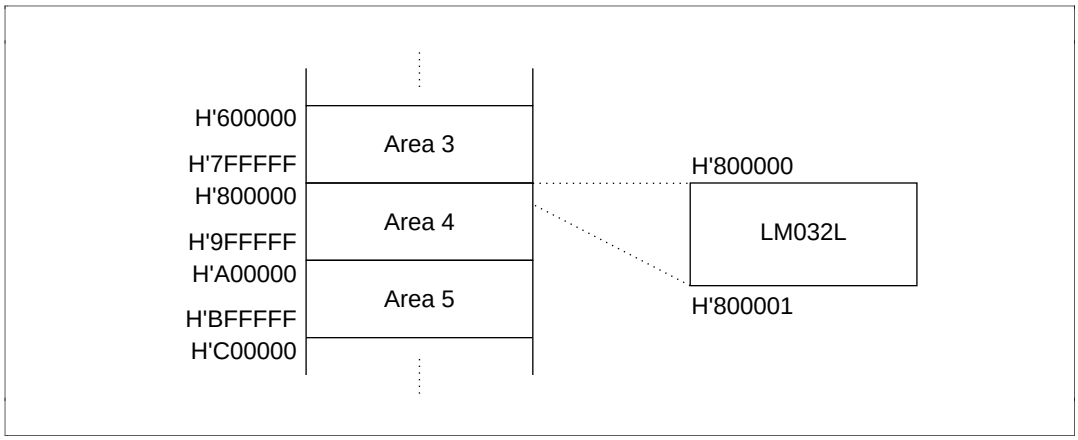


Figure 3.46 Memory Map

3.10.2 E Clock Generator

Figure 3.47 shows the E clock generator and figure 3.48 the E clock timing chart. When connecting the H8/3003 and LM032L, it is necessary to synchronize timing according to the E clock. Therefore, a ϕ clock count is made by decimal counter (74HC4017) to generate the E clock. Also, 9 wait states must be inserted to satisfy the E clock cycle time. With the H8/3003, insertion of more than 3 wait states is under control of the WAIT signal.

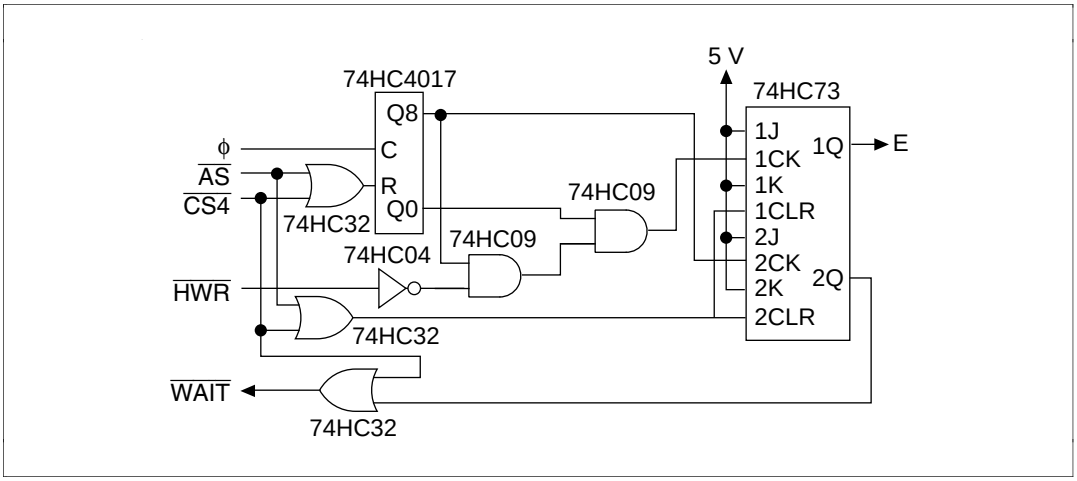


Figure 3.47 E Clock Generator Circuit

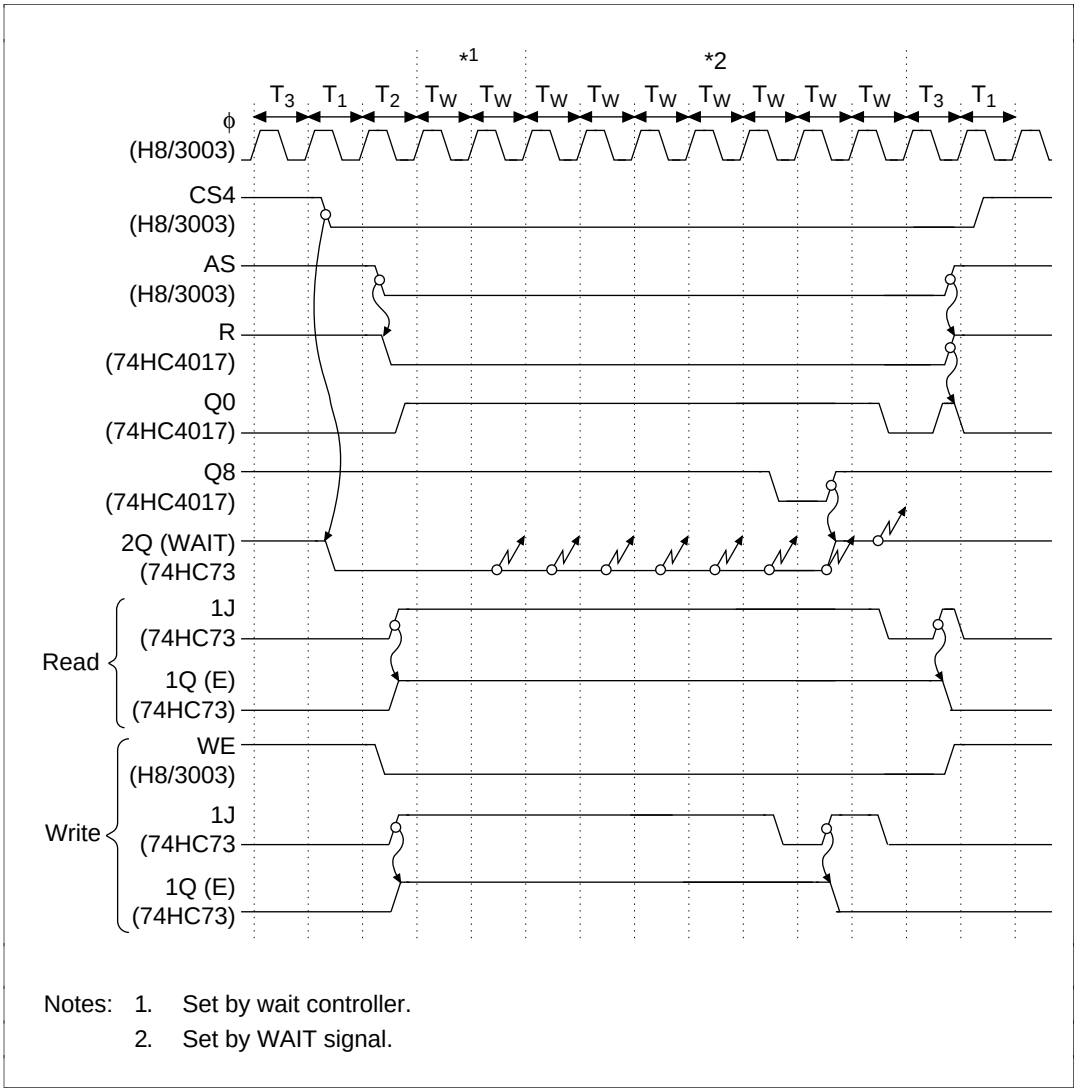


Figure 3.48 E Clock Timing Chart

3.10.3 Data Read/Write

Figures 3.49 and 3.50 show the read/write timing chart. When connecting the H8/3003 and LM032L, check that the following are satisfied:

- H8/3003:
  - — t_{RDS} (read data setup time)
  - — t_{RDH} (read data hold time)
- LM032L:
  - — PW_{EH} (enable pulse width)
  - — t_{DSW} (read data access time)
  - — t_H (write access time)
- E clock:
  - — t_{CYC} (enable cycle time).

From figure 3.49 and 3.50, the timings are as follows:

- H8/3003:
  - — t_{RDS} and t_{RDH}

$$t_{RDS} = t_{CL}\ (\text{min}) + T_W \times 9 + t_{CH}\ (\text{min}) - t_{DEL1}\ (\text{max}) - t_{DEL2}\ (\text{max}) - t_{DDR}\ (\text{max})$$
$$= 30 + 83.3 \times 9 + 30 - 46 - 30 - 320$$
$$= 413.7\ \text{ns} \geq 10\ \text{ns}\ (\text{H8/3003}\ t_{RDS})$$

$$t_{RDH} = t_{DEL1}\ (\text{min}) + t_{DEL2}\ (\text{min}) + t_H\ (\text{min}) - t_{ASD}\ (\text{max})$$
$$= 0 + 0 + 30 - 30$$
$$= 0\ \text{ns} \geq 0\ \text{ns}\ (\text{H8/3003}\ t_{RDS})$$

- Determine for LM032L:
  - — PW_{EH} and t_{CYC} from the following equations:

$$PW_{EH} = t_{CL}\ (\text{min}) + T_W \times 9 + t_{CH}\ (\text{min}) + t_{DEL1}\ (\text{min}) + t_{DEL2}\ (\text{min}) - t_{DEL1}\ (\text{max}) - t_{DEL2}\ (\text{max})$$
$$= 30 + 83.3 \times 9 + 30 + 0 + 0 - 46 - 30$$
$$= 733.7\ \text{ns} \geq 450\ \text{ns}\ (\text{LM032L}\ PW_{EH})$$

$$t_{CYC} = t_{CYC} \times 12$$
$$= 83.3 \times 12$$
$$= 1000\ \text{ns} \geq 1000\ \text{ns}\ (\text{LM032L}\ t_{CYC})$$

  - — t_{DSW} and t_H from the following equations:

$$t_{DSW} = T_2 + T_W \times 7 + t_{CH}\ (\text{min}) + t_{DEL1}\ (\text{min}) + t_{DEL2}\ (\text{min}) - t_{WSD}\ (\text{max}) + t_{WSD2}\ (\text{min})$$
$$= 83.3 + 83.3 \times 7 + 30 + 0 + 0 - 30 + 10$$
$$= 676.4\ \text{ns} \geq 195\ \text{ns}\ (\text{LM032L}\ t_{DSW})$$

t_H = t_{CL} (min) + T_{W9} + t_{CH} (min) + t_{ASD} (min) + t_{WDH} (min) – t_{DEL1} (max) – t_{DEL2} (max)

= 30 + 83.3 + 30 + 0 + 20 – 46 – 30

= 87.3 ns ≥ 20 ns (LM032L t_H)

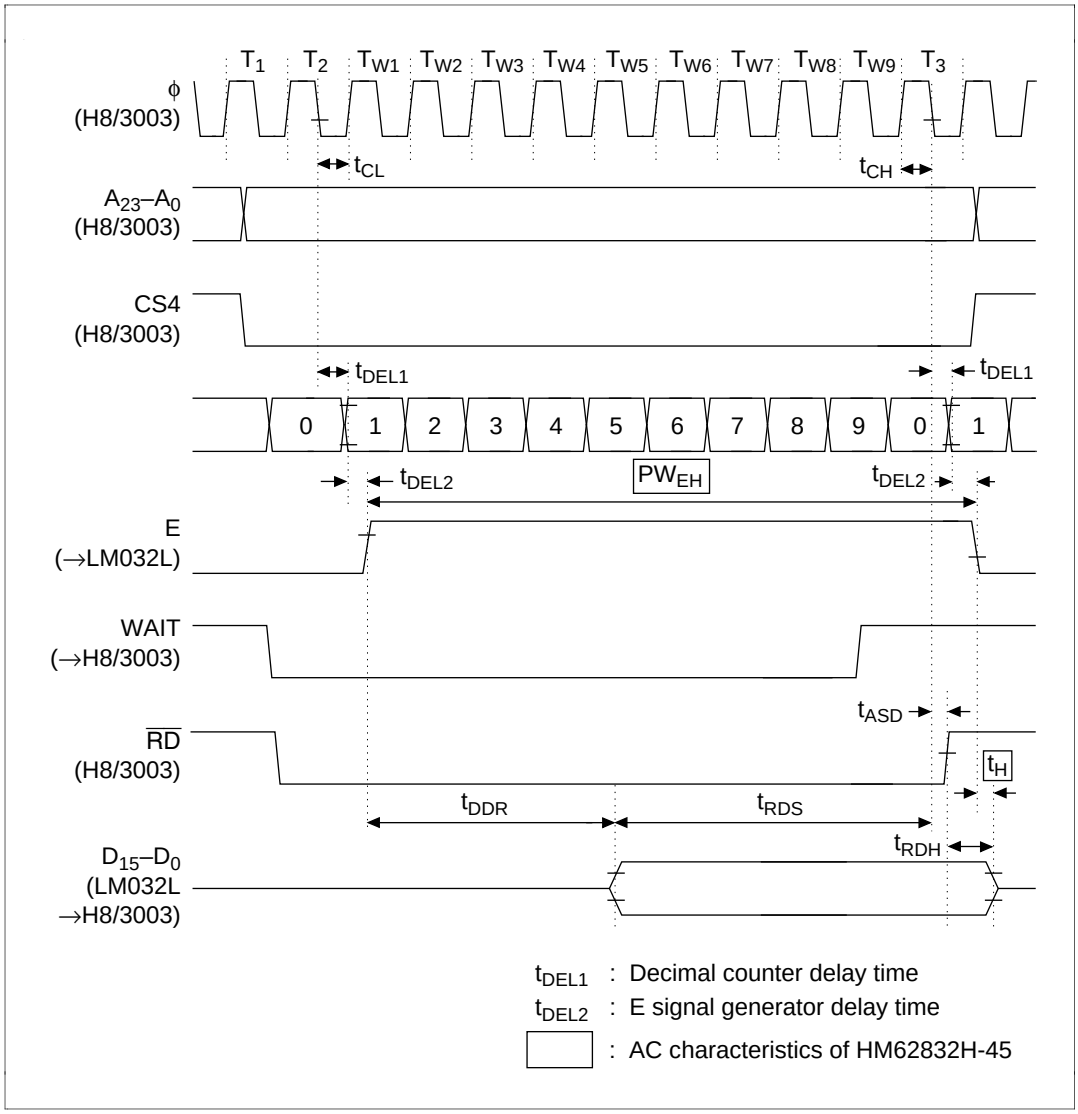


Figure 3.49 Read Timing Chart

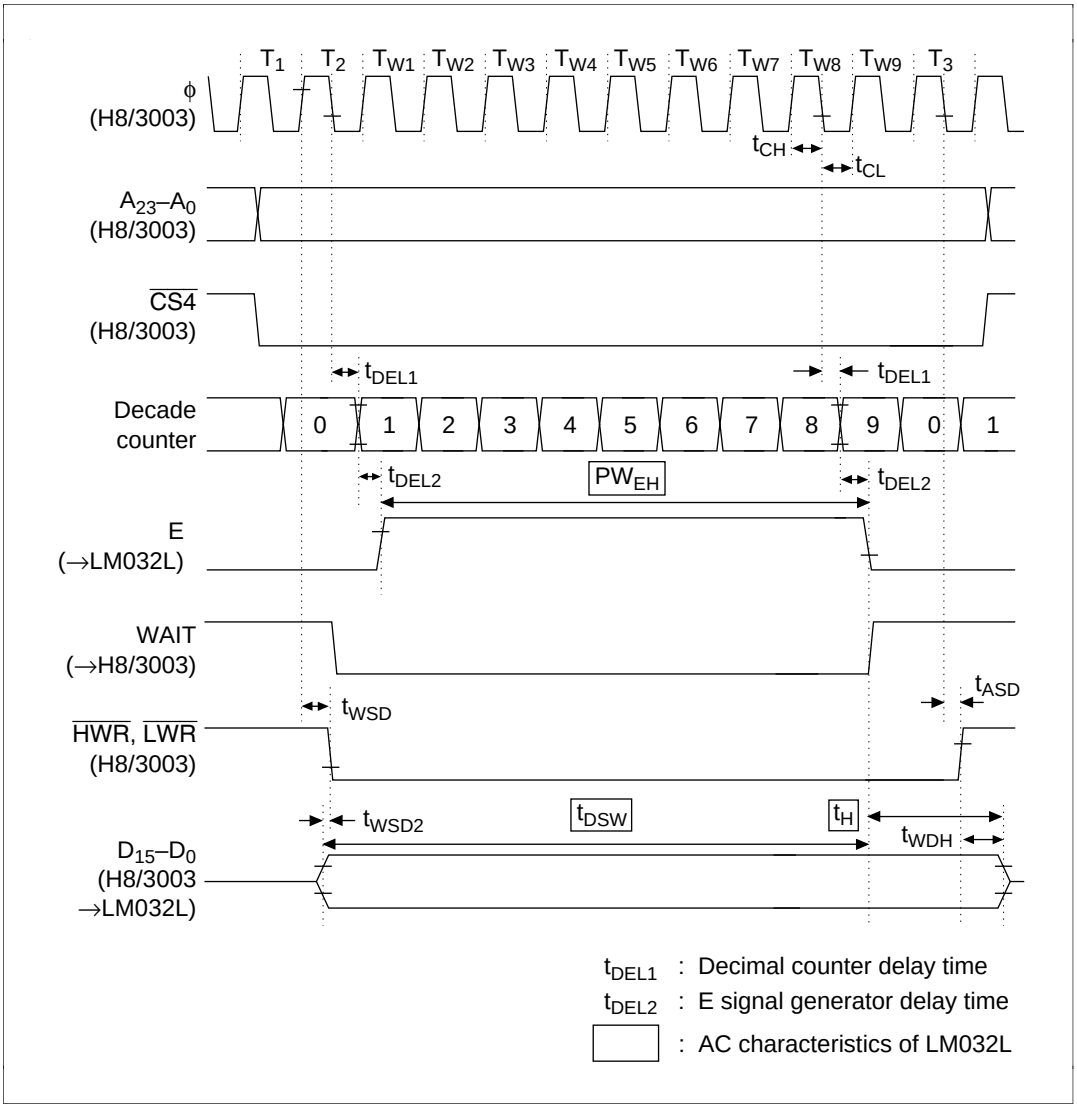


Figure 3.50 Write Timing Chart

3.10.4 Circuit Diagram

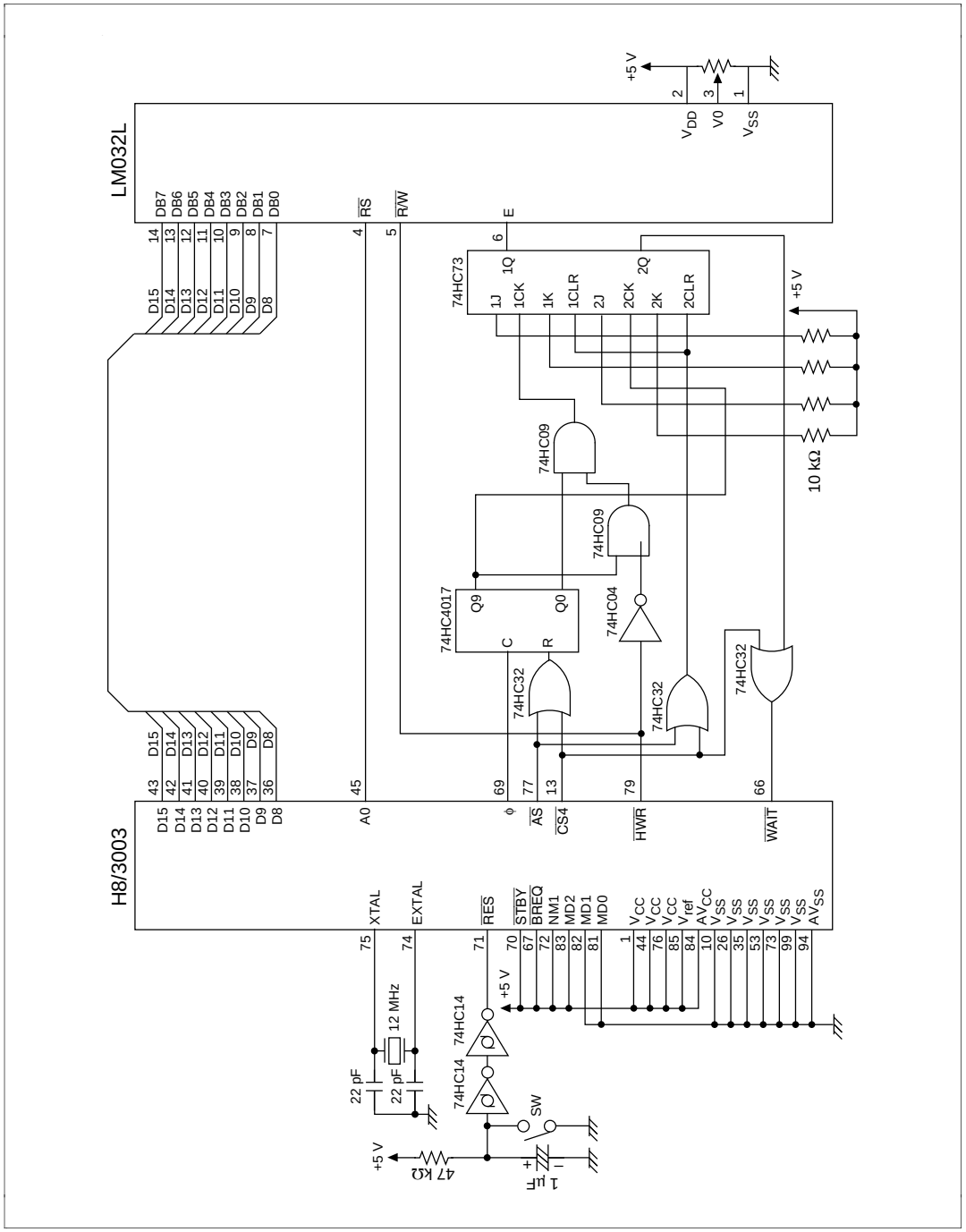


Figure 3.51 Circuit Diagram

Section 4 AC Characteristics of the H8/3003

Table 4.1 lists bus timing under various conditions within the H8/3003.

Table 4.1 Bus Timing (1) (Units: ns)

		Condition A*[1]		Condition B*[2]					
		8 MHz		10 MHz		12 MHz		16 MHz	
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Clock cycle time	t_{cyc}	125	500	100	500	83.3	500	62.5	500
Clock low pulse width	t_{CL}	40	—	40	—	30	—	20	—
Clock high pulse width	t_{CH}	40	—	40	—	30	—	20	—
Clock rise time	t_{CR}	—	20	—	10	—	10	—	10
Clock fall time	t_{CF}	—	20	—	10	—	10	—	10
Address delay time	t_{AD}	—	60	—	40	—	35	—	30
Address hold time	t_{AH}	25	—	20	—	15	—	10	—
Address strobe delay time	t_{ASD}	—	60	—	40	—	35	—	30
Write strobe delay time	t_{WSD}	—	60	—	40	—	35	—	30
Strobe delay time	t_{SD}	—	60	—	40	—	35	—	30
Write data strobe pulse width 1	t_{WSW1}*[3]	85	—	70	—	55	—	35	—
Write data strobe pulse width 2	t_{WSW2}*[3]	150	—	120	—	95	—	65	—
Address setup time 1	t_{AS1}	20	—	15	—	10	—	10	—
Address setup time 2	t_{AS2}	80	—	65	—	50	—	40	—
Read data setup time	t_{RDS}	50	—	20	—	20	—	20	—
Read data hold time	t_{RDH}	0	—	0	—	0	—	0	—
Write data delay time	t_{WDD}	—	75	—	65	—	60	—	60
Write data setup time 1	t_{WDS1}	90	—	75	—	60	—	35	—
Write data setup time 2	t_{WDS2}	15	—	10	—	10	—	5	—
Write data hold time	t_{WDH}	25	—	20	—	20	—	20	—
Read data access time 1	t_{ACC1}*[3]	—	110	—	100	—	80	—	55
Read data access time 2	t_{ACC2}*[3]	—	230	—	200	—	160	—	115

Notes: 1. Condition A: V_{CC} = 2.7–5.5 V, AV_{CC} = 2.7–5.5 V, Vref = 2.7–AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2–8 MHz, Ta = –20 to +75°C (normal specification), Ta = –40 to +85°C (wide temperature range specification)

2. Condition B: Vcc = 5.0 V ±10%, AVcc = 5.0 V ±10%, Vref = 4.5–AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2–16 MHz, Ta = –20 to +75°C (normal specification), Ta = –40 to +85°C (wide temperature range specification)

3. See note 3 following table 4.2

Table 4.2 Bus Timing (2) (Units: ns)

		Condition A*1		Condition B*2					
		8 MHz		10 MHz		12 MHz		16 MHz	
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Read data access time 3	t_{ACC3}*3	—	55	—	50	—	40	—	25
Read data access time 4	t_{ACC4}*3	—	160	—	150	—	120	—	85
Precharge time	t_{PCH}*3	85	—	70	—	55	—	40	—
Wait setup time	t_{WTS}	40	—	35	—	25	—	25	—
Wait set hold time	t_{WTH}	10	—	10	—	5	—	5	—
Bus request setup time	t_{BRQS}	40	—	40	—	40	—	40	—
Bus acknowledge delay time 1	t_{BACD1}	—	60	—	50	—	40	—	30
Bus acknowledge delay time 2	t_{BACD2}	—	60	—	50	—	40	—	30
Bus floating time	t_{BZD}	—	70	—	60	—	50	—	40

Notes: 1: Condition A: V_{CC} = 2.7–5.5 V, AV_{CC} = 2.7–5.5 V, Vref = 2.7–AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2–8 MHz, Ta = –20 to +75°C (normal specification), Ta = –40 to +85°C (wide temperature range specification)

2: Condition B: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, Vref = 4.5–AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2–16 MHz, Ta = –20 to +75°C (normal specification), Ta = –40 to +85°C (wide temperature range specification)

3: During 8-MHz operation the following times are dependent on the clock cycle time as indicated:

$t_{ACC1} = 1.5 \times t_{cyc} - 78$ (ns)
$t_{ACC2} = 2.5 \times t_{cyc} - 83$ (ns)
$t_{ACC3} = 1.0 \times t_{cyc} - 70$ (ns)
tACC4 = $2.0 \times t_{cyc} - 90$ (ns)
$t_{WSW1} = 1.0 \times t_{cyc} - 40$ (ns)
$t_{WSW2} = 1.5 \times t_{cyc} - 38$ (ns)
$t_{PCH} = 1.0 \times t_{cyc} - 40$ (ns)

During-10 MHz operation the following times are dependent on the clock cycle time as indicated:

$t_{ACC1} = 1.5 \times t_{cyc} - 50$ (ns)
$t_{ACC2} = 2.5 \times t_{cyc} - 50$ (ns)
$t_{ACC3} = 1.0 \times t_{cyc} - 50$ (ns)
$t_{ACC4} = 2.0 \times t_{cyc} - 50$ (ns)
$t_{WSW1} = 1.0 \times t_{cyc} - 30$(ns)
$t_{WSW2} = 1.5 \times t_{cyc} - 30$ (ns)
$t_{PCH} = 1.0 \times t_{cyc} - 30$ (ns)

During-12 MHz operation the following times are dependent on the clock cycle time as indicated:

$t_{ACC1} = 1.5 \times t_{cyc} - 45$ (ns)
$t_{ACC2} = 2.5 \times t_{cyc} - 48$ (ns)
$t_{ACC3} = 1.0 \times t_{cyc} - 43$ (ns)
$t_{ACC4} = 2.0 \times t_{cyc} - 47$ (ns)
$t_{WSW1} = 1.0 \times t_{cyc} - 28$ (ns)
$t_{WSW2} = 1.5 \times t_{cyc} - 30$ (ns)
$t_{PCH} = 1.0 \times t_{cyc} - 28$ (ns)

During 16-MHz operation the following times are dependent on the clock cycle time as indicated:

$t_{ACC1} = 1.5 \times t_{cyc} - 39$ (ns) $t_{WSW1} = 1.0 \times t_{cyc} - 28$ (ns)
$t_{ACC2} = 2.5 \times t_{cyc} - 41$ (ns) $t_{WSW2} = 1.5 \times t_{cyc} - 28$ (ns)
$t_{ACC3} = 1.0 \times t_{cyc} - 38$ (ns) $t_{PCH} = 1.0 \times t_{cyc} - 23$ (ns)
$t_{ACC4} = 2.0 \times t_{cyc} - 40$ (ns)

Table 4.3 Bus Timing (Refresh Controller) (Units: ns)

		Condition A*[1]		Condition B*[2]					
		8 MHz		10 MHz		12 MHz		16 MHz	
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
$\overline{RAS}$ delay time 1	t_{RAD1}	—	60	—	30	—	30	—	30
$\overline{RAS}$ delay time 2	t_{RAD2}	—	60	—	30	—	30	—	30
$\overline{RAS}$ delay time 3	t_{RAD3}	—	60	—	30	—	30	—	30
Row address hold time	t_{RAH}*[3]	25	—	20	—	15	—	15	—
$\overline{RAS}$ precharge time	t_{RP}*[3]	85	—	70	—	55	—	40	—
$\overline{CAS}$ to RAS precharge time	t_{CRP}*[3]	85	—	70	—	55	—	40	—
$\overline{CAS}$ pulse width	t_{CAS}	110	—	40	—	40	—	40	—
$\overline{RAS}$ access time	t_{RAC}*[3]	—	160	—	150	—	120	—	85
Address access time	t_{AA}	—	105	—	55	—	55	—	55
$\overline{CAS}$ access time	t_{CAC}*[3]	—	50	—	50	—	40	—	25
Write data setup time 3	t_{WDS3}	75	—	40	—	40	—	40	—
$\overline{CAS}$ setup time	t_{CSR}*[3]	20	—	15	—	15	—	15	—
Read strobe delay time	t_{RSD}	—	60	—	30	—	30	—	30

Notes: 1. Condition A: V_{CC} = 2.7–5.5V, AV_{CC} = 2.7–5.5V, Vref = 2.7–AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2–8 MHz, Ta = –20 to +75°C (normal specification), Ta = –40 to +85°C (wide temperature range specification)

2. Condition B: Vcc = 5.0 V ±10%, AVcc = 5.0 V ±10%, Vref = 4.5–AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2–16 MHz, Ta = –20 to +75°C (normal specification), Ta = –40 to +85°C (wide temperature range specification)

3. During 8-MHz operation the following times are dependent on the clock cycle time as indicated:

$t_{RAH} = 0.5 \times t_{cyc} - 38$ (ns) $t_{CAC} = 1.0 \times t_{cyc} - 75$ (ns)
$t_{RAC} = 2.0 \times t_{cyc} - 90$ (ns) $t_{CSR} = 0.5 \times t_{cyc} - 43$ (ns)
$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 40$ (ns)

During 10-MHz operation the following times are dependent on the clock cycle time as indicated:

$t_{RAH} = 0.5 \times t_{cyc} - 30$ (ns) $t_{CAC} = 1.0 \times t_{cyc} - 50$ (ns)

$t_{RAC} = 2.0 \times t_{cyc} - 50$ (ns) $t_{CSR} = 0.5 \times t_{cyc} - 35$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 30$ (ns)

During 12-MHz operation the following times are dependent on the clock cycle time as indicated:

$t_{RAH} = 0.5 \times t_{cyc} - 27$ (ns) $t_{CAC} = 1.0 \times t_{cyc} - 43$ (ns)

$t_{RAC} = 2.0 \times t_{cyc} - 47$ (ns) $t_{CSR} = 0.5 \times t_{cyc} - 27$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 28$ (ns)

During 16-MHz operation the following times are dependent on the clock cycle time as indicated.

$t_{RAH} = 0.5 \times t_{cyc} - 16$ (ns) $t_{CAC} = 1.0 \times t_{cyc} - 38$ (ns)

$t_{RAC} = 2.0 \times t_{cyc} - 40$ (ns) $t_{CSR} = 0.5 \times t_{cyc} - 16$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 23$ (ns)

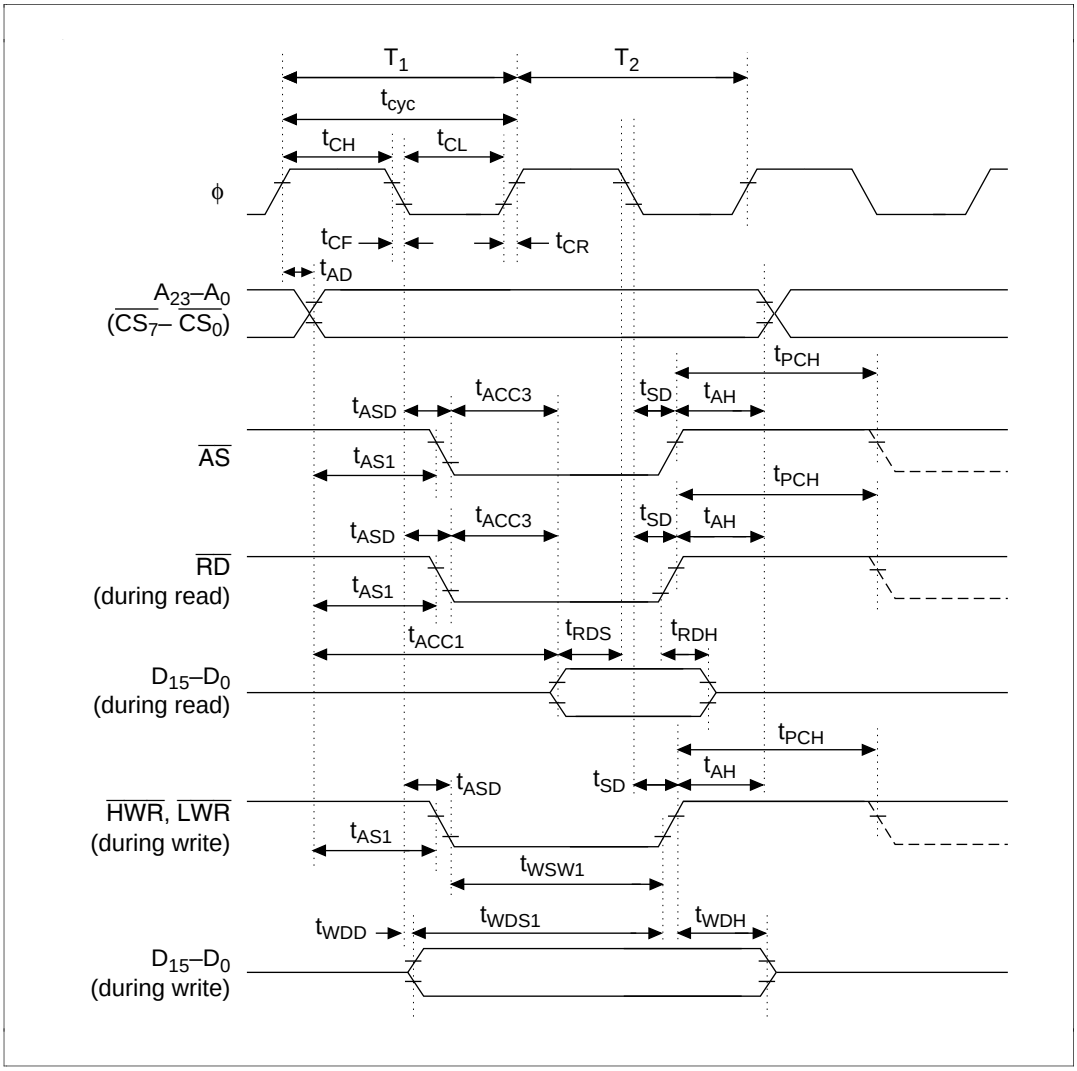


Figure 4.1 Timing Waveforms (Basic Bus Timing/2 States)

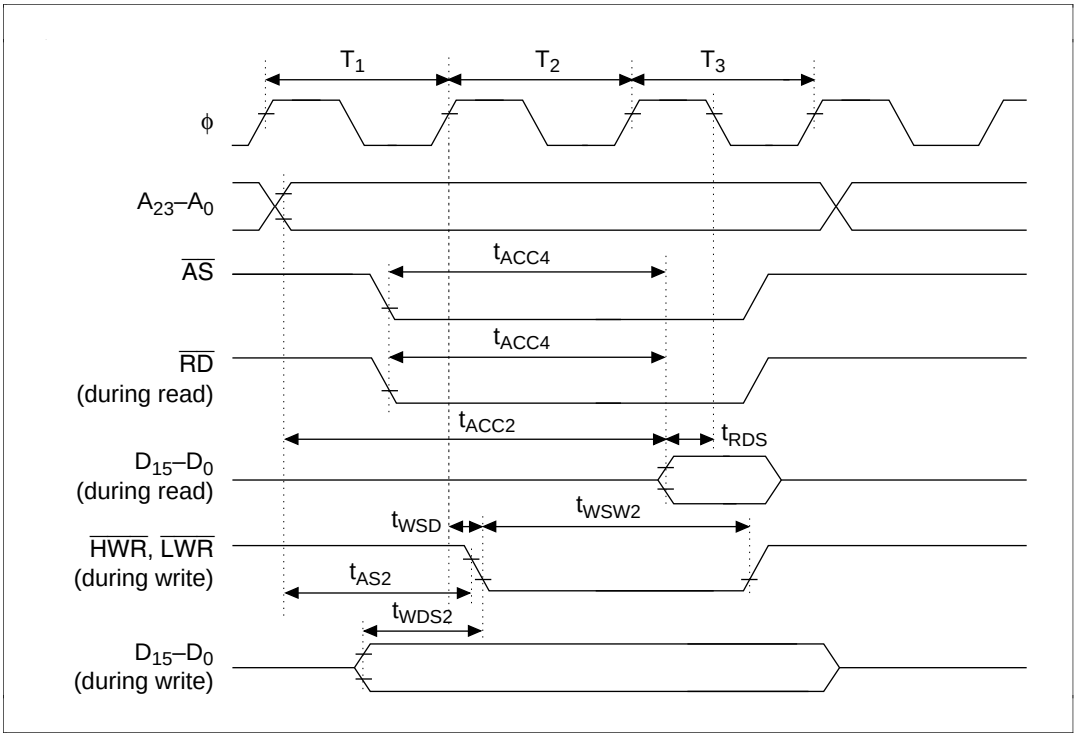


Figure 4.2 Timing Waveforms (Basic Bus Timing/3 States)

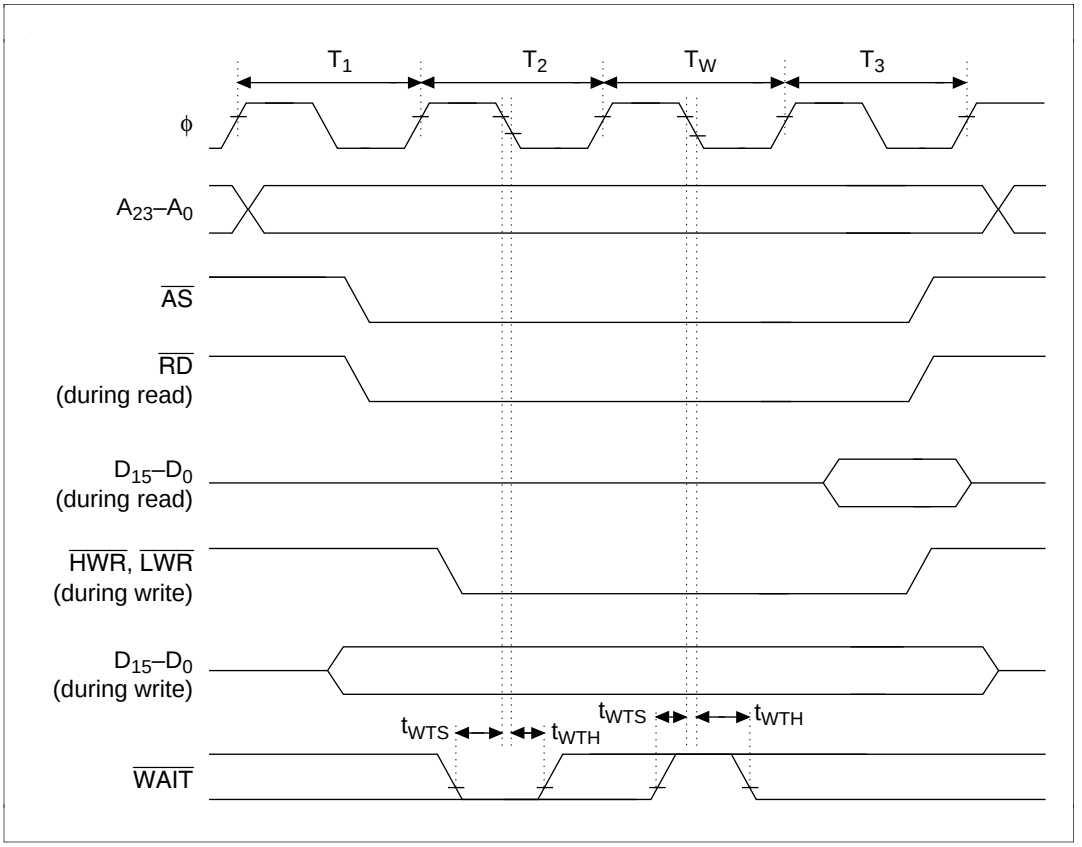


Figure 4.3 Timing Waveforms (Basic Bus Timing/2 States + 1 Wait)

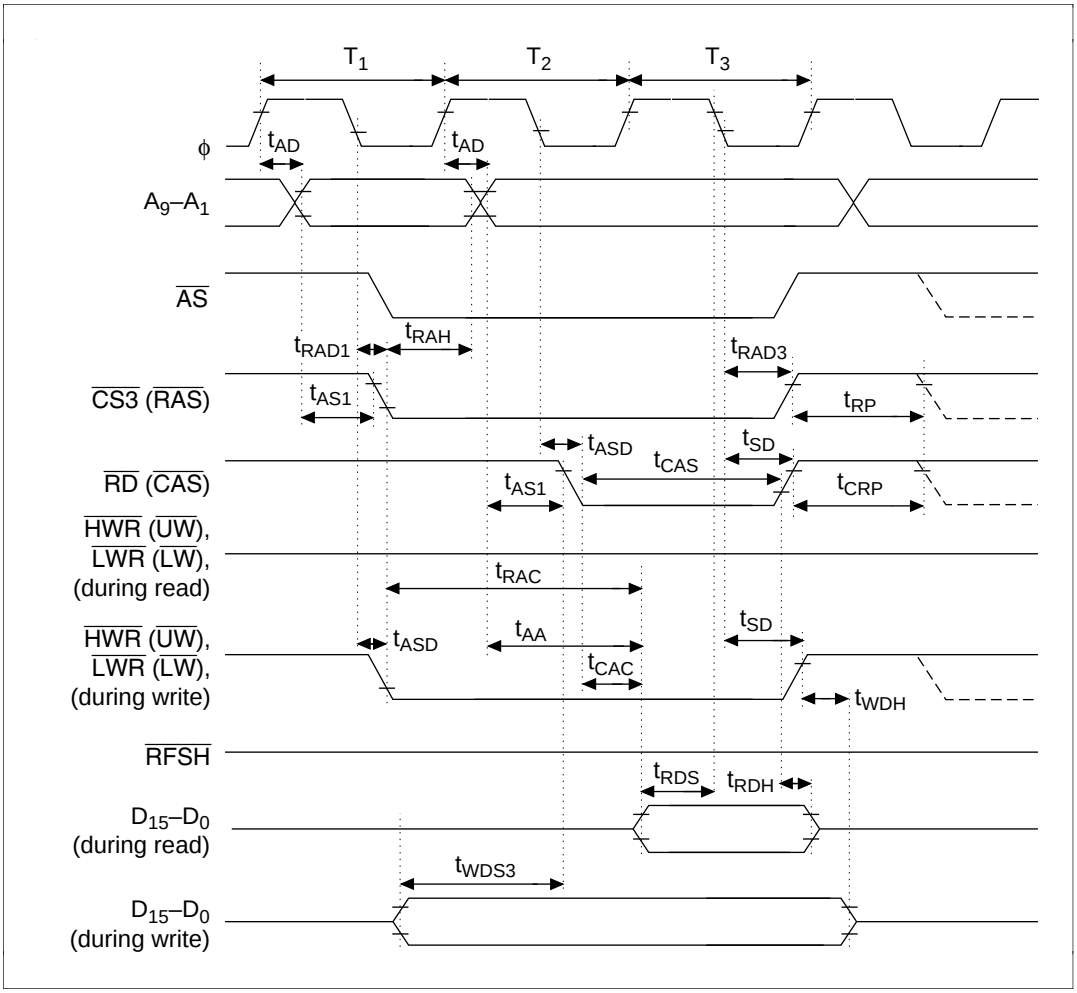


Figure 4.4 Timing Waveforms (DRAM Bus Timing/Read-Write/2 WE Method)

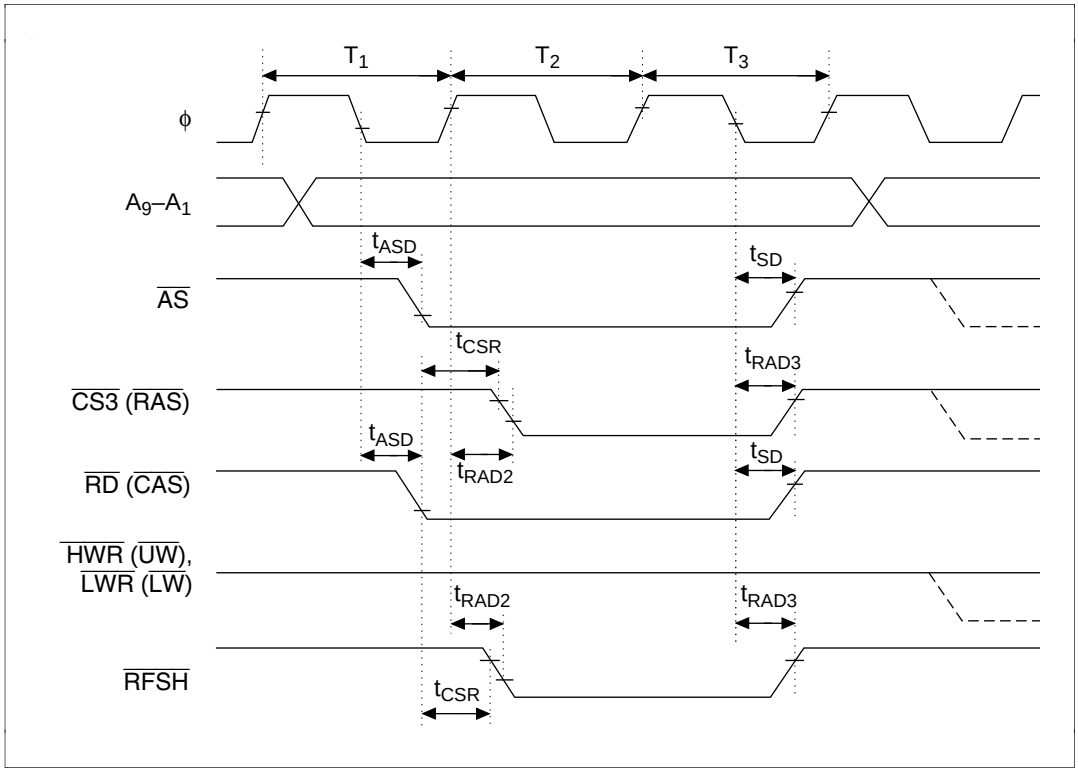


Figure 4.5 Timing Waveforms (DRAM Bus Timing/Refresh)

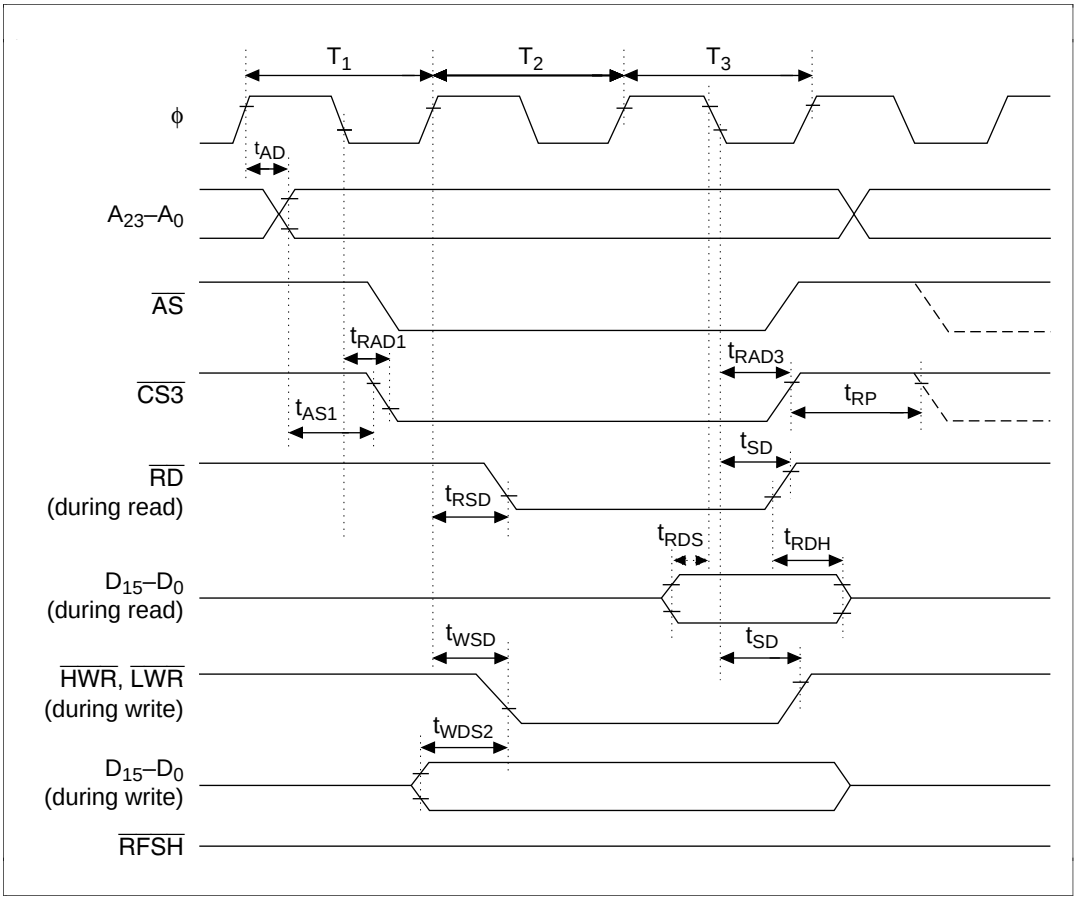


Figure 4.6 Timing Waveforms (PSRAM Bus Timing/Read-Write)

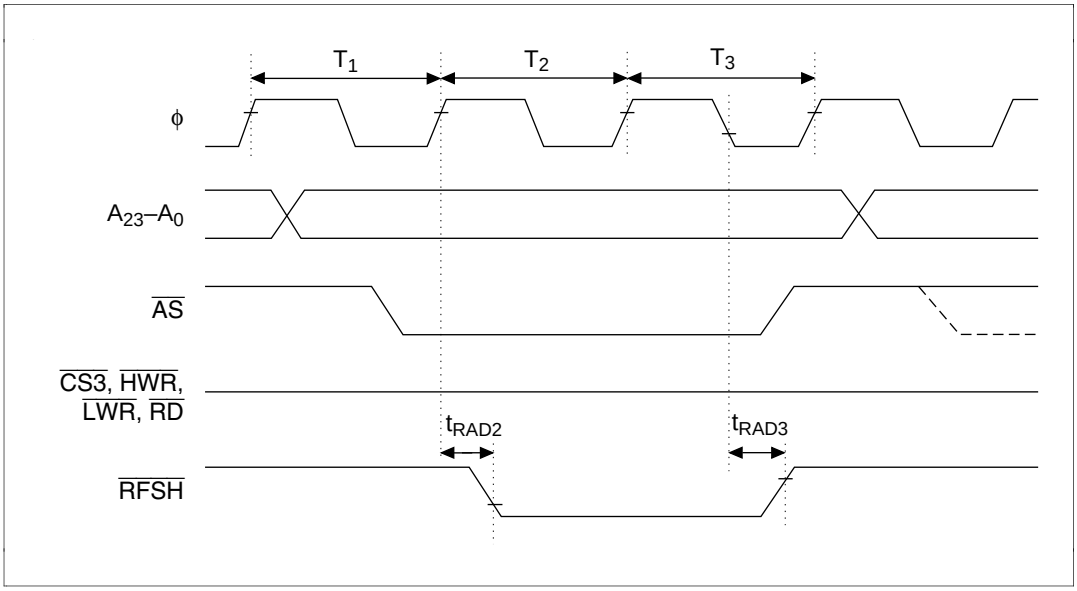


Figure 4.7 Timing Waveforms (PSRAM Bus Timing/Refresh)

Section 5 Memory AC Characteristics

5.1 HM62832H-45 AC Characteristics

Measuring Conditions:

- V_{CC} = 5 V ± 10%, Ta = 0 to +70°C
- Input pulse level: V_{SS} to 3.0 V
- Input rise/fall time: 5 ns
- I/O timing reference level: 1.5 V
- Output load: see figure 5.1

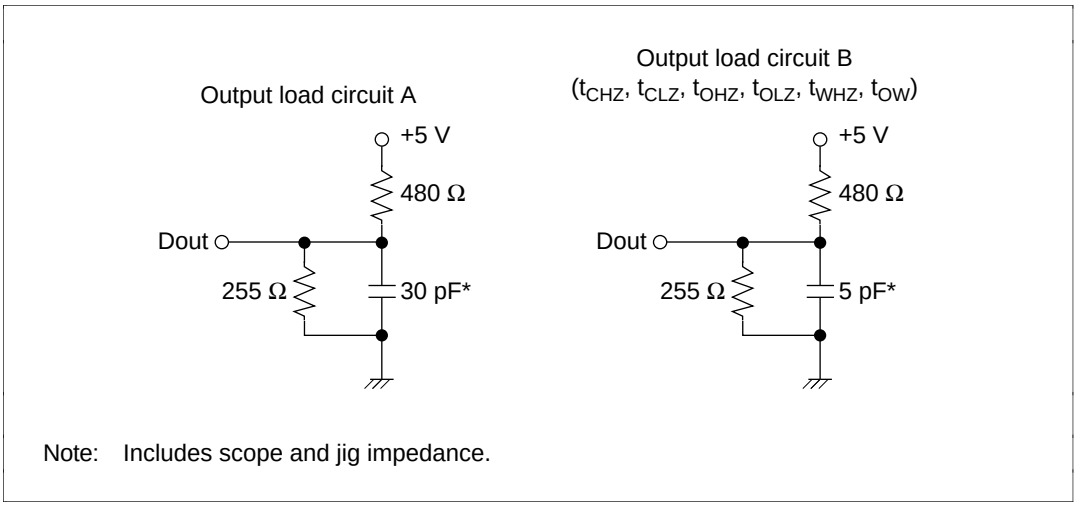


Figure 5.1 Output Loading Conditions

Table 5.1 Bus Timing (Read)

		HM62832H-25		HM62832H-35		HM62832H-45		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
CS output set time	t_{CLZ*}	5	—	5	—	5	—	ns
Output enable access time	t_{OE}	—	12	—	15	—	20	ns
Output enable/output set time	t_{OLZ*}	0	—	0	—	0	—	ns
Chip deselect/output floating time	t_{CHZ*}	0	12	0	15	0	20	ns
Output disable/output floating time	t_{OHZ*}	0	12	0	15	0	20	ns
Output hold time	t_{OH}	5	—	5	—	5	—	ns

Note: Transition is measured at ±200 mV from the high impedance voltage due to load circuit (B) (figure 5.1). This parameter is not measured for all items but is a sample value.

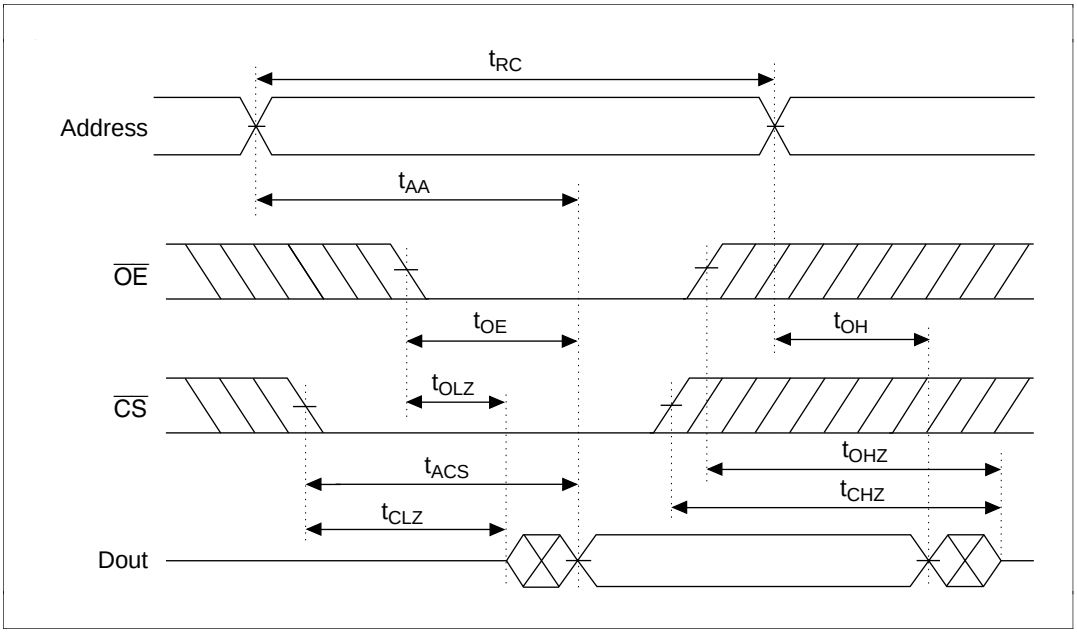
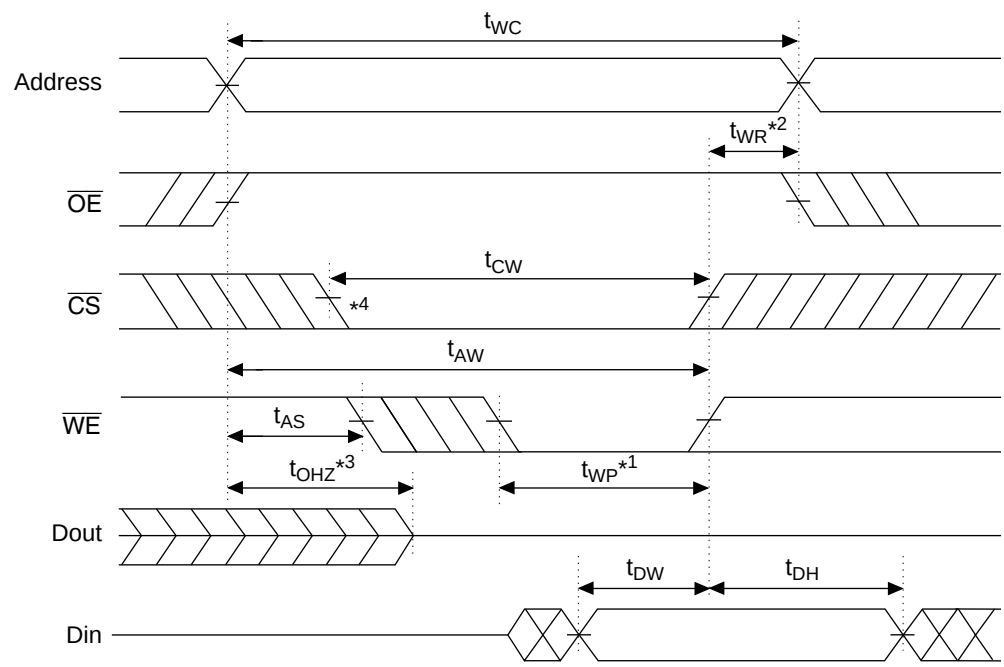


Figure 5.2 Timing Waveforms (Read)

Table 5.2 Bus Timing (Write)

		HM62832H-25		HM62832H-35		HM62832H-45		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write cycle time	t_{WC}	25	—	35	—	45	—	ns
Chip select time	t_{CW}	15	—	20	—	25	—	ns
Address valid time	t_{AW}	20	—	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write pulse time	t_{WP}	15	—	20	—	25	—	ns
Address hold time	t_{WR}	0	—	0	—	0	—	ns
Output disable/output floating time	t_{OHZ*}	0	12	0	15	0	20	ns
$\overline{WE}$/output floating time	t_{WHZ*}	0	12	0	15	0	20	ns
Input data set time	t_{DW}	12	—	15	—	20	—	ns
Input data hold time	t_{DH}	0	—	0	—	0	—	ns
$\overline{WE}$ output set time	t_{OW}	5	—	5	—	5	—	ns

Note: Transition is measured at ±200 mV from the high impedance voltage due to load circuit (B) (figure 5.1). This parameter is not measured for all items but is a sample value.



Notes:
1. Write conducted during the overlap (t_{WP}) when $\overline{CS}$ is low and $\overline{WE}$ is low.
2. t_{WR} specified for the end of the write cycle from whichever transition comes earlier, the $\overline{WE}$ or $\overline{CS}$ high transition.
3. I/O pin in output mode during this period. At this time, a data input signal of inverse phase to the output must not be applied.
4. When the $\overline{CS}$ low transition occurs simultaneously with $\overline{WE}$ low transition or after it, output stays at high impedance.
5. $\overline{OE} = V_{IL}$
6. Drive $\overline{WE}$ or $\overline{CS}$ high during address transition.

Figure 5.3 Timing Waveforms (Write)

5.2 HN27C256HG-70 AC Characteristics

Table 5.3 Bus Timing (Read)

		HN27C256HG-70		HN27C256HG-85		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Access time	t_{ACC}	—	70	—	85	ns
$\overline{CE}$/output delay time	t_{CE}	—	70	—	85	ns
$\overline{OE}$/output delay time	t_{OE}	—	40	—	45	ns
Output disable delay time	t_{DF}*	0	30	0	30	ns
Data output hold time	t_{OH}	5	—	5	—	ns

Note: t_{DF} defined as the condition when the release state is reached and the output level can no longer be referenced.

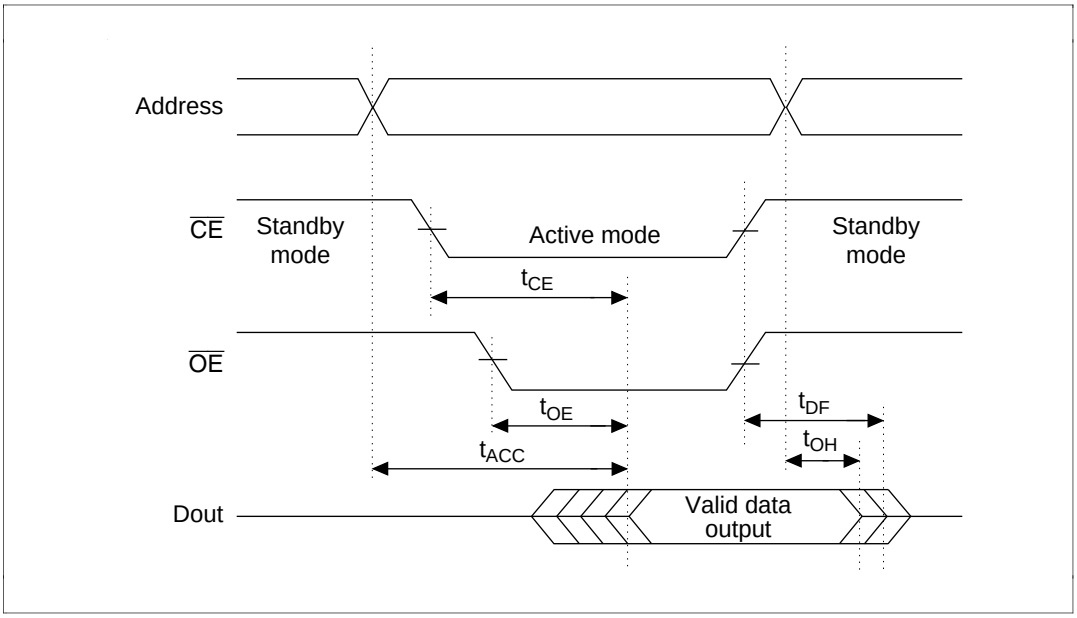


Figure 5.4 HN27C256HG-70 Timing Waveforms (Read)

5.3 HN62444BNP AC Characteristics

Table 5.4 Bus Timing

Item	Symbol	Min	Max	Units
Cycle time	t_{RC}	120	—	ns
Nibble cycle time	t_{NC}	70	—	ns
Address access time	t_{AA}	—	120	ns
Nibble address access time	t_{NA}	—	70	ns
$\overline{CE}$ access time	t_{ACE}	—	120	ns
$\overline{OE}$ access time	t_{OE}	—	55	ns
Address/output hold time	t_{DHA}	0	—	ns
$\overline{CE}$/output hold time	t_{DHC}	0	—	ns
$\overline{OE}$/output hold time	t_{DHO}	0	—	ns
$\overline{CE}$/output floating time	t_{CHZ*}	—	40	ns
$\overline{OE}$/output floating time	t_{OHZ*}	—	40	ns
$\overline{CE}$/output set time	t_{CLZ}	5	—	ns
$\overline{OE}$/output set time	t_{OLZ}	5	—	ns

Note: t_{CHZ} and t_{OHZ} are specified as times until output reaches the release state, and are not determined by output voltage level.

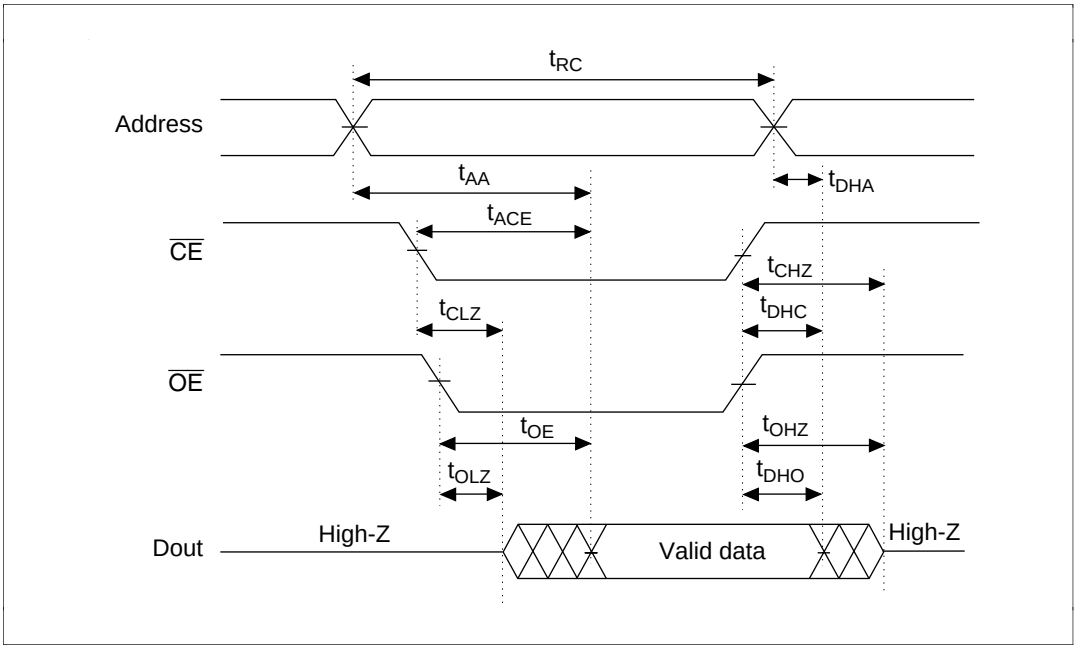


Figure 5.5 HN62444BNP Timing Waveforms (Read)

5.4 HM65256B-12 AC Characteristics

Table 5.5 Bus Timing

Item	Sym-bol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Random read/write cycle time	t_{RC}	160	—	190	—	235	—	310	—	ns
SC mode read/write cycle time	t_{RSC}	55	—	65	—	80	—	105	—	ns
Chip enable access time	t_{CEA}	—	100	—	120	—	150	—	200	ns
Address access time	t_{AA}	—	50	—	60	—	75	—	100	ns
Output enable access time	t_{OEA}	—	40	—	50	—	60	—	75	ns
Chip disable/ output delay (high Z)	t_{CHZ}	—	25	—	25	—	30	—	35	ns
Chip enable/ output delay (low Z)	t_{CLZ}	30	—	30	—	35	—	40	—	ns
Output enable/ output delay (low Z)	t_{OLZ}	10	—	10	—	10	—	10	—	ns
Output disable/ output delay (high Z)	t_{OHZ}	—	25	—	25	—	30	—	35	ns
Chip enable pulse width	t_{CE}	100n	4m	120n	4m	150n	4m	200n	4m	s
Chip enable pre-charge time	t_{P}	50	—	60	—	75	—	100	—	ns

Table 5.5 Bus Timing (cont)

Item	Sym-bol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Row address hold time	t_{RAH}	20	—	20	—	25	—	30	—	ns
Column address hold time	t_{CAH}	100	—	120	—	150	—	200	—	ns
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns
Output enable hold time	t_{OHC}	0	—	0	—	0	—	0	—	ns
Output enable/ chip enable delay time	t_{OCD}	0	—	0	—	0	—	0	—	ns
Output hold time (from column address)	t_{OH}	5	—	5	—	5	—	10	—	ns
Write command pulse width	t_{WP}	25	—	25	—	30	—	35	—	ns
Chip enable time	t_{CW}	100	—	120	—	150	—	200	—	ns
Column address setup time (for write)	t_{ASW}	0	—	0	—	0	—	0	—	ns
Column address hold time (after write)	t_{AHW}	0	—	0	—	0	—	0	—	ns

Table 5.5 Bus Timing (cont)

Item	Sym-bol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Input data set time	t_{DW}	20	—	20	—	25	—	30	—	ns
Input data hold time (after write)	t_{DH}	0	—	0	—	0	—	0	—	ns
Write disable/ output delay (low Z)	t_{OW}	5	—	5	—	5	—	5	—	ns
Write enable/ output delay (high Z)	t_{WHZ}	—	25	—	25	—	30	—	35	ns
Transition time (rise/fall)	t_T	3	50	3	50	3	50	3	50	ns
Refresh com-mand delay time	t_{RFD}	50	—	60	—	75	—	100	—	ns
Refresh pre-charge time	t_{FP}	30	—	30	—	30	—	30	—	ns
Refresh com-mand pulse width (auto-refresh)	t_{FAP}	80	10000	80	10000	80	10000	80	10000	ns
Auto-refresh cycle time	t_{FC}	160	—	190	—	235	—	310	—	ns
Refresh com-mand pulse width (self-refresh)	t_{FAS}	10000	—	10000	—	10000	—	10000	—	ns
Refresh set time (self-refresh)	t_{FRS}	160	—	190	—	235	—	310	—	ns
Refresh cycle	t_{REF}	—	4	—	4	—	4	—	4	ms

Notes: 1. Measuring conditions (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)
Input pulse level = 2.4 V, 0.4 V
Input rise and fall time = 5 ns
Input timing reference level = 2.2 V, 0.8 V
Output reference level = V_{OH} = 2.0 V, V_{OL} = 0.8 V
Output load = 1TTL + 100 pF (including jig and scope)

2. t_{CHZ}, t_{OHz} and, t_{WHZ} are specified as times when output has reached open circuit condition.

3. Sample value under conditions of tr = 5 ns for t_{CLZ}, t_{OLZ}, and t_{OW}. This value is not measured for all items.
4. Write is conducted in the overlap when $\overline{CE}$ and $\overline{WE}$ are low.
5. When $\overline{CS}$ low occurs simultaneously with $\overline{WE}$ low or after it, output stays at high impedance.
6. When an input signal of inverse phase to the output is applied in the write cycle, $\overline{OE}$ or $\overline{WE}$ must disable the output buffer prior to applying data to the device. Then data input must be floated before the output buffer's $\overline{OE}$ or $\overline{WE}$ is asserted.
7. V_{IH} (min) and V_{IL} (max) are input signal measurement timing reference levels. Therefore, the transition time is measured between VI_H and V_{IL}.
8. Standby for 100 µs or more after power on, and add at least 8 initialize cycles.
9. When self-refresh ends, fix $\overline{CE}$ and $\overline{OE}$ High during self-refresh set time (t_{FRS}) to reset self-refresh operation in RAM. When conducting an auto-refresh following a self-refresh, drive $\overline{OE}$ low on completion of t_{FRS} at the start of auto-refresh.

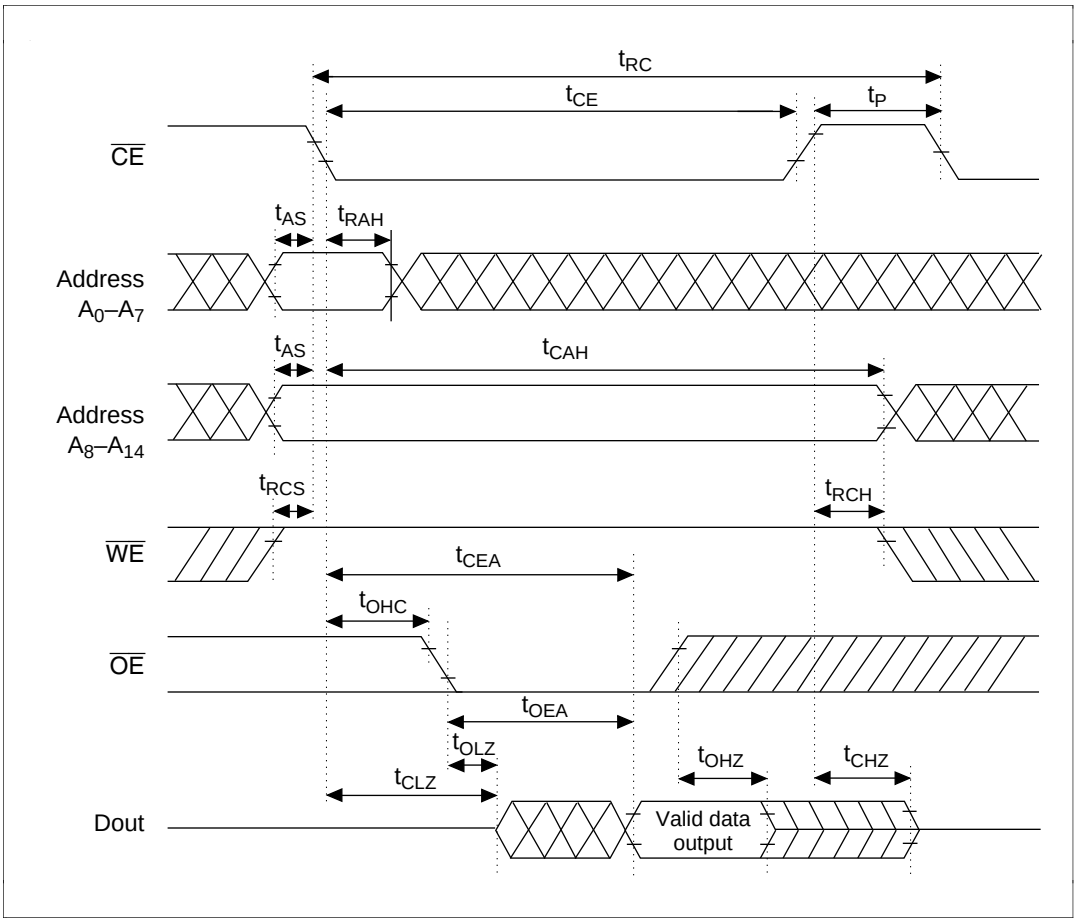


Figure 5.6 HM65256B-12 Timing Waveforms (Read)

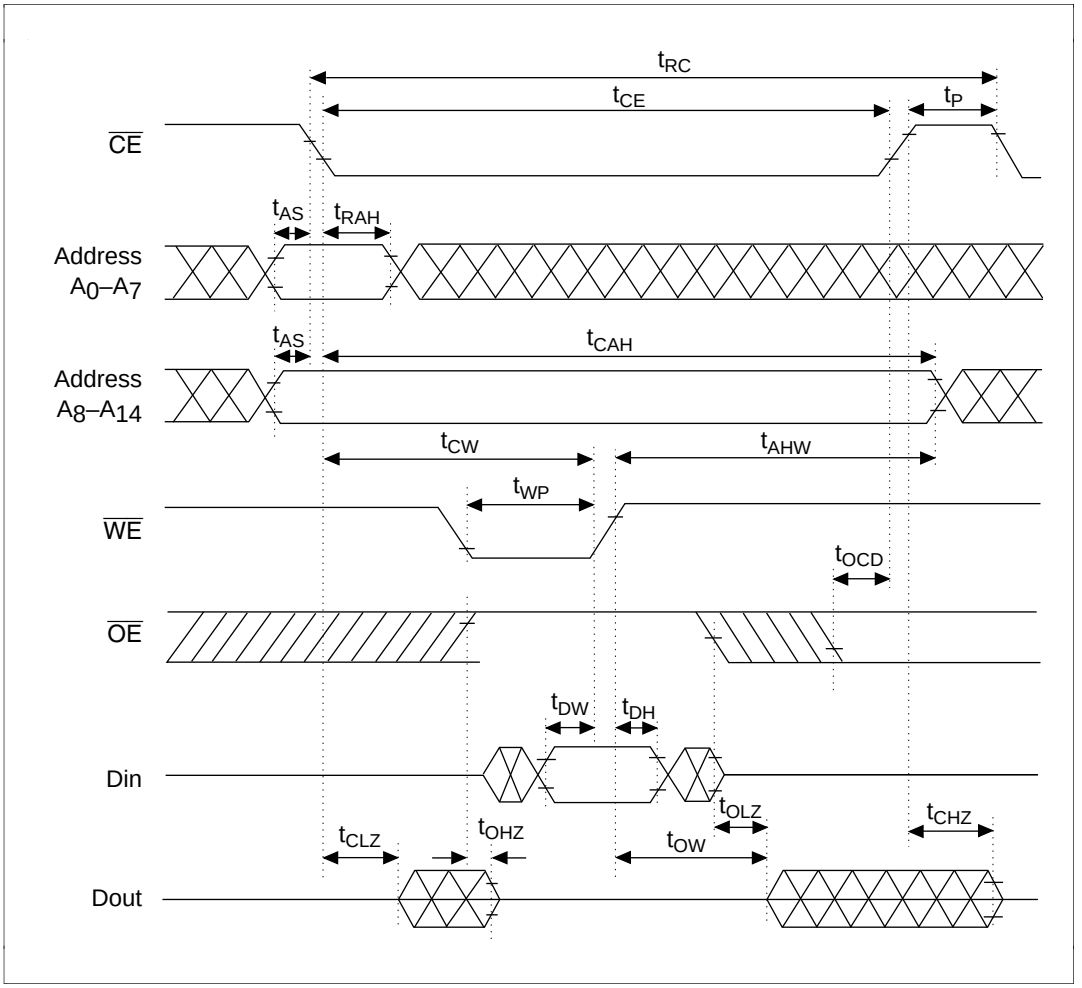


Figure 5.7 HM65256B-12 Timing Waveforms (Write)

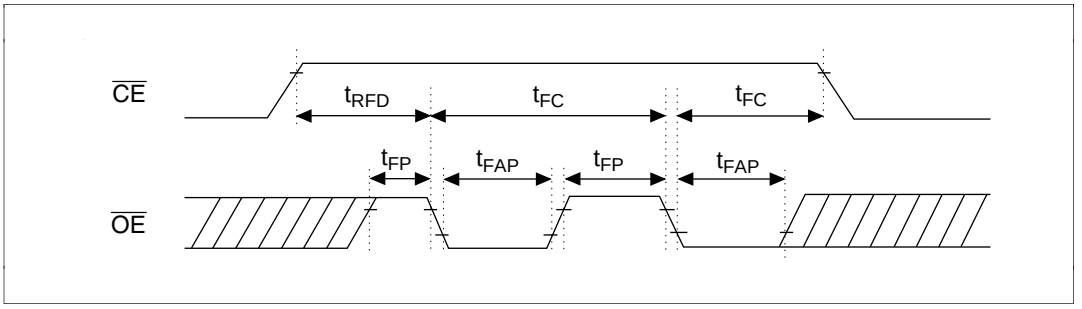


Figure 5.8 HM65256B-12 Timing Waveforms (Refresh)

5.5 HM514260 AC Characteristics

Table 5.6 Bus Timing (Common)

		HM514260A-7 HM51S4260A-7		HM514260A-8 HM51S4260A-8		HM514260A-10 HM51S4260A-10		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Random read/write cycle	t_{RC}	130	—	150	—	180	—	ns
$\overline{RAS}$ precharge time	t_{RP}	50	—	60	—	70	—	ns
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	30	10000	25	10000	ns
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns
Row address hold time	t_{RAH}	10	—	10	—	15	—	ns
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns
Column address hold time	t_{CAH}	15	—	15	—	20	—	ns
$\overline{RAS}$ $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns
$\overline{RAS}$ column address delay time	t_{RAD}	15	35	15	40	20	55	ns
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	25	—	ns
$\overline{CAS}$ hold time	t_{CSH}	70	—	80	—	100	—	ns
$\overline{CAS}$ $\overline{RAS}$ precharge time	t_{CRP}	15	—	15	—	15	—	ns
$\overline{OE}$/data input delay time	t_{ODD}	20	—	20	—	25	—	ns
$\overline{OE}$ delay time from data input	t_{DZO}	0	—	0	—	0	—	ns
$\overline{CAS}$ delay time from data input	t_{DZC}	0	—	0	—	0	—	ns
Transition time (rise/fall)	t_T	3	50	3	50	3	50	ns
Refresh cycle	t_{REF}	—	8	—	8	—	8	ms
Refresh cycle (L version)	t_{REF}	—	128	—	128	—	128	ms

Note: Measuring Conditions (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0V)
Input rise and fall time = 5 ns
Input timing reference level = 2.4 V, 0.8 V

Output load = 2 TTL + C_L (100 pF) (including jig and scope)

Table 5.7 Bus Timing (Read)

		HM514260A-7 HM51S4260A-7		HM514260A-8 HM51S4260A-8		HM514260A-10 HM51S4260A-10		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns
Access time from address	t_{AA}	—	35	—	40	—	45	ns
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns
Read command hold time (for $\overline{CAS}$)	t_{RCH}	0	—	0	—	0	—	ns
Read command hold time (for $\overline{RAS}$)	t_{RRH}	0	—	0	—	0	—	ns
Column address/$\overline{RAS}$ read time	t_{RAL}	35	—	40	—	45	—	ns
Output buffer turn-off time	t_{OFF1}	0	15	0	15	0	20	ns
Output buffer turn-off time (for $\overline{OE}$)	t_{OFF2}	0	15	0	15	0	20	ns
$\overline{CAS}$/data input delay time	t_{CDD}	15	—	15	—	20	—	ns

Table 5.8 Bus Timing (Write)

		HM514260A-7 HM51S4260A-7		HM514260A-8 HM51S4260A-8		HM514260A-10 HM51S4260A-10		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns
Write command hold time	t_{WCH}	15	—	15	—	20	—	ns
Write command pulse width	t_{WP}	10	—	10	—	20	—	ns
Write command/$\overline{RAS}$ read time	t_{RWL}	20	—	20	—	25	—	ns
Write command/$\overline{CAS}$ read time	t_{CWL}	20	—	20	—	25	—	ns
Data input setup time	t_{DS}	0	—	0	—	0	—	ns
Data input hold time	t_{DH}	15	—	15	—	20	—	ns
$\overline{CAS}$/$\overline{OE}$ delay time	t_{COD}	—	0	—	0	—	0	ns

Table 5.9 Bus Timing (Refresh)

		HM514260A-7 HM51S4260A-7		HM514260A-8 HM51S4260A-8		HM514260A-10 HM51S4260A-10		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
$\overline{CAS}$ setup time ($\overline{CAS}$ before $\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns
$\overline{RAS}$ precharge/$\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns
Normal mode/$\overline{CAS}$ precharge time	t_{CPN}	10	—	10	—	10	—	ns

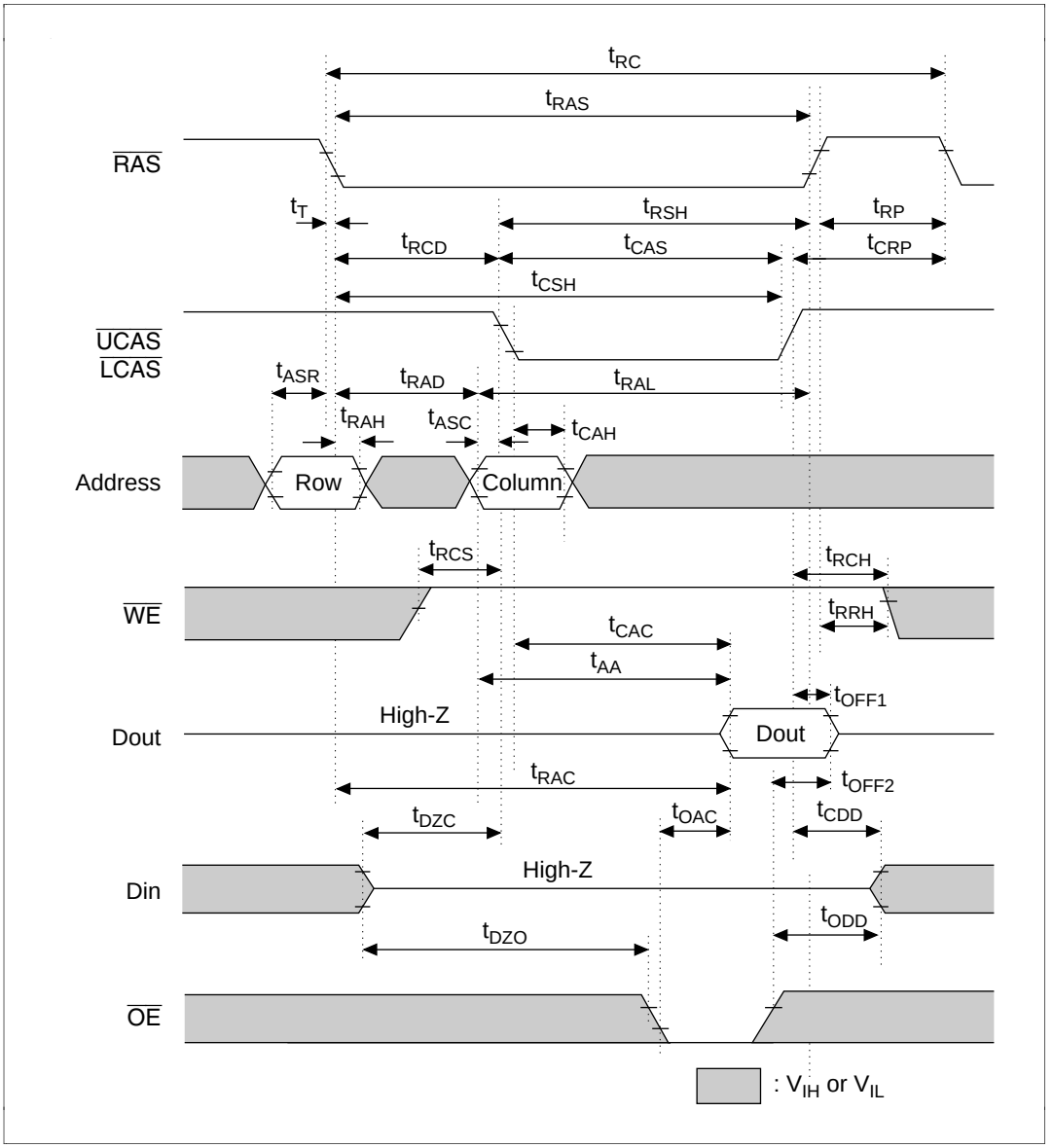


Figure 5.9 HN5116640 Timing Waveforms (Read)

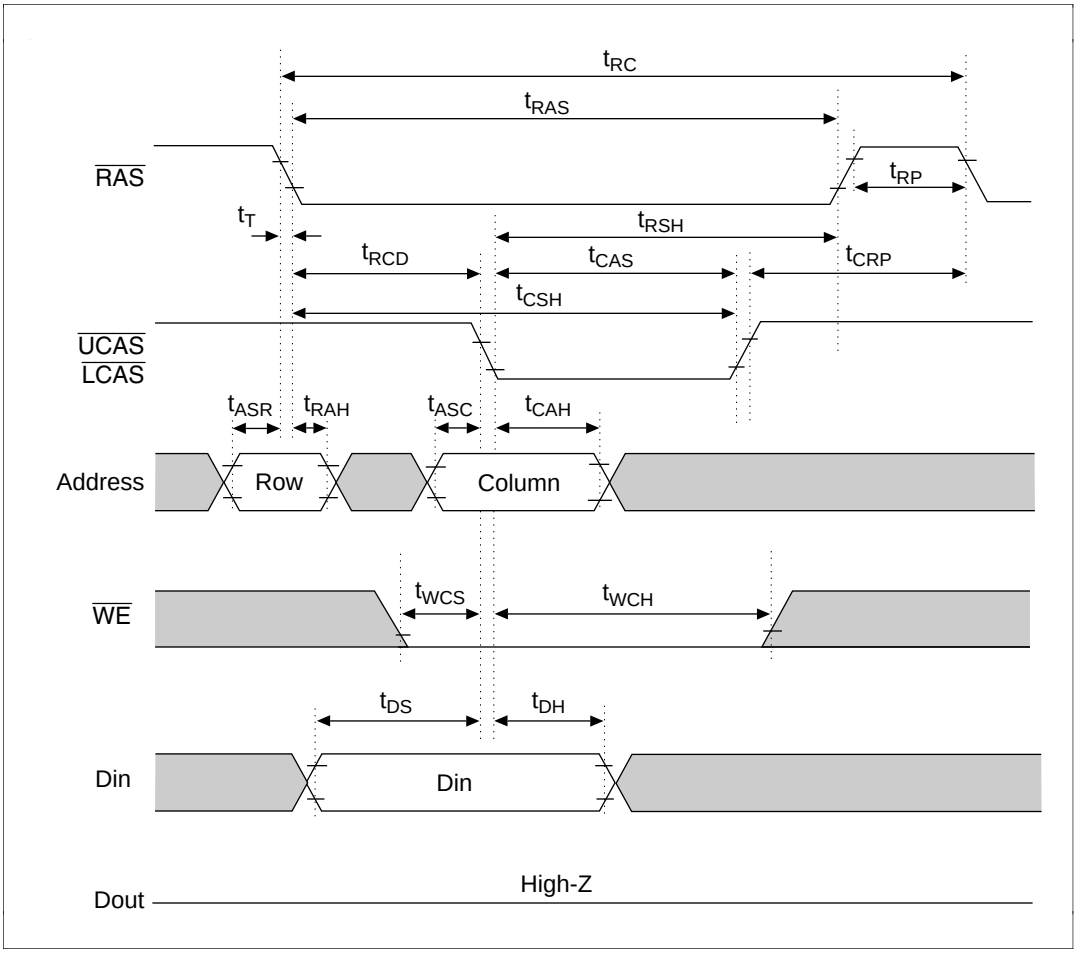


Figure 5.10 HN5116640 Timing Waveforms (Write)

Section 6 Peripheral LSI AC Characteristics

6.1 HD63310RP20 AC Characteristics

Table 6.1 Bus Timing

Number	Item		Symbol	HD63310RP20 Min	HD63310RP20 Max	Units
1	Address setup time (A0–A9)		t_{AS}	0	—	ns
2	Address hold time (A0–A9)		t_{AH}	0	—	ns
3	Address setup time (RS)		t_{ASRS}	0	—	ns
4	Address hold time (RS)		t_{AHRS}	15	—	ns
5	Address setup time (AS)		t_{ASAS}	40	—	ns
6	Address hold time (AS)		t_{AHAS}	0	—	ns
7	$\overline{AS}$ input Low pulse width		t_{ASLW}	40	—	ns
8	$\overline{AS}$ setup time		t_{ASS}	0	—	ns
9	$\overline{READY}$ delay time (during read)		t_{RYRD}	—	*1	ns
10	$\overline{READY}$ release time (during read)		t_{RYRH}	0	60	ns
11	Data output delay time	Direct addressing mode	t_{DDR}	—	120	ns
		Indirect addressing/FIFO mode		—	170	ns
11A	Access time *2	Direct addressing mode	t_{ACC}	—	200	ns
		Indirect addressing/FIFO mode		—	250	ns
12	Data output hold time		t_{DHR}	10	—	ns
13	Data output 3-state off time		t_{DTOF}	—	60	ns
14	Data output 3-state on time		t_{DTON}	—	60	ns
15	$\overline{READY}$ delay time (during write)		t_{RYWD}	—	*1	ns
16	$\overline{READY}$ release time (during write)		t_{RYWH}	0	60	ns
17	Data input setup time		t_{DSW}	60	—	ns
18	Data input hold time		t_{DHW}	0	—	ns

Table 6.1 Bus Timing (cont)

Number	Item		Symbol	HD63310RP20 Min	HD63310RP20 Max	Units
19	$\overline{RDS}$ hold time	Direct addressing mode	t_{RDSH}	120	—	ns
		Indirect addressing/FIFO mode		170	—	ns
20	$\overline{WRS}$ hold time	Other than FIFO mode	t_{WRSH}	120	—	ns
		During FIFO mode		170	—	ns
21	$\overline{RDS}$ recovery time		t_{RRC}	70	—	ns
22	$\overline{WRS}$ recovery time		t_{WRC}	70	—	ns
23	$\overline{RDS} \times \overline{WRS}$ recovery time		t_{RWRC}	70	—	ns
24	$\overline{WRS} \times \overline{RDS}$ recovery time		t_{WRRC}	70	—	ns

Notes: 1. The READY signal is for synchronization, and the output delay time varies according to the access request state of both ports. For example, if a read request is sent out from two ports simultaneously, one waits for request accepted, a wait is generated, and READY assert is late.

2. Timing when two ports are not accessed simultaneously.

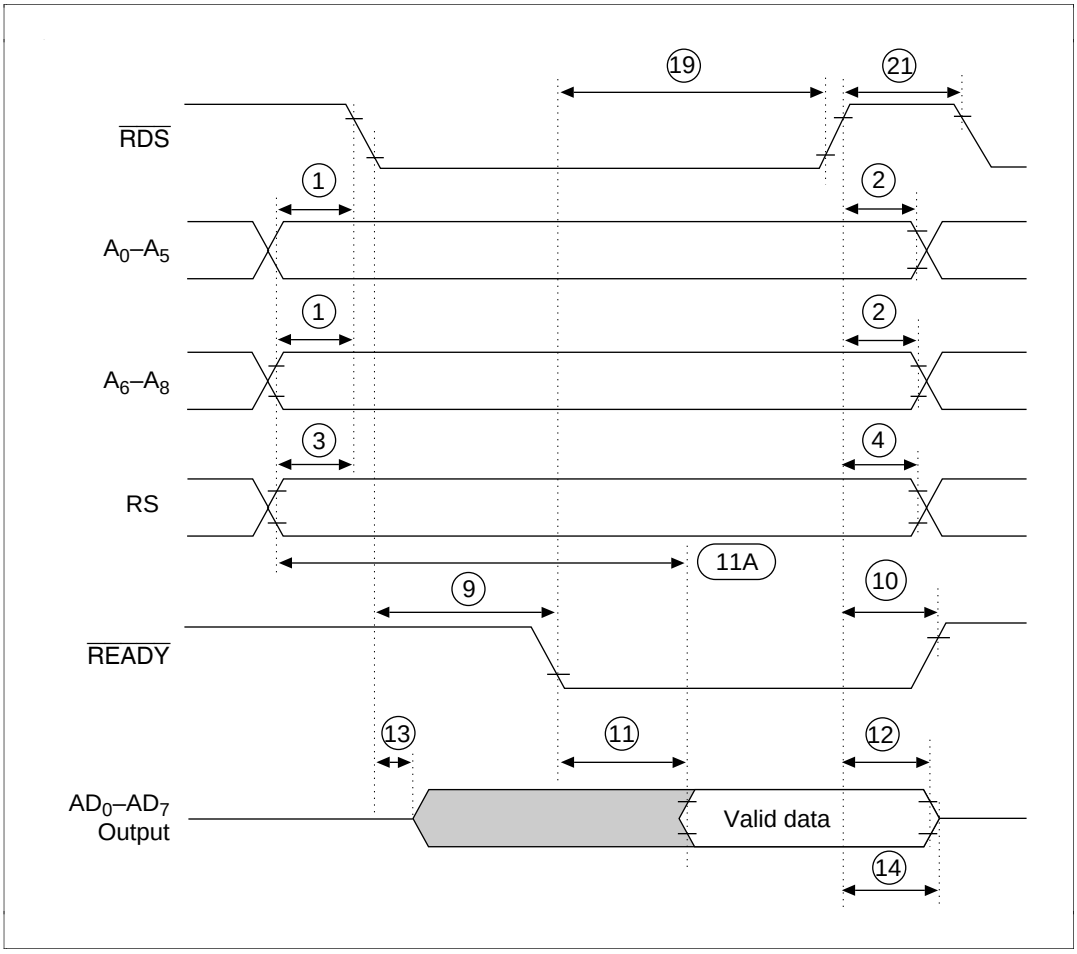


Figure 6.1 Timing Waveforms (Read)

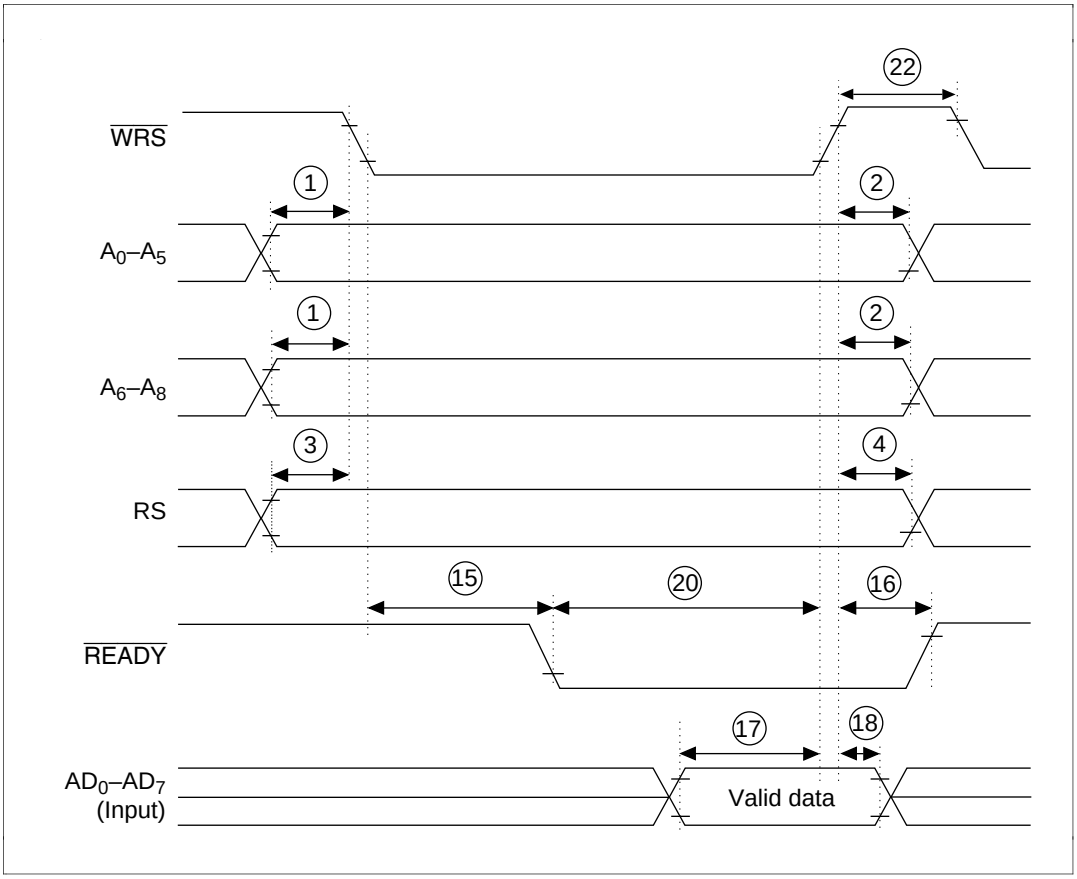


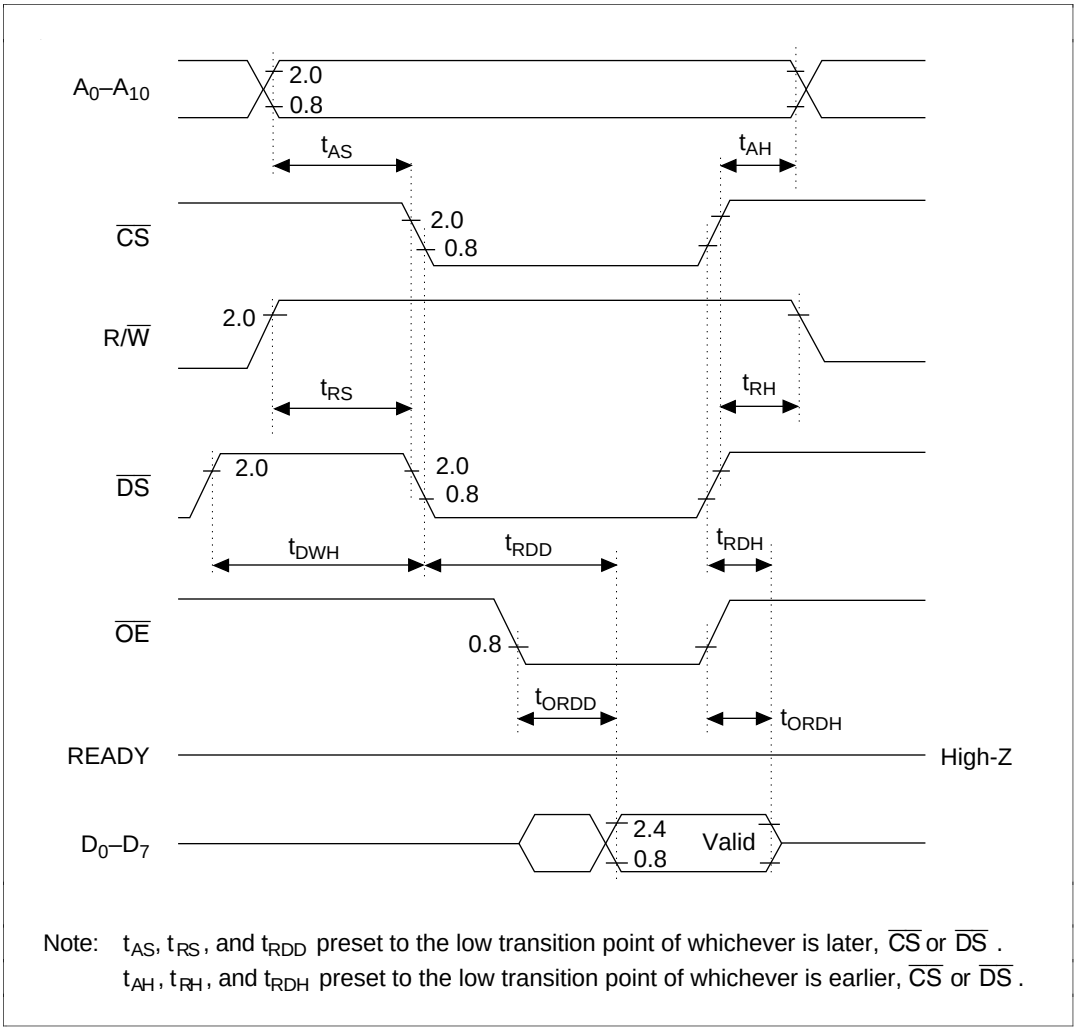
Figure 6.2 Timing Waveforms (Write)

6.2 HD63143 AC Characteristics

Table 6.2 Bus Timing

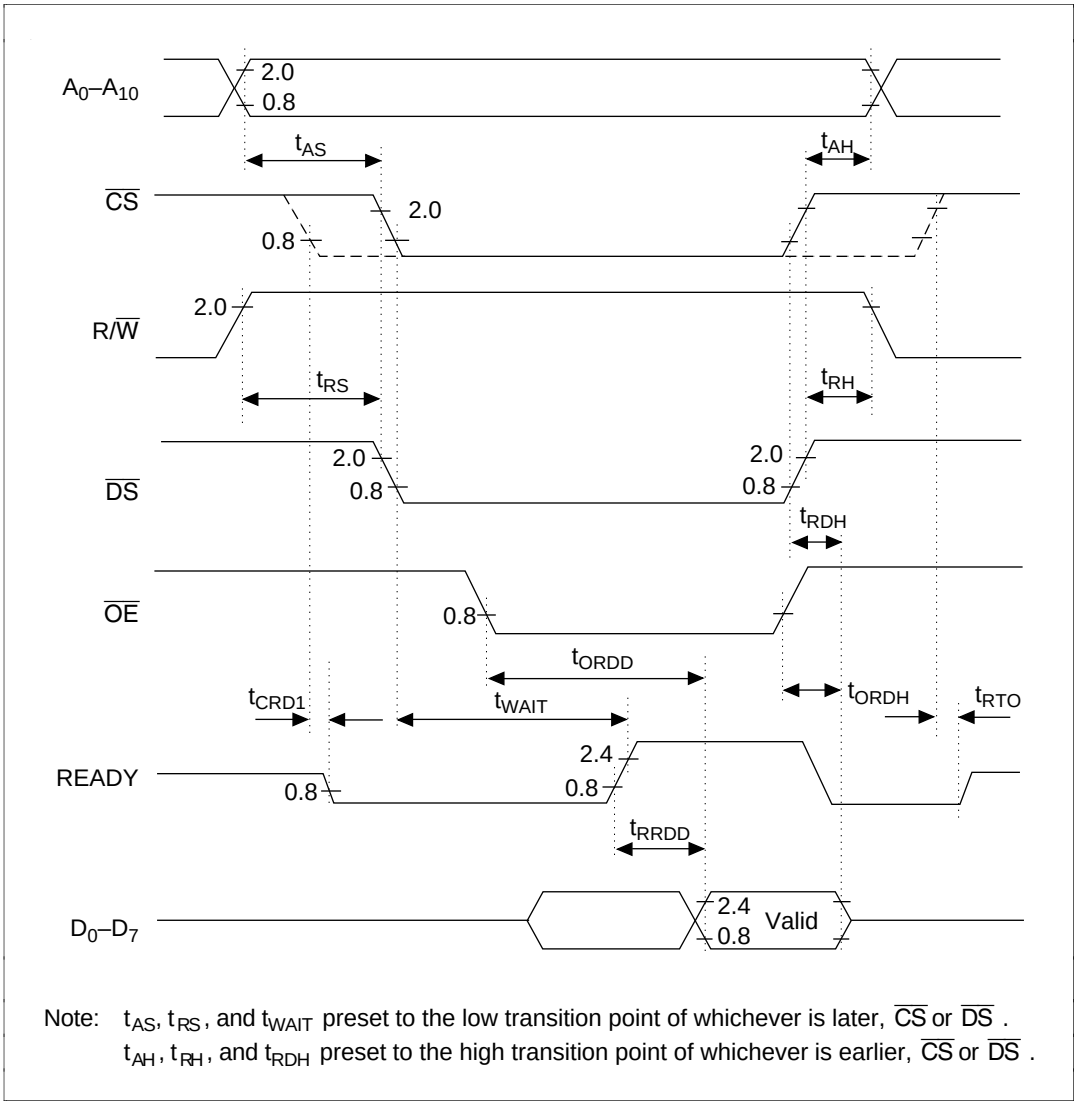
Item		Symbol	Min	Typ	Max	Units
Oscillator stable time		t_{RC}	—	—	20	ms
Operating frequency		f_{opr}	1.0	—	4.0	MHz
Output clock frequency		f_{CLK}	—	$f_{opr} \times 2$	—	MHz
Output clock high level pulse width		t_{CWH}	55	—	—	ns
Output clock low level pulse width		t_{CWL}	55	—	—	ns
Output clock rise time		t_{Cr}	—	—	10	ns
Output clock fall time		t_{Cf}	—	—	10	ns
Address setup time		t_{AS}	30	—	—	ns
Address hold time		t_{AH}	5	—	—	ns
Delay time from $\overline{CS}$ low to READY low (excluding RAM)		t_{CRD1}	—	—	60	ns
Delay time from $\overline{DS}$ low to READY high	UDR (UPC)*	t_{WAIT}	—	—	3	µs
	Others		—	—	750	ns
Delay time from $\overline{DS}$ high to READY low		t_{CRD2}	—	—	80	ns
$\overline{DS}$ high pulse width		t_{DWH}	80	—	—	ns
R/W setup time		t_{RS}	10	—	—	ns
R/W hold time		t_{RH}	5	—	—	ns
Read data delay time (RAM)		t_{RDD}	—	—	140	ns
Delay time from READY high to read data		t_{RRDD}	—	—	60	ns
Delay time from $\overline{OE}$ to read data		t_{ORDD}	—	—	80	ns
Read data hold time		t_{RDH}	10	—	—	ns
Time from $\overline{OE}$ high to read data hold		t_{ORDH}	10	—	—	ns
Write data delay time		t_{WDD}	—	—	120	ns
Write data setup time		t_{WDS}	100	—	—	ns
Write pulse hold time from READY high		t_{WH}	120	—	—	ns
Write pulse low width (RAM)		t_{WWL}	100	—	—	ns
Write data hold time		t_{WDH}	5	—	—	ns
READY turn-off time from $\overline{CS}$ high		t_{RTO}	—	—	50	ns

Note: Inverse proportion to f_{opr} when f_{opr} = 4 MHz.



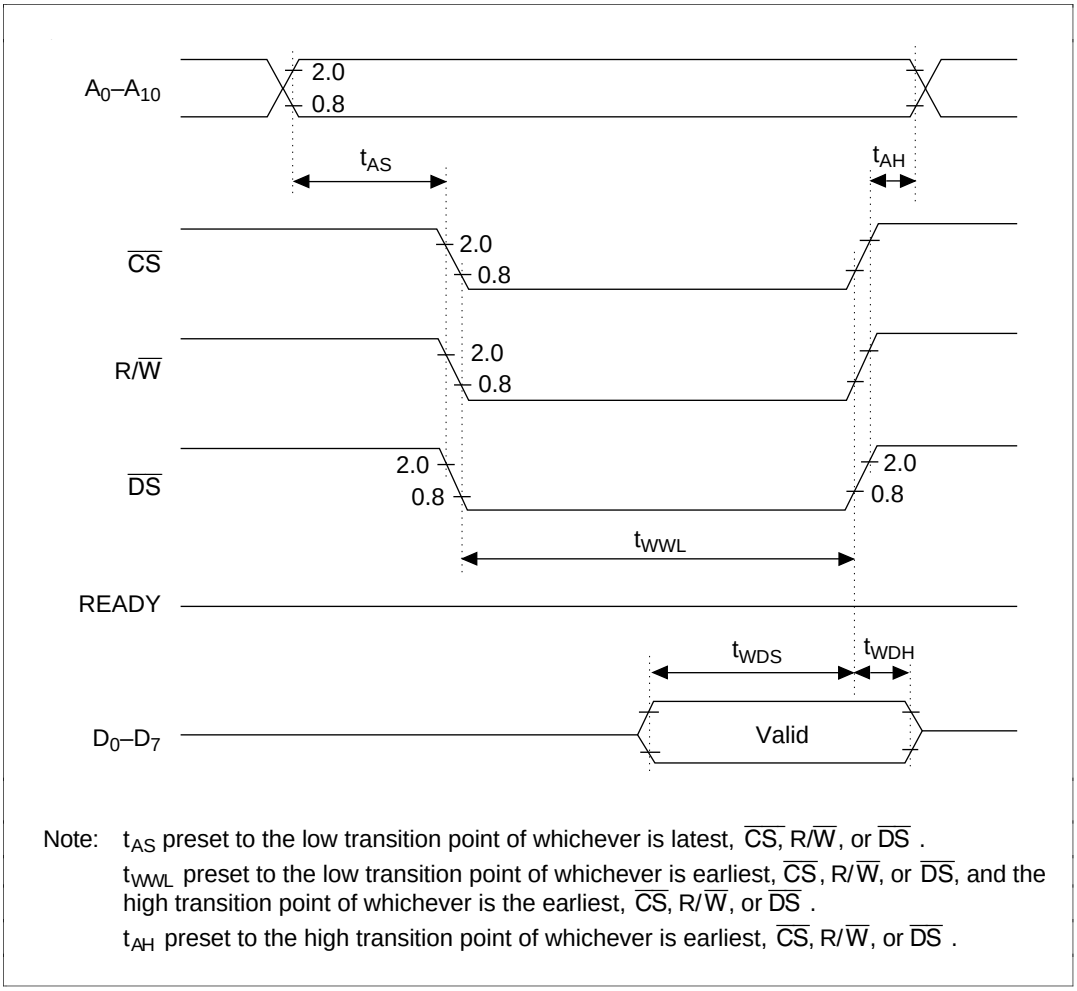
Note: t_{AS}, t_{RS}, and t_{RDD} preset to the low transition point of whichever is later, $\overline{CS}$ or $\overline{DS}$.
t_{AH}, t_{RH}, and t_{RDH} preset to the low transition point of whichever is earlier, $\overline{CS}$ or $\overline{DS}$.

Figure 6.3 Timing Waveforms (RAM Read)



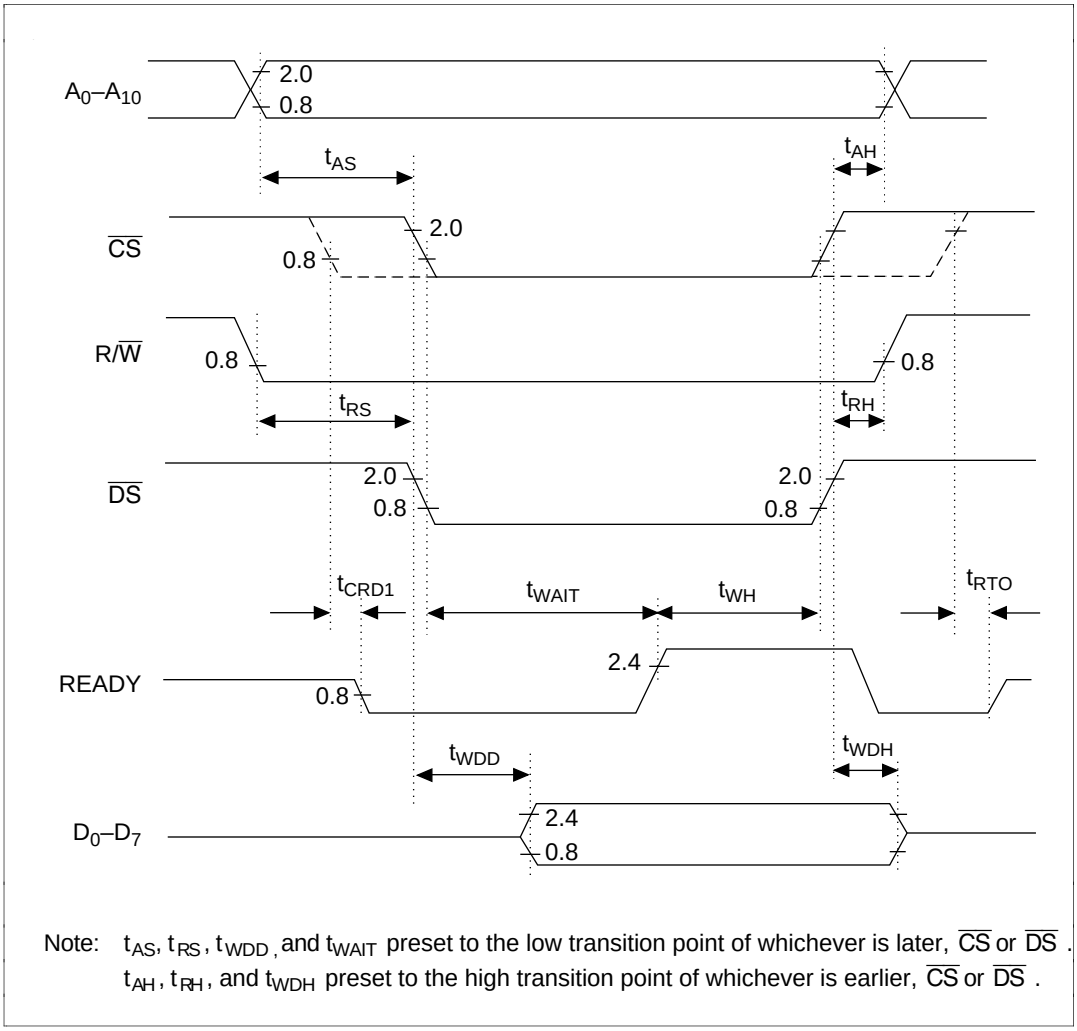
Note: t_{AS}, t_{RS}, and t_{WAIT} preset to the low transition point of whichever is later, $\overline{CS}$ or $\overline{DS}$.
t_{AH}, t_{RH}, and t_{RDH} preset to the high transition point of whichever is earlier, $\overline{CS}$ or $\overline{DS}$.

Figure 6.4 Timing Waveforms (Read other than RAM)



Note: t_{AS} preset to the low transition point of whichever is latest, $\overline{CS}$, R/$\overline{W}$, or $\overline{DS}$.
t_{WWL} preset to the low transition point of whichever is earliest, $\overline{CS}$, R/$\overline{W}$, or $\overline{DS}$, and the high transition point of whichever is the earliest, $\overline{CS}$, R/$\overline{W}$, or $\overline{DS}$.
t_{AH} preset to the high transition point of whichever is earliest, $\overline{CS}$, R/$\overline{W}$, or $\overline{DS}$.

Figure 6.5 Timing Waveforms (RAM Write)



Note: t_{AS}, t_{RS}, t_{WDD}, and t_{WAIT} preset to the low transition point of whichever is later, $\overline{CS}$ or $\overline{DS}$.
t_{AH}, t_{RH}, and t_{WDH} preset to the high transition point of whichever is earlier, $\overline{CS}$ or $\overline{DS}$.

Figure 6.6 Timing Waveforms (Write other than RAM)

6.3 TMP82C55AP-10 AC Characteristics

Table 6.3 Bus Timing

		AP-2/AM-2		AP-10/AM-10	
Symbol	**Item**	**Min**	**Max**	**Min**	**Max**
t_{AR}	Address setup time against $\overline{RD}$ falling edge	0	—	0	—
t_{RA}	Address hold time against $\overline{RD}$ rising edge	0	—	0	—
t_{RR}	$\overline{RD}$ pulse width	160	—	150	—
t_{RD}	Delay time from $\overline{RD}$ falling edge to definite data output	—	140	—	100
t_{DF}	Time from $\overline{RD}$ rising edge until data bus floating	0	40	0	40
t_{RV}	Time from $\overline{RD}$ or $\overline{WR}$ rising edge to the next $\overline{RD}$/$\overline{WR}$ rising edge	200	—	150	—
t_{AW}	Address setup time against $\overline{WR}$ falling edge	0	—	0	—
t_{WA}	Address hold time against $\overline{WR}$ rising edge	0	—	0	—
t_{WW}	$\overline{WR}$ pulse width	120	—	120	—
t_{DW}	Bus data setup time against $\overline{WR}$ rising edge	100	—	100	—
t_{WD}	Bus data hold time against $\overline{WR}$ rising edge	0	—	0	—
t_{WB}	Time from $\overline{WR}$ rising edge to definite data output	—	350	—	350
t_{IR}	Port data setup time against $\overline{RD}$ falling edge	0	—	0	—
t_{HR}	Port data hold time against $\overline{RD}$ rising edge	0	—	0	—
t_{AK}	$\overline{ACK}$ pulse width	300	—	300	—
t_{ST}	$\overline{STB}$ pulse width	350	—	350	—
t_{PS}	Port data setup time against $\overline{STB}$ rising edge	0	—	0	—
t_{PH}	Port data hold time against $\overline{STB}$ rising edge	150	—	150	—
t_{AD}	Time from $\overline{ACK}$ falling edge to definite data output	—	300	—	300
t_{KD}	Time from $\overline{ACK}$ rising edge until port (mode 2, port A) is floating	25	250	20	250
t_{WOB}	Delay time from $\overline{WR}$ rising edge to $\overline{OBF}$ falling edge	—	300	—	300
t_{AOB}	Delay time from $\overline{ACK}$ falling edge to $\overline{OBF}$ rising edge	—	350	—	350
t_{SIB}	Delay time from $\overline{STB}$ falling edge to IBF rising edge	—	300	—	300
t_{RIB}	Delay time from $\overline{RD}$ rising edge to IBF falling edge	—	300	—	300

Table 6.3 Bus Timing (cont)

Symbol	Item	AP-2/AM-2 Min	AP-2/AM-2 Max	AP-10/AM-10 Min	AP-10/AM-10 Max
t_{RIT}	Delay time from $\overline{RD}$ falling edge to INTR falling edge	—	400	—	400
t_{SIT}	Delay time from $\overline{STB}$ rising edge to INTR rising edge	—	300	—	300
t_{AIT}	Delay time from $\overline{ACK}$ rising edge to INTR rising edge	—	350	—	350
t_{WIT}	Delay time from $\overline{WR}$ falling edge to INTR falling edge	—	450	—	450

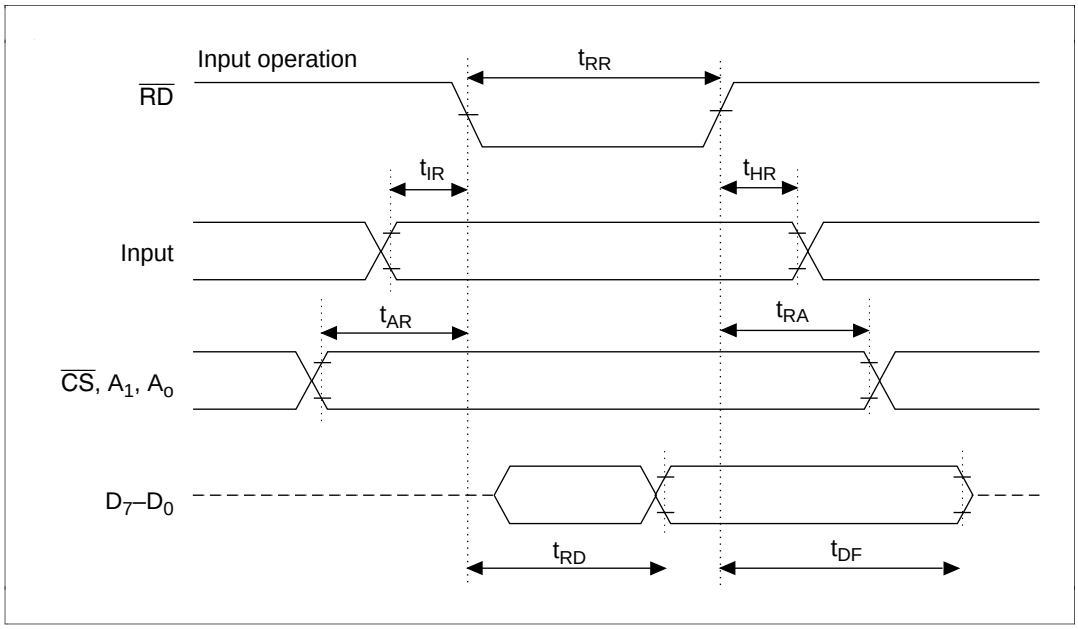


Figure 6.7 Timing Waveforms (Read)

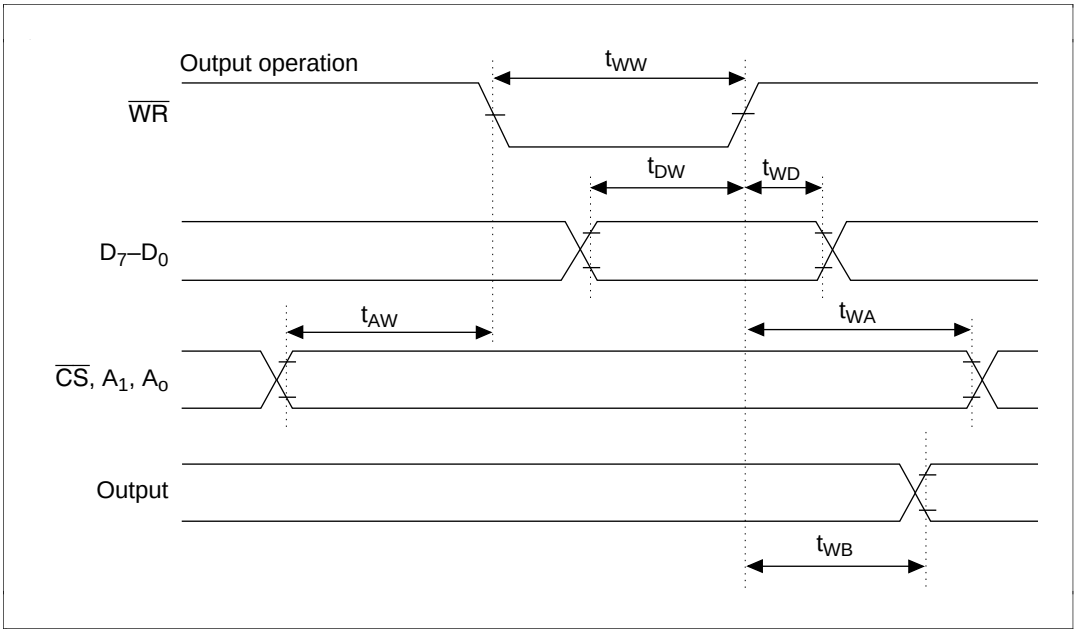


Figure 6.8 Timing Waveforms (Write)

6.4 HD64610 AC Characteristics

Unless otherwise specified: V_{CC} = 5 V ±10%, V_{SS} = 0 V, Ta = –20 to +75°C (normal specification), Ta = –40 to +85°C (wide temperature range specification).

Table 6.4 Bus Timing (Read)

Item	Symbol	Min	Max	Units
Read cycle time	t_{RC}	85	—	ns
Address access time	t_{AA}	—	85	ns
Chip select access time	t_{ACS}	—	85	ns
Output enable access time	t_{OE}	—	45	ns
Output hold time	t_{OH}	10	—	ns
Chip select/output set time	t_{CLZ}	10	—	ns
Output enable/output set time	t_{OLZ}	5	—	ns
Chip deselect/output floating	t_{CHZ}	0	35	ns
Output disable/output floating	t_{OHZ}	0	35	ns

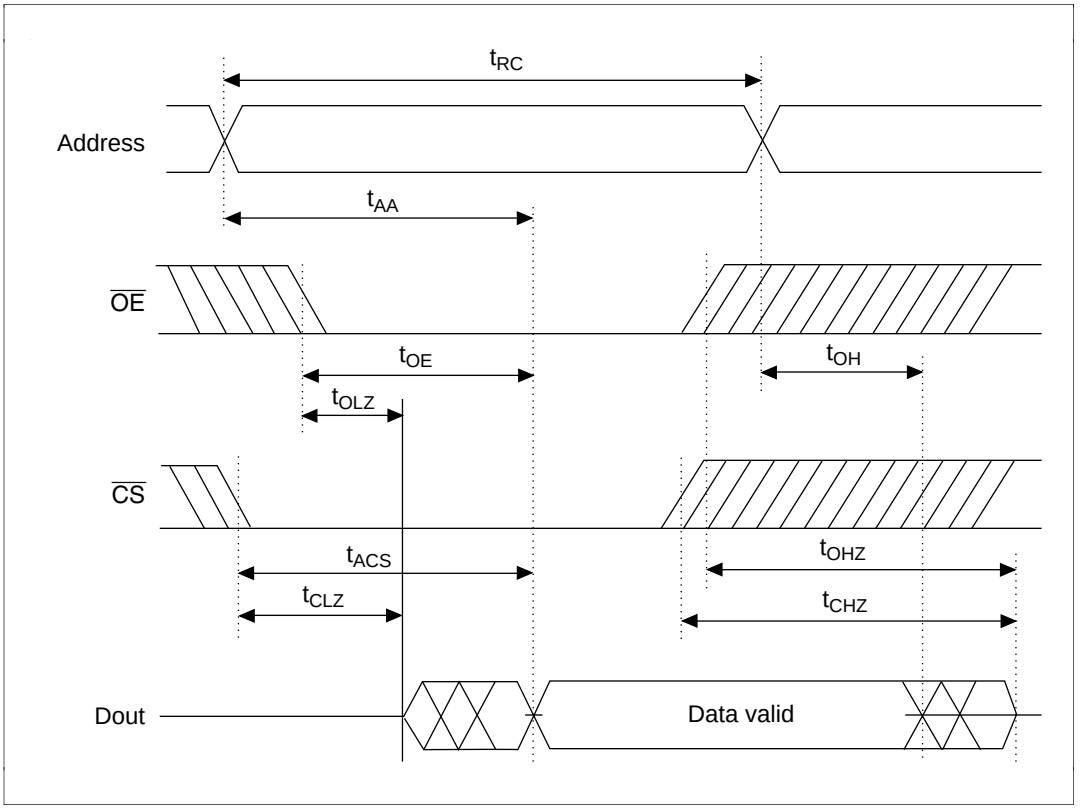
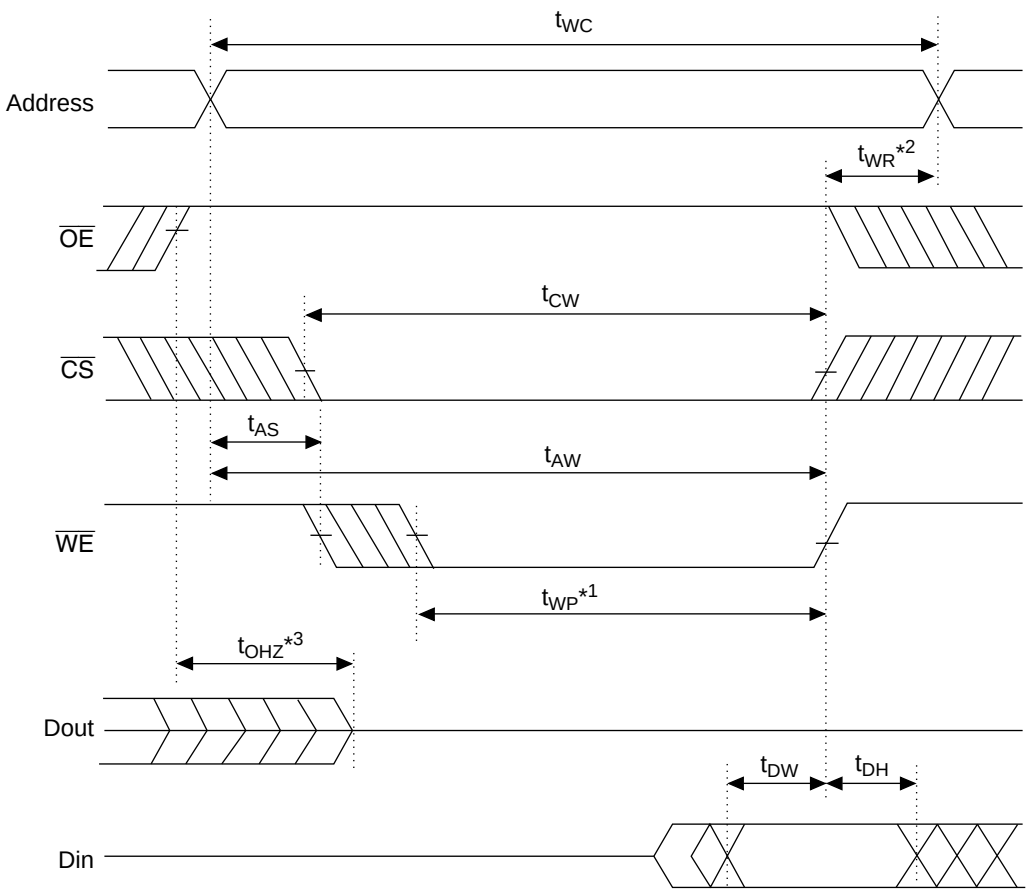


Figure 6.9 Timing Waveforms (Read)

Table 6.5 Bus Timing (Write)

Item	Symbol	Min	Max	Units
Write cycle time	t_{WC}	85	—	ns
Chip select time	t_{CW}	75	—	ns
Address valid time	t_{AW}	75	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse width	t_{WP}	60	—	ns
Address hold time	t_{WR}	10	—	ns
WE/output floating	t_{WHZ}	0	35	ns
Input data set time	t_{DW}	40	—	ns
Input data hold time	t_{DH}	0	—	ns
Output disable/output floating	t_{OHZ}	0	35	ns
WE/output set time	t_{OW}	5	—	ns



Notes: 1. Write operation conducted in the overlap (t_{WP}) between $\overline{CS}$ = low and $\overline{WE}$ = low.

2. t_{WR} measured from the high transition point of whichever is earlier ($\overline{CS}$ or $\overline{WE}$) to the end of the write cycle.

3. I/O pin is in output state during this period. Input signals must not apply an inverse phase to that of the output.

Figure 6.10 Timing Waveforms (Write)

6.5 LM032L AC Characteristics

Table 6.6 Bus Timing

Item	Symbol	Min	Typ	Max	Units
Enable cycle time	t_{cyc}	1.0	—	—	µs
Enable pulse width	PW_{EH}	450	—	—	ns
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25	ns
RS and R/W setup time	t_{AS}	140	—	—	ns
Data delay time	t_{DDR}	—	—	320	ns
Data setup time	t_{DSW}	195	—	—	ns
Hold time	t_H	20	—	—	ns

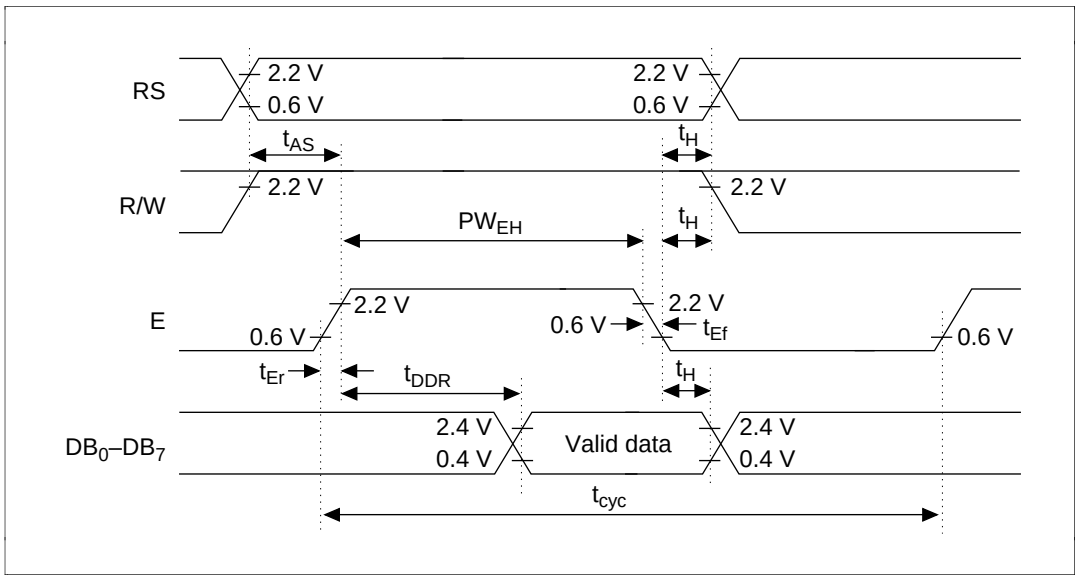


Figure 6.11 Timing Waveforms (Read)

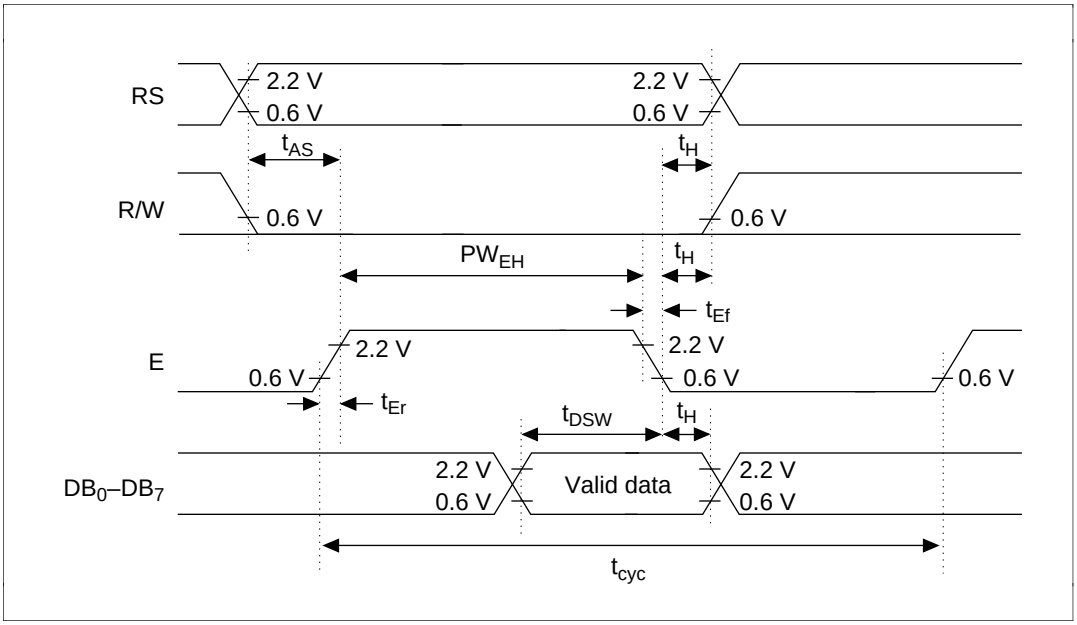


Figure 6.12 Timing Waveforms (Write)