Hitachi America, Ltd.

TN-0224

Application Engineering
TechNote

Cristian Tomescu

H8/300H Instruction Timing

In order to obtain an accurate estimate of a particular CPU performance in terms of the execution speed of a particular task or function, the following 2 factors need to be considered:

1. The instruction fetch and execution time.
2. Any overhead CPU and/or On-chip Module delays such as interrupt latency time, DMA latency time, A/D or D/A conversion times, and serial bit rates.

This technote will discuss how the H8/300H CPU performs in terms of instruction fetch and execution only. The H8/300H CPU uses a 16-bit word instruction set. In general, the time it takes a particular instruction to be executed is determined by the system clock speed, the instruction fetch time, and the instruction execution time. The H8/300H can run at a maximum internal clock rate of 16MHz, which translates into a minimum clock cycle of 62.5ns. The instruction fetch time depends upon where the instruction is located, the number of words in the instruction, and the data path width from that location to the CPU. An instruction can be located either in on-chip memory (ROM or RAM) or in external memory. The on-chip memory modules are always accessed in 2 clock cycles (either byte or word) via an internal 16-bit wide data path. External memory can be accessed as fast as 2 clock cycles via an external 16-bit data bus, but it depends upon how fast the external memory devices can perform the data transfer as well as the size of these devices (8 or 16-bit). In order to accomodate for these situations, the H8/300H has a built-in Bus Controller module that can "slow down" the external data access to 3 clock cycles plus any additional wait states that may be needed. Also, the Bus Controller can be set for either 8-bit or 16-bit data path to match the size of the external memory device. Table A-2 in Appendix A of the H8/3003 Hardware Manual indicates the number of clock states per instruction fetch cycle for all access conditions explained above. Table A-3 in the same appendix indicates the number of instruction fetch cycles for each type of instruction.

Example 1 - instruction is accessed from the on-chip RAM:

Instruction	Hex code	# words	x	# clocks/16 bits	=	Fetch time
MOV.B R0L,@H'00FFD4	38D4	1		2		2 clocks

Example 2 - instruction is accessed from off-chip memory in a 3-state access and via an 8-bit data bus (m = number of wait states induced in the cycle):

Instruction	Hex code	# words	x	# clocks/8 bits	=	Fetch time
MOV.B R0L,@H'00FFD4	38D4	1		6+2m		6+2m

The instruction execution time depends upon the type of operation, the data path width, and the access timing to the destination location. The H8/300H has 5 types of instruction operations that determine the number of additional cycles to be added to the instruction fetch cycle for each type of instruction and addressing mode.

1. Branch Address Read: indicates the number of cycles needed to fetch the destination address during an 8-bit indirect jump or jump to subroutine (JMP, JSR @@aa:8), or during the execution of a TRAP instruction.
2. Stack Operation: indicates additional cycles needed for incrementing or decrementing the stack pointer and storing the program counter and CCR on the stack (jump/branch to subroutine instructions).
3. Byte Data Access: indicates the time required to obtain non-immediate (or indirect) 8-bit data or address locations.

4. Word Data Access: indicates the time required to obtain non-immediate (or indirect) 16, 24, or 32-bit data or address locations.
5. Internal Operation: indicates additional cycles needed for arithmetic address or data calculations.

The instruction execution time takes into account each of the above operations (see table A-3 again). In addition, the bus width (8 or 16-bits wide) and the number of clock states per access to the destination is a determinig factor in the instruction execution time (see table A-2 again). The total instruction time is the sum of the instruction fetch time plus any additional cycle time needed to complete the instruction execution, and is calculated by using the formula:

Instruction time = $IxS_I + JxS_J + KxS_K + LxS_L + MxS_M + NxS_N$

I, J, K, L, M, N, and S refer to the number of instruction fetch and execution cycles for each instruction. S_I, S_J, S_K, S_L, S_M, and S_N refer to the number of states required per cycle according to the bus size.

Example 3 - instruction is accessed from on-chip memory and the destination is an on-chip peripheral register:

MOV.L ER0,@H'00FF2F

From table A-3: I=M=2. From table A-2: S_I=2 and S_M=3 (there is a 16-bit data path to the peripheral register).

Instruction time = $IxS_I + MxS_M$ = 2x2 + 2x3 = 10 clock states.

Example 4 - instruction is accessed from off-chip memory via an 8-bit bus, 3-state access with 1 wait state, and the destination is a CPU register:

MOV.L #H'005000,@-ER0

From table A-3: I=M=N=2. From table A-2: S_I= 6+2x1= 8, S_M= 6+2x1=8, and S_N= 1.

Instruction time = $IxS_I + MxS_M + NxS_N$ = 2x8 + 2x8 + 2x1 = 34 clock states.

HITACHI
Hitachi America, Ltd. • San Francisco Center • 2000 Sierra Point Parkway • Brisbane, CA 94005-1819 • (415) 589-8300