Hitachi America, Ltd.

TN-0230

Application Engineering
TechNote

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Serial Port Expansion for the H8/300 family

The Serial Communications Interface (SCI) is a fairly standard feature on the H8/300 family of Microprocessors. This feature facilitates the easy transfer of data between processors and a wide range of peripheral devices. Data may be transferred in ether synchronous or asynchronous modes. One of the major advantages to this interface is the simple three wire hardware connection.

This application note gives two schematics that illustrate a way to expand the processor with additional parallel ports using the serial port. The advantage is the ability to read and write to a parallel port located some distance from the main processor's physical location. This eliminates long transmission lines and problems with skew across a long parallel bus. Some applications that could use the input scheme would be remote key pads and keyboards. These applications would produce an eight bit parallel data pattern with a data ready strobe.

The schematic shown in diagram A is a simple example of the external interface required for the input circuit. The data is input (loaded) into U3 with a Kybd Strobe and then serially clocked out from U3 through U4 into the processor on SCI Data. This operation is synchronized by the SCI Clk to insure proper timing for the set-up and hold of the SCI interface. This circuit will present a stream of 1's with SCI clock running until data is loaded with the key board strobe. Then the serial data is clocked into the microprocessor. A software routine then can be looking for data at the SCI register and input the data for use in the processor. Care must be used in this routine to avoid sending "repeat" characters during the clocking cycle.

This input scheme can be useful in an application such as a remote key pad entry system such as in security systems. Another could be the remote setting of temperature for control of air conditioner and heating systems.

The schematic shown in diagram B is a simple method of decoding the serial data stream into an eight bit latched parallel port. This output decode would be useful sending ASCII code to a remote device that requires a parallel input. The circuit is designed to clock data into U2 serially based on the proper timing of the SCI bus. If 1's are transmitted to the shift register U2 pin 13 will toggle causing U6 to toggle and thus enabling data transfer into U1 at the correct edge of SCI Clk. The data is held latched in U1. U7 is toggled causing a strobe to the target system and clearing U2 to all zero's. For this "feedback" to work properly the SCI port must be programmed to output 9 bit data patterns.

Some of the reasons to use these interfaces are the ability to produce/receive data at a reasonable distance over just three wire. This may be also useful to produce another parallel port right at the processor if all the other ports are being used. One draw back however is the speed is not really high and there is more software required than just using the other parallel ports.

Diagram A

Parallel Input Configuration

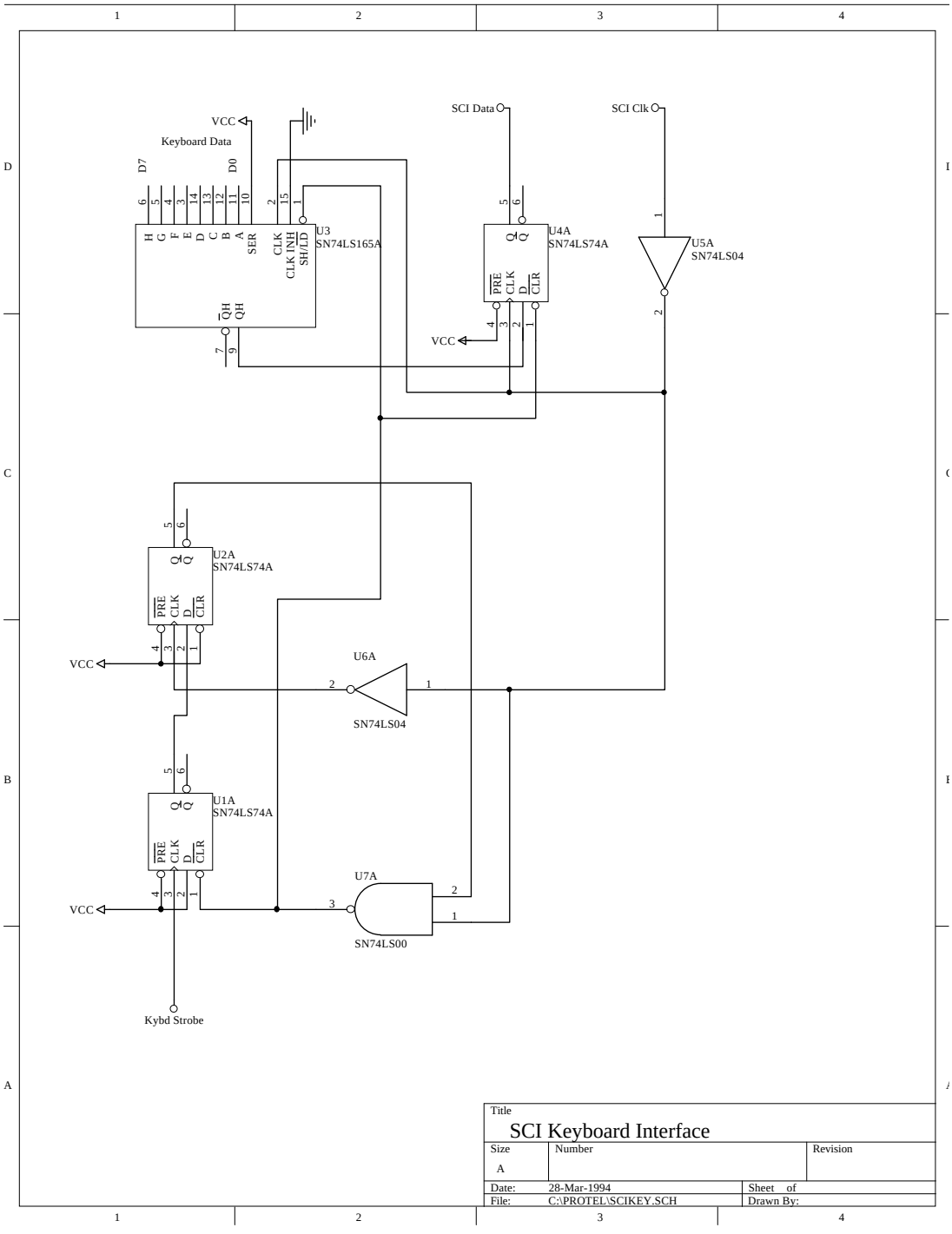

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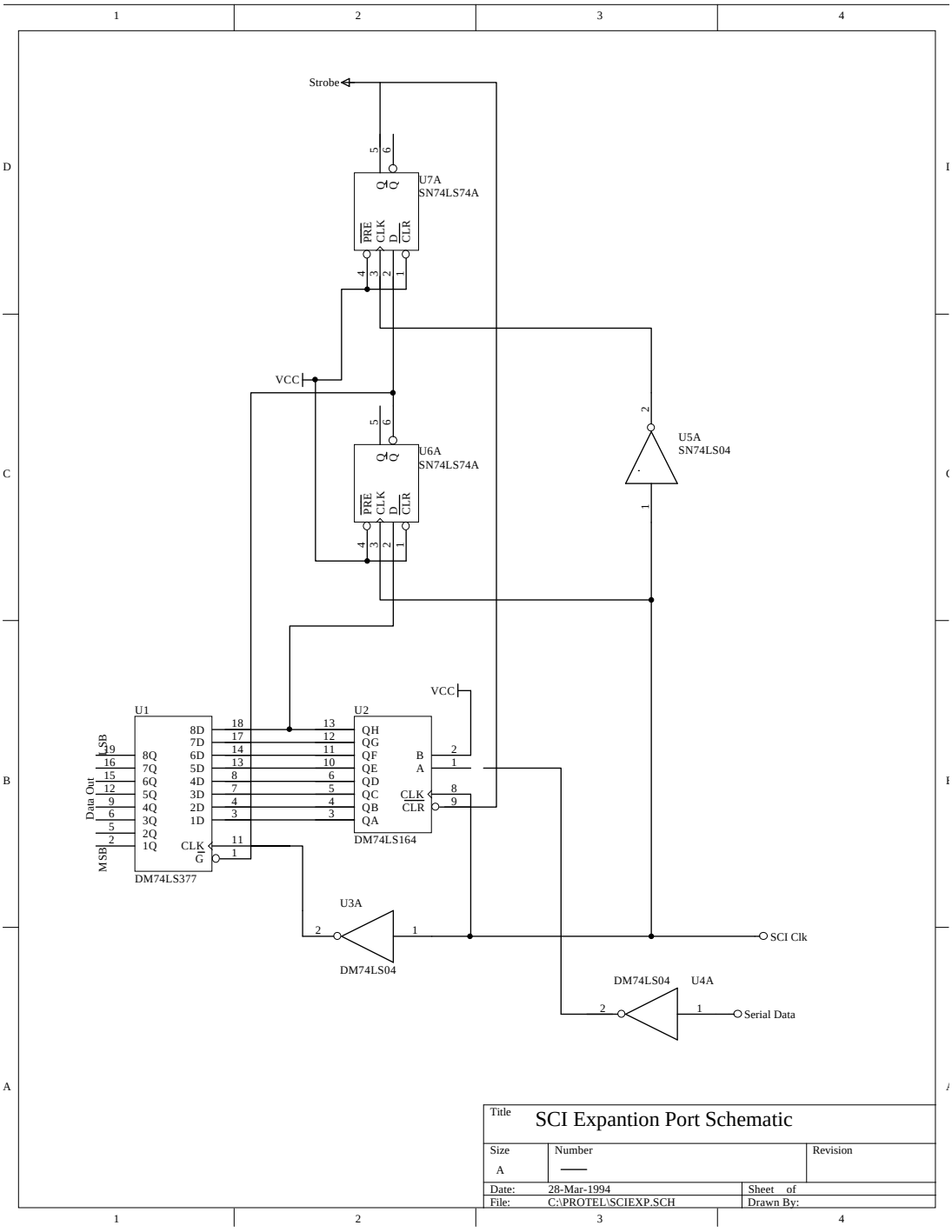
Diagram B

Parallel Output Port



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