Hitachi America, Ltd.

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Application Engineering
TechNote

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Servicing Interrupts in the H8/300 Family

Introduction

The H8/300 family can service 2 types of interrupts: externally requested and internally generated. The external interrupts are triggered through dedicated input pins, and they fall into 2 categories: non-maskable (NMI) and maskable (IRQn). Chapter 4 in the hardware manuals discuss in detail the conditions under which they enabled and recognized. The internal interrupts are generated from various on-chip peripheral modules such as the timers, SCI, and A/D, and they may or may not be recognized depending upon the state of their specifically assigned control bits. Please refer to the appropriate manual sections for more information.

Interrupt Servicing

In order for the external interrupt requests to be recognized, the corresponding control bits in the IER registers must be set to 1. For internal interrupt(s) to be generated, their respective enable control bit(s) must be set as well. All enabled interrupts will be accepted if the I-bit of the CCR is cleared (usually at the beginning of the program, and right after the stackpointer initialization). The accepted interrupts will be serviced according to the following 3 considerations:

1. If 2 or more interrupt requests occur simultaneously during the main program execution, they are always serviced in the order of priority shown in table 4-2 in the hardware manuals.
2. After an interrupt is accepted (after completion of the current instruction), the current contents of the program counter (PC) and the CCR are pushed onto the stack. The I-bit of the CCR is set to 1, thus inhibiting all subsequent interrupts from occuring. The PC is loaded with the contents in the corresponding interrupt vector location and program execution starts from the address location now present in the program counter. Any subsequent interrupt requests are held pending, and their execution is deferred until the current interrupt-generated routine is completed (and the I-bit is automatically cleared to 0). Level-sensed interrupts must remain low until they are acknowledged.
3. If the user clears the I-bit anytime during the execution of the current interrupt handling routine and prior to its completion, any requested (nested) interrupts will be serviced as soon as the current instruction is executed.

Figure 1 on the following page illustrates this process.

An internally-generated interrupt occurs when the event completion flag and its enable bit are both set. Using the A/D converter as an example, an end-of-conversion interrupt (ADI) is requested when both the end-of-conversion flag (ADF) and the A/D Interrupt enable bit (ADIE) are set to 1. However, the interrupt controller does not reset the event completion flag (in this case ADF) while the interrupt handling routine is being executed; the user must employ software commands to achieve that. If the flag bit is not reset, ADI interrupts will continously occur upon completion of the interrupt handling routine, and not upon end-of-conversion.

In addition and as a general precautionary rule, the interrupt-mask (I) bit must be set **before** any interrupt is disabled in order to avoid contention between interrupt disable and a request on the same interrupt occuring during the execution of the interrupt clearing instruction.

Also, any interrupt requests occuring during execution of CCR-specific instructions (LDC, STC, ANDC, ORC, and XORC) will be deferred until the next non-such instruction will be executed.

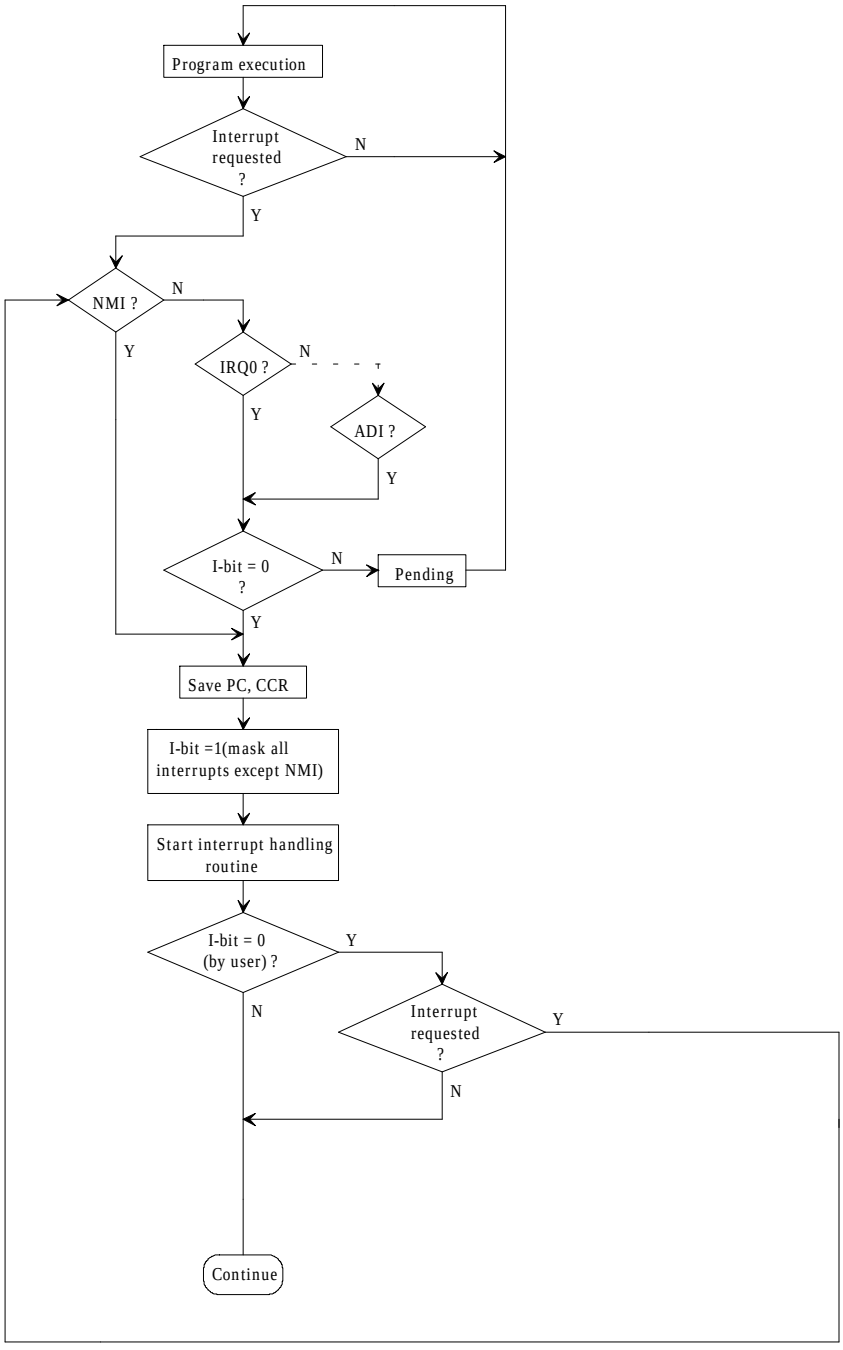

Figure 1. Interrupt Servicing Process.

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