

OMC952723055

H8/3614 Series

H8/3614
HD6473614, HD6433614
H8/3613
HD6433613
H8/3612
HD6433612

Hardware Manual

Preface

The H8/3614 Series of single-chip microcomputers has an H8/300L CPU core and a variety of peripheral functions needed in system configurations.

This manual describes the CPU architecture, peripheral functions, electrical characteristics, and package dimensions of the H8/3614 Series.

Refer to the H8/300L Series Programming Manual (ADE-602-040) for a detailed description of the instruction set.

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Section 1 Overview

1.1 Overview

The H8/300L Series is a series of single-chip microcomputers (MCU: microcomputer unit), built around the high-speed H8/300L CPU and equipped with peripheral system functions on-chip.

Within the H8/300L Series, the H8/3614 Series of microcomputers are equipped with five timers, a 14-bit pulse width modulator (PWM), two serial communication interface channels, an A/D converter, and other on-chip peripheral functions. The H8/3614 series includes three chips: the H8/3612, which has a 16-kbyte ROM and 512-byte RAM; the H8/3613, which has a 24-kbyte ROM and 1024-byte RAM; and the H8/3614, which has a 32-kbyte ROM and 1024-byte RAM. The H8/3612 does not have the 14-bit PWM.

The ZTAT™* versions of the H8/3614 come with user-programmable PROM on-chip.

Table 1-1 summarizes the main features of the H8/3614 Series.

Note: * ZTAT (zero turn around time) is a trademark of Hitachi, Ltd.

Table 1-1 Features

Item	Specification
CPU	<p>High-speed H8/300L CPU</p> <ul style="list-style-type: none">• General-register architecture General registers: Sixteen 8-bit registers (can be used as eight 16-bit registers)• Operating speed<ul style="list-style-type: none">— Max. operating speed: 4.19 MHz— Add/subtract: 0.5 μs (operating at ϕ = 4 MHz)— Multiply/divide: 3.5 μs (operating at ϕ = 4 MHz)— Can run on 32 kHz subclock• Instruction set compatible with H8/300 CPU<ul style="list-style-type: none">— Instruction length of 2 bytes or 4 bytes— Basic arithmetic operations between registers— MOV instruction for data transfer between memory and registers• Typical instructions<ul style="list-style-type: none">— Multiply (8 bits \times 8 bits)— Divide (16 bits \div 8 bits)— Bit accumulator— Register-indirect designation of bit position
Interrupts	<p>15 interrupt sources</p> <ul style="list-style-type: none">• Six external interrupt pins: $\overline{\text{IRQ}}_5$ to $\overline{\text{IRQ}}_0$• Nine internal interrupt sources
Low-power operation modes	<p>4 power-down modes</p> <ul style="list-style-type: none">• Sleep mode• Standby mode• Watch mode• Subactive mode
Clock oscillators	<p>Two on-chip clock oscillators</p> <ul style="list-style-type: none">• System clock oscillator: 1 to 8.4 MHz• Subclock oscillator: 32.768 kHz
I/O ports	<p>54 I/O pins</p> <ul style="list-style-type: none">• PMOS open-drain I/O pins: 6• Standard-voltage I/O pins: 38• Standard-voltage input pins: 10

Table 1-1 Features (cont)

Item	Specification
Timers	<p>Five on-chip timers</p> <ul style="list-style-type: none"> • Timer A: 8-bit interval timer Count-up timer with selection of eight internal clock signals divided from the system clock (ϕ)* and four clock signals divided from the subclock (ϕ_{SUB}) Operating on the subclock, timer A can provide a time base for timekeeping. • Timer B: 8-bit reload timer Count-up timer with selection of seven internal clock signals or event input from pin P1₀/IRQ₀ • Timer C: 8-bit reload timer Count-up/count-down timer with selection of seven internal clock signals or event input from pin P1₁/IRQ₁ • Timer D: 8-bit event counter Up-counter for counting input from pin P1₆/EVENT • Timer E: 8-bit reload timer Count-up timer with selection of eight internal clock signals. A fixed-frequency waveform can be output from pin P1₅/IRQ₅/TMOE, or an arbitrary square wave (50% duty) can be output by timer E overflow. <p>Note: * ϕ indicates a clock frequency that is divided in half from the original oscillator frequency</p>
14-bit PWM*	<ul style="list-style-type: none"> • Pulse-division PWM designed for less ripple • Can be used as a 14-bit D/A converter by connecting to an external low-pass filter <p>Note: * The H8/3612 does not have this function.</p>
Serial communication interface	<p>Two channels on chip</p> <ul style="list-style-type: none"> • Choice of 8-bit or 16-bit transfer data (SCI1) • Automatic transfer of 32-byte data (SCI2)
A/D converter	<ul style="list-style-type: none"> • Successive approximations using a resistance ladder • Resolution: 8 bits • 8-channel analog input port • Conversion time: 31/ϕ or 62/ϕ per channel

Table 1-1 Features (cont)

Item	Specification			
Memory	Large on-chip memory			
	H8/3612: 16-kbyte ROM, 512-byte RAM			
	H8/3613: 24-kbyte ROM, 1024-byte RAM			
	H8/3614: 32-kbyte ROM, 1024-byte RAM			
	H8/3614ZTAT: 32-kbyte PROM, 1024-byte RAM			
Product lineup	Product Code			
	Mask ROM Version	ZTAT™ Version	Package	ROM/RAM Size
	HD6433612H	—	64-pin QFP (FP-64A)	ROM: 16 kbytes RAM: 512 bytes
	HD6433612P	—	64-pin SDIP (DP-64S)	
	HD6433613H	—	64-pin QFP (FP-64A)	ROM: 24 kbytes RAM: 1024 bytes
	HD6433613P	—	64-pin SDIP (DP-64S)	
	HD6433614H	HD6473614H	64-pin QFP (FP-64A)	ROM: 32 kbytes RAM: 1024 bytes
	HD6433614P	HD6473614P	64-pin SDIP (DP-64S)	

1.2 Internal Block Diagram

Figure 1-1 shows an internal block diagram of the H8/3612. Figure 1-2 shows an internal block diagram of the H8/3613 and H8/3614.

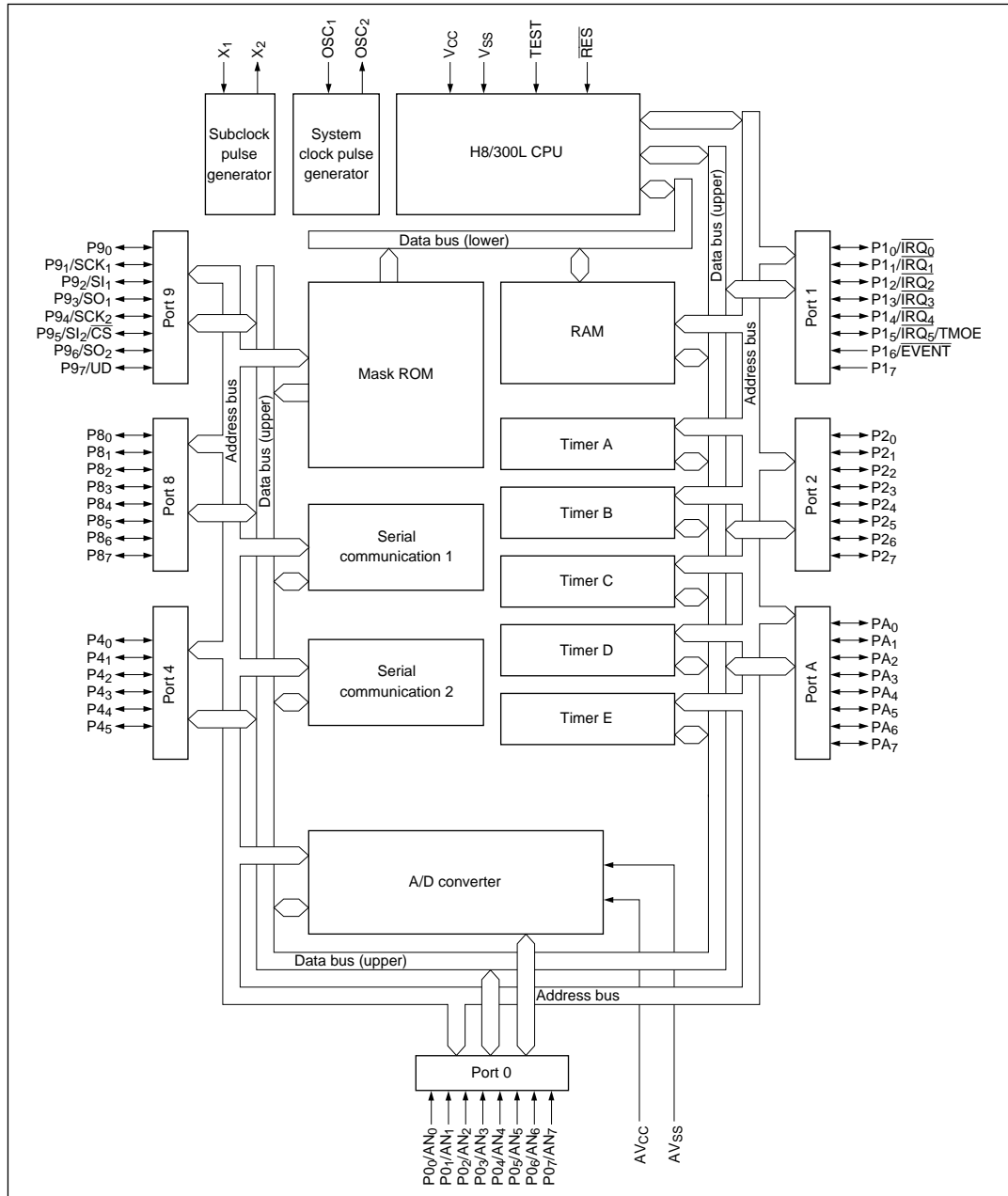


Figure 1-1 Block Diagram (H8/3612)

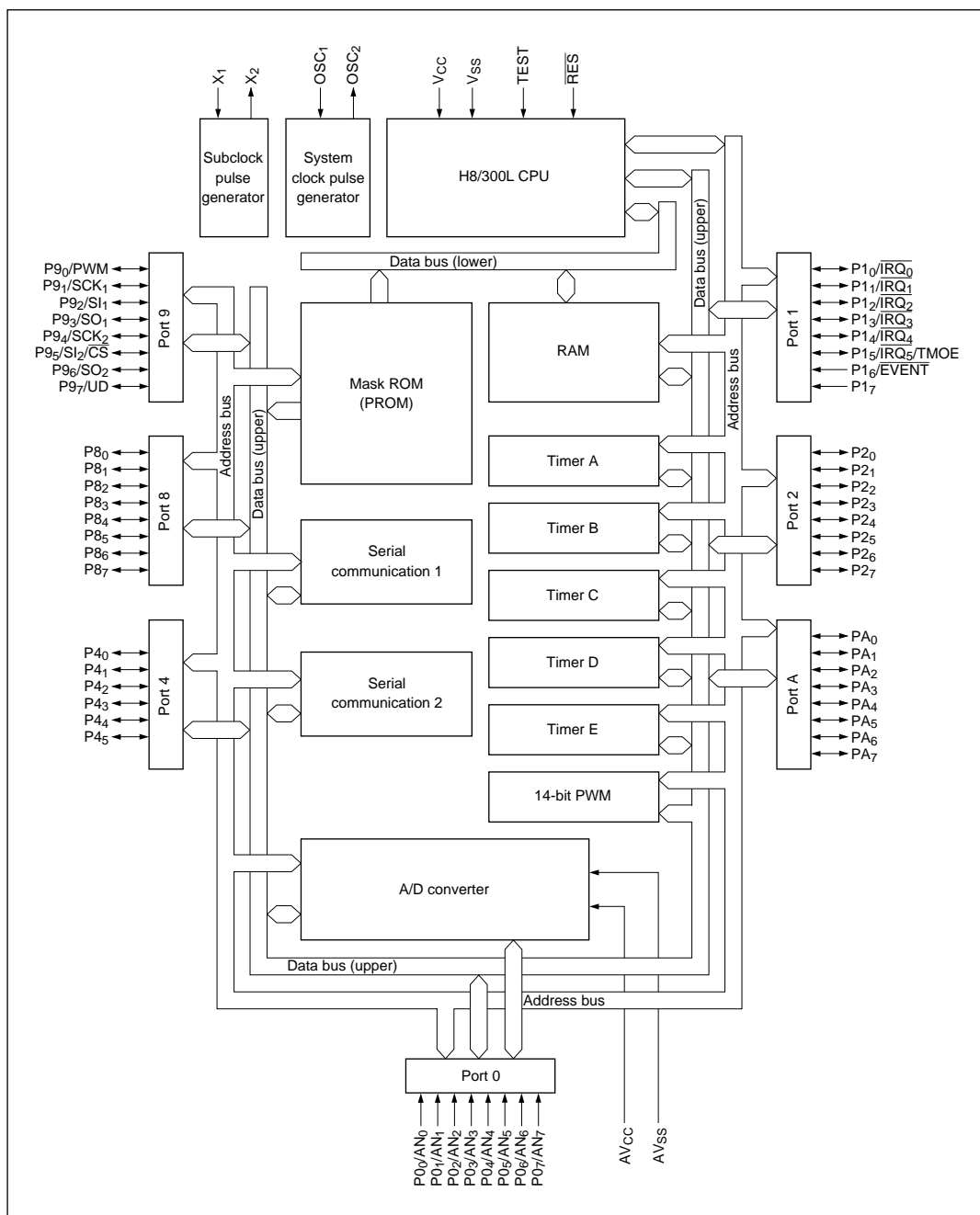


Figure 1-2 Block Diagram (H8/3613 and H8/3614)

1.3 Pin Arrangement and Functions

1.3.1 Pin Arrangement

The pin arrangements for the H8/3612 are shown in figures 1-3 (FP-64A) and 1-4 (DP-64S). The pin arrangements for the H8/3613 and H8/3614 are shown in figures 1-5 (FP-64A) and 1-6 (DP-64S).

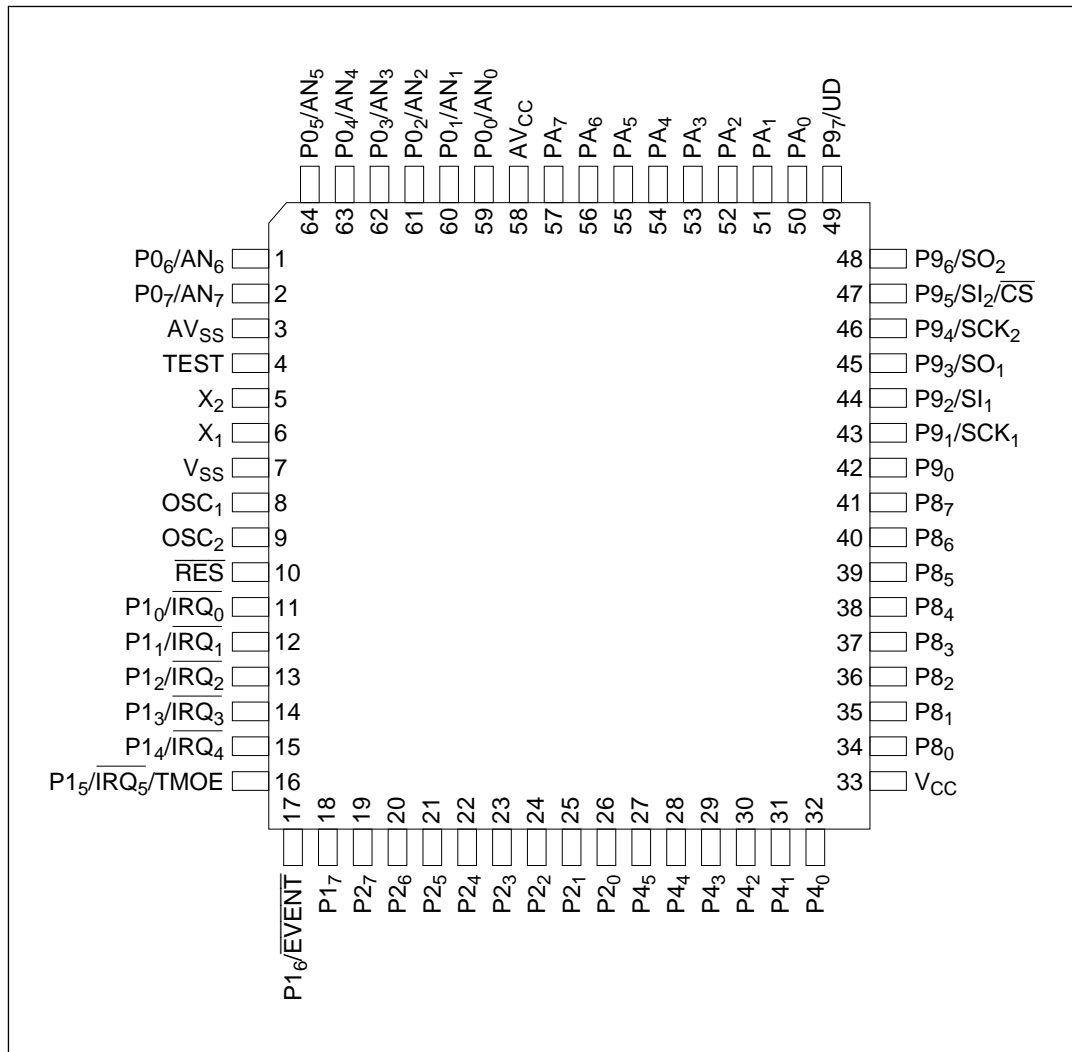


Figure 1-3 H8/3612 Pin Arrangement (FP-64A: Top View)

PA ₇	1	64	PA ₆
AV _{CC}	2	63	PA ₅
P0 ₀ /AN ₀	3	62	PA ₄
P0 ₁ /AN ₁	4	61	PA ₃
P0 ₂ /AN ₂	5	60	PA ₂
P0 ₃ /AN ₃	6	59	PA ₁
P0 ₄ /AN ₄	7	58	PA ₀
P0 ₅ /AN ₅	8	57	P9 ₇ /UD
P0 ₆ /AN ₆	9	56	P9 ₆ /SO ₂
P0 ₇ /AN ₇	10	55	P9 ₅ /SI ₂ / \overline{CS}
AV _{SS}	11	54	P9 ₄ /SCK ₂
TEST	12	53	P9 ₃ /SO ₁
X ₂	13	52	P9 ₂ /SI ₁
X ₁	14	51	P9 ₁ /SCK ₁
V _{SS}	15	50	P9 ₀
OSC ₁	16	49	P8 ₇
OSC ₂	17	48	P8 ₆
RES	18	47	P8 ₅
P1 ₀ /IRQ ₀	19	46	P8 ₄
P1 ₁ /IRQ ₁	20	45	P8 ₃
P1 ₂ /IRQ ₂	21	44	P8 ₂
P1 ₃ /IRQ ₃	22	43	P8 ₁
P1 ₄ /IRQ ₄	23	42	P8 ₀
P1 ₅ /IRQ ₅ /TMOE	24	41	V _{CC}
P1 ₆ /EVENT	25	40	P4 ₀
P1 ₇	26	39	P4 ₁
P2 ₇	27	38	P4 ₂
P2 ₆	28	37	P4 ₃
P2 ₅	29	36	P4 ₄
P2 ₄	30	35	P4 ₅
P2 ₃	31	34	P2 ₀
P2 ₂	32	33	P2 ₁

Figure 1-4 H8/3612 Pin Arrangement (DP-64S: Top View)

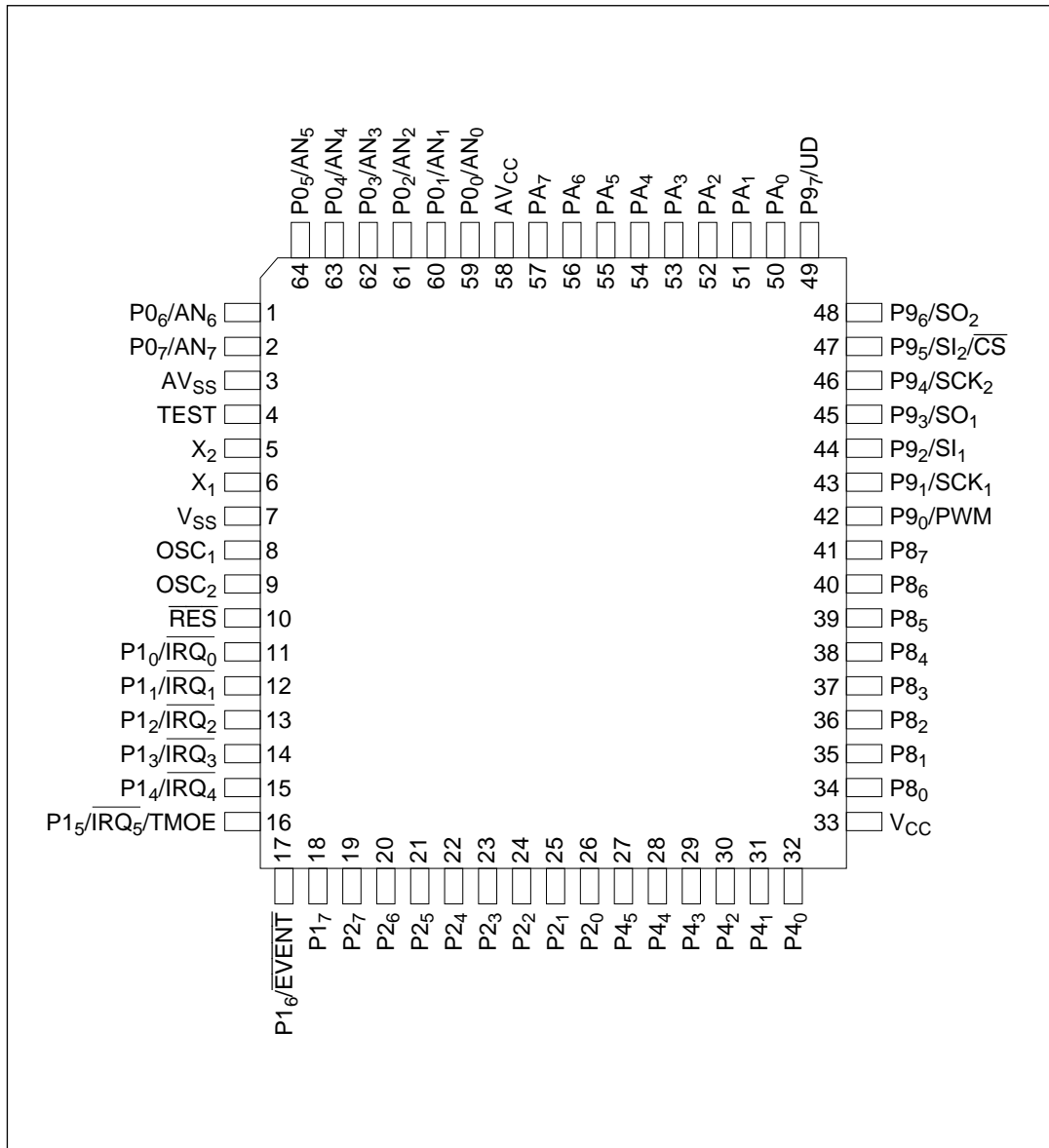


Figure 1-5 H8/3613 and H8/3614 Pin Arrangement (FP-64A: Top View)

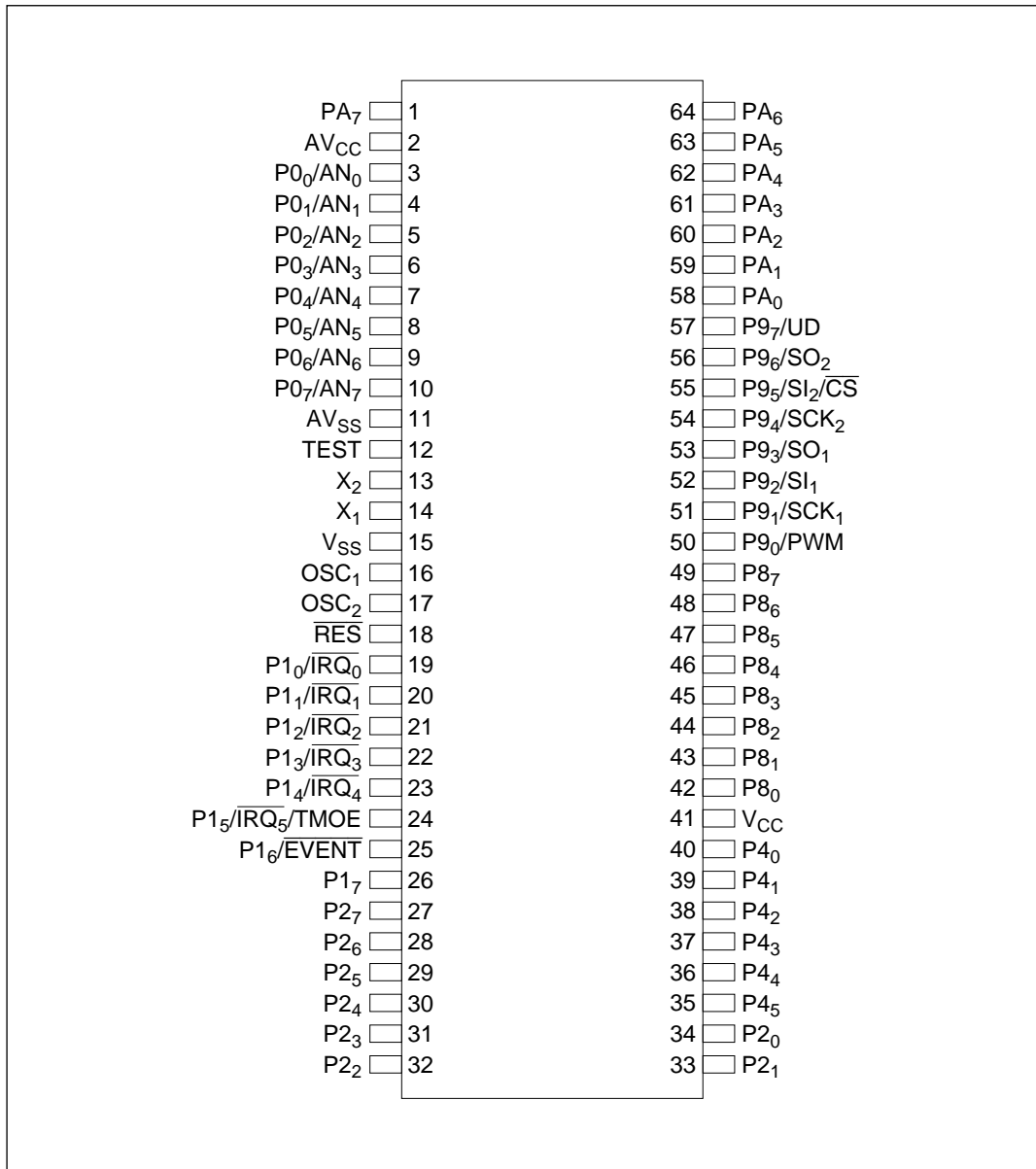


Figure 1-6 H8/3613 and H8/3614 Pin Arrangement (DP-64S: Top View)

1.3.2 Pin Functions

Table 1-3 explains the functions of each pin.

Table 1-3 Pin Functions

Type	Symbol	Pin No.		I/O	Name and Functions
		FP-64A	DP-64S		
Power supply pins	V_{CC}	33	41	Input	Power supply: All V_{CC} pins should be connected to the system power supply (+5 V).
	V_{SS}	7	15	Input	Ground: All V_{SS} pins should be connected to the system power supply (0 V).
	AV_{CC}	58	2	Input	Analog power supply: This is the power supply pin for the A/D converter. When the A/D converter is not used, connect this pin to the system power supply (+5 V).
	AV_{SS}	3	11	Input	Analog ground: This is the A/D converter ground pin. It should be connected to the system power supply (0 V).
Clock pins	OSC_1	8	16	Input	This pin connects to a crystal or ceramic oscillator, or can be used to input an external clock. See section 4, Clock Pulse Generators, for a typical connection diagram.
	OSC_2	9	17	Output	This pin connects to a crystal or ceramic oscillator.
	X_1	6	14	Input	This pin connects to a 32.768 kHz crystal oscillator. For a typical connection diagram, see section 4, Clock Pulse Generators.
	X_2	5	13	Output	This pin connects to a 32.768 kHz crystal oscillator.
System control	\overline{RES}	10	18	Input	Reset: When this pin goes to low level, the chip is reset.
	TEST	4	12	Input	Test: This pin is not for use in application systems. It should be grounded to a V_{SS} potential.

Table 1-3 Pin Functions (cont)

Type	Symbol	Pin No.		I/O	Name and Functions
		FP-64A	DP-64S		
Interrupt pins	$\overline{\text{IRQ}}_0$	11	19	Input	<p>External interrupt request 0: This is an input pin for external interrupts for which there is a choice between rising and falling edge sensing. It can be used to exit low-power mode.</p> <p>This pin can be used as the event input pin for timer B. A noise cancel function is also provided.</p>
	$\overline{\text{IRQ}}_1$	12	20	Input	<p>External interrupt request 1: This is an input pin for external interrupts for which there is a choice between rising and falling edge sensing. It can be used to exit low-power mode.</p> <p>This pin can be used as the event input pin for timer C.</p>
	$\overline{\text{IRQ}}_2$	13	21	Input	<p>External interrupt request 2: This is an input pin for external interrupts that are detected at the falling edge.</p>
	$\overline{\text{IRQ}}_3$	14	22	Input	<p>External interrupt request 3: This is an input pin for external interrupts that are detected at the falling edge.</p>
	$\overline{\text{IRQ}}_4$	15	23	Input	<p>External interrupt request 4: This is an input pin for external interrupts for which there is a choice between rising and falling edge sensing.</p>
	$\overline{\text{IRQ}}_5$	16	24	Input	<p>External interrupt request 5: This is an input pin for external interrupts that are detected at the falling edge.</p>
Timer pins	$\overline{\text{IRQ}}_0$	11	19	Input	<p>Timer B event counter input: This is an event input pin for input to the timer B counter.</p>
	$\overline{\text{IRQ}}_1$	12	20	Input	<p>Timer C event counter input: This is an event input pin for input to the timer C counter.</p>
	UD	49	57	Input	<p>Timer C up/down select: This pin selects whether the timer C counter is used for up- or down-counting. At high level it selects down-counting, and at low level up-counting.</p> <p>Input to this pin is valid only when bit TMC6 in timer mode register C (TMC) is set to 1.</p>

Table 1-3 Pin Functions (cont)

Type	Symbol	Pin No.		I/O	Name and Functions
		FP-64A	DP-64S		
Timer pins	EVENT	17	25	Input	Timer D event counter input: This is an event input pin for input to the timer D counter.
	TMOE	16	24	Output	Timer E output: This is an output pin for waveforms generated by the timer E output circuit.
14-bit PWM pin*	PWM	42	50	Output	14-bit PWM output: This is an output pin for waveforms generated by the 14-bit PWM.
Serial communication interface (SCI) pins	SO ₁	45	53	Output	Serial transmit data output (channels 1 and 2): These are SCI data output pins.
	SO ₂	48	56		
	SI ₁	44	52	Input	Serial receive data input (channels 1 and 2): These are SCI data input pins.
	SI ₂	47	55		
	SCK ₁	43	51	I/O	Serial clock I/O (channels 1 and 2): These are SCI clock I/O pins.
	SCK ₂	46	54		
	CS	47	55	Output	Chip select output: When SCI2 is in transmit mode and the serial clock is an internal clock, this pin goes low. This function is valid when bit SI2 in port mode register 2 (PMR2) is 1 and the CS bit in PMR3 is 1.
I/O ports	P0 ₇ to P0 ₀	2, 1, 64 to 59	10 to 3	Input	Port 0: This is an 8-bit input port.
	P1 ₇	18	26	Input	Port 1 (bit 7): This is a 1-bit input pin.
	P1 ₆	17	25	Input	Port 1 (bit 6): This is a 1-bit input pin.
	P1 ₅ to P1 ₀	16 to 11	24 to 19	I/O	Port 1: This is a 6-bit group of I/O pins. Input or output can be designated for each bit by means of port control register 1 (PCR1).
	P2 ₇ to P2 ₀	19 to 26	27 to 34	I/O	Port 2: This is an 8-bit I/O port.
	P4 ₅ to P4 ₀	27 to 32	35 to 40	I/O	Port 4: This is a 6-bit I/O port.
	P8 ₇ to P8 ₀	41 to 34	49 to 42	I/O	Port 8: This is an 8-bit I/O port. Input or output can be designated for each bit by means of port control register 8 (PCR8).

Note: * The H8/3612 does not have this function.

Table 1-3 Pin Functions (cont)

Type	Symbol	Pin No.		I/O	Name and Functions
		FP-64A	DP-64S		
I/O ports	P9 ₇ to P9 ₀	49 to 42	57 to 50	I/O	Port 9: This is an 8-bit I/O port. Input or output can be designated for each bit by means of port control register 9 (PCR9).
	PA ₇ to PA ₀	57 to 50	1, 64 to 58	I/O	Port A: This is an 8-bit I/O port. Input or output can be designated for each bit by means of port control register A (PCRA).
A/D converter	AN ₇ to AN ₀	2, 1, 64 to 59	10 to 3	Input	Analog input channels 7 to 0: These are analog data input channels to the A/D converter.

Section 2 CPU

2.1 Overview

The H8/300L CPU has sixteen 8-bit general registers, which can also be paired as eight 16-bit registers. Its concise, optimized instruction set is designed for high-speed operation.

2.1.1 Features

The main features of the H8/300L CPU are listed below.

- General-register architecture
 - Sixteen 8-bit general registers, also usable as eight 16-bit general registers
- Instruction set with 55 basic instructions, including:
 - Multiply and divide instructions
 - Powerful bit-manipulation instructions
- Eight addressing modes
 - Register direct Rn
 - Register indirect @Rn
 - Register indirect with displacement @(d:16, Rn)
 - Register indirect with post-increment or pre-decrement @Rn+ or @-Rn
 - Absolute address @aa:8 or @aa:16
 - Immediate #xx:8 or #xx:16
 - Program-counter relative @(d:8, PC)
 - Memory indirect @@aa:8
- 64-kbyte address space
- High-speed operation
 - All frequently used instructions are executed in two to four states
 - High-speed arithmetic and logic operations
 - 8- or 16-bit register-register add or subtract: 0.5 μ s*
 - 8 \times 8-bit multiply: 3.5 μ s*
 - 16 \div 8-bit divide: 3.5 μ s*
- Low-power operation modes
 - SLEEP instruction for transfer to low-power operation

Note: * These values are at $\phi = 4$ MHz.

2.1.2 Address Space

The H8/300L CPU supports an address space of up to 64 kbytes for storing program code and data.

The H8/3614 Series memory map varies with the ROM size, as shown in figure 2-1.

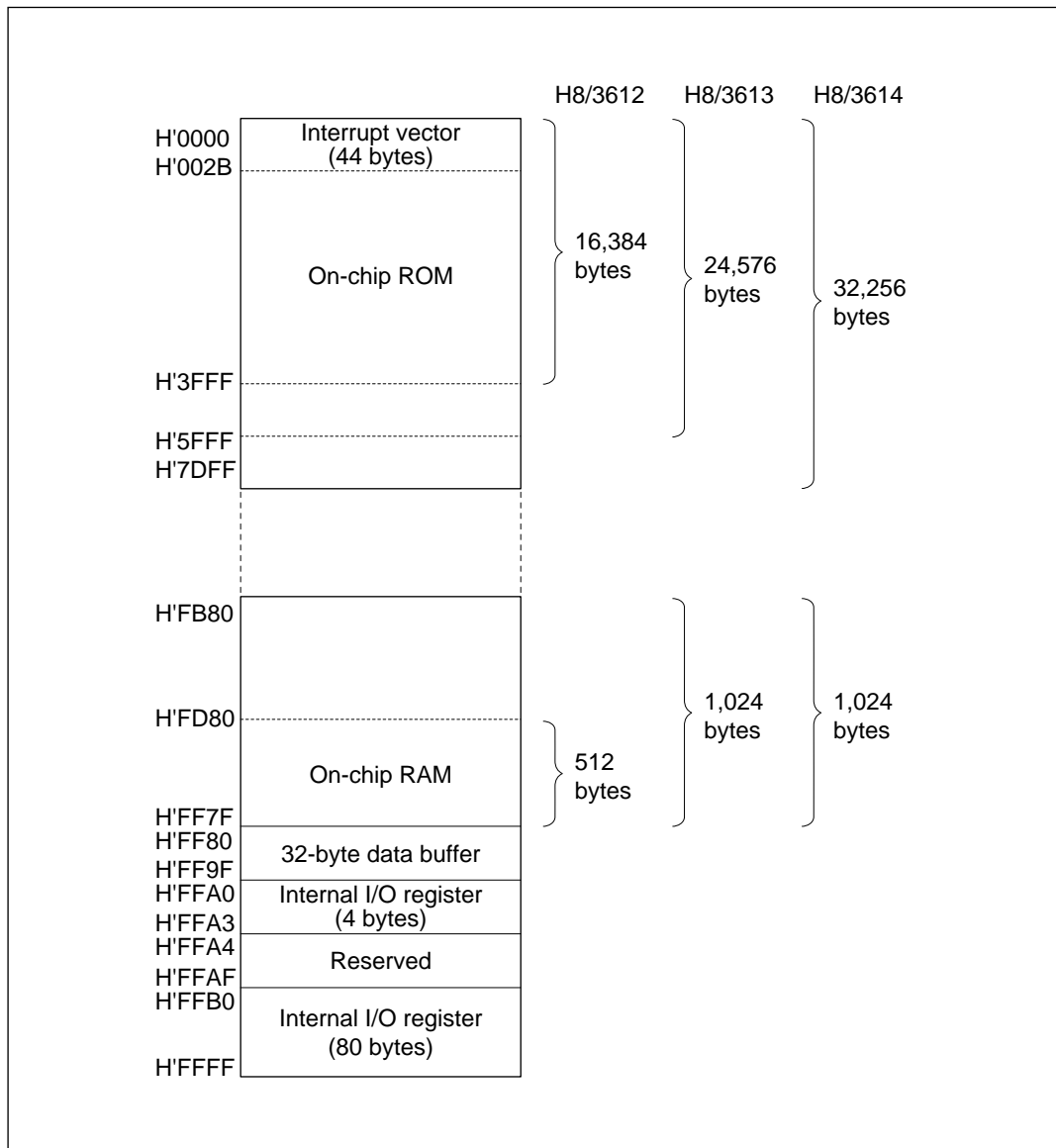


Figure 2-1 Memory Map

2.1.3 Register Configuration

Figure 2-2 shows the register structure of the H8/300L CPU. There are two groups of registers: the general registers and control registers.

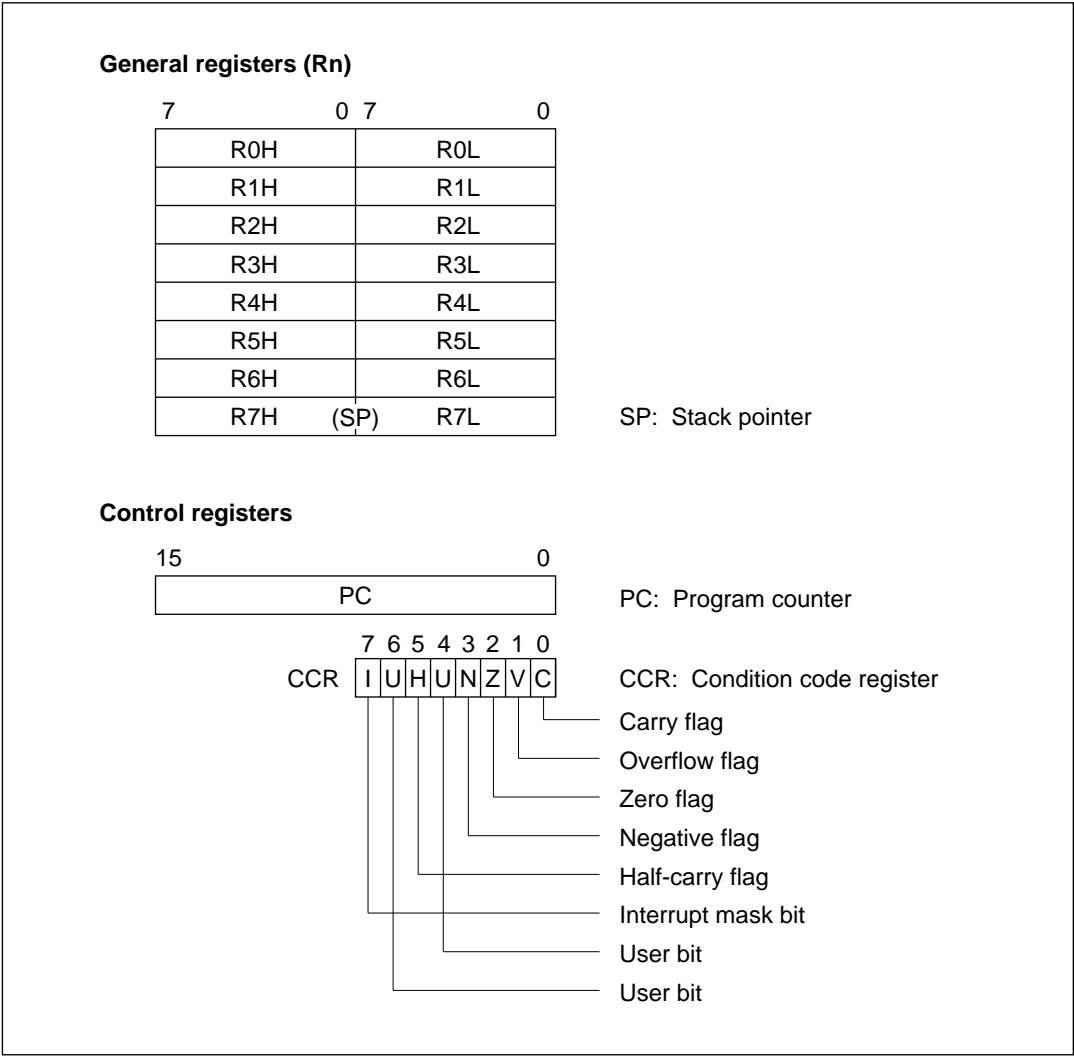


Figure 2-2 CPU Registers

2.2 Register Descriptions

2.2.1 General Registers

All the general registers can be used as both data registers and address registers.

When used as data registers, they can be accessed as 16-bit registers (R0 to R7), or the high bytes (R0H to R7H) and low bytes (R0L to R7L) can be accessed separately as 8-bit registers.

When used as address registers, the general registers are accessed as 16-bit registers (R0 to R7).

R7 also functions as the stack pointer (SP), used implicitly by hardware in exception processing and subroutine calls. When it functions as the stack pointer, as indicated in figure 2-3, SP (R7) points to the top of the stack.

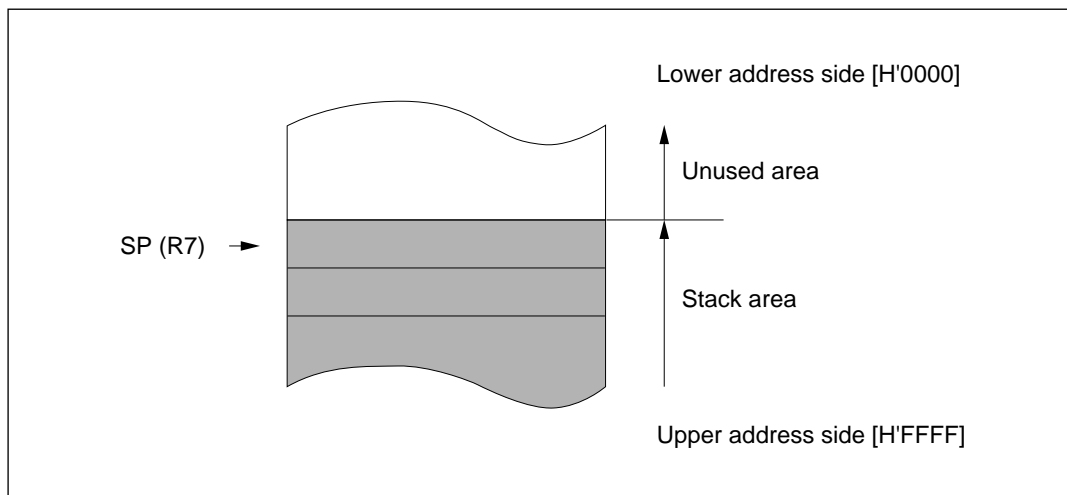


Figure 2-3 Stack Pointer

2.2.2 Control Registers

The CPU control registers include a 16-bit program counter (PC) and an 8-bit condition code register (CCR).

- 1. Program Counter (PC):** This 16-bit register indicates the address of the next instruction the CPU will execute. All instructions are fetched 16 bits (1 word) at a time, so the least significant bit of the PC is ignored (always regarded as 0).
- 2. Condition Code Register (CCR):** This 8-bit register contains internal status information, including the interrupt mask bit (I) and half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags.

Bit 7—Interrupt Mask Bit (I): When this bit is set to 1, interrupts are masked. This bit is set to 1 automatically at the start of exception handling. The interrupt mask bit may be read and written by software. For further details, see 3.2.2, Interrupts.

Bit 6—User Bit (U): Can be written and read by software for its own purposes (using the LDC, STC, ANDC, ORC, and XORC instructions).

Bit 5—Half-Carry Flag (H): When the ADD.B, ADDX.B, SUB.B, SUBX.B, CMP.B, or NEG.B instruction is executed, this flag is set to 1 if there is a carry or borrow at bit 3, and is cleared to 0 otherwise.

The H flag is used implicitly by the DAA and DAS instructions.

When the ADD.W, SUB.W, or CMP.W instruction is executed, the H flag is set to 1 if there is a carry or borrow at bit 11, and is cleared to 0 otherwise.

Bit 4—User Bit (U): Can be written and read by software for its own purposes (using the LDC, STC, ANDC, ORC, and XORC instructions).

Bit 3—Negative Flag (N): Indicates the most significant bit (sign bit) of the result of an instruction.

Bit 2—Zero Flag (Z): Set to 1 to indicate zero data, and cleared to 0 to indicate non-zero data.

Bit 1—Overflow Flag (V): Set to 1 when an arithmetic overflow occurs, and cleared to 0 at other times.

Bit 0—Carry Flag (C): Set to 1 when a carry occurs, and cleared to 0 otherwise. Used by:

- Add instructions, to indicate a carry
- Subtract instructions, to indicate a borrow
- Shift and rotate instructions, to store the value shifted out of the end bit

The carry flag is also used as a bit accumulator by bit manipulation instructions.

Some instructions leave some or all of the flag bits unchanged. The LDC, STC, ANDC, ORC, and XORC instructions enable the CPU to load and store the CCR, and to set or clear selected bits by logic operations. The N, Z, V, and C flags are used as branching conditions for conditional branching (Bcc) instructions.

Refer to the *H8/300L Series Programming Manual* for the action of each instruction on the flag bits.

2.2.3 Initial Register Values

When the CPU is reset, the program counter (PC) is initialized to a value loaded from vector address H'0000, and the I bit in the CCR is set to 1. The other CCR bits and the general registers are not initialized. In particular, the stack pointer (R7) is not initialized. The stack pointer should be initialized by software, by the first instruction executed after a reset.

2.3 Data Formats

The H8/300L CPU can process 1-bit data, 4-bit (BCD) data, 8-bit (byte) data, and 16-bit (word) data.

- Bit manipulation instructions operate on 1-bit data specified as bit *n* in a byte operand ($n = 0, 1, 2, \dots, 7$).
- All arithmetic instructions except ADDS and SUBS can operate on byte data.
- The MOV.W, ADD.W, SUB.W, CMP.W, ADDS, SUBS, MULXU (8 bits \times 8 bits), and DIVXU (16 bits \div 8 bits) instructions operate on word data.
- The DAA and DAS instructions perform decimal arithmetic adjustments on byte data in packed BCD form. Each nibble of the byte is treated as a decimal digit.

2.3.1 Data Formats in General Registers

Data of all the sizes above can be stored in general registers as shown in figure 2-4.

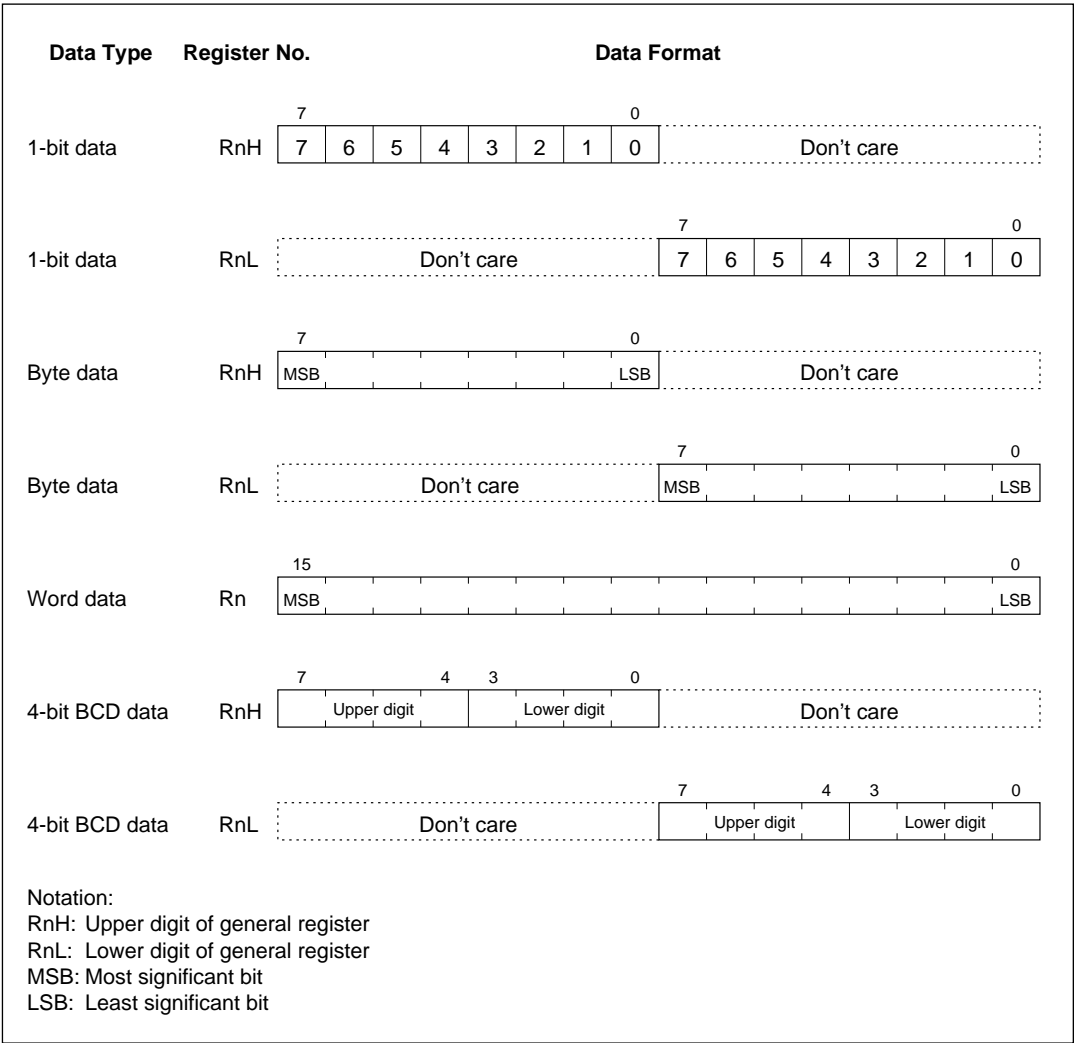


Figure 2-4 Register Data Formats

2.3.2 Memory Data Formats

Figure 2-5 indicates the data formats in memory. For access by the H8/300L CPU, word data stored in memory must always begin at an even address. In word access the least significant bit of the address is regarded as 0. If an odd address is specified, the access is performed at the preceding even address. This rule affects the MOV.W instruction, and also applies to instruction fetching. Word access is possible only to ROM and RAM areas. For details, see 2.8.1, Notes on Data Access.

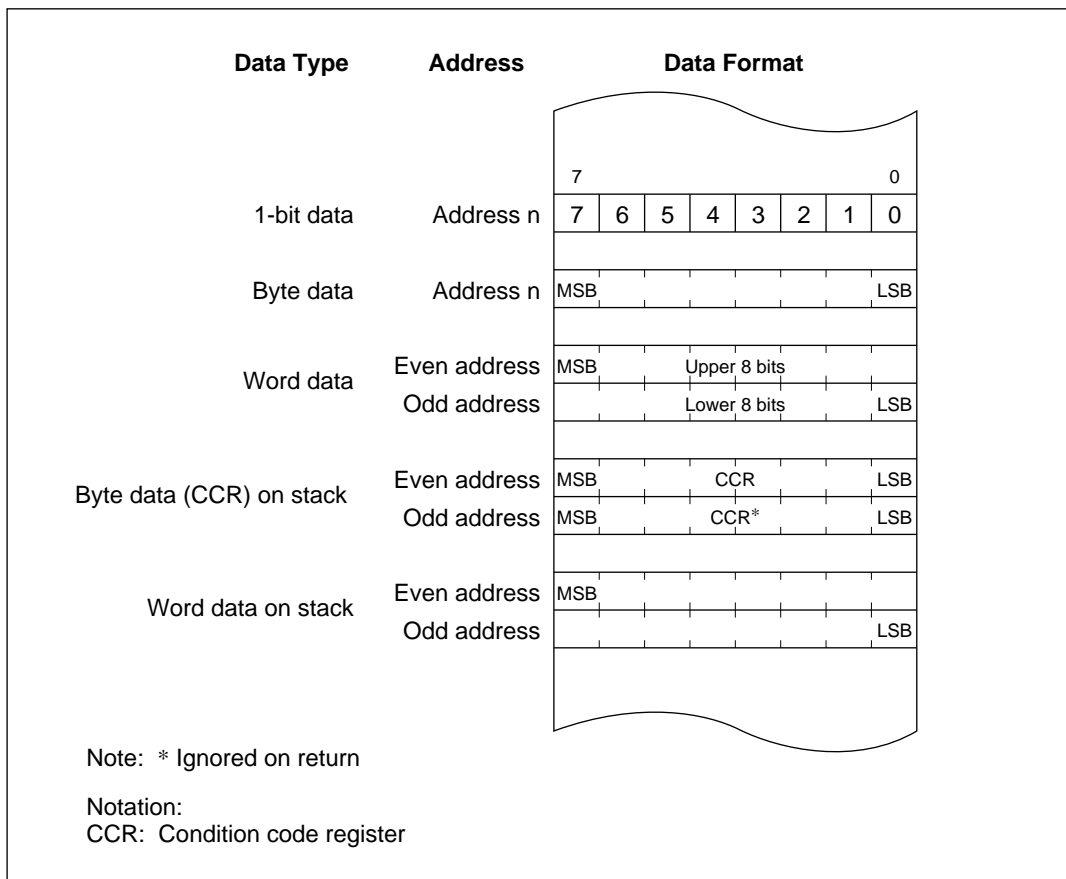


Figure 2-5 Memory Data Formats

When the stack is accessed using R7 as an address register, word access should always be performed. For details, see 3.2.10, Notes on Stack Area Use. When the CCR is pushed on the stack, two identical copies of the CCR are pushed to make a complete word. When they are restored, the lower byte is ignored.

2.4 Addressing Modes

2.4.1 Addressing Modes

The H8/300L CPU supports the eight addressing modes listed in table 2-1. Each instruction uses a subset of these addressing modes.

Table 2-1 Addressing Modes

No.	Address Modes	Symbol
1	Register direct	Rn
2	Register indirect	@Rn
3	Register indirect with displacement	@(d:16, Rn)
4	Register indirect with post-increment Register indirect with pre-decrement	@Rn+ @-Rn
5	Absolute address	@aa:8 or @aa:16
6	Immediate	#xx:8 or #xx:16
7	Program-counter relative	@(d:8, PC)
8	Memory indirect	@@aa:8

1. **Register Direct—Rn:** The register field of the instruction specifies an 8- or 16-bit general register containing the operand.

Only the MOV.W, ADD.W, SUB.W, CMP.W, ADDS, SUBS, MULXU (8 bits × 8 bits), and DIVXU (16 bits ÷ 8 bits) instructions have 16-bit operands.

2. **Register Indirect—@Rn:** The register field of the instruction specifies a 16-bit general register containing the address of the operand.

3. **Register Indirect with Displacement—@(d:16, Rn):** The instruction has a second word (bytes 3 and 4) containing a displacement which is added to the contents of the specified general register to obtain the operand address.

This mode is used only in MOV instructions. For the MOV.W instruction, the resulting address must be even.

4. Register Indirect with Post-Increment or Pre-Decrement—@Rn+ or @-Rn:

- Register indirect with post-increment—@Rn+

The @Rn+ mode is used with MOV instructions that load registers from memory.

The register field of the instruction specifies a 16-bit general register containing the address of the operand. After the operand is accessed, the register is incremented by 1 for MOV.B or 2 for MOV.W. For MOV.W, the original contents of the 16-bit general register must be even.

- Register indirect with pre-decrement—@-Rn

The @-Rn mode is used with MOV instructions that store register contents to memory.

The register field of the instruction specifies a 16-bit general register which is decremented by 1 or 2 to obtain the address of the operand in memory. The register retains the decremented value. The size of the decrement is 1 for MOV.B or 2 for MOV.W. For MOV.W, the original contents of the register must be even.

5. Absolute Address—@aa:8 or @aa:16: The instruction specifies the absolute address of the operand in memory.

The absolute address may be 8 bits long (@aa:8) or 16 bits long (@aa:16). The MOV.B and bit manipulation instructions can use 8-bit absolute addresses. The MOV.B, MOV.W, JMP, and JSR instructions can use 16-bit absolute addresses.

For an 8-bit absolute address, the upper 8 bits are assumed to be 1 (H'FF). The address range is H'FF00 to H'FFFF (65280 to 65535).

6. Immediate—#xx:8 or #xx:16: The instruction contains an 8-bit operand (#xx:8) in its second byte, or a 16-bit operand (#xx:16) in its third and fourth bytes. Only MOV.W instructions can contain 16-bit immediate values.

The ADDS and SUBS instructions implicitly contain the value 1 or 2 as immediate data. Some bit manipulation instructions contain 3-bit immediate data in the second or fourth byte of the instruction, specifying a bit number.

7. Program-Counter Relative—@(d:8, PC): This mode is used in the Bcc and BSR instructions. An 8-bit displacement in byte 2 of the instruction code is sign-extended to 16 bits and added to the program counter contents to generate a branch destination address. The possible branching range is -126 to +128 bytes (-63 to +64 words) from the current address. The displacement should be an even number.

- 8. Memory Indirect—@@aa:8:** This mode can be used by the JMP and JSR instructions. The second byte of the instruction code specifies an 8-bit absolute address. The word located at this address contains the branch destination address.

The upper 8 bits of the absolute address are assumed to be 0 (H'00), so the address range is from H'0000 to H'00FF (0 to 255). Note that in the H8/300L Series, low addresses are assigned to the vector table.

If an odd address is specified as a branch destination or as the operand address of a MOV.W instruction, the least significant bit is regarded as 0, causing word access to be performed at the address preceding the specified address. See 2.3.2, Memory Data Formats, for further information.

2.4.2 Effective Address Calculation

Table 2-2 shows how effective addresses are calculated in each of the addressing modes.

Arithmetic and logic instructions use register direct addressing (1). The ADD.B, ADDX, SUBX, CMP.B, AND, OR, and XOR instructions can also use immediate addressing (6).

Data transfer instructions can use all addressing modes except program-counter relative (7) and memory indirect (8).

Bit manipulation instructions use register direct (1), register indirect (2), or absolute addressing (5) to specify a byte operand, and 3-bit immediate addressing (6) to specify a bit position in that byte. The BSET, BCLR, BNOT, and BTST instructions can also use register direct addressing (1) to specify the bit position.

Table 2-2 Effective Address Calculation

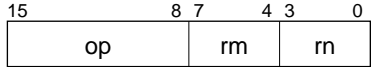
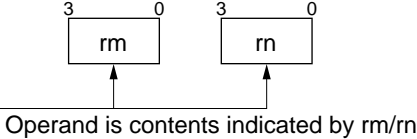
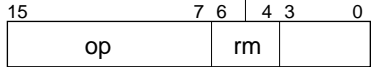
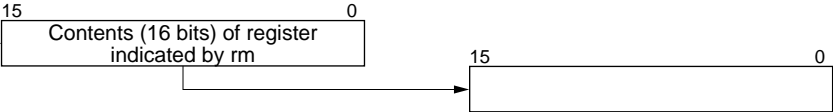
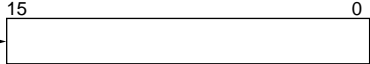
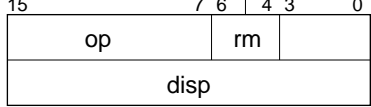
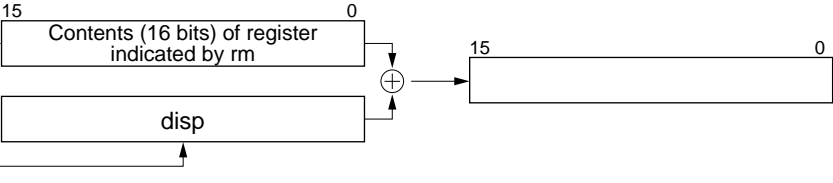

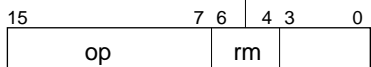
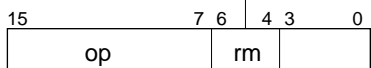
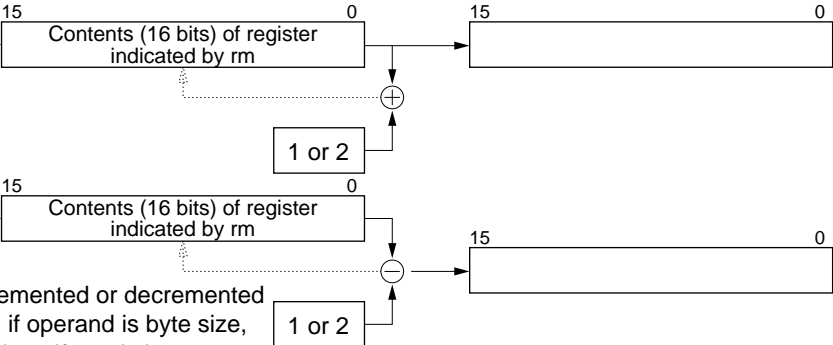
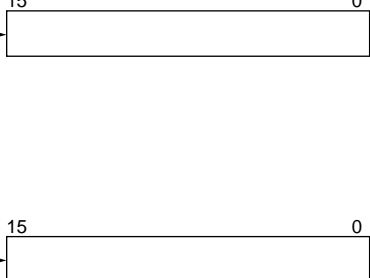
No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
1	Register direct, Rn 		
2	Register indirect, @Rn 		
3	Register indirect with displacement, @(d:16, Rn) 		
4	Register indirect with post-increment, @Rn+  Register indirect with pre-decrement, @-Rn 	 <p>Incremented or decremented by 1 if operand is byte size, and by 2 if word size.</p>	

Table 2-2 Effective Address Calculation (cont)

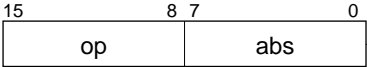
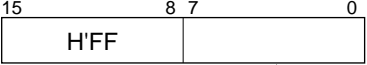
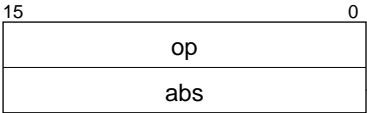
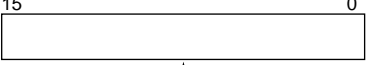
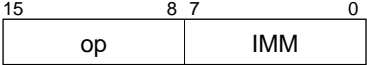
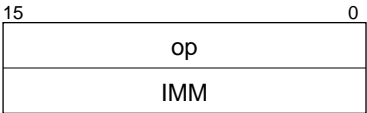
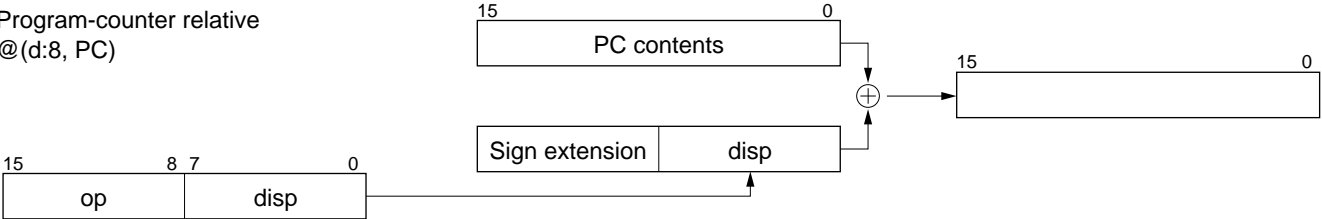
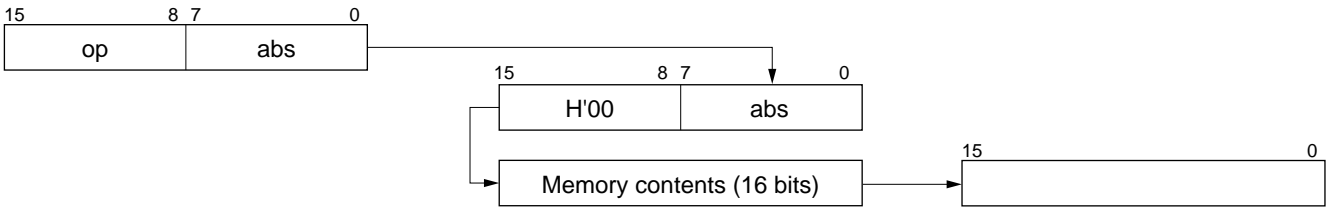
No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
5	Absolute address @aa:8		
	@aa:16		
6	Immediate #xx:8		Operand is 1- or 2-byte immediate data.
	#xx:16		
7	Program-counter relative @(d:8, PC)		

Table 2-2 Effective Address Calculation (cont)

No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
8	Memory indirect, @@aa:8		

Notation:
rm, rn: Register field
op: Operation field
disp: Displacement
IMM: Immediate data
abs: Absolute address

2.5 Instruction Set

The H8/300L CPU can use a total of 55 instructions, which are grouped by function in table 2-3.

Table 2-3 Instruction Set

Function	Instructions	Types
Data transfer	MOV, PUSH*1, POP*1	1
Arithmetic operations	ADD, SUB, ADDX, SUBX, INC, DEC, ADDS, SUBS, DAA, DAS, MULXU, DIVXU, CMP, NEG	14
Logic operations	AND, OR, XOR, NOT	4
Shift	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR	8
Bit manipulation	BSET, BCLR, BNOT, BTST, BAND, BAND, BOR, BIOR, BXOR, BIXOR, BLD, BILD, BST, BIST	14
Branch	Bcc*2, JMP, BSR, JSR, RTS	5
System control	RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP	8
Block data transfer	EEPMOV	1

Total: 55

Notes: 1. PUSH Rn is equivalent to MOV.W Rn, @-SP.

POP Rn is equivalent to MOV.W @SP+, Rn.

2. Bcc is a conditional branch instruction in which cc represents a condition code.

Tables 2-4 to 2-11 give a concise summary of the instructions in each category, and indicate the bit patterns of their object code. The notation used is defined next.

Notation

Rd	General register (destination)
Rs	General register (source)
Rn	General register
(EAd) <EAd>	Destination operand
(EAs) <EAs>	Source operand
CCR	Condition code register
N	N (negative) flag of CCR
Z	Z (zero) flag of CCR
V	V (overflow) flag of CCR
C	C (carry) flag of CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
−	Subtraction
×	Multiplication
÷	Division
^	AND logical
∨	OR logical
⊕	Exclusive OR logical
→	Move
~	Inverse logic (logical complement)
:3	3-bit length
:8	8-bit length
:16	16-bit length
() < >	Contents of operand effective address

2.5.1 Data Transfer Instructions

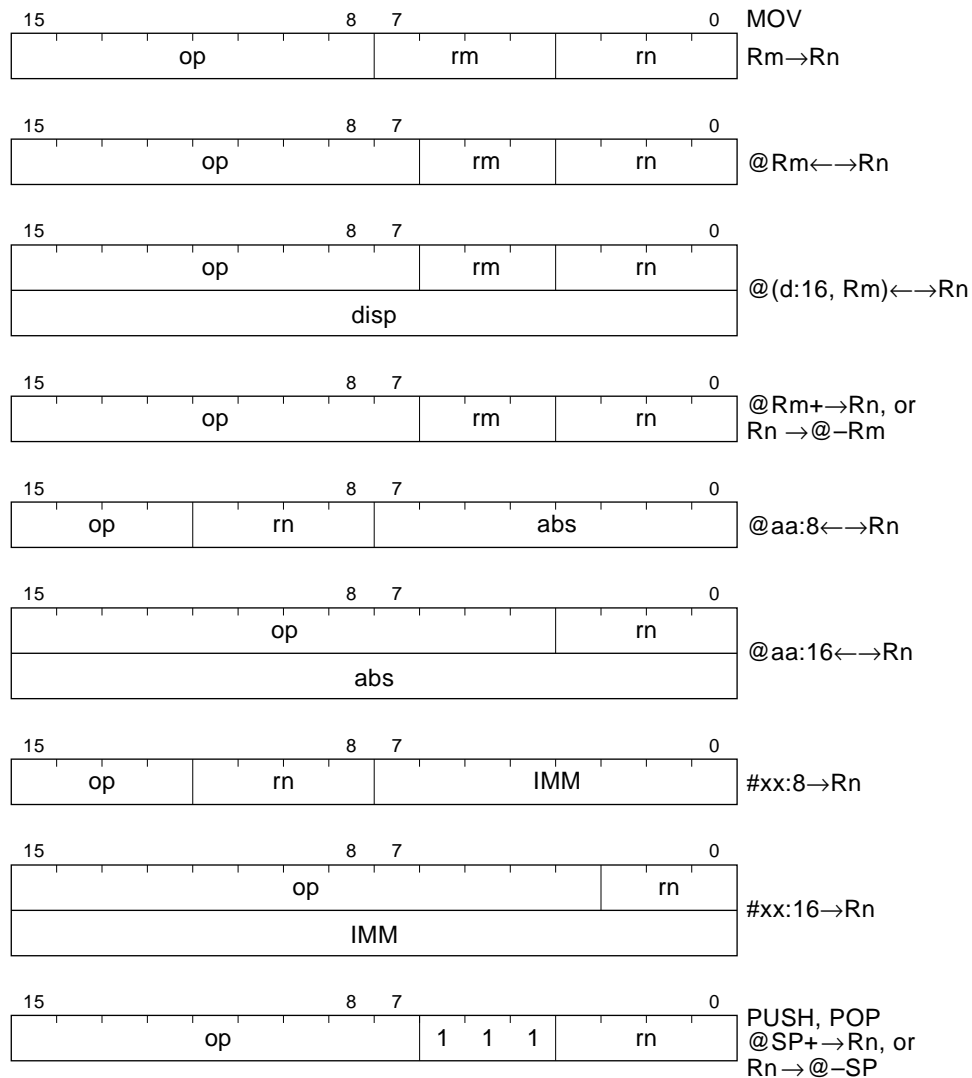
Table 2-4 describes the data transfer instructions. Figure 2-6 shows their object code formats.

Table 2-4 Data Transfer Instructions

Instruction	Size*	Function
MOV	B/W	(EAs) → Rd, Rs → (EAd) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register. The Rn, @Rn, @(d:16, Rn), @aa:16, #xx:16, @-Rn, and @Rn+ addressing modes are available for word data. The @aa:8 addressing mode is available for byte data only. The @-R7 and @R7+ modes require word operands. Do not specify byte size for these two modes.
PUSH	W	Rn → @-SP Pushes a 16-bit general register onto the stack. Equivalent to MOV.W Rn, @-SP.
POP	W	@SP+ → Rn Pops a 16-bit general register from the stack. Equivalent to MOV.W @SP+, Rn.

Notes: * Size: Operand size
B: Byte
W: Word

Certain precautions are required in data access. See 2.8.1, Notes on Data Access, for details.



Notation:
 op: Operation field
 rm, rn: Register field
 disp: Displacement
 abs: Absolute address
 IMM: Immediate data

Figure 2-6 Data Transfer Instruction Codes

2.5.2 Arithmetic Operations

Table 2-5 describes the arithmetic instructions.

Table 2-5 Arithmetic Instructions

Instruction	Size*	Function
ADD SUB	B/W	$Rd \pm Rs \rightarrow Rd$, $Rd + \#IMM \rightarrow Rd$ Performs addition or subtraction on data in two general registers, or addition on immediate data and data in a general register. Immediate data cannot be subtracted from data in a general register. Word data can be added or subtracted only when both words are in general registers.
ADDX SUBX	B	$Rd \pm Rs \pm C \rightarrow Rd$, $Rd \pm \#IMM \pm C \rightarrow Rd$ Performs addition or subtraction with carry or borrow on byte data in two general registers, or addition or subtraction on immediate data and data in a general register.
INC DEC	B	$Rd \pm 1 \rightarrow Rd$ Increments or decrements a general register.
ADDS SUBS	W	$Rd \pm 1 \rightarrow Rd$, $Rd \pm 2 \rightarrow Rd$ Adds or subtracts immediate data to or from data in a general register. The immediate data must be 1 or 2.
DAA DAS	B	Rd decimal adjust $\rightarrow Rd$ Decimal-adjusts (adjusts to packed BCD) an addition or subtraction result in a general register by referring to the CCR.
MULXU	B	$Rd \times Rs \rightarrow Rd$ Performs 8-bit \times 8-bit unsigned multiplication on data in two general registers, providing a 16-bit result.
DIVXU	B	$Rd \div Rs \rightarrow Rd$ Performs 16-bit \div 8-bit unsigned division on data in two general registers, providing an 8-bit quotient and 8-bit remainder.
CMP	B/W	$Rd - Rs$, $Rd - \#IMM$ Compares data in a general register with data in another general register or with immediate data, and sets the CCR according to the result. Word data can be compared only between two general registers.
NEG	B	$0 - Rd \rightarrow Rd$ Obtains the two's complement (arithmetic complement) of data in a general register.

Notes: * Size: Operand size

B: Byte

W: Word

2.5.3 Logic Operations

Table 2-6 describes the four instructions that perform logic operations.

Table 2-6 Logic Operation Instructions

Instruction	Size*	Function
AND	B	$Rd \wedge Rs \rightarrow Rd$, $Rd \wedge \#IMM \rightarrow Rd$ Performs a logical AND operation on a general register and another general register or immediate data.
OR	B	$Rd \vee Rs \rightarrow Rd$, $Rd \vee \#IMM \rightarrow Rd$ Performs a logical OR operation on a general register and another general register or immediate data.
XOR	B	$Rd \oplus Rs \rightarrow Rd$, $Rd \oplus \#IMM \rightarrow Rd$ Performs a logical exclusive OR operation on a general register and another general register or immediate data.
NOT	B	$\sim Rd \rightarrow Rd$ Obtains the one's complement (logical complement) of general register contents.

Notes: * Size: Operand size
B: Byte

2.5.4 Shift Operations

Table 2-7 describes the eight shift instructions.

Table 2-7 Shift Instructions

Instruction	Size*	Function
SHAL SHAR	B	$Rd \text{ shift} \rightarrow Rd$ Performs an arithmetic shift operation on general register contents.
SHLL SHLR	B	$Rd \text{ shift} \rightarrow Rd$ Performs a logical shift operation on general register contents.
ROTL ROTR	B	$Rd \text{ rotate} \rightarrow Rd$ Rotates general register contents.
ROTXL ROTXR	B	$Rd \text{ rotate through carry} \rightarrow Rd$ Rotates general register contents through the C (carry) bit.

Notes: * Size: Operand size
B: Byte

Figure 2-7 shows the instruction code format of arithmetic, logic, and shift instructions.

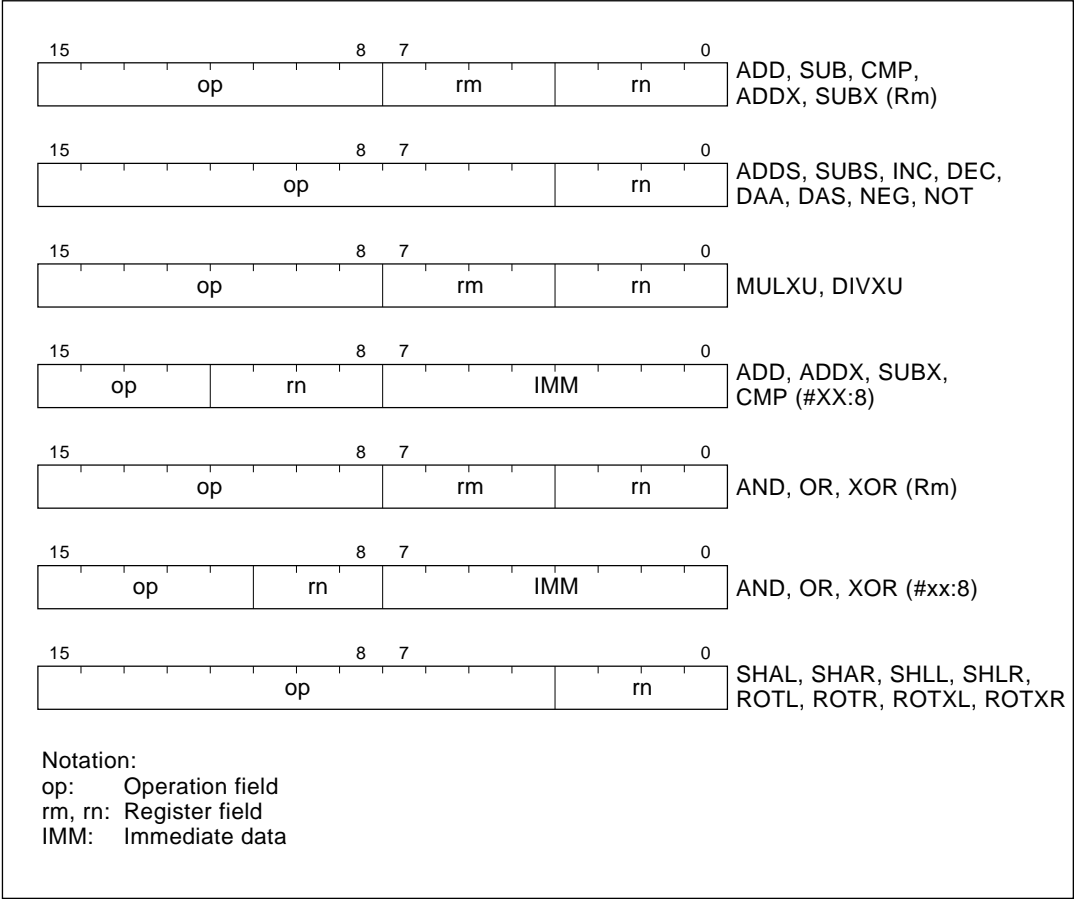


Figure 2-7 Arithmetic, Logic, and Shift Instruction Codes

2.5.5 Bit Manipulations

Table 2-8 describes the bit-manipulation instructions. Figure 2-8 shows their object code formats.

Table 2-8 Bit-Manipulation Instructions

Instruction	Size*	Function
BSET	B	$1 \rightarrow (\text{<bit-No.> of <EAd>})$ Sets a specified bit in a general register or memory to 1. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BCLR	B	$0 \rightarrow (\text{<bit-No.> of <EAd>})$ Clears a specified bit in a general register or memory to 0. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BNOT	B	$\sim (\text{<bit-No.> of <EAd>}) \rightarrow (\text{<bit-No.> of <EAd>})$ Inverts a specified bit in a general register or memory. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BTST	B	$\sim (\text{<bit-No.> of <EAd>}) \rightarrow Z$ Tests a specified bit in a general register or memory and sets or clears the zero flag accordingly. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BAND	B	$C \wedge (\text{<bit-No.> of <EAd>}) \rightarrow C$ ANDs the carry flag with a specified bit in a general register or memory and stores the result in the carry flag.
BIAND	B	$C \wedge [\sim (\text{<bit-No.> of <EAd>})] \rightarrow C$ ANDs the carry flag with the inverse of a specified bit in a general register or memory and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BOR	B	$C \vee (\text{<bit-No.> of <EAd>}) \rightarrow C$ ORs the carry flag with a specified bit in a general register or memory and stores the result in the carry flag.
BIOR	B	$C \vee [\sim (\text{<bit-No.> of <EAd>})] \rightarrow C$ ORs the carry flag with the inverse of a specified bit in a general register or memory and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.

Notes: * Size: Operand size
B: Byte

Table 2-8 Bit-Manipulation Instructions (cont)

Instruction	Size*	Function
BXOR	B	$C \oplus (\text{<bit-No.> of <EAd>}) \rightarrow C$ XORs the carry flag with a specified bit in a general register or memory and stores the result in the carry flag.
BIXOR	B	$C \oplus \sim [(\text{<bit-No.> of <EAd>})] \rightarrow C$ XORs the carry flag with the inverse of a specified bit in a general register or memory and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BLD	B	$(\text{<bit-No.> of <EAd>}) \rightarrow C$ Copies a specified bit in a general register or memory to the carry flag.
BILD	B	$\sim (\text{<bit-No.> of <EAd>}) \rightarrow C$ Copies the inverse of a specified bit in a general register or memory to the carry flag. The bit number is specified by 3-bit immediate data.
BST	B	$C \rightarrow (\text{<bit-No.> of <EAd>})$ Copies the carry flag to a specified bit in a general register or memory.
BIST	B	$\sim C \rightarrow (\text{<bit-No.> of <EAd>})$ Copies the inverse of the carry flag to a specified bit in a general register or memory. The bit number is specified by 3-bit immediate data.

Notes: * Size: Operand size
B: Byte

Certain precautions are required in bit manipulation. See 2.8.2, Notes on Bit Manipulation, for details.

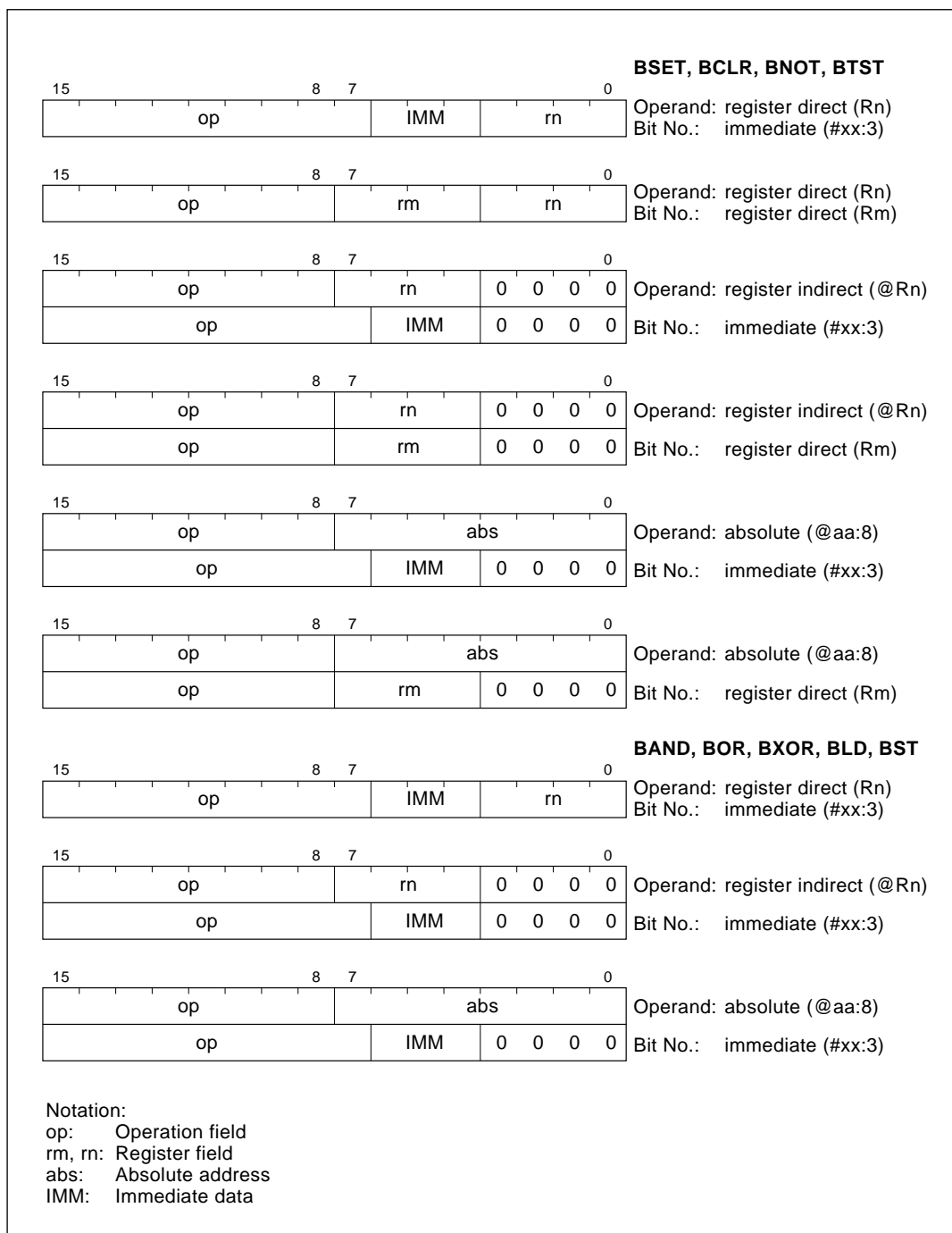


Figure 2-8 Bit Manipulation Instruction Codes

2.5.6 Branching Instructions

Table 2-9 describes the branching instructions.

Table 2-9 Branching Instructions

Instruction	Size	Function																																																			
Bcc	—	Branches to the designated address if condition cc is true. The branching conditions are given below.																																																			
		<table> <tr> <th>Mnemonic</th><th>Description</th><th>Condition</th></tr> <tr> <td>BRA (BT)</td><td>Always (true)</td><td>Always</td></tr> <tr> <td>BRN (BF)</td><td>Never (false)</td><td>Never</td></tr> <tr> <td>BHI</td><td>High</td><td>$C \vee Z = 0$</td></tr> <tr> <td>BLS</td><td>Low or same</td><td>$C \vee Z = 1$</td></tr> <tr> <td>BCC (BHS)</td><td>Carry clear (high or same)</td><td>$C = 0$</td></tr> <tr> <td>BCS (BLO)</td><td>Carry set (low)</td><td>$C = 1$</td></tr> <tr> <td>BNE</td><td>Not equal</td><td>$Z = 0$</td></tr> <tr> <td>BEQ</td><td>Equal</td><td>$Z = 1$</td></tr> <tr> <td>BVC</td><td>Overflow clear</td><td>$V = 0$</td></tr> <tr> <td>BVS</td><td>Overflow set</td><td>$V = 1$</td></tr> <tr> <td>BPL</td><td>Plus</td><td>$N = 0$</td></tr> <tr> <td>BMI</td><td>Minus</td><td>$N = 1$</td></tr> <tr> <td>BGE</td><td>Greater or equal</td><td>$N \oplus V = 0$</td></tr> <tr> <td>BLT</td><td>Less than</td><td>$N \oplus V = 1$</td></tr> <tr> <td>BGT</td><td>Greater than</td><td>$Z \vee (N \oplus V) = 0$</td></tr> <tr> <td>BLE</td><td>Less or equal</td><td>$Z \vee (N \oplus V) = 1$</td></tr> </table>	Mnemonic	Description	Condition	BRA (BT)	Always (true)	Always	BRN (BF)	Never (false)	Never	BHI	High	$C \vee Z = 0$	BLS	Low or same	$C \vee Z = 1$	BCC (BHS)	Carry clear (high or same)	$C = 0$	BCS (BLO)	Carry set (low)	$C = 1$	BNE	Not equal	$Z = 0$	BEQ	Equal	$Z = 1$	BVC	Overflow clear	$V = 0$	BVS	Overflow set	$V = 1$	BPL	Plus	$N = 0$	BMI	Minus	$N = 1$	BGE	Greater or equal	$N \oplus V = 0$	BLT	Less than	$N \oplus V = 1$	BGT	Greater than	$Z \vee (N \oplus V) = 0$	BLE	Less or equal	$Z \vee (N \oplus V) = 1$
Mnemonic	Description	Condition																																																			
BRA (BT)	Always (true)	Always																																																			
BRN (BF)	Never (false)	Never																																																			
BHI	High	$C \vee Z = 0$																																																			
BLS	Low or same	$C \vee Z = 1$																																																			
BCC (BHS)	Carry clear (high or same)	$C = 0$																																																			
BCS (BLO)	Carry set (low)	$C = 1$																																																			
BNE	Not equal	$Z = 0$																																																			
BEQ	Equal	$Z = 1$																																																			
BVC	Overflow clear	$V = 0$																																																			
BVS	Overflow set	$V = 1$																																																			
BPL	Plus	$N = 0$																																																			
BMI	Minus	$N = 1$																																																			
BGE	Greater or equal	$N \oplus V = 0$																																																			
BLT	Less than	$N \oplus V = 1$																																																			
BGT	Greater than	$Z \vee (N \oplus V) = 0$																																																			
BLE	Less or equal	$Z \vee (N \oplus V) = 1$																																																			
JMP	—	Branches unconditionally to a specified address.																																																			
JSR	—	Branches to a subroutine at a specified address.																																																			
BSR	—	Branches to a subroutine at a specified displacement from the current address.																																																			
RTS	—	Returns from a subroutine.																																																			

Figure 2-9 shows the instruction code format of branching instructions.

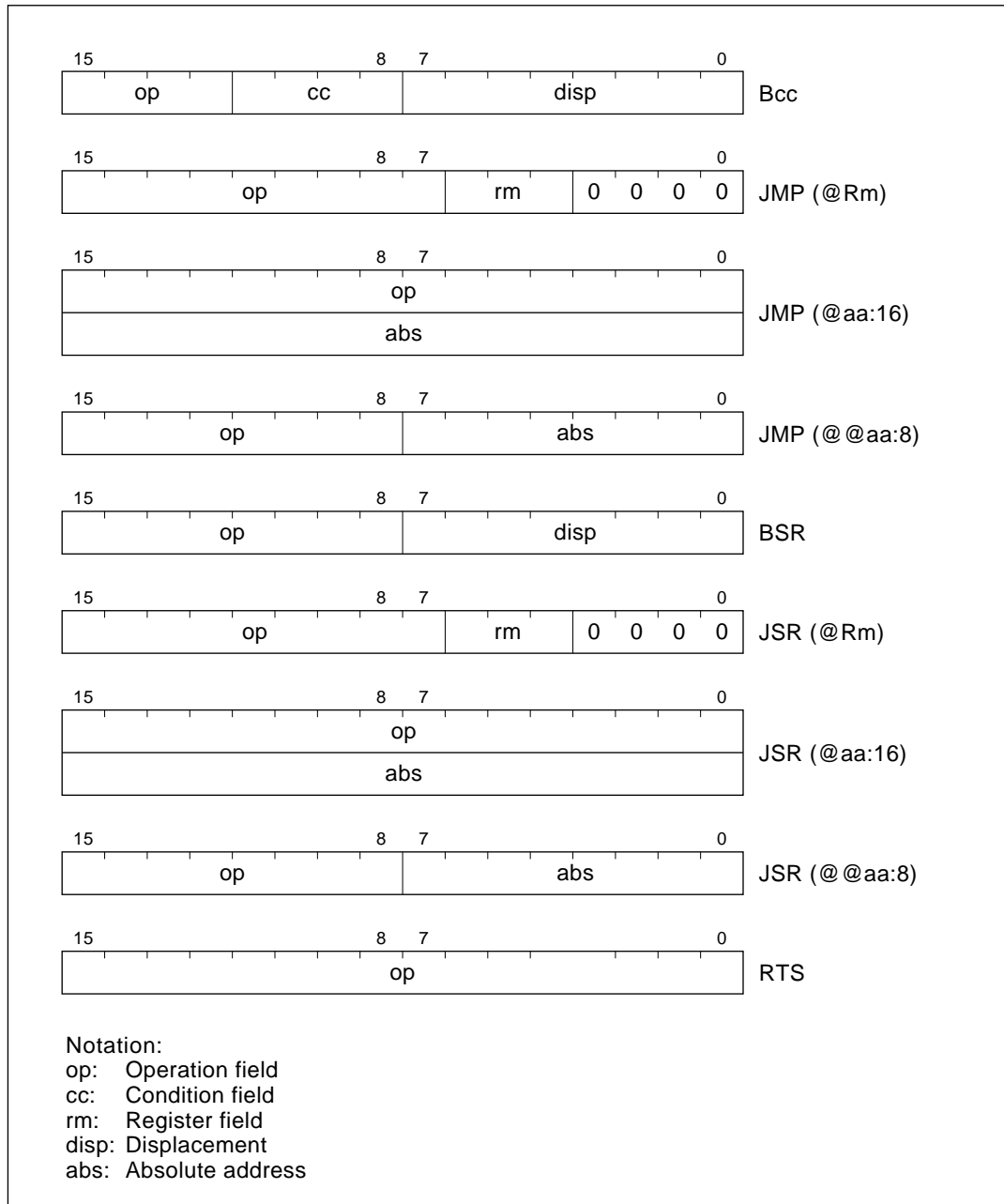


Figure 2-9 Branching Instruction Codes

2.5.7 System Control Instructions

Table 2-10 describes the system control instructions. Figure 2-10 shows their object code formats.

Table 2-10 System Control Instructions

Instruction	Size*	Function
RTE	—	Returns from an exception-handling routine.
SLEEP	—	Causes a transition from active mode to a power-down mode (sleep mode, standby mode, or watch mode), or from subactive mode to watch mode, or from subactive mode via watch mode to active mode. For details, see 3.3, System Modes.
LDC	B	$R_s \rightarrow CCR, \#IMM \rightarrow CCR$ Moves immediate data or general register contents to the condition code register.
STC	B	$CCR \rightarrow R_d$ Copies the condition code register to a specified general register.
ANDC	B	$CCR \wedge \#IMM \rightarrow CCR$ Logically ANDs the condition code register with immediate data.
ORC	B	$CCR \vee \#IMM \rightarrow CCR$ Logically ORs the condition code register with immediate data.
XORC	B	$CCR \oplus \#IMM \rightarrow CCR$ Logically exclusive-ORs the condition code register with immediate data.
NOP	—	$PC + 2 \rightarrow PC$ Only increments the program counter.

Notes: * Size: Operand size
B: Byte

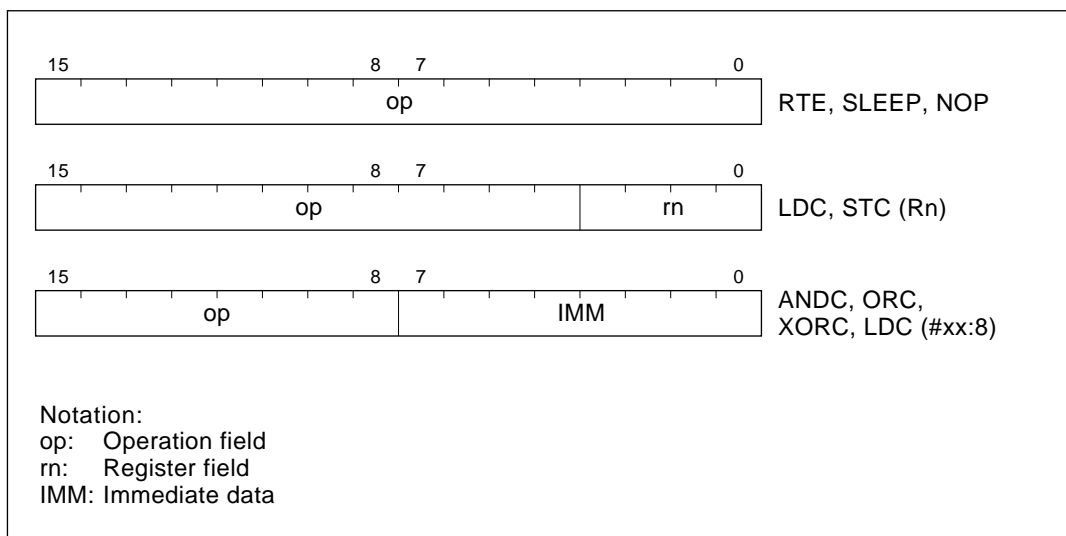


Figure 2-10 System Control Instruction Codes

2.5.8 Block Data Transfer Instruction

Table 2-11 describes the block data transfer instruction. Figure 2-11 shows its object code format.

Table 2-11 Block Data Transfer Instruction

Instruction	Size	Function
EEPMOV	—	<p>If R4L \neq 0 then</p> <p>repeat @R5+ \rightarrow @R6+ R4L - 1 \rightarrow R4L</p> <p>until R4L = 0</p> <p>else next;</p> <p>Moves a data block according to parameters set in general registers R4L, R5, and R6.</p> <p>R4L: Size of block (bytes)</p> <p>R5: Starting source address</p> <p>R6: Starting destination address</p> <p>Execution of the next instruction starts as soon as the block transfer is completed.</p>

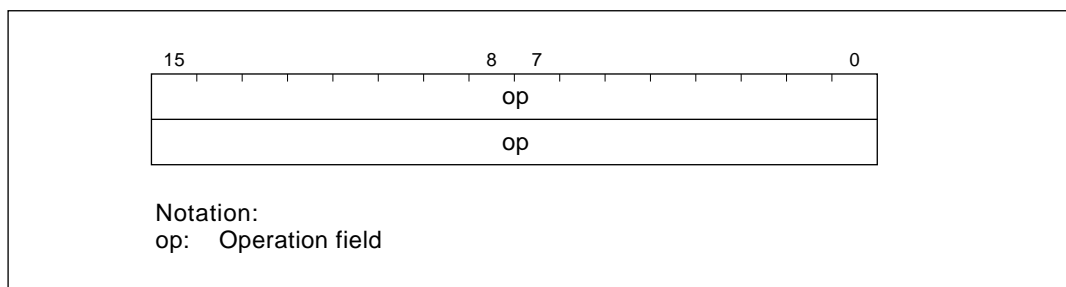
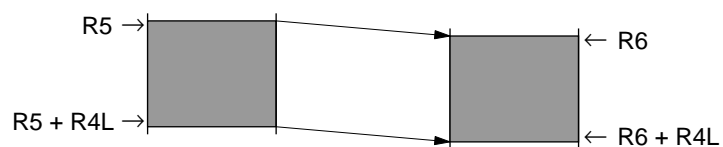


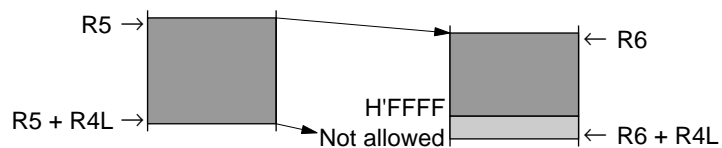
Figure 2-11 Block Data Transfer Instruction Code

Notes on EEPMOV Instruction

1. The EEPMOV instruction is a block data transfer instruction. It moves the number of bytes specified by R4L from the address specified by R5 to the address specified by R6.



2. When setting R4L and R6, make sure that the final destination address ($R6 + R4L$) does not exceed H'FFFF. The value in R6 must not change from H'FFFF to H'0000 during execution of the instruction.



2.6 CPU States

2.6.1 Overview

There are three CPU states: program execution state, program halt state, and exception-handling state. Program execution state includes active mode and subactive mode. In program halt state there are sleep mode, standby mode, and watch mode. These states are shown in figure 2-12. Figure 2-13 shows the state transitions.

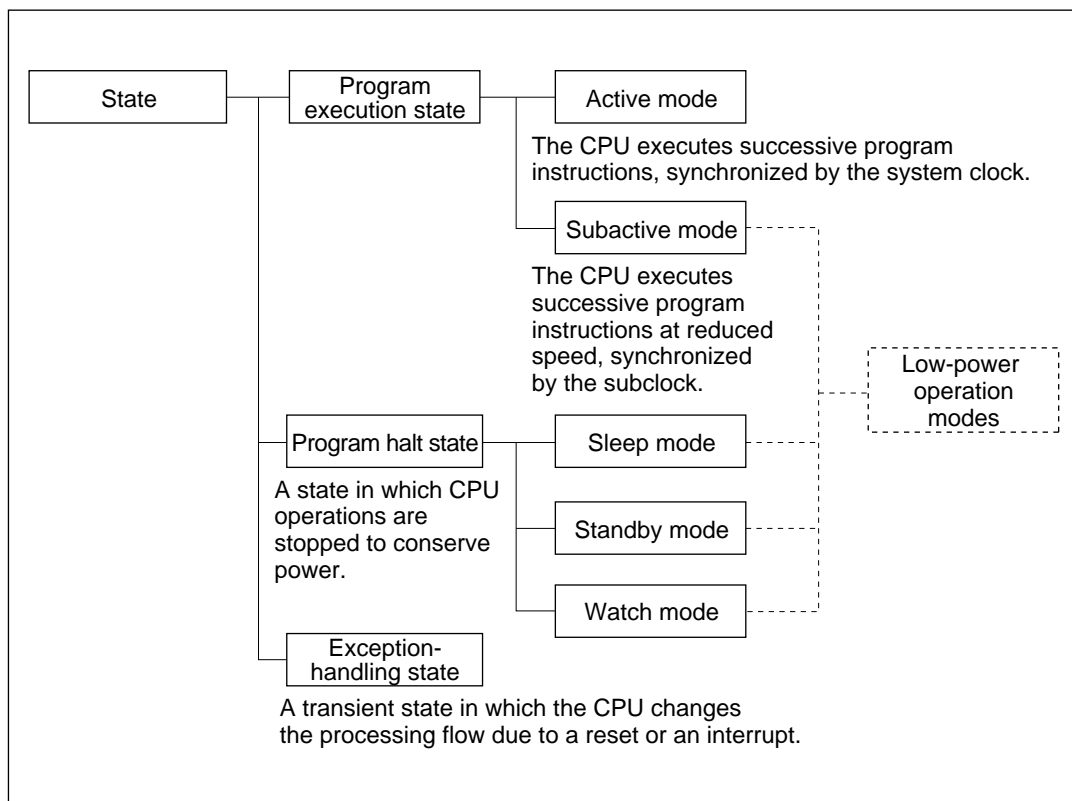


Figure 2-12 CPU Operation States

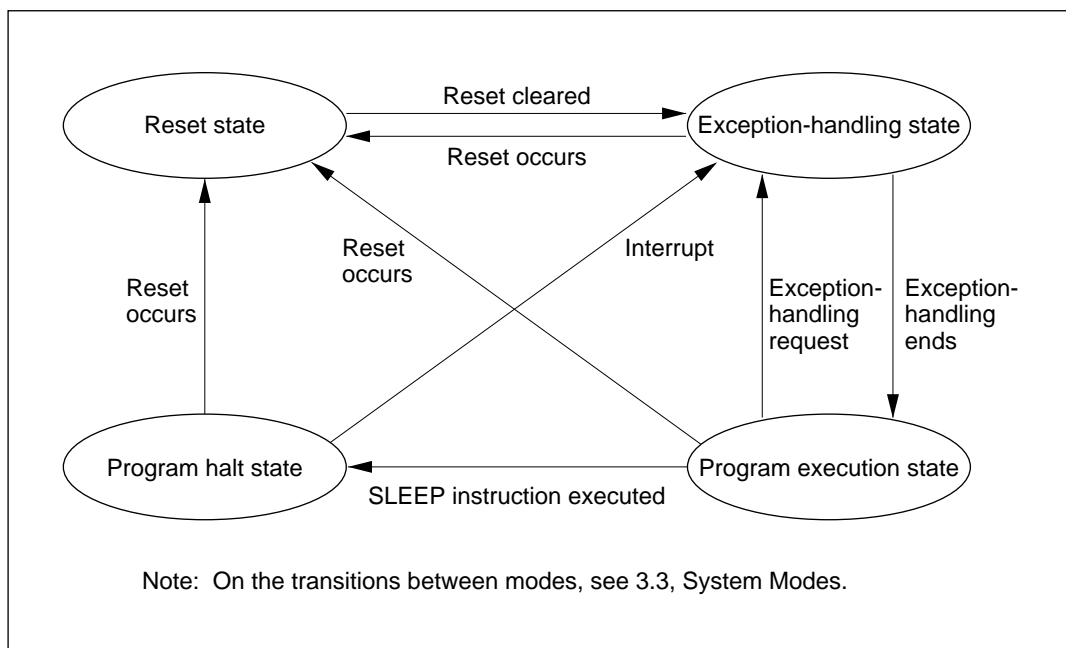


Figure 2-13 State Transitions

2.6.2 Program Execution State

In the program execution state the CPU executes program instructions in sequence.

There are two modes in this state, active mode and subactive mode. Operation is synchronized with the system clock in active mode, and with a subclock in subactive mode. For details on these modes, see 3.3, System Modes.

2.6.3 Program Halt State

In the program halt state there are three modes: sleep mode, standby mode, and watch mode. For details on these modes, see 3.3, System Modes.

2.6.4 Exception-Handling State

The exception-handling state is a transient state occurring when exception handling is started by a reset or interrupt, and the CPU changes its normal processing flow. In exception handling caused by an interrupt, SP (R7) is referenced and the PC and CCR values are saved on the stack.

For details on interrupt handling, see 3.2.2, Interrupts.

2.7 Basic Operation Timing

CPU operation is synchronized by a clock (ϕ_i). ϕ_i is either the system clock (ϕ) generated by the system clock oscillator circuit, or the subclock (ϕ_{SUB}) generated by the subclock oscillator circuit. ϕ_i denotes ϕ in active mode and ϕ_{SUB} in subactive mode. For details, see section 4, Clock Pulse Generators. The period from the rising edge of ϕ_i to the next rising edge is called one state. A memory cycle or bus cycle consists of two states; access to on-chip memory and to on-chip peripheral modules always takes place in two states.

2.7.1 Access to On-Chip Memory (RAM, ROM)

Two-state access is employed for on-chip memory. The data bus width is 16 bits, allowing access in byte or word size. Figure 2-14 shows the on-chip memory access cycle.

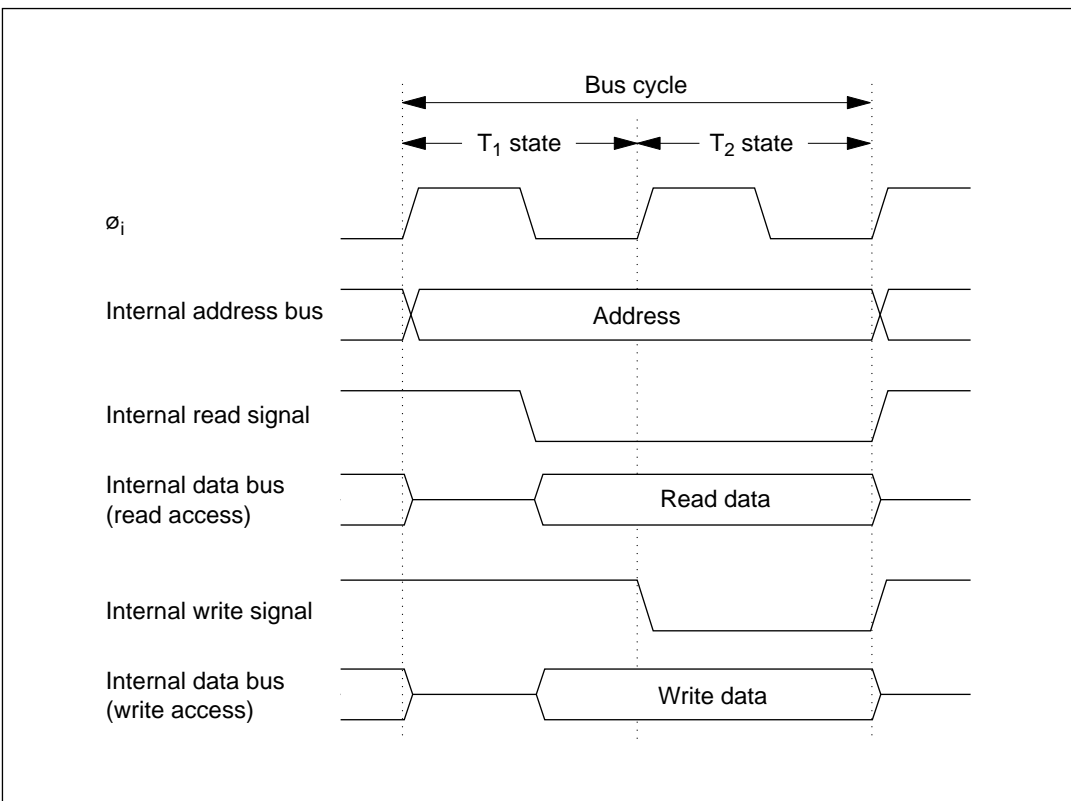


Figure 2-14 On-Chip Memory Access Cycle

2.7.2 Access to On-Chip Peripheral Modules

On-chip peripheral modules are accessed in two states. The data bus width is 8 bits, so access is made in byte size only. This means that two instructions must be used for a word size data access. Figure 2-15 shows the on-chip peripheral module access cycle.

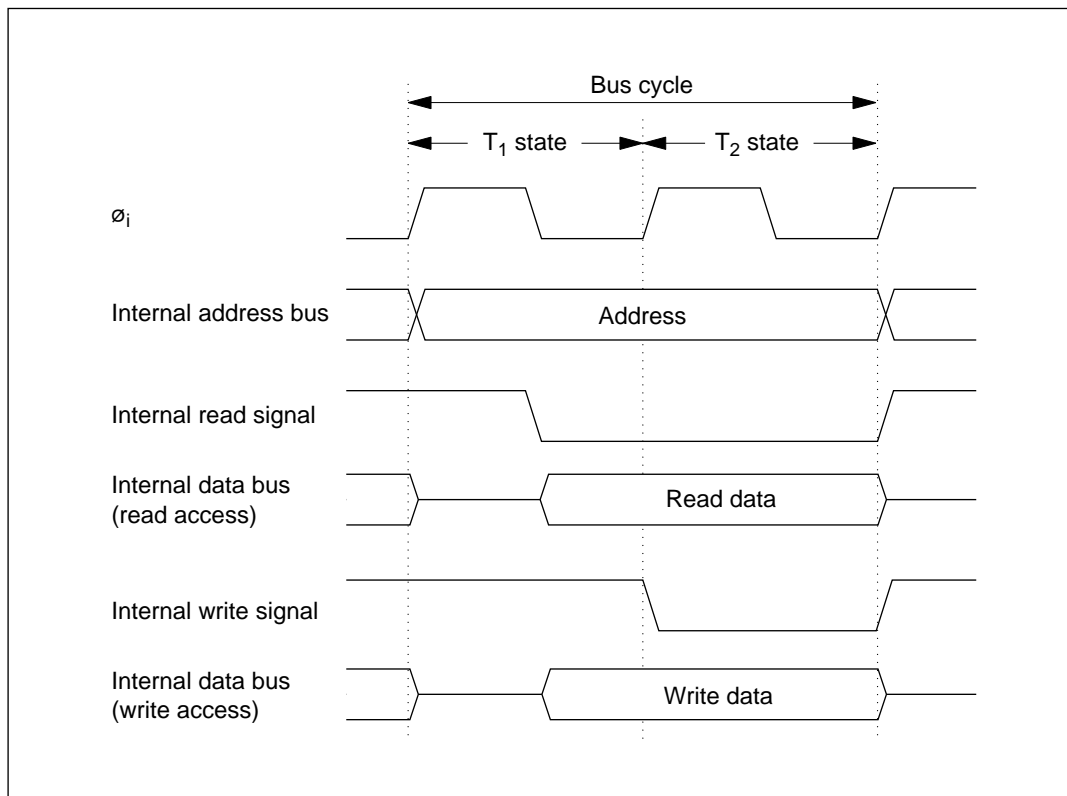


Figure 2-15 On-Chip Peripheral Module Access Cycle

2.8 Application Notes

The following points are to be observed in using the H8/300L CPU.

2.8.1 Notes on Data Access

1. The address space of the H8/300L CPU includes some empty areas in addition to the RAM, registers, and ROM areas available to the user. If these empty areas are mistakenly accessed by an application program, the following results will occur.

Transfer from CPU to empty area:

The transferred data will be lost. This action may also cause the CPU to misoperate.

Transfer from empty area to CPU:

Unpredictable data is transferred.

2. Internal data transfer to or from on-chip modules other than ROM and RAM areas makes use of an 8-bit data width. If word access is attempted to these areas, the following results will occur.

Word access from CPU to I/O register area:

Upper byte: Will be written to I/O register.

Lower byte: Transferred data will be lost.

Word access from I/O register to CPU:

Upper byte: Will be written to upper part of CPU register.

Lower byte: Data written to lower part of CPU register cannot be guaranteed.

Byte size instructions should therefore be used when transferring data to or from I/O registers outside the on-chip ROM and RAM areas. Figure 2-16 shows the data size in which access can be made with on-chip peripheral modules.

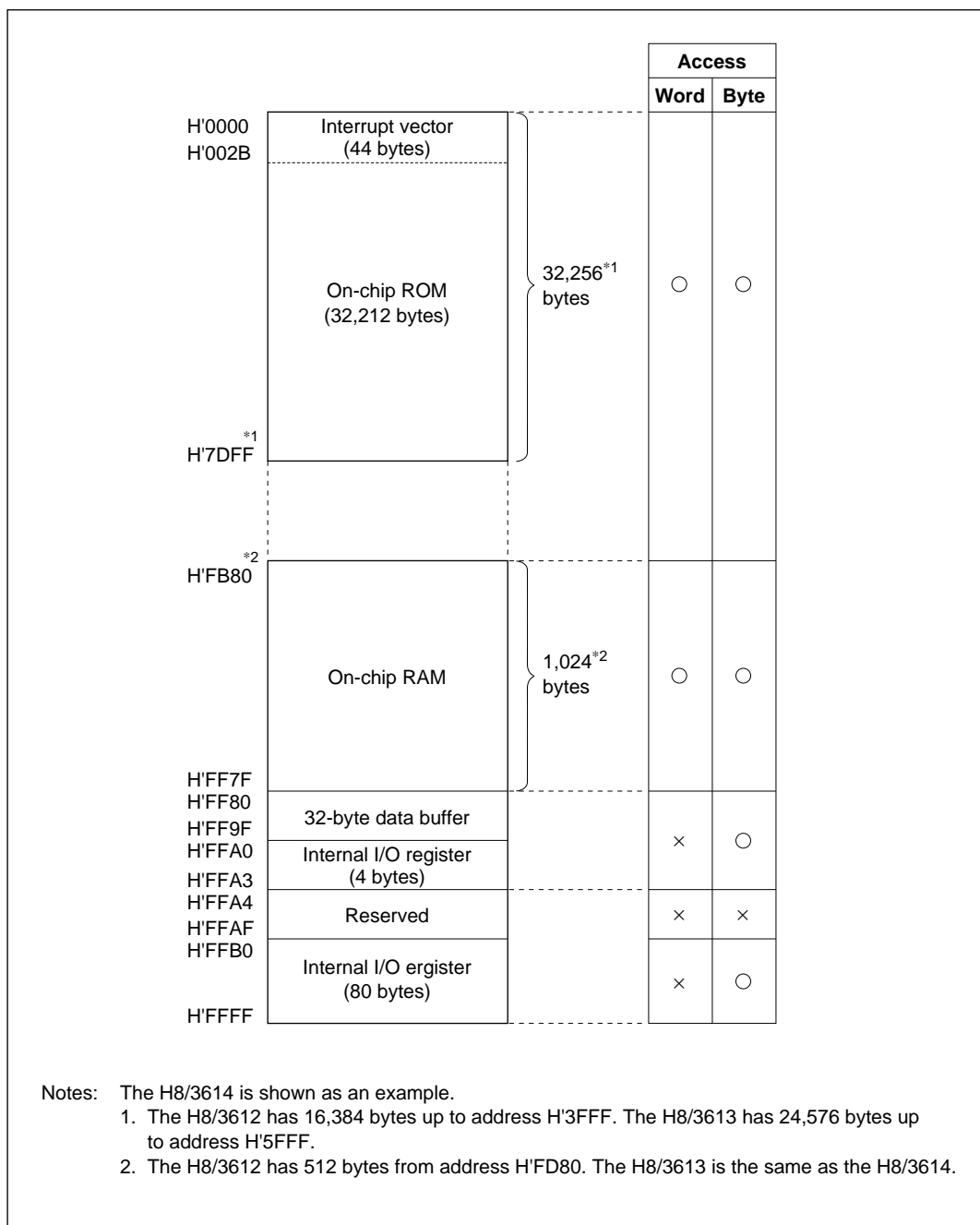


Figure 2-16 Data Size for Access to and from On-Chip Peripheral Modules

2.8.2 Notes on Bit Manipulation

The H8/300L CPU executes bit manipulation instructions by a read-modify-write operation on 8-bit data. When bit manipulation instructions are executed in the cases illustrated below, care must be taken since the operation may affect other bits besides those being manipulated.

1. Bit manipulation in two registers assigned to the same address (when the source and destination are different)

Example 1: Timer load register and timer counter

In this example, a bit manipulation instruction is executed in the timer load register and timer counter of a reloadable timer. Since the timer load register and timer counter share the same address, the operations take place as follows.

- a. Read: The timer counter value at the time is read.
- b. Modify: The CPU modifies (sets or resets) the bit designated with the instruction. (Other bits remain the same.)
- c. Write: The modified data is written to the timer load register.

The timer counter is counting based on the system clock (ϕ), so the value read is not necessarily the same as the value in the timer load register. As a result, bits other than the intended bit in the timer load register may be modified to the timer counter value.

Figure 2-17 shows the reloadable timer configuration.

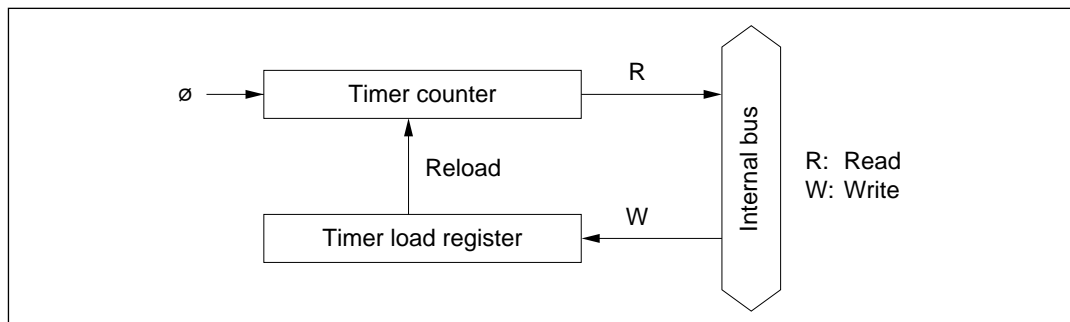


Figure 2-17 Reloadable Timer Configuration

Example 2: Port data register (pin input and data register)

When a bit manipulation instruction is executed designating a port data register, it may cause changes in pin I/O states or data register contents other than the intended bit.

As noted above, the H8/300L CPU executes bit manipulation instructions by a read-modify-write operation on 8-bit data. Since the same address is used for the I/O port data register and reading of pin input, a bit manipulation instruction designating a port functions as follows.

[1] PMOS open-drain pins: pins other than the modified bit

- When set as an input pin (data register = 0)

First the CPU reads the pin input level (read), then it sets or resets the designated bit (modify; other bits remain the same), and writes that value to the data register (write). If the input level is high (read data = 1), a value of 1 is written to the data register, changing the input pin to an output pin (high-level output). If the input level is low, no change occurs.

- When set as an output pin (data register = 1, high-level output)

If the output level is higher than the input high level (V_{IH}), there is no change.

If the output level is lower than the input low level (V_{IL}), a value of 0 is written to the data register, so that the PMOS buffer transistor is turned off resulting in pull-down (low level) or high-impedance state.

If the output level is pulled down by the load to an intermediate level, the resulting state is indeterminate.

and I/O pins: pins other than the modified bit

- When set as an input pin

The CPU reads the pin input level and writes that value to the data register, which may or may not result in a change to the data register contents.

- When set as an output pin

The data register is read, so no change occurs.

2. Bit manipulation in a register containing a write-only bit

Example: PWM data register, etc.

(Note that read and write characteristics can differ from bit to bit.)

Write-only bits cannot be read. Write-only bits other than the intended bit are set to 1.

Table 2-12 lists the registers that share the same address, while table 2-13 lists the registers that contain write-only bits.

Table 2-12 Registers Assigned to the Same Address

Register Name	Abbreviation	Address
Timer load register B/Timer counter B	TLB/TCB	H'FFC3
Timer load register C/Timer counter C	TLC/TCC	H'FFC5
Timer load register E/Timer counter E	TLE/TCE	H'FFC9
Port data register 1*	PDR1	H'FFD1
Port data register 2*	PDR2	H'FFD2
Port data register 4*	PDR4	H'FFD4
Port data register 8*	PDR8	H'FFD8
Port data register 9*	PDR9	H'FFD9
Port data register A*	PDRA	H'FFDA

Note: * These port data registers are used also for pin input.

Table 2-13 Registers with Write-Only Bits

Register Name	Abbreviation	Address
Serial mode register 1	SMR1	H'FFB0
PWM control register* ¹	PWCR	H'FFCC
PWM data register U* ¹	PWDRU	H'FFCD
PWN data register L* ¹	PWDRL	H'FFCE
Port control register 1	PCR1	H'FFE1
Port control register 2	PCR2	H'FFE2
Port control register 8	PCR8	H'FFE8
Port control register 9	PCR9	H'FFE9
Port control register A	PCRA	H'FFEA
Port mode register 0	PMR0	H'FFEF
Timer mode register D* ²	TMD	H'FFC6
System control register 2* ³	SYSCR2	H'FFF1

Notes: 1. Not present in the H8/3612.

2. Only bit CRL (bit 7) is write-only.

3. Bit DTON (bit 3) is a write-only bit only in subactive mode. In active mode it cannot be read or written.

Section 3 System Control

3.1 Overview

This section explains the reset state, exception handling, and system modes.

3.2 Exception Handling

Exception handling includes processing of reset exceptions and of interrupts. Table 3-1 summarizes the exception sources and their priorities. Reset exception handling has the highest priority.

Table 3-1 Types of Exception Handling and Priorities

Priority	Exception Source	Timing for Start of Exception Handling
High ↑	Reset	Reset exception handling starts as soon as $\overline{\text{RES}}$ pin changes from low to high.
Low	Interrupt	When interrupt request is made, interrupt exception handling starts after execution of present instruction is completed.

3.2.1 Reset

When the $\overline{\text{RES}}$ pin goes low, all processing stops and the chip enters the reset state. The internal state of the CPU and the registers of on-chip peripheral modules are initialized. The I bit of the condition code register (CCR) is set, masking all interrupts.

As soon as the $\overline{\text{RES}}$ pin goes from low to high, reset exception handling starts. The contents of the reset vector address (H'0000 to H'0001) are read and loaded into the program counter (PC). Then program execution starts from the address indicated in PC. Figure 3-1 shows the reset sequence.

- Notes:
1. To make sure a reset is carried out properly, when power is turned on the $\overline{\text{RES}}$ pin should be held low for at least 20 ms (ceramic oscillator) or 40 ms (crystal oscillator) after the power supply starts up.
 2. When resetting during operation, keep the $\overline{\text{RES}}$ pin at low level for at least 10 system clock cycles.
 3. After a reset, if an interrupt were to be accepted before the stack pointer (SP: R7) was initialized, PC and CCR would not be pushed onto the stack correctly, resulting in program runaway. To prevent this, immediately after reset exception handling all interrupts are masked. Programs should be coded to initialize the stack pointer before clearing the interrupt mask. An even-numbered address must be set in SP. It is recommended that programs start with an instruction initializing SP (e.g., MOV.W #xx:16, SP).

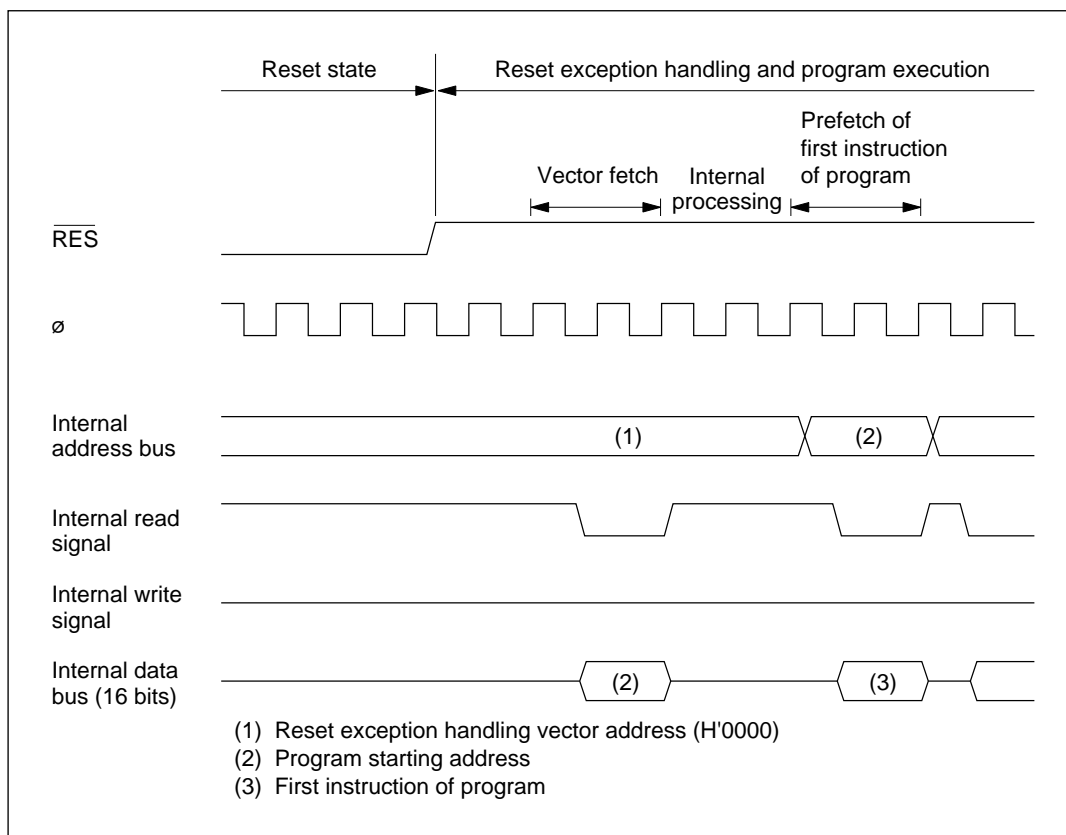


Figure 3-1 Reset Sequence

3.2.2 Interrupts

The interrupt sources include external interrupts ($\overline{\text{IRQ}}_5$ to $\overline{\text{IRQ}}_0$), and internal interrupts requested from on-chip peripheral modules. Table 3-2 shows the interrupt sources, their priorities, and their vector addresses. When more than one interrupt is requested, the interrupt with the highest priority is processed.

The interrupts have the following features.

1. Both internal and external interrupts ($\overline{\text{IRQ}}_5$ to $\overline{\text{IRQ}}_0$) can be masked by the I bit of CCR. When this bit is set to 1, the interrupt request flag is set but interrupts cannot be accepted.
2. The external interrupt pins $\overline{\text{IRQ}}_4$, $\overline{\text{IRQ}}_1$, and $\overline{\text{IRQ}}_0$ can each be set independently to either rising-edge sensing or falling-edge sensing. The remaining external interrupt pins, $\overline{\text{IRQ}}_5$, $\overline{\text{IRQ}}_3$, and $\overline{\text{IRQ}}_2$, are fixed at falling-edge sensing.

Table 3-2 Interrupt Sources

Priority	Interrupt	Origin of Interrupt	Vector Starting Address
<div>High</div> <div>↑</div>	Reset	External pin	H'0000
	(Reserved)* ¹	—	H'0002
			H'0004
			H'0006
	IRQ ₀	External pin	H'0008
	IRQ ₁		H'000A
	IRQ ₂		H'000C
	IRQ ₃		H'000E
	IRQ ₄		H'0010
	IRQ ₅		H'0012
	(Reserved)* ¹	—	H'0014
	Timer A overflow	Timer A	H'0016
	Timer B overflow	Timer B	H'0018
	Timer C overflow	Timer C	H'001A
	Timer D overflow	Timer D	H'001C
	Timer E overflow	Timer E	H'001E
	Direct transfer	Standby timer activator* ²	H'0020
	(Reserved)* ¹	—	H'0022
			H'0024
	SCI1 transfer complete, error	Serial communication interface 1	H'0026
	SCI2 transfer complete, error	Serial communication interface 2	H'0028
	A/D conversion complete	A/D converter	H'002A
Low			

Notes: 1. Vector addresses indicated as “Reserved” cannot be used.

2. This circuit is triggered by a SLEEP instruction and generates an interrupt after a certain time.

3.2.3 Interrupt Control Registers

Table 3-3 lists the registers that are used to control interrupts.

Table 3-3 Interrupt Control Registers

Register Name	Abbreviation	R/W	Initial Value	Address
Port mode register 1	PMR1	R/W	H'00	H'FFEB
IRQ edge select register	IEGR	R/W	H'EC	H'FFF2
Interrupt enable register 1	IENR1	R/W	H'C0	H'FFF3
Interrupt enable register 2	IENR2	R/W	H'00	H'FFF4
Interrupt enable register 3	IENR3	R/W	H'3C	H'FFF5
Interrupt request register 1	IRR1	R/W*	H'C0	H'FFF6
Interrupt request register 2	IRR2	R/W*	H'00	H'FFF7
Interrupt request register 3	IRR3	R/W*	H'3C	H'FFF8

Note: * Only a write of 0 for flag clearing is possible.

1. Port mode register 1 (PMR1)

Bit	7	6	5	4	3	2	1	0
	NOISE CANCEL	EVENT	IRQC5	IRQC4	IRQC3	IRQC2	IRQC1	IRQC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMR1 is an 8-bit read/write register that designates whether pins in port 1 are used for general-purpose I/O or for external interrupt input. It is also used to turn the noise canceller function of pin $\overline{\text{IRQ}}_0$ on or off.

Note: Before switching a pin function by modifying bits IRQ5 to IRQ0 in PMR1, first clear the interrupt enable flag to disable the interrupt. After the pin function has been switched, issue any instruction, then clear the interrupt request flag to 0.

Program example:

```

.....
MOV. B R0L, @IENR1 ..... Disable interrupt
MOV. B R0L, @PMR1 ..... Change pin function
NOP ..... Issue any instruction
MOV. B R0L, @IRR1 ..... Clear interrupt request flag
MOV. B R1L, @IENR1 ..... Enable interrupt
.....

```

Bit 7: Noise cancel (NOISE CANCEL)

This bit enables or disables the noise canceller function of pin $\overline{\text{IRQ}}_0$.

Bit 7**NOISE CANCEL****Description**

0	Disables the noise canceller function of pin $\overline{\text{IRQ}}_0$. (initial value)
1	Enables the noise canceller function of pin $\overline{\text{IRQ}}_0$. Input is sampled at intervals of 256 states. If two consecutive values do not match, the input is regarded as noise.

Bit 6: P1₆/ $\overline{\text{EVENT}}$ pin function switch (EVENT)**Bit 6****EVENT****Description**

0	P1 ₆ / $\overline{\text{EVENT}}$ pin functions as P1 ₆ pin. (initial value)
1	P1 ₆ / $\overline{\text{EVENT}}$ pin functions as $\overline{\text{EVENT}}$ pin.

Bit 5: P1₅/ $\overline{\text{IRQ}}_5$ /TMOE pin function switch (IRQC5)**Bit 5****IRQC5****Description**

0	P1 ₅ / $\overline{\text{IRQ}}_5$ /TMOE pin functions as P1 ₅ /TMOE pin.* (initial value)
1	P1 ₅ / $\overline{\text{IRQ}}_5$ /TMOE pin functions as $\overline{\text{IRQ}}_5$ pin.

Note: * On use of this pin as TMOE pin, see 5.3.2, Port Mode Register 4 (PMR4).

Bit 4: P1₄/ $\overline{\text{IRQ}}_4$ pin function switch (IRQC4)**Bit 4****IRQC4****Description**

0	P1 ₄ / $\overline{\text{IRQ}}_4$ pin functions as P1 ₄ pin. (initial value)
1	P1 ₄ / $\overline{\text{IRQ}}_4$ pin functions as $\overline{\text{IRQ}}_4$ pin.

Bit 3: P1₃/ $\overline{\text{IRQ}}_3$ pin function switch (IRQC3)**Bit 3****IRQC3****Description**

0	P1 ₃ / $\overline{\text{IRQ}}_3$ pin functions as P1 ₃ pin. (initial value)
1	P1 ₃ / $\overline{\text{IRQ}}_3$ pin functions as $\overline{\text{IRQ}}_3$ pin.

Bit 2: $P1_2/\overline{IRQ}_2$ pin function switch (IRQC2)

Bit 2 IRQC2	Description
0	$P1_2/\overline{IRQ}_2$ pin functions as $P1_2$ pin. (initial value)
1	$P1_2/\overline{IRQ}_2$ pin functions as \overline{IRQ}_2 pin.

Bit 1: $P1_1/\overline{IRQ}_1$ pin function switch (IRQC1)

Bit 1 IRQC1	Description
0	$P1_1/\overline{IRQ}_1$ pin functions as $P1_1$ pin. (initial value)
1	$P1_1/\overline{IRQ}_1$ pin functions as \overline{IRQ}_1 pin.

Bit 0: $P1_0/\overline{IRQ}_0$ pin function switch (IRQC0)

Bit 0 IRQC0	Description
0	$P1_0/\overline{IRQ}_0$ pin functions as $P1_0$ pin. (initial value)
1	$P1_0/\overline{IRQ}_0$ pin functions as \overline{IRQ}_0 pin.

2. IRQ edge select register (IEGR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	IEG4	—	—	IEG1	IEG0
Initial value	1	1	1	0	1	1	0	0
Read/Write	—	—	—	R/W	—	—	R/W	R/W

IEGR is an 8-bit read/write register, used to designate whether pins \overline{IRQ}_0 , \overline{IRQ}_1 , and \overline{IRQ}_4 are set to rising edge sensing or falling edge sensing.

Bits 7 to 5: Reserved bits

Bits 7 to 5 are reserved; they are always read as 1, and cannot be modified.

Bit 4: \overline{IRQ}_4 pin input edge select (IEG4)

Bit 4 IEG4	Description
0	Falling edge of \overline{IRQ}_4 pin input is detected. (initial value)
1	Rising edge of \overline{IRQ}_4 pin input is detected.

Bits 3 and 2: Reserved bits

Bits 3 and 2 are reserved; they are always read as 1, and cannot be modified.

Bit 1: $\overline{\text{IRQ}}_1$ pin input edge select (IEG1)

Bit 1 IEG1	Description
0	Falling edge of $\overline{\text{IRQ}}_1$ pin input is detected. (initial value)
1	Rising edge of $\overline{\text{IRQ}}_1$ pin input is detected.

Bit 0: $\overline{\text{IRQ}}_0$ pin input edge select (IEG0)

Bit 0 IEG0	Description
0	Falling edge of $\overline{\text{IRQ}}_0$ pin input is detected. (initial value)
1	Rising edge of $\overline{\text{IRQ}}_0$ pin input is detected.

3. Interrupt enable register 1 (IENR1)

Bit	7	6	5	4	3	2	1	0
	—	—	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

IENR1 is an 8-bit read/write register that enables or disables external interrupts.

Bits 7 and 6: Reserved bits

Bits 7 and 6 are reserved; they are always read as 1, and cannot be modified.

Bits 5 to 0: IRQ_5 to IRQ_0 interrupt enable (IEN5 to IEN0)

Bits 5 to 0 IEN5 to IEN0	Description
0	Disables interrupt requests by IRR15 to IRR10. (initial value)
1	Enables interrupt requests by IRR15 to IRR10.

4. Interrupt enable register 2 (IENR2)

Bit	7	6	5	4	3	2	1	0
	—	—	IENDT	IENTE	IENDT	IENTC	IENB	IENTA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IENR2 is an 8-bit read/write register that enables or disables direct transfer interrupts and timer A to E overflow interrupts.

Bits 7 and 6: Reserved bits

Bits 7 and 6 are reserved, but they can be written and read.

Bit 5: Direct transfer interrupt enable (IENDT)

Bit 5 IENDT	Description
0	Disables direct transfer interrupt requests by IRRDT. (initial value)
1	Enables interrupt requests by IRRDT.

Bits 4 to 0: Timer E to A interrupt enable (IENTE to IENTA)

Bits 4 to 0 IENTE to IENTA	Description
0	Disables interrupt requests by IRRTE to IRRTA. (initial value)
1	Enables interrupt requests by IRRTE to IRRTA.

5. Interrupt enable register 3 (IENR3)

Bit	7	6	5	4	3	2	1	0
	IENAD	—	—	—	—	—	IENS2	IENS1
Initial value	0	0	1	1	1	1	0	0
Read/Write	R/W	R/W	—	—	—	—	R/W	R/W

IENR3 is an 8-bit read/write register that enables or disables interrupts from the A/D converter and serial communication interfaces 1 and 2.

Bit 7: A/D conversion complete interrupt enable (IENAD)

Bit 7

IENAD	Description
0	Disables interrupt requests by IRRAD. (initial value)
1	Enables interrupt requests by IRRAD.

Bit 6: Reserved bit

Bit 6 is reserved, but it can be written and read.

Bits 5 to 2: Reserved bits

Bits 5 to 2 are reserved; they are always read as 1, and cannot be modified.

Bits 1 and 0: Serial communication interface 2 and 1 interrupt enable (IENS2 and IENS1)

Bits 1, 0

IENS2, IENS1	Description
0	Disables interrupt requests by IRRS2 and IRRS1. (initial value)
1	Enables interrupt requests by IRRS2 and IRRS1.

6. Interrupt request register 1 (IRR1)

Bit	7	6	5	4	3	2	1	0
	—	—	IRRI5	IRRI4	IRRI3	IRRI2	IRRI1	IRRI0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Note: * Only a write of 0 for flag clearing is possible.

IRR1 is an 8-bit read/write register with flags that are set to 1 when an external interrupt is requested.

Bits 7 and 6: Reserved bits

Bits 7 and 6 are reserved; they are always read as 1, and cannot be modified.

Bits 5 to 0: \overline{IRQ}_5 to \overline{IRQ}_0 interrupt request (IRRI5 to IRRIO)

Bits 5 to 0 IRRI5 to IRRIO	Description
0	No interrupt request from the corresponding pin (\overline{IRQ}_5 to \overline{IRQ}_0). (initial value)
1	<p>Setting conditions: Set when the corresponding pin (\overline{IRQ}_5 to \overline{IRQ}_0) designated for interrupt input in PMR1 and the designated edge is input.</p> <p>Clearing method: Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)</p>

7. Interrupt request register 2 (IRR2)

Bit	7	6	5	4	3	2	1	0
	—	—	IRRDT	IR RTE	IRRTD	IRRTC	IRRTB	IRRTA
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Note: * Only a write of 0 for flag clearing is possible.

IRR2 is an 8-bit read/write register with flags that are set to 1 when a direct transfer interrupt or timer A to E overflow interrupt is requested.

Bits 7 and 6: Reserved bits

Bits 7 and 6 are reserved; they are always read as 0, and only 0 may be written.

Bit 5: Direct transfer interrupt request (IRRDT)

Bit 5 IRRDT	Description
0	No direct transfer interrupt request. (initial value)
1	<p>Setting conditions: In subactive mode, when the system control register 2 (SYSCR2) DTON bit = 1, the system control register 1 (SYSCR1) LSON bit = 0, and the interrupt enable register 2 (IENR2) IENDT bit = 1, execution of a SLEEP instruction results in direct transfer to active mode via watch mode. During this process a direct transfer interrupt is requested and the IRRDT flag is set to 1.</p> <p>Clearing method: Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)</p>

Bits 4 to 0: Timers E to A interrupt request (IRRTE to IRRTA)

Bits 4 to 0

IRRTE to IRRTA	Description
0	No overflow interrupt request from the corresponding timer (E to A). (initial value)
1	<p>Setting conditions: When a timer E to A overflow interrupt is requested, the corresponding flag (IRRTE to IRRTA) is set to 1.</p> <p>Clearing method: Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)</p>

8. Interrupt request register 3 (IRR3)

Bit	7	6	5	4	3	2	1	0
	IRRAD	—	—	—	—	—	IRRS2	IRRS1
Initial value	0	0	1	1	1	1	0	0
Read/Write	R/W*	—	—	—	—	—	R/W*	R/W*

Note: * Only a write of 0 for flag clearing is possible.

Bit 7: A/D conversion complete interrupt request (IRRAD)

Bit 7

IRRAD	Description
0	No A/D conversion complete interrupt request. (initial value)
1	<p>Setting conditions: When the A/D converter completes A/D conversion, an interrupt is requested and the IRRAD flag is set to 1.</p> <p>Clearing method: Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)</p>

Bit 6: Reserved bit

Bit 6 is reserved; it is always read as 0, and only 0 may be written.

Bits 5 to 2: Reserved bits

Bits 5 to 2 are reserved; they are always read as 1, and cannot be modified.

Bits 1 and 0: Serial communication interface 2 and 1 interrupt request (IRRS2, IRRS1)

Bits 1, 0	
IRRS2, IRRS1	Description
0	No transfer complete or error interrupt request by the corresponding serial communication interface. (initial value)
1	<p>Setting conditions: When an interrupt is requested due to transfer complete or error on serial communication interface 2 or 1, the corresponding flag (IRRS2 or IRRS1) is set to 1.</p> <p>Clearing method: Cleared when software writes 0 in the flag. (The flag is not automatically cleared when an interrupt is accepted.)</p>

3.2.4 External Interrupts

There are six external interrupts, IRQ₅ to IRQ₀. These interrupts are requested by means of input signals at pins $\overline{\text{IRQ}}_5$ to $\overline{\text{IRQ}}_0$.

Interrupts IRQ₄, IRQ₁, and IRQ₀ are detected by either rising edge sensing or falling edge sensing, depending on the settings of bits IEG4, IEG1, and IEG0 in the IRQ edge select register (IEGR). The other external interrupts, IRQ₅, IRQ₃, and IRQ₂, are detected by falling edge sensing only. In order to enable external interrupt input, it is first necessary to set the corresponding bit in port mode register 1 (PMR1) to 1.

When the designated edge is input at pins $\overline{\text{IRQ}}_5$ to $\overline{\text{IRQ}}_0$, the corresponding flag in interrupt request register 1 (IRR1) is set to 1. After the interrupt is accepted, the flag that was set is not automatically cleared, so the interrupt handling routine must be programmed to clear the flag to 0. A given interrupt request can be disabled by clearing its interrupt enable flag to 0.

Interrupts IRQ₅ to IRQ₀ are enabled by setting bits IEN5 to IEN0 to 1 in interrupt enable register 1. All interrupts can be masked by setting the I bit in CCR to 1.

When IRQ₅ to IRQ₀ interrupt requests are accepted, the I bit is set to 1. The order of priority is from IRQ₀ (high) to IRQ₅ (low). For details see table 3-2.

A noise canceller function can be selected for IRQ₀ interrupts, in which case a noise cancellation circuit samples the IRQ₀ input every 256 states. If two consecutive sampling results do not match, noise is assumed and the request is not accepted.

3.2.5 Internal Interrupts

There are nine internal interrupts that can be requested by the on-chip peripheral modules. These interrupts can be masked (held pending) by setting the I bit in CCR to 1. When an internal interrupt request is accepted and an interrupt handler is executed, the I bit is set to 1. For the order of priority of interrupts from on-chip peripheral modules, see table 3-2.

3.2.6 Interrupt Operations

Interrupts are controlled by an interrupt controller. Figure 3-2 shows a block diagram of the interrupt controller, while figure 3-3 shows the flow up to interrupt acceptance.

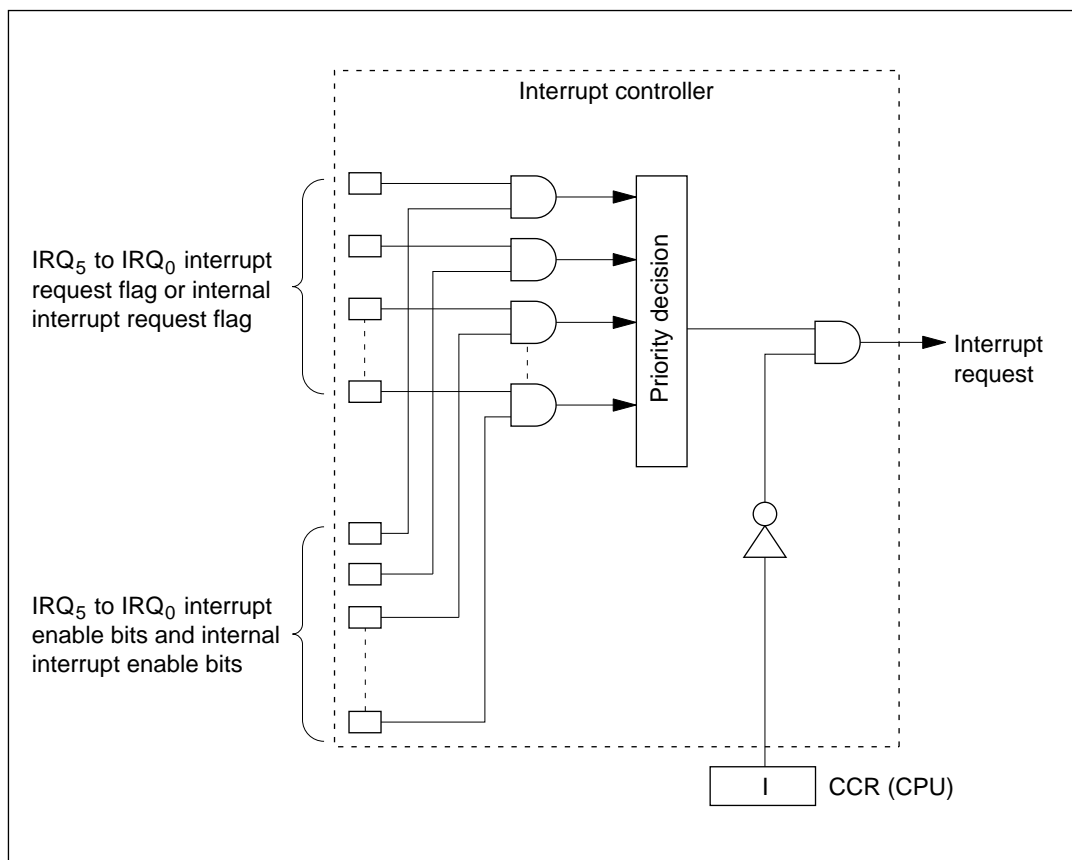


Figure 3-2 Block Diagram of Interrupt Controller

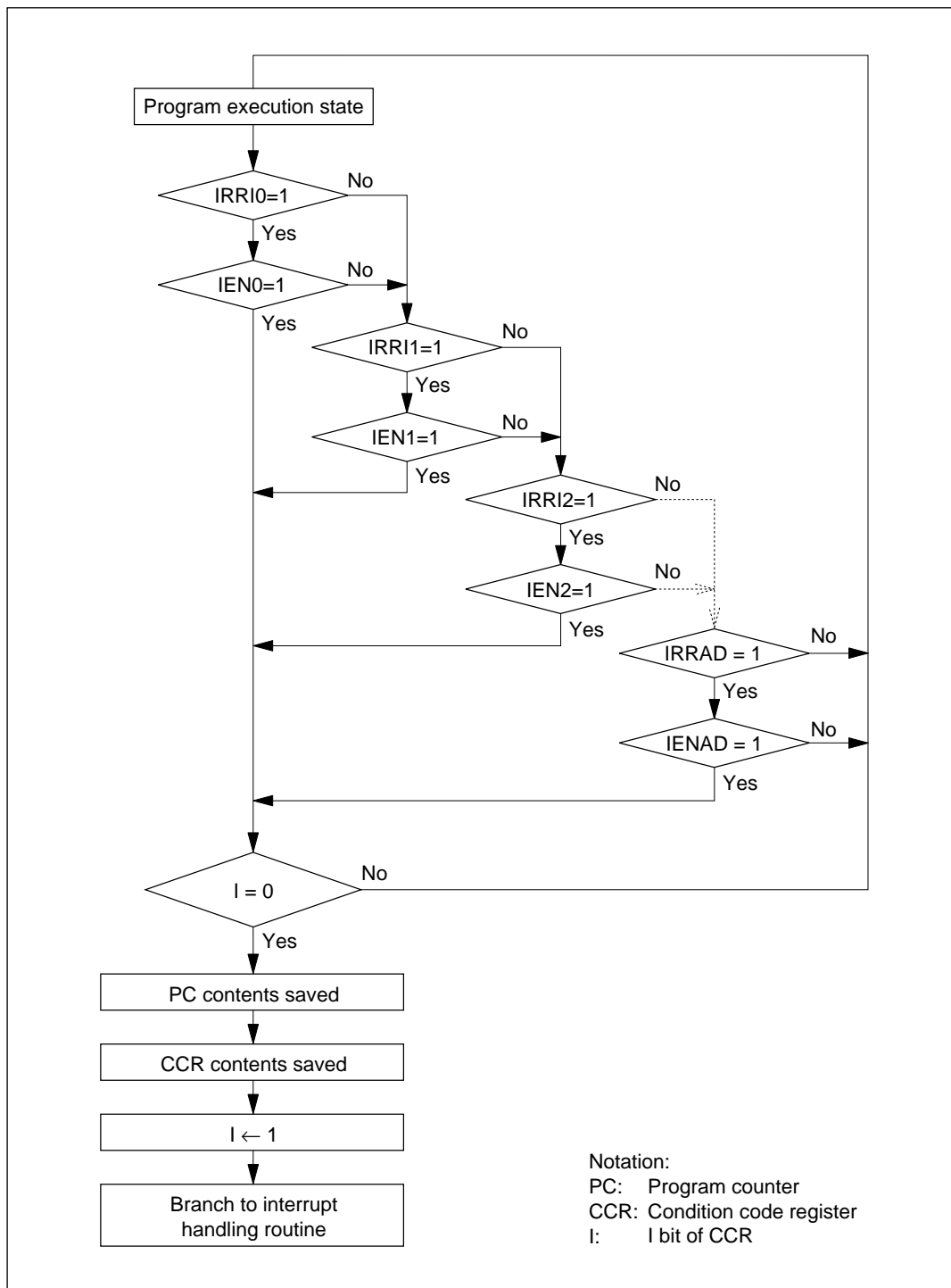


Figure 3-3 Flow up to Interrupt Acceptance

The following operations take place when an interrupt occurs.

1. When an interrupt is requested by external interrupt pin input or by a peripheral module, an interrupt request signal is sent to the interrupt controller.
2. When the interrupt controller receives an interrupt request signal, it sets the interrupt request flag.
3. From among the interrupts for which the corresponding interrupt enable bit is also set to 1, the interrupt controller selects the interrupt request with the highest priority and holds the others pending. (See table 3-2.)
4. The interrupt controller checks the I bit of CCR. If the I bit is 0, the selected interrupt request is accepted; if the I bit is 1, the interrupt request is held pending.
5. If the interrupt is accepted, after processing of the current instruction is completed, both PC and CCR are pushed onto the stack. The state of the stack at this time is shown in figure 3-4. The PC value pushed onto the stack is the address of the first instruction to be executed upon return from interrupt handling.
6. The I bit of CCR is set to 1, masking all further interrupts.
7. A vector address is generated for the accepted interrupt, and the contents of that address are read and loaded into PC. Program execution then resumes from the address indicated in PC.

Note: No interrupt detection takes place immediately after completion of ORC, ANDC, XORC, or LDC instructions.

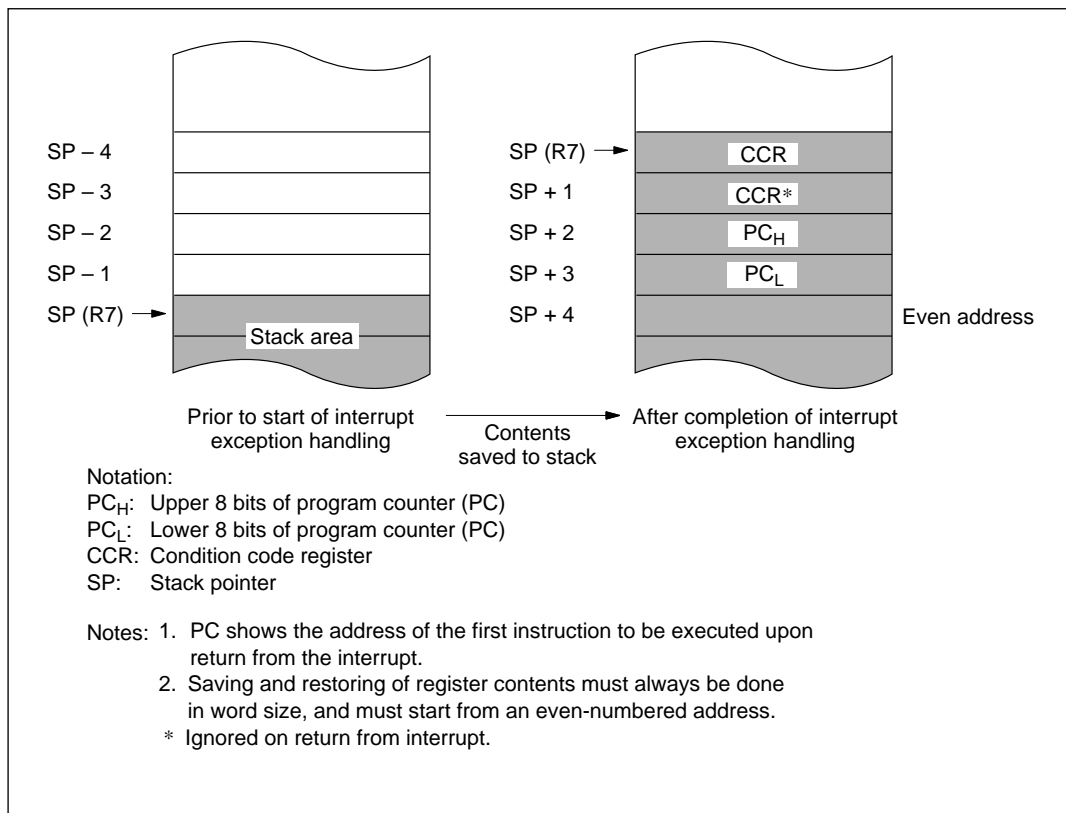
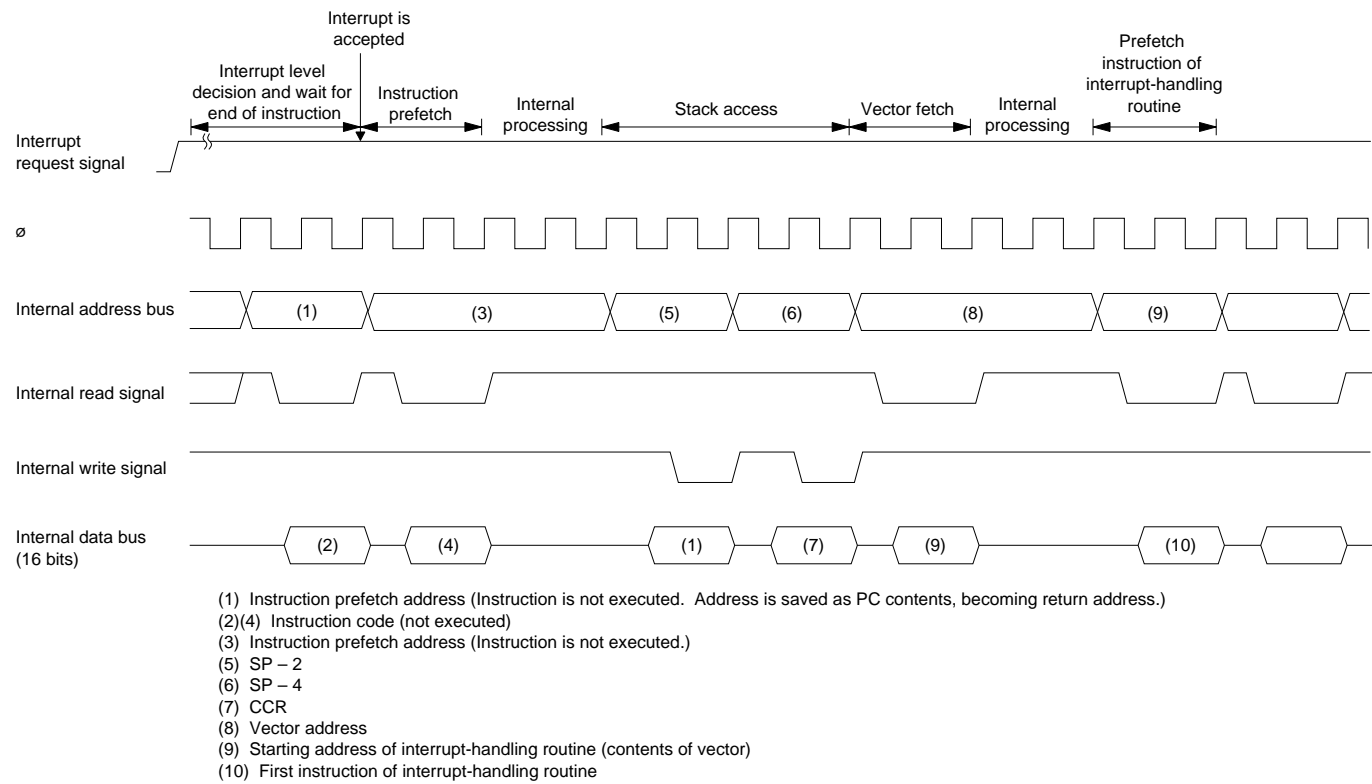


Figure 3-4 Stack State after Completion of Interrupt Exception Handling

Figure 3-5 shows a typical interrupt sequence.

Figure 3-5 Interrupt Sequence



3.2.7 Return from an Interrupt

After completion of interrupt handling, the handler routine ends by executing an RTE instruction, to resume the original program from the point of the interrupt. When RTE is executed, the values saved on the stack are restored to CCR and PC as shown in figure 3-6. Instruction execution resumes from the address indicated in PC.

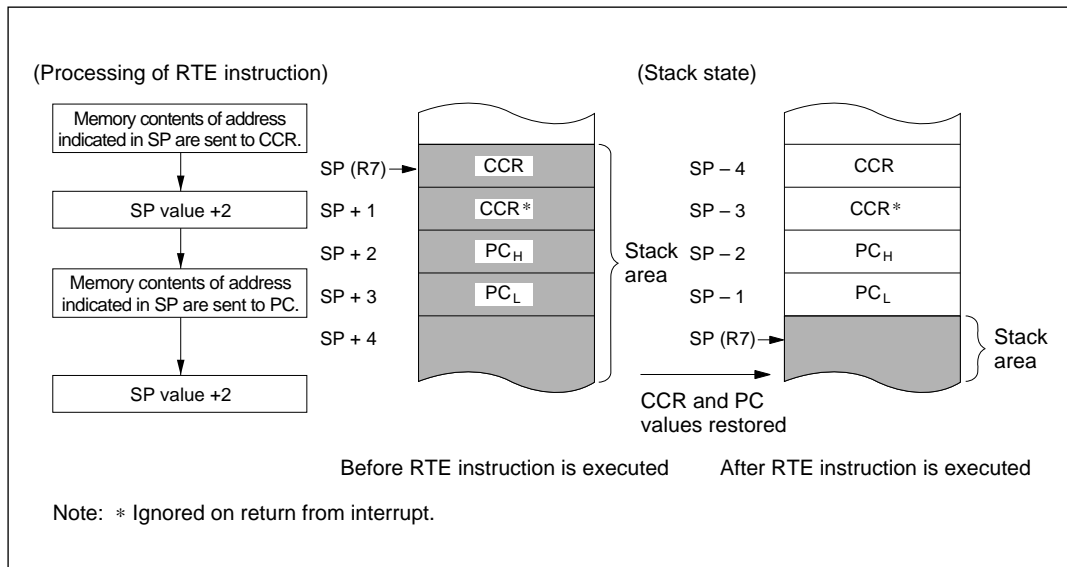


Figure 3-6 Stack State When RTE Instruction is Executed

3.2.8 Interrupt Response Time

Table 3-4 shows the number of wait states after an interrupt request flag is set and until the first instruction of the interrupt handler is executed.

Table 3-4 Interrupt Wait States

No.	Item	States
1	Waiting time for completion of executing instruction*	1 to 13
2	Saving of PC and CCR to stack	4
3	Vector fetch	2
4	Instruction fetch	4
5	Internal processing	4
Total		15 to 27

Note: * Not including EEPMOV instruction.

3.2.9 Valid Interrupts in Each Mode

Table 3-5 shows the valid interrupts in each mode. For details of the modes, see 3.3, System Modes.

Table 3-5 Valid Interrupts in Each Mode

Interrupt	Mode				
	Active	Sleep	Standby	Watch	Subactive
IRQ ₀	○	○	○	○	○
IRQ ₁	○	○	○	×	×
IRQ ₂	○	×	×	×	×
IRQ ₃	○	×	×	×	×
IRQ ₄	○	×	×	×	×
IRQ ₅	○	×	×	×	×
Timer A overflow	○	○	×	○	○
Timer B overflow	○	×	×	×	×
Timer C overflow	○	×	×	×	×
Timer D overflow	○	×	×	×	×
Timer E overflow	○	×	×	×	×
Direct transfer	×	×	×	×	△
SCI1 transfer complete or error	○	×	×	×	×
SCI2 transfer complete or error	○	×	×	×	×
A/D conversion end	○	×	×	×	×

Note: The above table does not include interrupts occurring during a mode transition.

Notation:

- : When an interrupt request flag is set, interrupt exception handling is started if the I bit = 0 in CCR and the interrupt enable bit = 1 for that interrupt. In sleep mode, standby mode, and watch mode, a mode transition takes place before interrupt exception handling starts.
- △: When a SLEEP instruction is executed while the DTON bit = 1 and the LSON bit = 0, first a transition is made to watch mode and the interrupt request flag is set in synchronization with the subclock. When the interrupt request flag is set, if the interrupt enable bit = 1 for that interrupt and the I bit = 0 in CCR, a transition is made to active mode and interrupt exception handling starts.
- ×: The interrupt request flag is not set, and no mode transition occurs.

3.2.10 Notes on Stack Area Use

When word data is accessed in the H8/300L Series, the least significant bit of the address is regarded as 0. Access to the stack always takes place in word size, so the stack pointer (SP: R7) should never indicate an odd address. Use PUSH Rn (MOV.W Rn, @-SP) or POP Rn (MOV.W @SP+, Rn) to save or restore register values.

Setting an odd address in SP may cause a program to crash. An example is shown in figure 3-7.

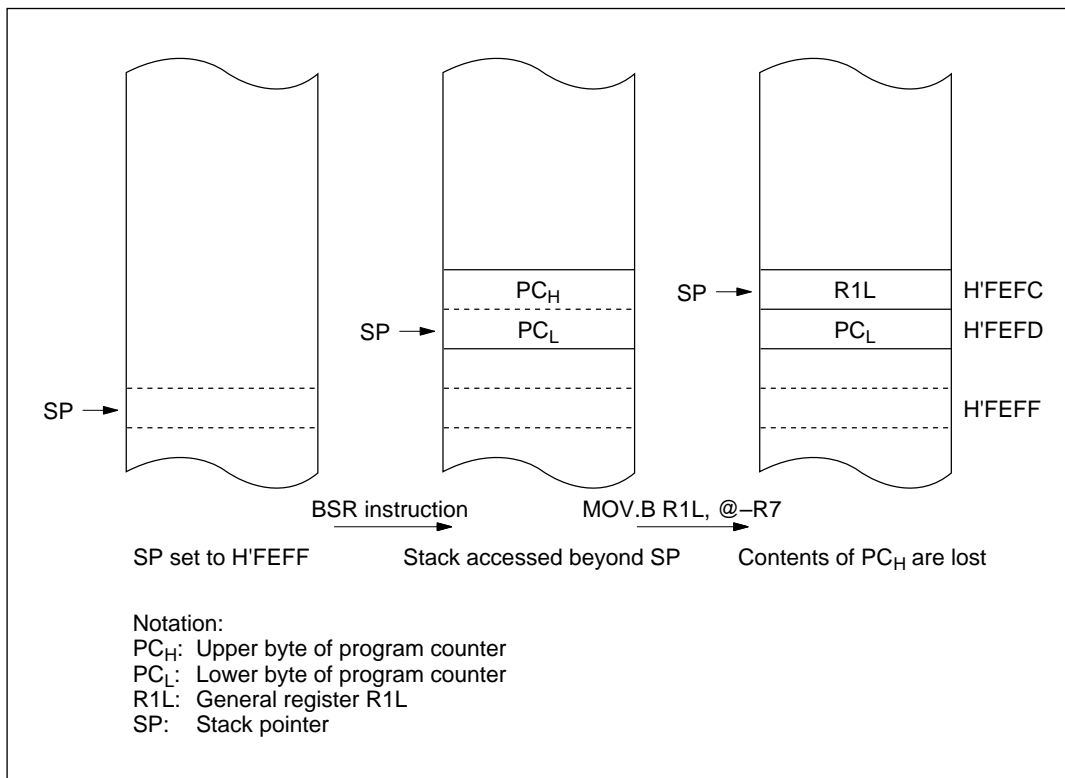


Figure 3-7 CPU Operation When Odd Address is Set in SP

Word access is also performed when the condition code register (CCR) is saved and restored by the interrupt exception-handling sequence and RTE instruction. When CCR is saved, the CCR value is saved in both the upper and lower bytes of the word data. When CCR is restored, it is loaded with the value at the even address. The value at the odd address is ignored.

3.2.11 Note on Clearing Interrupt Request Registers

When bits in IRR1, IRR2, and IRR3 are cleared, if an interrupt is requested during execution of the clearing instruction, setting of the interrupt request flag takes priority.

3.3 System Modes

3.3.1 Overview

The H8/3614 Series has five modes, including power-down modes with reduced power dissipation. Table 3-6 summarizes the modes.

Table 3-6 Modes

Mode	Description
Active mode	The CPU executes programs on the system clock
Power-down modes	Sleep mode The CPU halts, but the time-base function of timer A operates on the system clock
	Standby mode The CPU and all on-chip peripheral modules halt
	Watch mode The CPU halts, but the time-base function of timer A operates on the subclock
	Subactive mode The CPU and the time-base function of timer A operate on the subclock

Figure 3-8 shows the transitions among these modes.

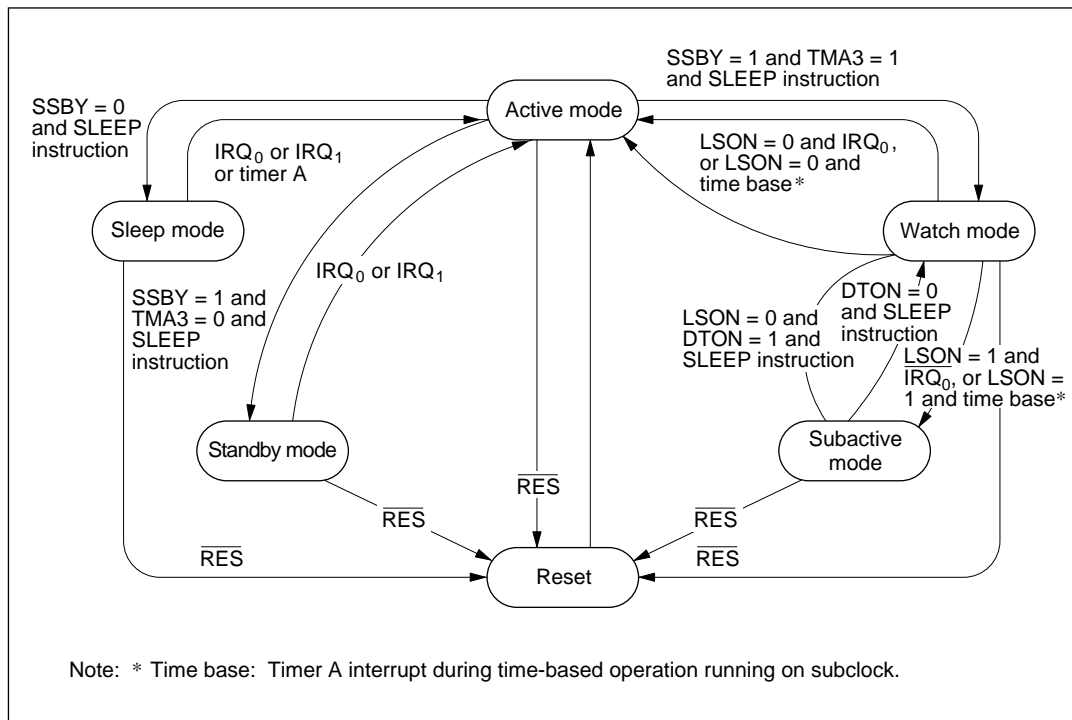


Figure 3-8 System Mode Transition Diagram

Table 3-7 shows the internal states in each mode.

Table 3-7 Internal States in Operation Modes

Function		Active	Sleep	Standby	Watch	Subactive
System clock		Functions	Functions	Halted	Halted	Halted
Subclock		Functions	Functions	Functions	Functions	Functions
CPU operation	Instruction	Functions	Halted	Halted	Halted	Functions
	RAM	Functions	Retained	Retained	Retained	Functions
	Register	Functions	Retained	Retained	Retained	Functions
	I/O	Functions	Retained	Retained* ¹	Retained* ¹	Functions* ²
Peripheral module interrupts	IRQ ₀	Functions	Functions	Functions	Functions	Functions
	IRQ ₁	Functions	Functions	Functions	Retained	Retained
	IRQ ₂ to IRQ ₅	Functions	Retained	Retained	Retained	Retained
	Timer A	Functions	Functions	Retained	Functions* ³	Functions* ³
	Timer B	Functions	Retained	Retained	Retained	Retained
	Timer C	Functions	Retained	Retained	Retained	Retained
	Timer D	Functions	Retained	Retained	Retained	Retained
	Timer E	Functions	Retained	Retained	Retained	Retained
	SCI1, SCI2	Functions	Retained	Retained	Retained	Retained
	PWM	Functions	Retained	Retained	Retained	Retained
	A/D	Functions	Retained	Retained	Retained	Retained

Notes: 1. Register contents retained; output high-impedance.
2. Register contents retained; output high-impedance; ports can be read.
3. Functions when the time base function is selected.

3.3.2 Active Mode

In active mode, the CPU executes programs in synchronization with the system clock.

3.3.3 Sleep Mode

- Transition to sleep mode

The system goes from active mode to sleep mode when a SLEEP instruction is executed while the SSBY bit in system control register 1 (SYSCR1) is cleared to 0. In this mode CPU operation is halted but the register, RAM, and port contents are retained. The clock pulse generator operates, as do external interrupts (IRQ₁ and IRQ₀) and timer A.

- Clearing sleep mode

Sleep mode is cleared by an interrupt (IRQ₁, IRQ₀, or timer A) or by input at the $\overline{\text{RES}}$ pin.

— Clearing by interrupt (IRQ₁, IRQ₀, or timer A)

When an IRQ₁, IRQ₀, or timer A interrupt is requested, sleep mode is cleared and interrupt exception handling starts. Sleep mode is not cleared if the I bit in the condition code register (CCR) is set to 1 or the particular interrupt is disabled in the interrupt enable register.

Before transition to sleep mode, other interrupts should be disabled.

— Clearing by $\overline{\text{RES}}$ input

When the $\overline{\text{RES}}$ pin goes low, the CPU goes into the reset state and sleep mode is cleared.

3.3.4 Standby Mode

- Transition to standby mode

The system goes from active mode to standby mode when a SLEEP instruction is executed while the SSBY bit in system control register 1 (SYSCR1) is set to 1 and bit TMA3 in timer mode register A (TMA) is cleared to 0. In standby mode the clock pulse generator stops, so the CPU and on-chip peripheral modules stop functioning. As long as a minimum required voltage is applied, the CPU register contents and data in the on-chip RAM will be retained. The I/O ports go to the high-impedance state.

- Clearing standby mode

Standby mode is cleared by an external interrupt (IRQ₁, IRQ₀) or by input at the $\overline{\text{RES}}$ pin.

— Clearing by interrupt (IRQ₁, IRQ₀)

When an IRQ₁ or IRQ₀ interrupt signal is input, the clock pulse generator starts. After the time set in bits STS2 to STS0 in system control register 1 (SYSCR1) has elapsed, a stable clock signal is supplied to the entire chip, standby mode is cleared, and interrupt exception handling starts. Before the transition to standby mode, other interrupts should be disabled. Standby mode is not cleared if the I bit in the condition code register (CCR) is set to 1 or the particular interrupt is disabled in the interrupt enable register.

— Clearing by $\overline{\text{RES}}$ input

When the $\overline{\text{RES}}$ pin goes low, the clock pulse generator starts and standby mode is cleared. After the pulse generator output has stabilized, if the $\overline{\text{RES}}$ pin is driven high, the CPU starts reset exception handling.

Since clock signals are supplied to the entire chip as soon as the clock pulse generator starts functioning, the $\overline{\text{RES}}$ pin should be kept at the low level until the pulse generator output stabilizes.

3.3.5 Watch Mode

- Transition to watch mode

The system goes from active mode to watch mode when a SLEEP instruction is executed while the SSBY bit in SYSCR1 is set to 1 and bit TMA3 in TMA is set to 1. The system also goes from subactive mode to watch mode when a SLEEP instruction is executed while the DTON bit in system control register 2 (SYSCR2) is cleared to 0.

In watch mode, operation of the system clock pulse generator and of on-chip peripheral modules is halted, except for the time-base function of timer A. Output from the on-chip peripheral modules is reset; but as long as a minimum required voltage is applied, the contents of the internal registers of the CPU and on-chip peripheral modules, and the on-chip RAM contents, are retained.

- Clearing watch mode

Watch mode is cleared by a time-base interrupt from timer A, by an IRQ_0 interrupt, or by input at the \overline{RES} pin.

- Clearing by timer A time-base interrupt or IRQ_0 interrupt

When timer A overflows or an IRQ_0 interrupt signal is input, if the LSON bit in system control register 1 (SYSCR1) is cleared to 0, the clock pulse generator starts. After the time set in bits STS2 to STS0 in system control register 1 (SYSCR1) has elapsed, a stable clock signal is supplied to the entire chip, watch mode is cleared, and interrupt exception handling starts. If LSON = 1, the system goes to subactive mode.

In watch mode, the subclock (ϕ_{SUB}) is prescaled to generate a clock signal which is supplied to timer A. Timer A operates as a time base.

Before the transition to watch mode, other external interrupts should be disabled. Watch mode is not cleared if the I bit in the condition code register (CCR) is set to 1 or the particular interrupt is disabled in the interrupt enable register.

- Clearing by \overline{RES} input

Clearing by the \overline{RES} pin is as described in 3.3.4, Standby Mode.

3.3.6 Subactive Mode

- Transition to subactive mode

The system goes from watch mode to subactive mode if the LSON bit in system control register 1 (SYSCR1) is set to 1 at the time of a timer A time-base interrupt or IRQ_0 interrupt request.

In subactive mode, the CPU operates in synchronization with the subclock (ϕ_{SUB}). The on-chip peripheral modules halt operation, except for the time base function of timer A. Output from the on-chip peripheral modules is reset; but as long as a minimum required voltage is applied, the contents of the internal registers of the on-chip peripheral modules are retained. The I/O ports go to the high-impedance state.

- Clearing subactive mode

Subactive mode is cleared by a SLEEP instruction or by input at the $\overline{\text{RES}}$ pin.

— Clearing by SLEEP instruction

When a SLEEP instruction is executed in subactive mode, subactive mode is cleared.

If the DTON bit of system control register 2 (SYSCR2) is cleared to 0 when the SLEEP instruction is executed, the system goes to watch mode. If DTON = 1 and LSON = 0, a direct transfer interrupt is requested and the clock pulse generator starts. After the time set in bits STS2 to STS0 in system control register 1 (SYSCR1) has elapsed, a stable clock signal is supplied to the entire chip, and the system goes to active mode.

Before the transition to active mode, other interrupts should be disabled. The direct transfer from subactive mode to active mode does not take place if the I bit in the condition code register (CCR) is set to 1 or the direct transfer interrupt is disabled in the interrupt enable register.

— Clearing by $\overline{\text{RES}}$ input

Clearing by the $\overline{\text{RES}}$ pin is as described in 3.3.4, Standby Mode.

3.3.7 Application Notes

1. In order to ensure sufficient time for the clock pulse generator to reach stable operation after clearing of standby mode or watch mode, or after direct transfer from subactive to active mode, bits STS2–STS0 in system control register 1 (SYSCR1) should be set as follows.

- When a ceramic oscillator is used

Set bits STS2–STS0 for a waiting time of at least 10 ms (see figure 3-9). For details, see 3.4.1, System Control Register 1 (SYSCR1).

- When an external clock is used

Any values may be set. Normally the minimum time ($STS2 = STS1 = STS0 = 0$) should be set.

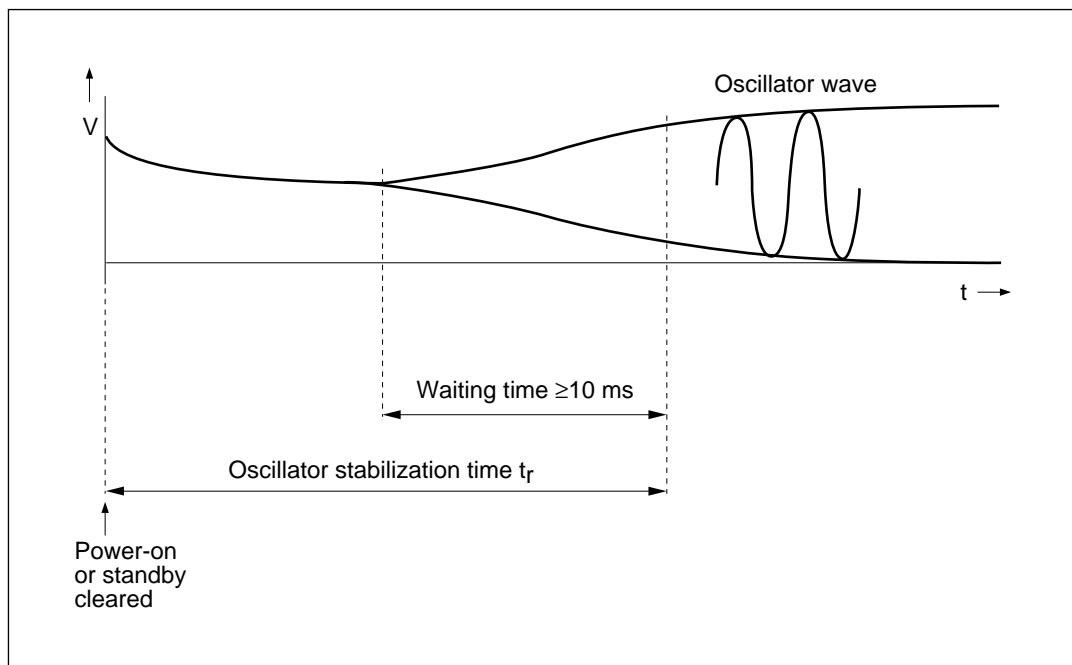


Figure 3-9 Waiting Time

2. To make a transition from subactive mode to active mode, the LSON bit in SYSCR1 should be cleared to 0 and the DTON bit in system control register 2 (SYSCR2) should be set to 1. Direct transfer is not possible when the LSON bit = 1.

3.4 System Control Registers

Table 3-7 shows how the system control registers (SYSCR1 and SYSCR2) are configured. These two registers are used to control the power-down modes.

Table 3-7 Register Configuration

Name	Abbreviation	R/W	Initial Value	Address
System control register 1	SYSCR1	R/W	H'00	H'FFF0
System control register 2	SYSCR2	R/W	H'F4	H'FFF1

3.4.1 System Control Register 1 (SYSCR1)

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	LSON	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*	R/W	R/W	R/W	R/W	R/W	—	—

Note: * Write is enabled only in active mode.

SYSCR1 is an 8-bit read/write register for control of power-down modes.

Bit 7: Standby (SSBY)

This bit designates transition to standby mode or watch mode.

When standby mode is cleared by an external interrupt and the system goes to active mode, this bit remains set to 1. It must be cleared by writing a 0. Writing is possible only in active mode.

Bit 7

SSBY	Explanation
0	When a SLEEP instruction is executed, a transition is made to sleep mode. (initial value)
1	When a SLEEP instruction is executed, a transition is made to standby mode or watch mode.

Bits 6 to 4: Standby timer select 2 to 0 (STS2 to STS0)

When a mode in which the system clock is stopped (standby, watch, or subactive mode) is cleared, the system waits for stable clock operation for a time set in these bits. The designation should be made according to the clock frequency so that the waiting time is at least 10 ms.

Bit 6 STS2	Bit 5 STS1	Bit 4 STS0	Explanation
0	0	0	Wait time = 8,192 states. (initial value)
0	0	1	Wait time = 16,384 states.
0	1	0	Wait time = 32,768 states.
0	1	1	Wait time = 65,536 states.
1	*	*	Wait time = 131,072 states.

Note: * Don't care.

Bit 3: Low speed on flag (LSON)

This bit chooses the system clock (ϕ) or subclock (ϕ_{SUB}) as the CPU operating clock when watch mode is cleared. Since this relates to the transitions between operation modes, this bit functions in combination with other control bits and interrupt input.

Bit 3 LSON	Explanation
0	The CPU operates on the system clock (ϕ). (initial value)
1	The CPU operates on the subclock (ϕ_{SUB}).

Bit 2: Reserved bit

This bit is reserved, but it can be written and read.

Bits 1 and 0: Reserved bits

These bits are reserved; they are always read as 0, and cannot be modified.

3.4.2 System Control Register 2 (SYSCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	DTON	—	—	—
Initial value	1	1	1	1	0	1	0	0
Read/Write	—	—	—	—	W*	—	—	—

Note: * Write is enabled only in subactive mode.

SYSCR2 is an 8-bit read/write register for control of direct transfer from subactive mode to active mode.

Bits 7 to 4: Reserved bits

These bits are reserved; they are always read as 1, and cannot be modified.

Bit 3: Direct transfer on flag (DTON)

This bit designates whether a transition is made to active mode or to watch mode when a SLEEP instruction is executed in subactive mode. When transfer to active mode is designated, the transition takes place via watch mode to allow time for the clock pulse generator to stabilize.

Bit 3

DTON	Explanation
0	When a SLEEP instruction is executed in subactive mode, a transition is (initial value) made to watch mode.
1	When a SLEEP instruction is executed in subactive mode while the LSON bit in system control register 1 (SYSCR1) is cleared to 0, a direct transfer interrupt is requested, and the system goes to active mode via watch mode.

Bit 2: Reserved bit

This bit is reserved; it is always read as 1, and cannot be modified.

Bits 1 and 0: Reserved bits

These bits are reserved; they are always read as 0, and cannot be modified.

Section 4 Clock Pulse Generators

4.1 Overview

Clock oscillator circuitry (CPG: Clock Pulse Generator) is provided on-chip, including both a system clock pulse generator and a subclock pulse generator. The system clock pulse generator consists of a system clock oscillator, system clock divider, and a clock divider (prescaler S) for the on-chip peripheral modules. The subclock pulse generator consists of a subclock oscillator, subclock divider, and a further subclock divider (prescaler W) for time-base use.

4.1.1 Block Diagram

Figure 4-1 shows a block diagram of the clock pulse generators.

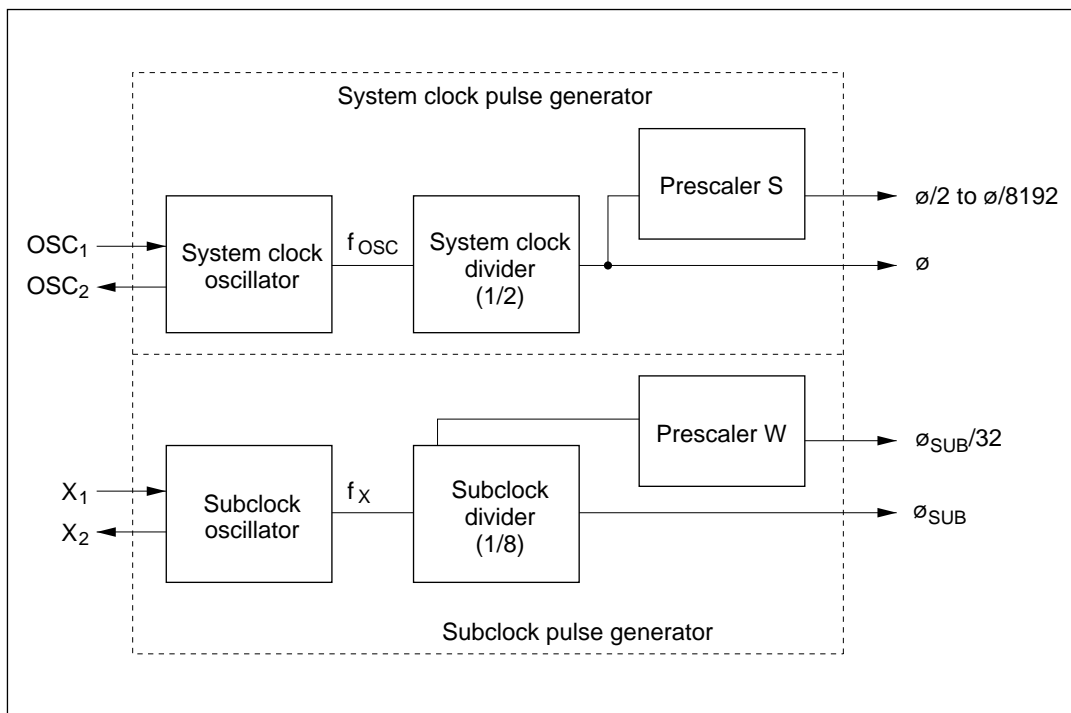


Figure 4-1 Block Diagram of Clock Pulse Generators

4.2 System Clock Generator

Clock pulses can be supplied to the system clock divider either by connecting a crystal or ceramic oscillator, or by providing external clock input.

1. Connecting a crystal oscillator

- Circuit configuration

Figure 4-2 shows a typical method of connecting a crystal oscillator.

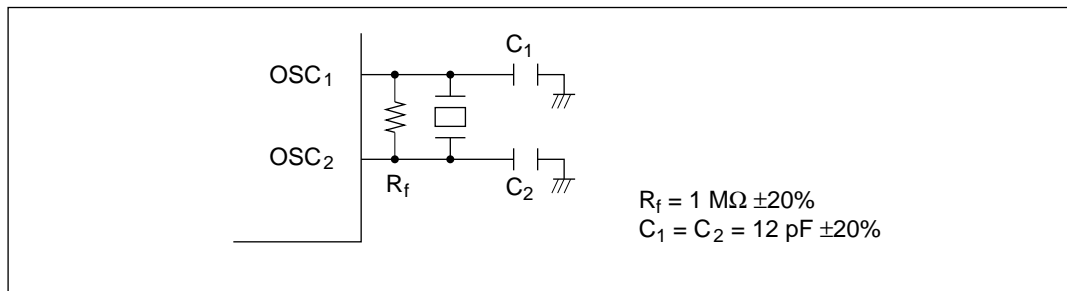


Figure 4-2 Typical Connection to Crystal Oscillator

- Crystal oscillator

Figure 4-3 shows the equivalent circuit of the crystal oscillator. An oscillator having the characteristics given in table 4-1 should be used.

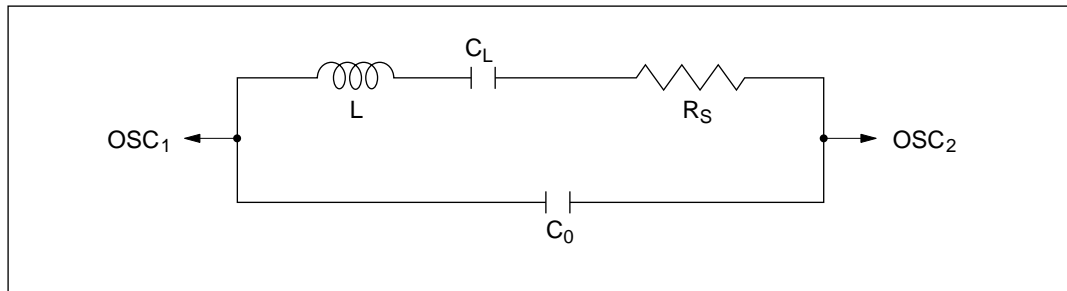


Figure 4-3 Equivalent Circuit of Crystal Oscillator

Table 4-1 Crystal Oscillator Parameters

	Frequency (MHz)		
	2	4	8
R_s max (Ω)	500	100	50
C_o max (pF)	7	7	7

2. Connecting a ceramic oscillator

- Circuit configuration

Figure 4-4 shows a typical method of connecting a ceramic oscillator.

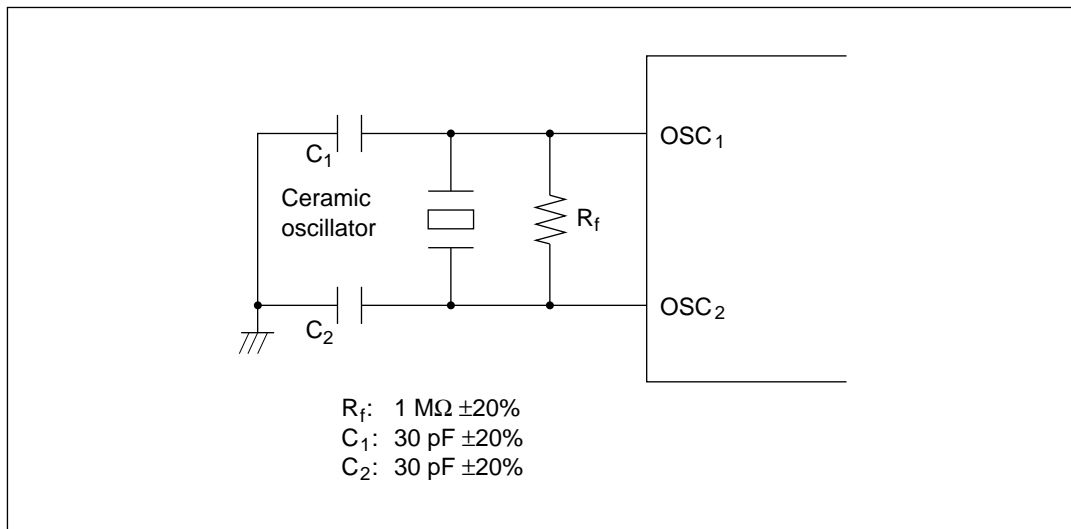


Figure 4-4 Typical Connection to a Ceramic Oscillator

3. Notes on board design

When generating clock pulses by connecting a crystal or ceramic oscillator, pay careful attention to the following points.

Avoid running signal lines close to the oscillator circuit, since the oscillator may be adversely affected by induction currents. (See figure 4-5.)

The board should be designed so that the oscillator and load capacitors are located as close as possible to pins OSC₁ and OSC₂.

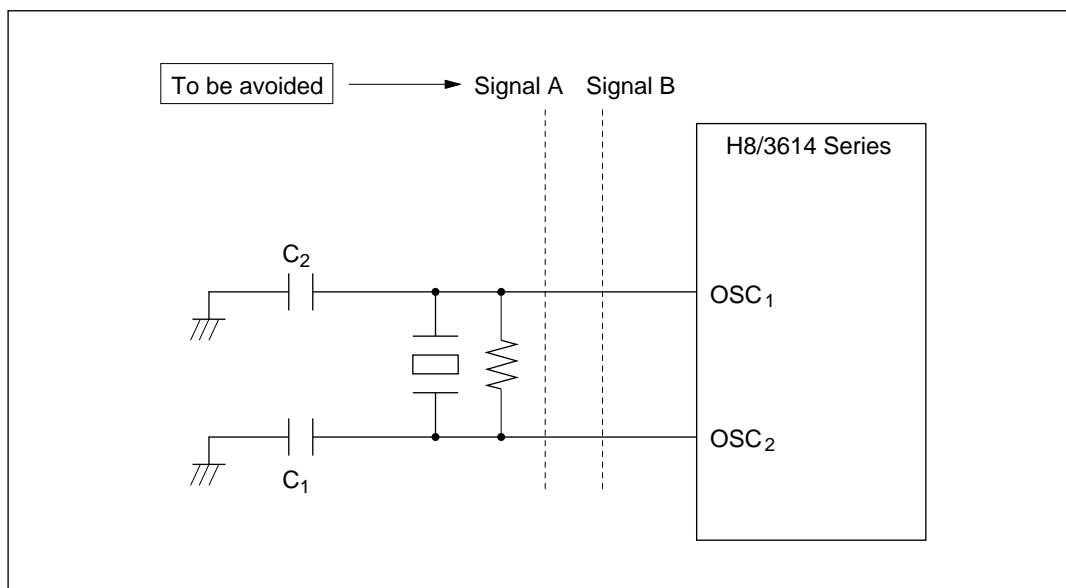


Figure 4-5 Note on Board Design of Oscillator Circuit

4. External clock input

- Circuit configuration

When an external clock is used, it is input at pin OSC₁. Pin OSC₂ should be left open. Figure 4-6 shows a typical connection.

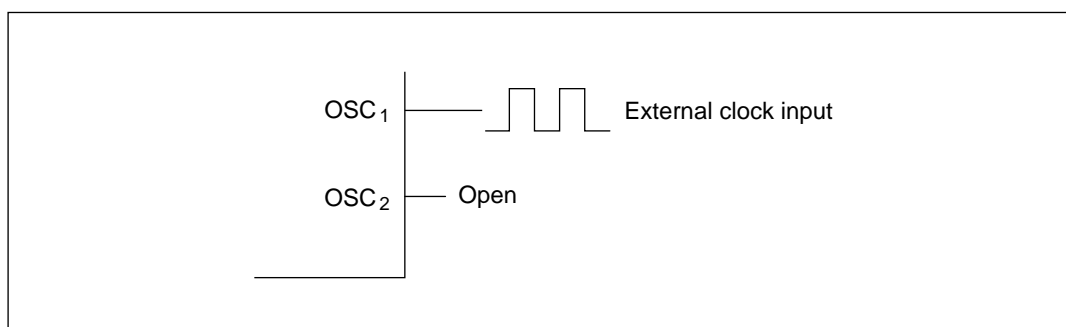


Figure 4-6 External Clock Input (example)

- External clock

Frequency	Twice clock frequency (ø)
Duty	45% to 55%

4.3 Subclock Generator

1. Connecting to 32.768 kHz crystal oscillator

Clock pulses can be supplied to the subclock divider by connecting a 32.768 kHz crystal oscillator, as shown in figure 4-7. Follow the same precautions as noted for the system clock.

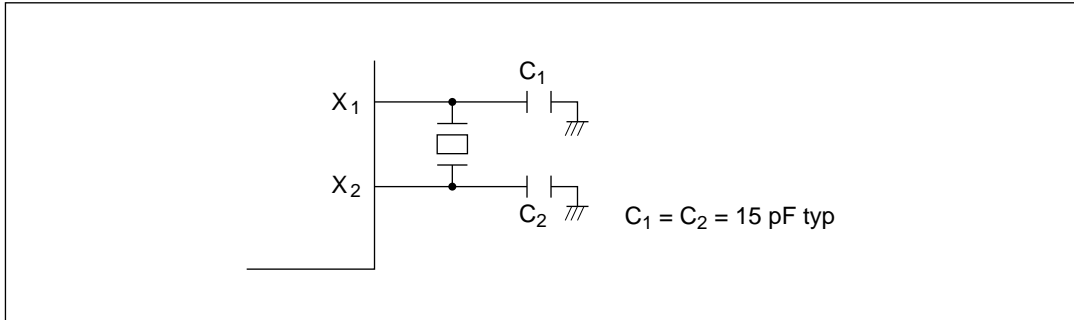


Figure 4-7 Typical Connection to Crystal Oscillator (subclock)

Figure 4-8 shows the equivalent circuit of the crystal oscillator.

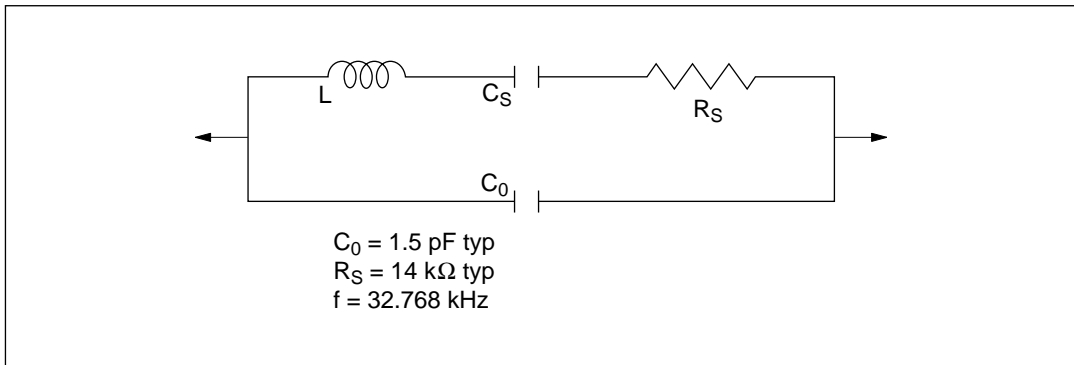


Figure 4-8 Equivalent Circuit of Crystal Oscillator

2. Pin connection when not using subclock

When the subclock is not used, connect V_{CC} to pin X_1 and leave pin X_2 open, as shown in figure 4-9.

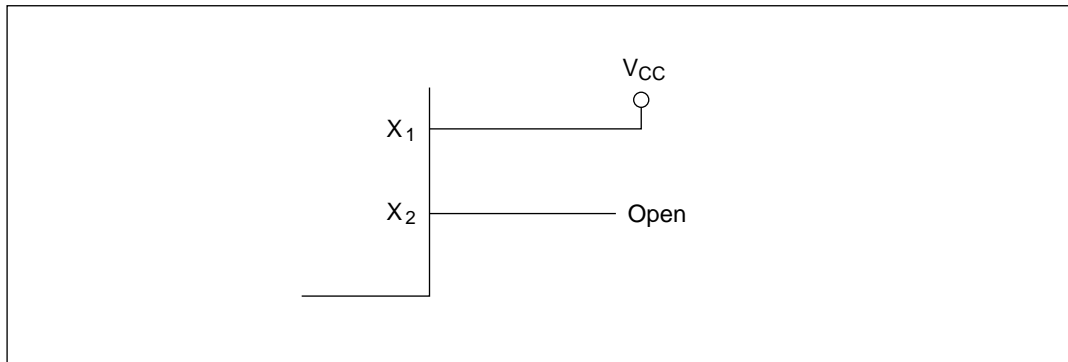


Figure 4-9 Pin Connection When Not Using Subclock

Section 5 I/O Ports

5.1 Overview

The H8/3614 Series has five 8-bit CMOS I/O ports,* one 6-bit PMOS open-drain I/O port, and one 8-bit input port. Table 5-1 indicates the functions of each port.

The CMOS I/O ports (ports 1, 2, 8, 9, and A) each have a port control register (PCR) that controls the input/output direction, and a port data register (PDR) that stores output data. Input or output can be assigned to individual bits.

The PMOS open-drain I/O port (port 4) has a port data register (PDR) that stores output data. Output can be controlled on a bit-by-bit basis.

Block diagrams of each port are given in Appendix C.

Note: * Pins P1₇ and P1₆ of port 1 are input-only pins.

When read, the ports operate as follows.

- CMOS I/O ports
 - Pins set for general-purpose port usage with PCR = 0 return the pin level.
 - Pins set for general-purpose port usage with PCR = 1 return the PDR bit data.
 - Pins set for on-chip peripheral function usage return the pin level.
- PMOS open-drain I/O port
 - All pins return the pin level.

Table 5-1 Port Functions

Port	Description	Pins	Other Functions	Function Switching Register
Port 0	8-bit input port	P0 ₇ to P0 ₀ / AN ₇ to AN ₀	Analog data input channels 7 to 0	PMR0
Port 1	Pins P1 ₇ and P1 ₆ : 2-bit input ports	P1 ₇	None	None
		P1 ₆ /EVENT	Timer D event input	PMR1
	Pins P1 ₅ to P1 ₀ : 6-bit CMOS I/O port	P1 ₅ /IRQ ₅ / TMOE	External interrupt 5; Timer E output	PMR1 PMR4
		P1 ₄ to P1 ₀ / IRQ ₄ to IRQ ₀	External interrupts 4 to 0	PMR1
Port 2	8-bit CMOS I/O port	P2 ₇ to P2 ₀	None	None
Port 4	6-bit PMOS open-drain I/O port	P4 ₅ to P4 ₀	None	None
Port 8	8-bit CMOS I/O port	P8 ₇ to P8 ₀	None	None
Port 9	8-bit CMOS I/O port	P9 ₇ /UD	Timer C count-up/down setting	PMR2
		P9 ₆ /SO ₂	Serial communication interface 2 data output	PMR3
		P9 ₅ /SI ₂	Serial communication interface 2 data input	
		P9 ₄ /SCK ₂	Serial communication interface 2 clock I/O	
		P9 ₃ /SO ₁	Serial communication interface 1 data output	
		P9 ₂ /SI ₁	Serial communication interface 1 data input	
		P9 ₁ /SCK ₁	Serial communication interface 1 clock I/O	
		P9 ₀ /PWM*	14-bit PWM waveform output pin*	
Port A	8-bit CMOS I/O port	PA ₁ to PA ₀	None	None

Note: * The H8/3612 does not have this function.

5.1.1 Port Types and Mask Options

The choice of I/O pin options and the resulting states are shown in table 5-2.

Upon reset, registers PDR, PCR, and PMR are initialized, cancelling the choices of peripheral functions.

Table 5-2 Choice of I/O Port Options

Class	Pins	With MOS Pull-Up	No MOS Pull-Up
I/O pins	P1 ₅ to P1 ₀ , P2 ₇ to P2 ₀ , P8 ₇ to P8 ₀ , P9 ₇ to P9 ₀ , PA ₇ to PA ₀	With MOS pull-up	No MOS pull-up
Input-only pins	P1 ₆	With MOS pull-up	No MOS pull-up
	P1 ₇	No option	No MOS pull-up
On-chip peripheral function I/O pins	SCK ₂ , SCK ₁ (output mode)	With MOS pull-up	No MOS pull-up
On-chip peripheral function output pins	SO ₂ , SO ₁ , PWM, TMOE	With MOS pull-up	No MOS pull-up
On-chip peripheral function input pins	SI ₂ , SI ₁ , $\overline{\text{IRQ}}_5$ to $\overline{\text{IRQ}}_0$, UD, EVENT	With MOS pull-up	No MOS pull-up

Note: Ports 0 and 4 have no MOS pull-up. There is no option for these ports.
If external clock input mode is selected when the serial communication interface is used, pins SCK₂ and SCK₁ will be input-only pins.

Table 5-3 shows the mask options with mask ROM versions. The mask ROM versions are compatible with the ZTAT™ versions only when the no MOS pull-up option is selected for all pins.

Table 5-3 Correspondence between Mask ROM and ZTAT™ Versions

Type	With MOS Pull-Up	No MOS Pull-Up
Mask ROM	Option	Option
ZTAT™	—	Fixed

5.1.2 Pull-Up MOS

Ports 1, 2, 8, 9, and A can be designated by mask options as having or not having MOS pull-up transistors for their (CMOS) outputs. (This does not apply to ZTAT™ versions.) The MOS pull-up option cannot be selected for pin P17.

Figure 5-1 shows the MOS pull-up circuit configuration.

When “with MOS pull-up” is selected by mask option, the MOS pull-up will normally be on, regardless of the port data register (PDR) and port control register (PCR) settings. (See table 5-4.)

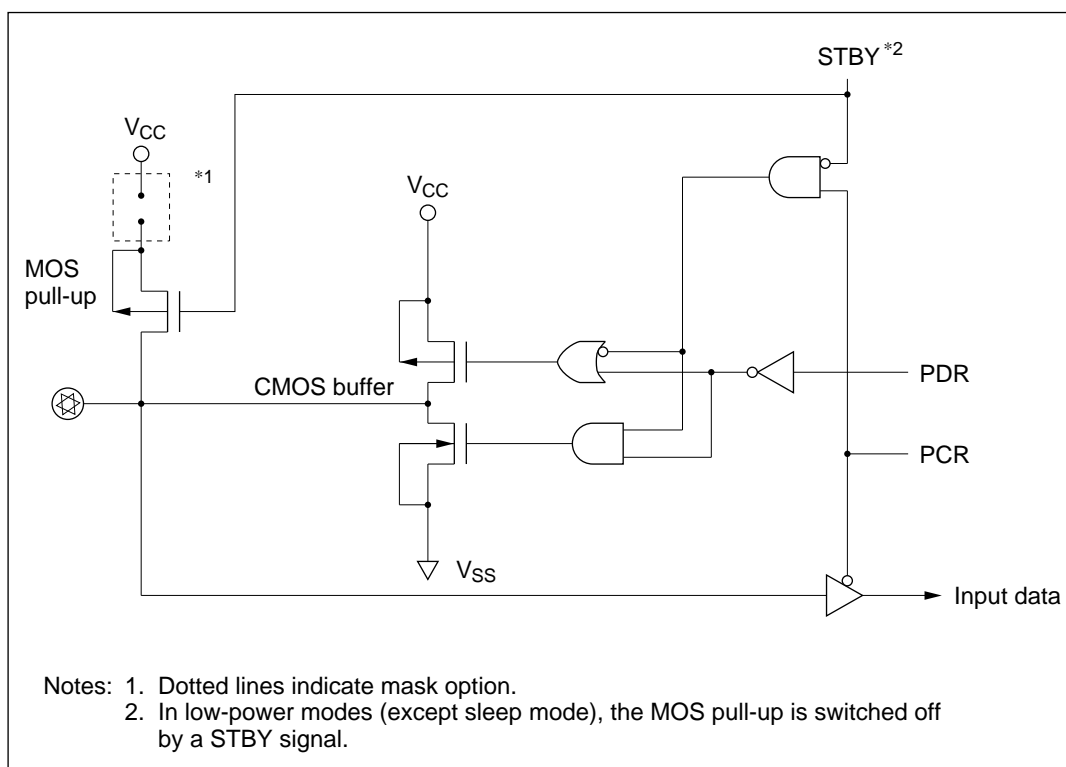


Figure 5-1 Pull-Up MOS Circuit Configuration

Table 5-4 MOS Pull-Up Control

Mask Option		With MOS Pull-Up				No MOS Pull-Up			
PCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	Off	Off	Off	On	Off	Off	Off	On
	NMOS	Off	Off	On	Off	Off	Off	On	Off
MOS pull-up		On	On	On	On	—	—	—	—

5.2 Port 0

5.2.1 Overview

Port 0 is an 8-bit input-only port. Figure 5-2 shows the pin configuration.

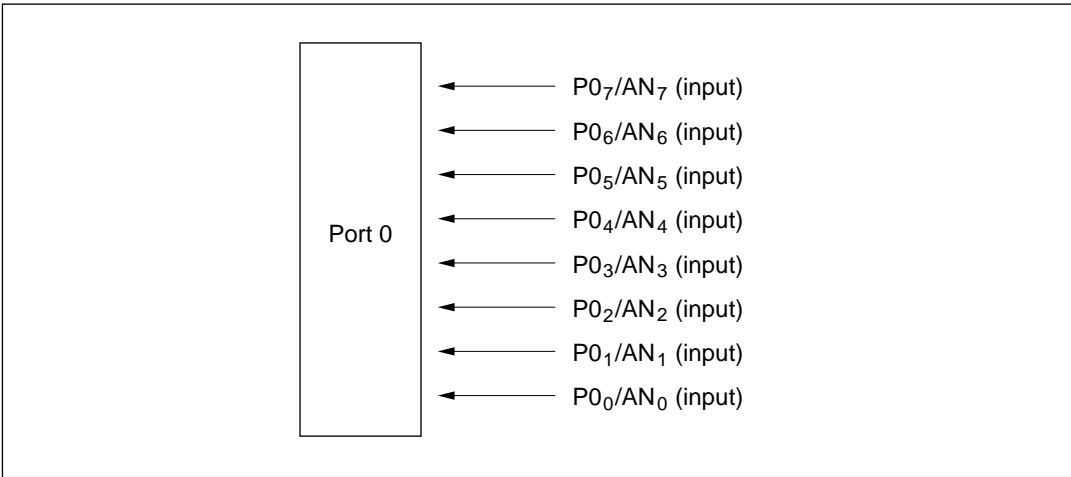


Figure 5-2 Port 0 Pin Configuration

5.2.2 Register Configuration and Description

Table 5-5 shows the port 0 register configuration.

Table 5-5 Port 0 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port mode register 0	PMR0	W	H'00	H'FFEF
Port data register 0	PDR0	R	—	H'FFD0

1. Port mode register 0 (PMR0)

Bit	7	6	5	4	3	2	1	0
	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Each PMR0 bit designates whether the corresponding port 0 pin is to be used for general input or as an analog input channel to the A/D converter.

Upon reset, PMR0 is initialized to H'00.

Bit n ANn	Explanation
0	P0 _n /AN _n pin function for P0 _n input. (initial value)
1	P0 _n /AN _n pin function for AN _n input.

(n = 0 to 7)

2. Port data register 0 (PDR0)

Bit	7	6	5	4	3	2	1	0
	PDR0 ₇	PDR0 ₆	PDR0 ₅	PDR0 ₄	PDR0 ₃	PDR0 ₂	PDR0 ₁	PDR0 ₀
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

When port 0 is read while the corresponding PMR bit is 0, the pin state can be read. If the corresponding PMR0 bit is 1, PDR0 is read as 1.

5.2.3 Pin Functions

Table 5-6 gives the port 0 pin functions.

Table 5-6 Port 0 Pin Functions

Pin	Pin Functions and Selection Method	
P0 ₇ /AN ₇ to P0 ₀ /AN ₀	Functions are switched as follows by means of bits AN ₇ to AN ₀ in PMR0.	
	AN _n	
	0	1
	Pin function	Pin function
	P0 _n input pin	AN _n input pin

(n = 7 to 0)

5.2.4 Pin States

Table 5-7 shows the port 0 pin states in each operating mode.

Table 5-7 Port 0 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
P0 ₇ /AN ₇ to P0 ₀ /AN ₀	High impedance	Previous state retained	High impedance	High impedance	High impedance	Normal operation

5.3 Port 1

5.3.1 Overview

Port 1 consists of six I/O pins and two input-only pins. Figure 5-3 shows the pin configuration.

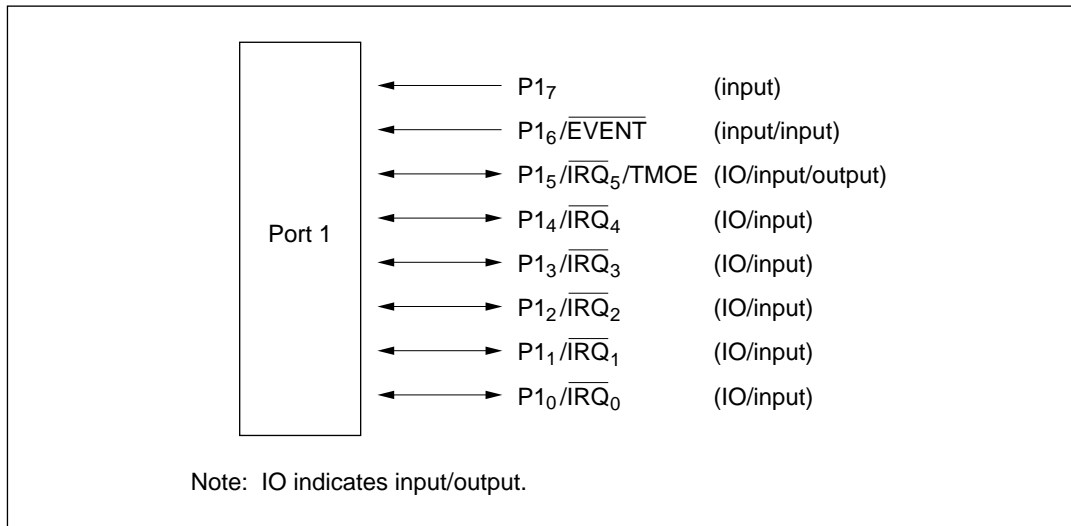


Figure 5-3 Port 1 Pin Configuration

5.3.2 Register Configuration and Description

Table 5-8 shows the port 1 register configuration.

Table 5-8 Port 1 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port mode register 1	PMR1	R/W	H'00	H'FFEB
Port control register 1	PCR1	W	H'C0	H'FFE1
Port data register 1	PDR1	R/W	Not fixed	H'FFD1
Port mode register 4	PMR4	R/W	H'0F	H'FFEE

1. Port mode register 1 (PMR1)

Bit	7	6	5	4	3	2	1	0
	NOISE CANCEL	EVENT	IRQC5	IRQC4	IRQC3	IRQC2	IRQC1	IRQC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMR1 is an 8-bit read/write register that controls the selection of pin functions for pin $P1_6/\overline{EVENT}$ and pins $P1_5/\overline{IRQ_5}$ to $P1_0/\overline{IRQ_0}$, and turns the pin $\overline{IRQ_0}$ noise canceller function on and off.

Upon reset, PMR1 is initialized to H'00.

Bit 7: Noise cancel (NOISE CANCEL)

This bit turns the $\overline{IRQ_0}$ noise canceller function on and off. In standby, watch, and subactive modes the noise canceller function is off regardless of the setting of this bit.

Bit 7

NOISE CANCEL	Explanation
0	Noise canceller function is off. (initial value)
1	Noise canceller function is on. Input is sampled at intervals of 256 states. If two consecutive input values do not match, noise is assumed.

Bit 6: $P1_6/\overline{EVENT}$ pin function switch (EVENT)

This bit selects whether pin $P1_6/\overline{EVENT}$ is used as $P1_6$ or as \overline{EVENT} .

Bit 6

EVENT	Explanation
0	$P1_6/\overline{EVENT}$ pin functions as $P1_6$.* (initial value)
1	$P1_6/\overline{EVENT}$ pin functions as \overline{EVENT} (timer D event input).

Note: * Even when pin $P1_6/\overline{EVENT}$ is used as $P1_6$, the timer D counter may increment when pin $P1_6$ is read. If timer D is used the counter must be cleared by means of the CLR bit in timer mode register D (TMD).

Bit 5: $P1_5/\overline{IRQ_5}$ /TMOE pin function switch (IRQC5)

This bit selects whether pin $P1_5/\overline{IRQ_5}$ /TMOE is used as $P1_5$ /TMOE or as $\overline{IRQ_5}$.

Bit 5

IRQC5	Explanation
0	$P1_5/\overline{IRQ_5}$ /TMOE pin functions as $P1_5$ /TMOE. (initial value)
1	$P1_5/\overline{IRQ_5}$ /TMOE pin functions for $\overline{IRQ_5}$ input.

Bit 4: P1₄/ $\overline{\text{IRQ}}_4$ pin function switch (IRQC4)

This bit selects whether pin P1₄/ $\overline{\text{IRQ}}_4$ is used as P1₄ or as $\overline{\text{IRQ}}_4$.

Bit 4

IRQC4	Explanation	
0	P1 ₄ / $\overline{\text{IRQ}}_4$ pin functions as P1 ₄ .	(initial value)
1	P1 ₄ / $\overline{\text{IRQ}}_4$ pin functions for $\overline{\text{IRQ}}_4$ * input.	

Note: * Rising or falling edge sensing can be designated for pin $\overline{\text{IRQ}}_4$.
For details see 3.2.3 (2), IRQ edge select register (IEGR).

Bit 3: P1₃/ $\overline{\text{IRQ}}_3$ pin function switch (IRQC3)

This bit selects whether pin P1₃/ $\overline{\text{IRQ}}_3$ is used as P1₃ or as $\overline{\text{IRQ}}_3$.

Bit 3

IRQC3	Explanation	
0	P1 ₃ / $\overline{\text{IRQ}}_3$ pin functions as P1 ₃ .	(initial value)
1	P1 ₃ / $\overline{\text{IRQ}}_3$ pin functions for $\overline{\text{IRQ}}_3$ input.	

Bit 2: P1₂/ $\overline{\text{IRQ}}_2$ pin function switch (IRQC2)

This bit selects whether pin P1₂/ $\overline{\text{IRQ}}_2$ is used as P1₂ or as $\overline{\text{IRQ}}_2$.

Bit 2

IRQC2	Explanation	
0	P1 ₂ / $\overline{\text{IRQ}}_2$ pin functions as P1 ₂ .	(initial value)
1	P1 ₂ / $\overline{\text{IRQ}}_2$ pin functions for $\overline{\text{IRQ}}_2$ input.	

Bit 1: P1₁/ $\overline{\text{IRQ}}_1$ pin function switch (IRQC1)

This bit selects whether pin P1₁/ $\overline{\text{IRQ}}_1$ is used as P1₁ or as $\overline{\text{IRQ}}_1$.

Bit 1

IRQC1	Explanation	
0	P1 ₁ / $\overline{\text{IRQ}}_1$ pin functions as P1 ₁ .	(initial value)
1	P1 ₁ / $\overline{\text{IRQ}}_1$ pin functions for $\overline{\text{IRQ}}_1$ * input.	

Note: * Rising or falling edge sensing can be designated for pin $\overline{\text{IRQ}}_1$.
For details see 3.2.3 2, IRQ edge select register (IEGR).

Bit 0: P1₀/ $\overline{\text{IRQ}}_0$ pin function switch (IRQC0)

This bit selects whether pin P1₀/ $\overline{\text{IRQ}}_0$ is used as P1₀ or as $\overline{\text{IRQ}}_0$.

Bit 0**IRQC0 Explanation**

0	P1 ₀ / $\overline{\text{IRQ}}_0$ pin functions as P1 ₀ . (initial value)
1	P1 ₀ / $\overline{\text{IRQ}}_0$ pin functions for $\overline{\text{IRQ}}_0$ * input.

Note: * Rising or falling edge sensing can be designated for pin $\overline{\text{IRQ}}_0$.

For details see 3.2.3 (2), IRQ edge select register (IEGR).

2. Port control register 1 (PCR1)

Bit	7	6	5	4	3	2	1	0
	—	—	PCR1 ₅	PCR1 ₄	PCR1 ₃	PCR1 ₂	PCR1 ₁	PCR1 ₀
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

PCR1 is an 8-bit register for controlling whether each of port 1 pins P1₅ to P1₀ functions as an input pin or output pin. Setting a PCR1 bit to 1 makes the corresponding pin from P1₅ to P1₀ an output pin, while clearing the bit to 0 makes it an input pin. PCR1 is a write-only register. All bits are read as 1.

Bits 7 and 6 are reserved; they are always read as 1, and cannot be modified. The settings in PCR1 and in PDR1 are valid only when the corresponding pin is designated in PMR1 as a general I/O pin.

Upon reset, PCR1 is initialized to H'C0.

3. Port data register 1 (PDR1)

Bit	7	6	5	4	3	2	1	0
	—	—	PDR1 ₅	PDR1 ₄	PDR1 ₃	PDR1 ₂	PDR1 ₁	PDR1 ₀
Initial value	— *	— *	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Pins P1₇ and P1₆ are for input only; reading PDR1 always gives the level of these pins.

PDR1 is an 8-bit register for storing data of pins P1₅ through P1₀. When port 1 is read while a PCR1 bit is set to 1, the PDR1 value will be read directly, regardless of the actual pin states. When port 1 is read while a PCR1 bit is cleared to 0, the pin state will be read.

4. Port mode register 4 (PMR4)

Bit	7	6	5	4	3	2	1	0
	TEO	TEO ON	FREQ	VRFR	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

PMR4 is an 8-bit read/write register that switches the $P1_5/\overline{IRQ}_5$ /TMOE pin function and controls TMOE pin waveform output. Bits 3 to 0 are reserved; they are always read as 1, and cannot be modified.

Upon reset, PMR4 is initialized to H'0F.

Bit 7: Timer E output select (TEO)

Bit 6: Timer E output on/off (TEO ON)

Bit 5: Fixed frequency select (FREQ)

Bit 4: Variable frequency select (VRFR)

The $P1_5/\overline{IRQ}_5$ /TMOE pin functions are switched as follows, by means of bits 7 to 4 of PMR4 and bit IRQC5 of PMR1.

PMR1	PMR4				Description	
Bit 5 IRQC5	Bit 7 TEO	Bit 6 TEO ON	Bit 5 FREQ	Bit 4 VRFR	Pin Function	Pin State
0	0	0	0	0	$P1_5$ pin	I/O port (initial value)
0	0	*	*	*	$P1_5$ pin	I/O port
0	1	0	*	*	TMOE output pin (off)	Low level output
0	1	1	0	0	TMOE output pin (on)	Fixed frequency output: ($\phi/2048$) 1.95 kHz ($\phi = 4$ MHz) 0.98 kHz ($\phi = 2$ MHz)
0	1	1	1	0	TMOE output pin (on)	Fixed frequency output: ($\phi/1024$) 3.9 kHz ($\phi = 4$ MHz) 1.95 kHz ($\phi = 2$ MHz)
0	1	1	*	1	TMOE output pin (on)	Variable frequency output: toggled by timer E overflow
1	*	*	*	*	\overline{IRQ}_5 input pin	External interrupt input

Note: * Don't care

5.3.3 Pin Functions

Table 5-9 shows the port 1 pin functions.

Table 5-9 Port 1 Pin Functions

Pin	Pin Functions and Selection Method												
P1 ₇	Functions as P1 ₇ input pin.												
P1 ₆ /EVENT	Function is switched as follows by EVENT bit in PMR1 <table><tr><td>EVENT</td><td>0</td><td>1</td></tr><tr><td>Pin function</td><td>P1₆ input pin</td><td>$\overline{\text{EVENT}}$ input pin*</td></tr></table> <p>Note: Timer D event input</p>	EVENT	0	1	Pin function	P1 ₆ input pin	$\overline{\text{EVENT}}$ input pin*						
EVENT	0	1											
Pin function	P1 ₆ input pin	$\overline{\text{EVENT}}$ input pin*											
P1 ₅ / $\overline{\text{IRQ}}_5$ /TMOE, P1 ₄ / $\overline{\text{IRQ}}_4$ to P1 ₀ / $\overline{\text{IRQ}}_0$	Function switched as follows by bits IRQC5 to IRQC0* in PMR1 and bit PCR1 _n in PCR1 (n = 5 to 0) <table><tr><td>PMR1</td><td colspan="2">0</td><td>1</td></tr><tr><td>PCR1_n</td><td>0</td><td>1</td><td>—</td></tr><tr><td>Pin function</td><td>P1_n input pin</td><td>P1_n output pin</td><td>$\overline{\text{IRQ}}_n$ input pin</td></tr></table>	PMR1	0		1	PCR1 _n	0	1	—	Pin function	P1 _n input pin	P1 _n output pin	$\overline{\text{IRQ}}_n$ input pin
PMR1	0		1										
PCR1 _n	0	1	—										
Pin function	P1 _n input pin	P1 _n output pin	$\overline{\text{IRQ}}_n$ input pin										

Notes:

1. Before switching pin functions using bits IRQ5 to IRQ0 in PMR1, first disable the corresponding interrupts by clearing their interrupt enable bits. After the pin functions have been switched, issue any instruction then clear the interrupt request flags to 0. For details see section 3.2.3 (1), Port mode register (PMR1).
2. Before entering power-down mode, pins set to external interrupt input by bits IRQC5 to IRQC0 in PMR1 should be kept from floating by external connection or should be set to general I/O in PMR1 prior to the state transition.
3. For details on the TMOE function, refer to section 5.3.2 4, Port mode register 4 (PMR4). $\overline{\text{IRQ}}_4$, $\overline{\text{IRQ}}_1$, and $\overline{\text{IRQ}}_0$ input can be set for either rising edge or falling edge detection by register IEGR. For details, refer to section 3.2.3 2, IRQ edge select register (IEGR). $\overline{\text{IRQ}}_0$ and $\overline{\text{IRQ}}_1$ can be used as event input pins for timer B and timer C, respectively. For details, refer to section 6, Timers.

5.3.4 Pin States

Table 5-10 shows the port 1 pin states in each operating mode.

Table 5-10 Port 1 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
P1 ₇	High impedance	Previous state retained	High impedance	High impedance	High impedance	Normal operation
P1 ₆ /EVENT ₇ , P1 ₅ /IRQ ₅ / TMOE ₇ , P1 ₄ /IRQ ₄ to P1 ₀ /IRQ ₀	High impedance or pulled up					

5.4 Port 2

5.4.1 Overview

Port 2 is an 8-bit I/O port. Figure 5-4 shows the pin configuration.

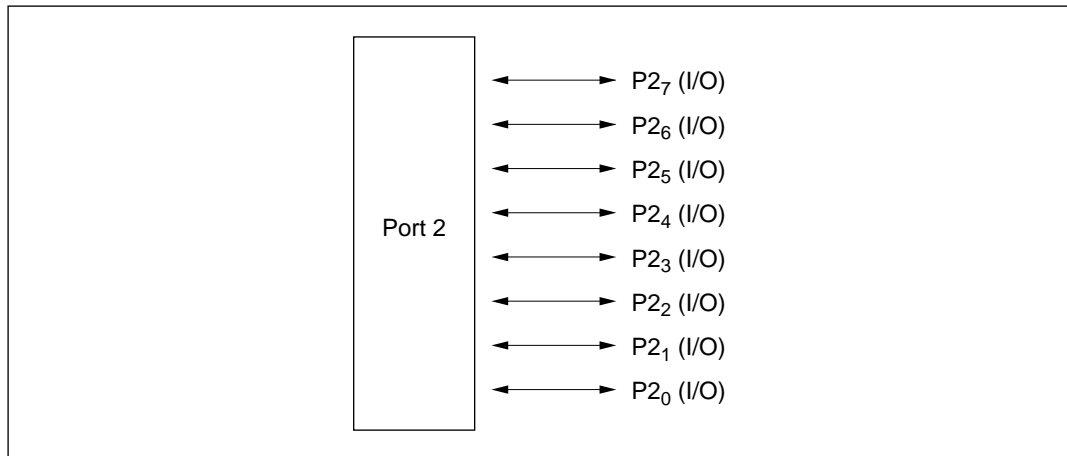


Figure 5-4 Port 2 Pin Configuration

5.4.2 Register Configuration and Description

Table 5-11 shows the port 2 register configuration.

Table 5-11 Port 2 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port control register 2	PCR2	W	H'00	H'FFE2
Port data register 2	PDR2	R/W	H'00	H'FFD2

1. Port control register 2 (PCR2)

Bit	7	6	5	4	3	2	1	0
	PCR2 ₇	PCR2 ₆	PCR2 ₅	PCR2 ₄	PCR2 ₃	PCR2 ₂	PCR2 ₁	PCR2 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCR2 is an 8-bit register for controlling whether each of port 2 pins P2₇ to P2₀ functions as an input pin or output pin. Setting a PCR2 bit to 1 makes the corresponding pin from P2₇ to P2₀ an output pin, while clearing the bit to 0 makes it an input pin.

PCR2 is a write-only register. All bits are read as 1. Upon reset, PCR2 is initialized to H'00.

2. Port data register 2 (PDR2)

Bit	7	6	5	4	3	2	1	0
	PDR2 ₇	PDR2 ₆	PDR2 ₅	PDR2 ₄	PDR2 ₃	PDR2 ₂	PDR2 ₁	PDR2 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR2 is an 8-bit register that stores data for port 2 pins P2₇ to P2₀. If port 2 is read while a PCR2 bit is set to 1, the PDR2 value will be read directly, regardless of the actual pin state. If port 2 is read while a PCR2 bit is cleared to 0, the pin state will be read.

Upon reset, PDR2 is initialized to H'00.

5.4.3 Pin Functions

Table 5-12 shows the port 2 pin functions.

Table 5-12 Port 2 Pin Functions

Pin	Selection Method and Pin Function	
P2 ₇ to P2 ₀	Switched as follows by PCR2 _n bits in PCR2.	
	PCR2 _n	
	0	1
	Pin function	P2 _n input pin
		P2 _n output pin

(n = 7 to 0)

5.4.4 Pin States

Table 5-13 shows the port 2 pin states in each operating mode.

Table 5-13 Port 2 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
P2 ₇ to P2 ₀	High impedance or pulled up	Previous state retained	High impedance	High impedance	High impedance	Normal operation

5.5 Port 4

5.5.1 Overview

Port 4 is a 6-bit PMOS open-drain I/O port. Figure 5-5 shows the pin configuration.

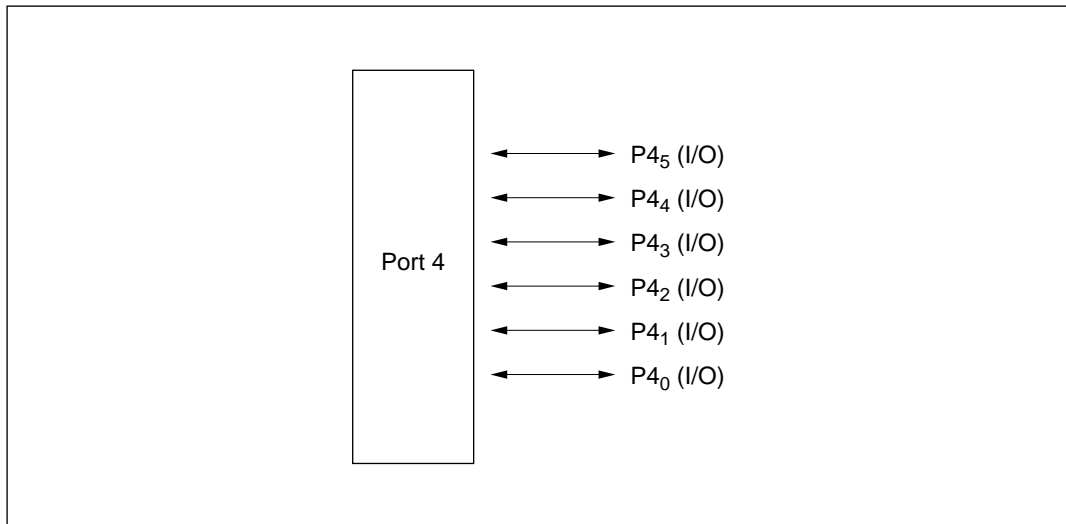


Figure 5-5 Port 4 Pin Configuration

5.5.2 Register Configuration and Description

Table 5-14 shows the port 4 register configuration.

Table 5-14 Port 4 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port data register 4	PDR4	R/W	H'C0	H'FFD4

1. Port data register 4 (PDR4)

Bit	7	6	5	4	3	2	1	0
	—	—	PDR4 ₅	PDR4 ₄	PDR4 ₃	PDR4 ₂	PDR4 ₁	PDR4 ₀
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

PDR4 is a 6-bit register that stores data for port 4 pins P4₅ to P4₀. Bits 7 and 6 are reserved. They are always read as 1 and cannot be modified. Upon reset, PDR4 is initialized to H'C0.

5.5.3 Pin Functions

Table 5-15 shows the port 4 pin functions.

Table 5-15 Port 4 Pin Functions

Pin	Selection Method and Pin Function		
P4 ₅ to P4 ₀	PMOS open-drain I/O pins, switched as follows by the PDR4 _n bits in PDR4.		
	PDR4 _n	0	1
	Pin function	I/O pin	Output pin
	Pin state	High impedance	High level

(n = 5 to 0)

5.5.4 Pin States

Table 5-16 shows the port 4 pin states in each operating mode.

Table 5-16 Port 4 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
P4 ₀ to P4 ₅	High impedance	Previous state retained	High impedance	High impedance	High impedance	Normal operation

5.6 Port 8

5.6.1 Overview

Port 8 is an 8-bit I/O port. Figure 5-6 shows the pin configuration.

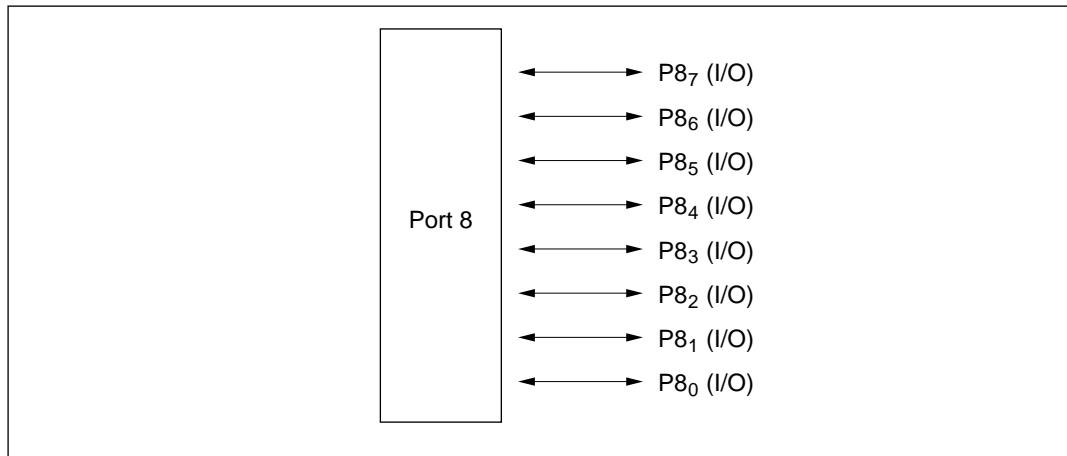


Figure 5-6 Port 8 Pin Configuration

5.6.2 Register Configuration and Description

Table 5-17 shows the port 8 register configuration.

Table 5-17 Port 8 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port control register 8	PCR8	W	H'00	H'FFE8
Port data register 8	PDR8	R/W	H'00	H'FFD8

1. Port control register 8 (PCR8)

Bit	7	6	5	4	3	2	1	0
	PCR8 ₇	PCR8 ₆	PCR8 ₅	PCR8 ₄	PCR8 ₃	PCR8 ₂	PCR8 ₁	PCR8 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCR8 is an 8-bit register for controlling whether each of port 8 pins P8₇ to P8₀ functions as an input or output pin. Setting a PCR8 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes it an input pin. PCR8 is a write-only register. All bits are read as 1.

Upon reset, PCR8 is initialized to H'00.

2. Port data register 8 (PDR8)

Bit	7	6	5	4	3	2	1	0
	PDR8 ₇	PDR8 ₆	PDR8 ₅	PDR8 ₄	PDR8 ₃	PDR8 ₂	PDR8 ₁	PDR8 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR8 is an 8-bit register for storing the data of port 8 pins P8₇ to P8₀. If port 8 is read while a PCR8 bit is set to 1, the PDR8 value will be read directly, regardless of the actual pin state. If port 8 is read while a PCR8 bit is cleared to 0, the pin state will be read.

Upon reset, PDR8 is initialized to H'00.

5.6.3 Pin Functions

Table 5-18 gives the port 8 pin functions.

Table 5-18 Port 8 Pin Functions

Pin	Selection Method and Pin Function	
P8 ₇ to P8 ₀	Functions are switched as follows by means of the PCR8 _n bits in PCR8.	
	PCR8 _n	
	0	1
	Pin function	P8 _n input pin
		P8 _n output pin

(n = 7 to 0)

5.6.4 Pin States

Table 5-19 shows the port 8 pin states in each operating mode.

Table 5-19 Port 8 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
P8 ₇ to P8 ₀	High impedance or pulled up	Contents retained	High impedance	High impedance	High impedance	Normal operation

5.7 Port 9

5.7.1 Overview

Port 9 is an 8-bit I/O port. Figure 5-7 shows the pin configuration.

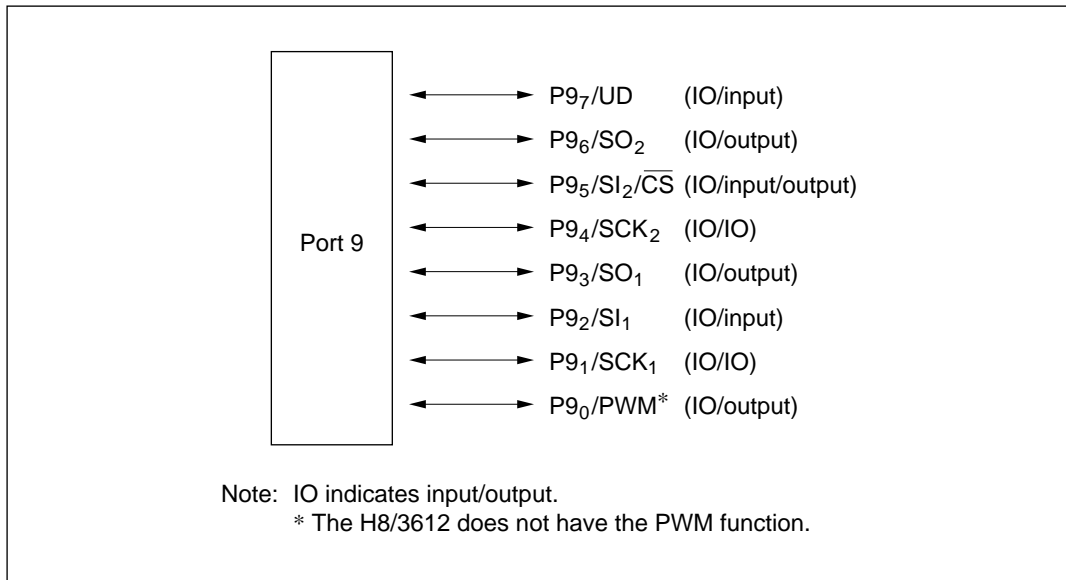


Figure 5-7 Port 9 Pin Configuration

5.7.2 Register Configuration and Description

Table 5-20 shows the port 9 register configuration.

Table 5-20 Port 9 Registers

Name	Abbrev.	R/W	Initial Value	Address
Port mode register 2	PMR2	R/W	H'00	H'FFEC
Port control register 9	PCR9	W	H'00	H'FFE9
Port data register 9	PDR9	R/W	H'00	H'FFD9

1. Port mode register 2 (PMR2)

Bit	7	6	5	4	3	2	1	0
	UP/ DOWN	SO2	SI2	SCK2	SO1	SI1	SCK1	PWM*
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * The H8/3612 does not have the PWM function.

PMR2 is an 8-bit read/write register, controlling the selection of port 9 pin functions.

Upon reset, PMR2 is initialized to H'00.

Bit 7: P9₇/UD pin function switch (UP/DOWN)

This bit selects whether pin P9₇/UD function as the P9₇ I/O pin or the UD input pin. Up/down control input (UD) is valid only when bit TMC6 = 1 in timer mode register C (TMC).

Bit 7

UP/DOWN	Description
0	P9 ₇ /UD pin functions for P9 ₇ input/output. (initial value)
1	P9 ₇ /UD pin functions for UD input. If bit TMC6 in TMC is set to 1, then when the UD input is high, timer C counts down, and when UD is low, timer C counts up.

Bit 6: P9₆/SO₂ pin function switch (SO2)

This bit selects whether pin P9₆/SO₂ functions as the P9₆ I/O pin or the SO₂ output pin.

Bit 6

SO2	Description
0	P9 ₆ /SO ₂ pin functions for P9 ₆ input/output. (initial value)
1	P9 ₆ /SO ₂ pin functions for SO ₂ output.

Bit 5: P9₅/SI₂/ \overline{CS} pin function switch (SI2)

This bit selects whether pin P9₅/SI₂/ \overline{CS} functions as the P9₅ I/O pin or the SI₂ input/ \overline{CS} output pin. For the switching between SI₂ input and \overline{CS} output see 9.2.5, Port Mode Register 3 (PMR3).

Bit 5

SI2	Description
0	P9 ₅ /SI ₂ / \overline{CS} pin functions for P9 ₅ input/output. (initial value)
1	P9 ₅ /SI ₂ / \overline{CS} pin functions for SI ₂ input or \overline{CS} output.

Bit 4: P9₄/SCK₂ pin function switch (SCK2)

This bit selects whether pin P9₄/SCK₂ functions as the P9₄ I/O pin or the SCK₂ I/O pin.

Bit 4 SCK2	Description
0	P9 ₄ /SCK ₂ pin functions for P9 ₄ input/output. (initial value)
1	P9 ₄ /SCK ₂ pin functions for SCK ₂ input/output. The clock input/output direction and the divider ratio are set in serial mode register 2 (SMR2).

Bit 3: P9₃/SO₁ pin function switch (SO1)

This bit selects whether pin P9₃/SO₁ functions as the P9₃ I/O pin or the SO₁ output pin.

Bit 3 SO1	Description
0	P9 ₃ /SO ₁ pin functions for P9 ₃ input/output. (initial value)
1	P9 ₃ /SO ₁ pin functions for SO ₁ output.

Bit 2: P9₂/SI₁ pin function switch (SI1)

This bit selects whether pin P9₂/SI₁ functions as the P9₂ I/O pin or the SI₁ input pin.

Bit 2 SI1	Description
0	P9 ₂ /SI ₁ pin functions for P9 ₂ input/output. (initial value)
1	P9 ₂ /SI ₁ pin functions for SI ₁ input.

Bit 1: P9₁/SCK₁ pin function switch (SCK1)

This bit selects whether pin P9₁/SCK₁ functions as the P9₁ I/O pin or the SCK₁ I/O pin.

Bit 1 SCK1	Description
0	P9 ₁ /SCK ₁ pin functions for P9 ₁ input/output. (initial value)
1	P9 ₁ /SCK ₁ pin functions for SCK ₁ input/output. The clock input/output direction and the divider ratio are set in serial mode register 1 (SMR1).

Bit 0: P9₀/PWM pin function switch (PWM)*

This bit selects whether pin P9₀/PWM pin functions as the P9₀ I/O pin or the PWM output pin.

Bit 0**PWM****Description**

0	P9 ₀ /PWM pin functions for P9 ₀ input/output. (initial value)
1	P9 ₀ /PWM pin functions for PWM output.

Note: * The H8/3612 does not have the PWM function.

2. Port control register 9 (PCR9)

Bit	7	6	5	4	3	2	1	0
	PCR9 ₇	PCR9 ₆	PCR9 ₅	PCR9 ₄	PCR9 ₃	PCR9 ₂	PCR9 ₁	PCR9 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCR9 is an 8-bit register for controlling whether each of port 9 pins P9₇ to P9₀ functions as an input or output pin. Setting a PCR9 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR9 and PDR9 are valid when the affected pin is designated in PMR2 as a general-purpose I/O pin. PCR9 is a write-only register. All bits are read as 1.

Upon reset, PCR9 is initialized to H'00.

3. Port data register 9 (PDR9)

Bit	7	6	5	4	3	2	1	0
	PDR9 ₇	PDR9 ₆	PDR9 ₅	PDR9 ₄	PDR9 ₃	PDR9 ₂	PDR9 ₁	PDR9 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR9 is an 8-bit register that stores data for port 9 pins P9₇ to P9₀. If port 9 is read while PCR9 bits are set to 1, the values stored in PDR9 are read, regardless of the actual pin states. If port 9 is read while PCR9 bits are cleared to 0, the pin states are read.

Upon reset, PDR9 is initialized to H'00.

5.7.3 Pin Functions

Table 5-21 shows the port 9 pin functions.

Table 5-21 Port 9 Pin Functions

Pin	Pin Functions and Selection Method			
P9 ₇ /UD	Functions are switched as follows by means of the UP/DOWN bit* in PMR2 and bit PCR9 ₇ in PCR9.			
	UP/DOWN	0		1
	PCR9 ₇	0	1	—
	Pin function	P9 ₇ input pin	P9 ₇ output pin	UD input pin
Note: * Before entering power-down mode, if this pin is set to UD input by the UP/DOWN bit in PMR2, it should be kept from floating by external connection or should be set to general I/O use by clearing the UP/DOWN bit to 0 prior to the state transition.				
P9 ₆ /SO ₂ *	Functions are switched as follows by means of bit SO2 in PMR2 and bit PCR9 ₆ in PCR9.			
	SO2	0		1
	PCR9 ₆	0	1	—
	Pin function	P9 ₆ input pin	P9 ₆ output pin	SO ₂ output pin
Note: * The PMOS buffer transistor of pin P9 ₆ /SO ₂ can be enabled or disabled by the SO2PMOS bit in PMR3. For details see 9.2.5, Port Mode Register 3 (PMR3).				
P9 ₅ /SI ₂ / CS	Functions are switched as follows by means of bit SI2 in PMR2,* bit CS in PMR3, and bit PCR9 ₅ in PCR9.			
	SI2	0		1
	CS	—		0 1
	PCR9 ₅	0	1	— —
	Pin function	P9 ₅ input pin	P9 ₅ output pin	SI ₂ input pin $\overline{\text{CS}}$ output pin
Note: * Before entering power-down mode, if this pin is set to SI ₂ input by bit SI2 in PMR2, it should be kept from floating by external connection or should be set to general I/O use by clearing bit SI2 to 0 prior to the state transition.				

Table 5-21 Port 9 Pin Functions (cont)

Pin	Pin Functions and Selection Method			
P9 ₄ /SCK ₂	Functions are switched as follows by means of bit SCK2* in PMR2, bits PS1 and PS0* in serial control register 2 (SCR2), and bit PCR9 ₄ in PCR9.			
	SCK2	0		1
	PS1, 0	—		Not 11 11
	PCR9 ₄	0	1	— —
	Pin function	P9 ₄ input pin	P9 ₄ output pin	SCK ₂ output pin SCK ₂ input pin
<p>Note: * Before entering power-down mode, if this pin is set to SCK₂ input by bit SCK2 in PMR2 and bits PS1 and PS0 in SCR2, it should be kept from floating by external connection, or else should be set to some other use by changing bits SCK2 and bits PS1 and PS0 prior to the state transition.</p> <p>For the settings of bits PS1 and PS0 in SCR2, see 9.2.3, Serial Control Register 2 (SCR2).</p>				
P9 ₃ /SO ₁ *	Functions are switched as follows by means of bit SO1 in PMR2 and bit PCR9 ₃ in PCR9.			
	SO1	0		1
	PCR9 ₃	0	1	—
	Pin function	P9 ₃ input pin	P9 ₃ output pin	SO ₁ output pin
<p>Note: * The PMOS buffer transistor of pin P9₃/SO₁ can be enabled or disabled by the SO1PMOS bit in PMR3. For details see 8.2.6, Port Mode Register 3 (PMR3).</p>				
P9 ₂ /SI ₁	Functions are switched as follows by means of bit SI1* in PMR2 and bit PCR9 ₂ in PCR9.			
	SI1	0		1
	PCR9 ₂	0	1	—
	Pin function	P9 ₂ input pin	P9 ₂ output pin	SI ₁ input pin
<p>Note: * Before entering power-down mode, if this pin is set to SI₁ input by bit SI1 in PMR2, it should be kept from floating by external connection or should be set to general I/O use by clearing bit SI1 to 0 prior to the state transition.</p>				

Table 5-21 Port 9 Pin Functions (cont)

Pin	Selection Method and Pin Function			
P9 ₁ /SCK ₁	Functions are switched as follows by means of bit SCK1 in PMR2,* bits SMR13 to SMR10 in serial mode register 1 (SMR1)*, and bit PCR9 ₁ in PCR9.			
	SCK1	0		1
	SMR13 to 10	—		Not 1111 1111
	PCR9 ₁	0	1	— —
	Pin function	P9 ₁ input pin	P9 ₁ output pin	SCK ₁ output pin SCK ₁ input pin
<p>Note: * Before entering power-down mode, if this pin is set to SCK₁ input by bit SCK1 in PMR2 and bits SMR13 to SMR10 in SMR1, it should be kept from floating by external connection, or else should be set to some other use by changing the SCK1 bit or bits SMR13 to SMR10 prior to the state transition.</p> <p>For the settings of bits SMR13 to SMR10 in SMR1, see 8.2.1, Serial Mode Register 1 (SMR1).</p>				
P9 ₀ /PWM*	Functions are switched as follows by means of bit PWM in PMR2 and bit PCR9 ₀ in PCR9.			
	PWM	0		1
	PCR9 ₀	0	1	—
	Pin function	P9 ₀ input pin	P9 ₀ output pin	PWM output pin
Note: * The H8/3612 does not have the PWM function.				

5.7.4 Pin States

Table 5-22 shows the port 9 pin states in each operating mode.

Table 5-22 Port 9 Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
P9 ₇ /UD, P9 ₆ /SO ₂ , P9 ₅ /SI ₂ /CS, P9 ₄ /SCK ₂ , P9 ₃ /SO ₁ , P9 ₂ /SI ₁ , P9 ₁ /SCK ₁ , P9 ₀ /PWM	High impedance or pulled up	Previous state retained	High impedance	High impedance	High impedance	Normal operation

5.8 Port A

5.8.1 Overview

Port A is an 8-bit I/O port. Figure 5-8 shows the pin configuration.

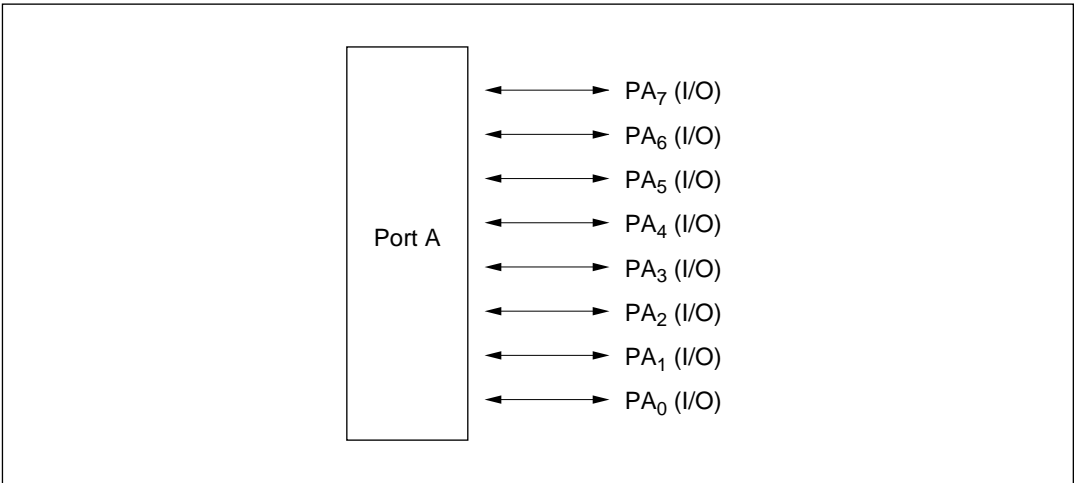


Figure 5-8 Port A Pin Configuration

5.8.2 Register Configuration and Description

Table 5-23 shows the port A register configuration.

Table 5-23 Port A Registers

Name	Abbrev.	R/W	Initial Value	Address
Port control register A	PCRA	W	H'00	H'FFEA
Port data register A	PDRA	R/W	H'00	H'FFDA

1. Port control register A (PCRA)

Bit	7	6	5	4	3	2	1	0
	PCRA ₇	PCRA ₆	PCRA ₅	PCRA ₄	PCRA ₃	PCRA ₂	PCRA ₁	PCRA ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCRA is an 8-bit register for controlling whether each of port A pins PA₁ and PA₀ functions as an input or output pin. Setting a PCRA bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin.

PCRA is a write-only register, which is always read as 1.

Upon reset, PCRA is initialized to H'00.

2. Port data register A (PDRA)

Bit	7	6	5	4	3	2	1	0
	PDRA ₇	PDRA ₆	PDRA ₅	PDRA ₄	PDRA ₃	PDRA ₂	PDRA ₁	PDRA ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDRA is an 8-bit register for storing the data of port A pins PA₇ to PA₀. If port A is read while a PCRA bit is set to 1, the PDRA value will be read directly, regardless of the actual pin state. If port A is read while a PCRA bit is cleared to 0, the pin state will be read.

Upon reset, PDRA is initialized to H'00.

5.8.3 Pin Functions

Table 5-24 shows the port A pin functions.

Table 5-24 Port A Pin Functions

Pin	Selection Method and Pin Function	
PA ₇ to PA ₀	Functions are switched as follows by means of the PCRA _n bit in PCRA.	
	PCRA _n	0
	Pin function	PA _n input pin
		1
		PA _n output pin

(n = 7 to 0)

5.8.4 Pin States

Table 5-25 shows the port A pin states in each operating mode.

Table 5-25 Port A Pin States

Pins	Reset	Sleep	Standby	Watch	Subactive	Active
PA ₇ to PA ₀	High impedance or pulled up	Previous state retained	High impedance	High impedance	High impedance	Normal operation

Section 6 Timers

6.1 Overview

The H8/3614 Series provides on-chip two prescalers (prescaler S and prescaler W) with different input clocks, and five timers (timers A to E).

Prescaler S (PSS) is a 13-bit counter clocked by the system clock ($\phi = f_{OSC}/2$). Its prescaled outputs are used by timers A to C and timer E.

Prescaler W (PSW) is a 5-bit counter clocked by the subclock ($\phi_{SUB} = f_X/8$). Its prescaled output is used for time-base operation by timer A.

Table 6-1 outlines the functions of timers A to E.

Table 6-1 Timer A to E Functions

Name	Functions	Operating Clock (Internal)	Event Input Pin	Waveform Output Pin	Remarks
Timer A	• 8-bit interval timer	$\phi/8$ to $\phi/8192$ (choice of 8 sources)	—	—	—
	• Time base	$\phi_{SUB}/32$ (choice of 4 overflow periods)		—	—
Timer B	• 8-bit reloadable timer	$\phi/8$ to $\phi/8192$ (choice of 7 sources)	$P1_0/\overline{IRQ_0}$	—	—
	• 8-bit interval timer				
	• Event counter				
Timer C	• 8-bit reloadable timer	$\phi/8$ to $\phi/8192$ (choice of 7 sources)	$P1_1/\overline{IRQ_1}$	—	Counting direction can be controlled by software or hardware.
	• 8-bit interval timer				
	• Event counter				
	• Choice of up- or down-counting				
Timer D	• 8-bit event counter	—	$P1_6/\overline{EVENT}$	—	—
Timer E	• 8-bit reloadable timer	$\phi/8$ to $\phi/8192$ (choice of 8 sources)	—	$P1_5/\overline{IRQ_5}/$ TMOE	Can output square wave with 50% duty cycle
	• 8-bit interval timer				

6.1.1 Prescaler Operation

1. Prescaler S (PSS)

PSS is a 13-bit counter using the system clock ($\phi = f_{OSC}/2$) as its input clock. Each input clock cycle causes prescaler S to increment once.

PSS is initialized to H'0000 by a reset, and starts counting upon return to active mode.

In standby mode, watch mode, and subactive mode, the system clock (ϕ) pulse generator stops, so PSS also stops functioning. Its value is reset to H'0000.

The CPU cannot read or write PSS data.

The output from PSS is shared by timers A to C and E as well as serial communication interfaces 1 and 2. The frequency division ratio can be set separately for each on-chip peripheral function.

2. Prescaler W (PSW)

PSW is a 5-bit counter using the subclock ($\phi_{SUB} = f_X/8$) as its input clock.

PSW is initialized to H'00 by a reset, and starts counting upon return to active mode.

Even in standby mode, watch mode, or subactive mode, PSW continues functioning so long as clock signals are supplied to pins X_1 and X_2 .

PSW can be reset by setting bits TMA3 and TMA2 to 1 in timer mode register A (TMA).

The output from PSW can be used as the clock source for timer A, in which case timer A functions as a time base.

Figure 6-1 shows the clock signals supplied by PSS and PSW to peripheral modules.

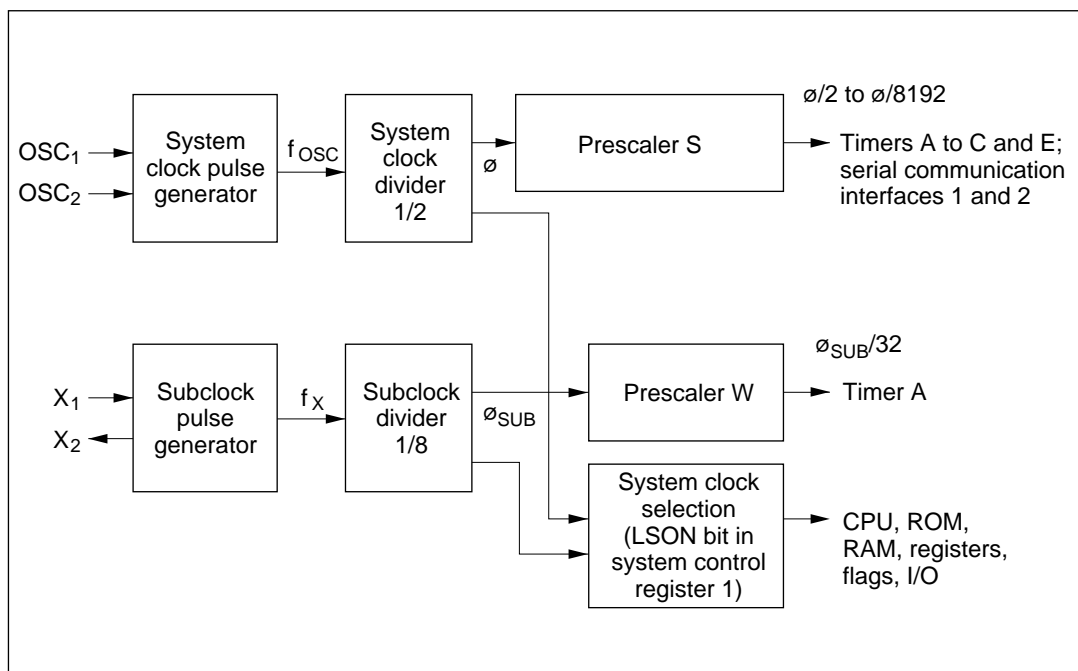


Figure 6-1 Clock Supply

6.2 Timer A

6.2.1 Overview

Timer A is an 8-bit interval timer. It can be connected to a 32.768 kHz crystal oscillator for use as a real-time clock time base.

1. Features

Features of timer A are given below.

- Choice of eight internal clock sources ($\phi/8192$, $\phi/4096$, $\phi/2048$, $\phi/512$, $\phi/256$, $\phi/128$, $\phi/32$, $\phi/8$).
- Choice of four overflow periods (2 s, 1 s, 0.5 s, 125 ms) when timer A is used as a time base (using a 32.768 kHz crystal oscillator).
- An interrupt is requested when the counter overflows.

2. Block diagram

Figure 6-2 shows a block diagram of timer A.

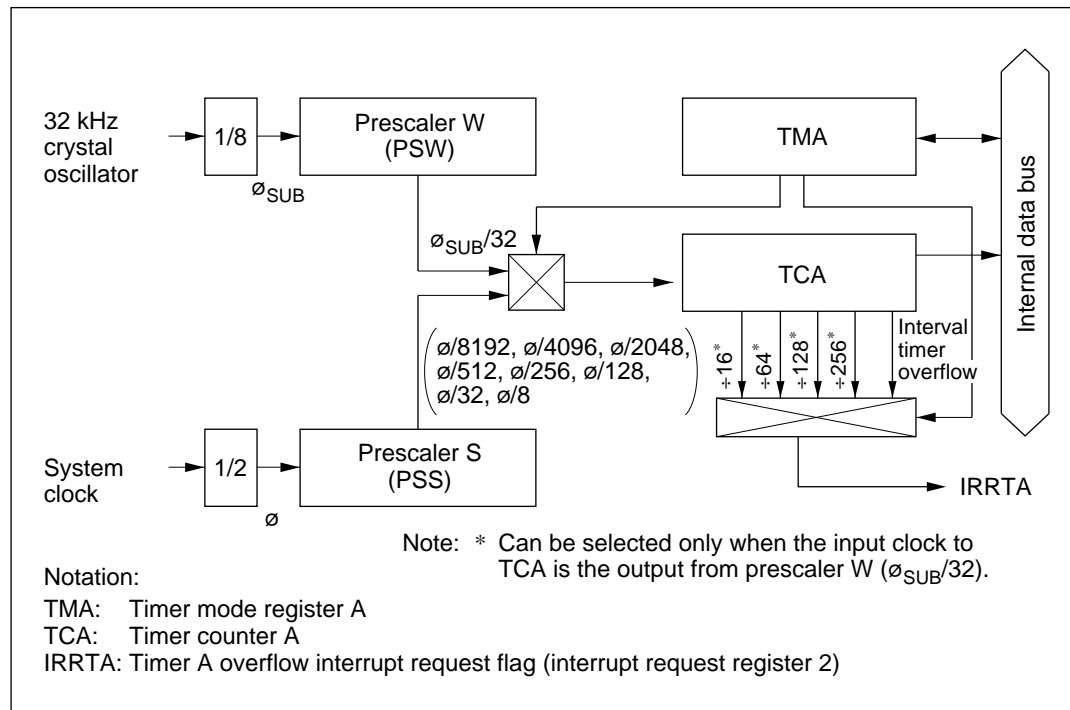


Figure 6-2 Block Diagram of Timer A

3. Register configuration

Table 6-2 shows the register configuration of timer A.

Table 6-2 Timer A Registers

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register A	TMA	R/W	H'F0	H'FFC0
Timer counter A	TCA	R	H'00	H'FFC1

6.2.2 Register Descriptions

1. Timer mode register A (TMA)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	TMA3	TMA2	TMA1	TMA0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

TMA is an 8-bit read/write register for selecting the prescaler and input clock.

Upon reset, TMA is initialized to H'F0.

Bits 7 to 4: Reserved bits

Bits 7 to 4 are reserved; they are always read as 1, and cannot be modified.

Bit 3: Prescaler select (TMA3)

Bit 3 selects either prescaler S or prescaler W as the clock input source for timer A.

Bit 3

TMA3	Description
0	Prescaler S (PSS) is clock input source for timer A. (initial value)
1	Prescaler W (PSW) is clock input source for timer A.

Bits 2 to 0: Clock select (TMA2 to TMA0)

Bits 2 to 0 select the clock input to TCA. The selection is made as follows by the combination of these bits and bit TMA3.

Bit 3 TMA3	Bit 2 TMA2	Bit 1 TMA1	Bit 0 TMA0	Description	
				Prescaler divider ratio (interval timer) or overflow period (time base)	Operation mode
0	0	0	0	PSS, $\varnothing/8192$ (initial value)	Interval timer mode
			1	PSS, $\varnothing/4096$	
		1	0	PSS, $\varnothing/2048$	
			1	PSS, $\varnothing/512$	
	1	0	0	PSS, $\varnothing/256$	
			1	PSS, $\varnothing/128$	
		1	0	PSS, $\varnothing/32$	
			1	PSS, $\varnothing/8$	
1	0	0	0	PSW, 2 s	Time-base mode
			1	PSW, 1 s	
		1	0	PSW, 0.5 s	
			1	PSW, 125 ms	
	1	0	0	PSW and TCA are cleared to H'00	
			1		
		1	0		
			1		

Note: $\varnothing = f_{OSC}/2$

2. Timer counter A (TCA)

Bit	7	6	5	4	3	2	1	0
	TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCA is an 8-bit read-only up-counter, which is incremented by internal clock input. The clock source for input to this counter is selected by bits TMA3 to TMA0 in timer mode register A (TMA). The TCA value can be read by the CPU at any time.

TCA is cleared to H'00 by setting bits TMA3 and TMA2 of TMA to 1.

When TCA overflows, the IRRTA bit in interrupt request register 2 (IRR2) is set to 1.

Upon reset, TCA is initialized to H'00.

6.2.3 Timer Operation

Timer A is an 8-bit timer which can be used either as an interval timer or, if a 32.768 kHz crystal oscillator is connected, as a real-time clock time base.

1. Interval timer operation

When bit TMA3 in timer mode register A (TMA) is cleared to 0, timer A functions as an 8-bit interval timer.

Upon reset, TCA is cleared to H'00 and bit TMA3 is cleared to 0, so up-counting and interval timing resume immediately after the reset. The clock input to timer A is selected by bits TMA2 to TMA0 in TMA; any of eight internal clock signals output by prescaler S can be selected.

After the count value in TCA reaches H'FF, the next clock signal input causes timer A to overflow, setting bit IRRTA to 1 in interrupt request register 2 (IRR2). If IENTA = 1 in interrupt enable register 2 (IENR2), a CPU interrupt is requested.*

At overflow, TCA returns to H'00 and starts counting up again. In this mode timer A functions as an interval timer that generates an overflow output at intervals of 256 input clock pulses.

During interval timer operation (when bit TMA3 = 0), TCA cannot be cleared.

Note: * For details on interrupts, see 3.2.2, Interrupts.

2. Real-time clock time base operation

When bit TMA3 in TMA is set to 1, timer A functions as a time base for a real-time clock by counting clock signals output by prescaler W.

The overflow period of timer A is set by bits TMA1 and TMA0 in TMA. A choice of four periods is available. During clock time-base operation (when bit TMA3 = 1), if bit TMA2 is set to 1, TCA and prescaler W are both cleared to H'00.

6.3 Timer B

6.3.1 Overview

Timer B is an 8-bit up-counter that increments each time a clock pulse is input. This timer has two operation modes, interval and auto reload. It can also function as an event counter.

1. Features

Features of timer B are given below.

- Choice of seven internal clock sources ($\phi/8192$, $\phi/2048$, $\phi/512$, $\phi/256$, $\phi/128$, $\phi/32$, $\phi/8$) or an external clock (can be used to count external events).
- An interrupt is requested when the counter overflows.

2. Block diagram

Figure 6-3 shows a block diagram of timer B.

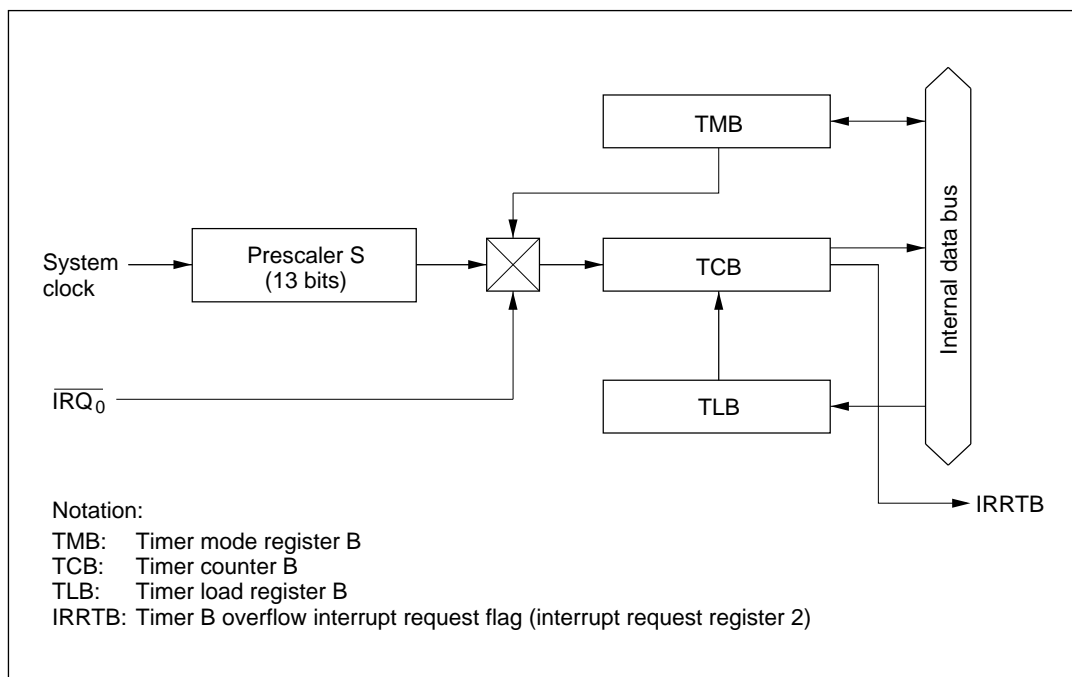


Figure 6-3 Block Diagram of Timer B

3. Pin configuration

Table 6-3 shows the timer B pin configuration.

Table 6-3 Pin Configuration

Name	Abbrev.	I/O	Function
Event input pin	P1 ₀ /IRQ ₀	Input	Timer B event input

4. Register configuration

Table 6-4 shows the register configuration of timer B.

Table 6-4 Timer B Registers

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register B	TMB	R/W	H'78	H'FFC2
Timer counter B	TCB	R	H'00	H'FFC3
Timer load register B	TLB	W	H'00	H'FFC3

6.3.2 Register Descriptions

1. Timer mode register B (TMB)

Bit	7	6	5	4	3	2	1	0
	TMB7	—	—	—	—	TMB2	TMB1	TMB0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

TMB is an 8-bit read/write register for selecting the auto-reload function and input clock.

Upon reset, TMB is initialized to H'78.

Bit 7: Auto-reload function select (TMB7)

Bit 7 selects the auto-reload function of timer B.

Bit 7

TMB7	Description
0	Interval timer function selected. (initial value)
1	Auto-reload function selected.

Bits 6 to 3: Reserved bits

Bits 6 to 3 are reserved; they are always read as 1, and cannot be modified.

Bits 2 to 0: Clock select (TMB2 to TMB0)

Bits 2 to 0 select the clock input to TCB. For external clock counting, either the rising or falling edge can be selected.

Bit 2 TMB2	Bit 1 TMB1	Bit 0 TMB0	Description
0	0	0	Internal clock: $\phi/8192$. (initial value)
0	0	1	Internal clock: $\phi/2048$.
0	1	0	Internal clock: $\phi/512$.
0	1	1	Internal clock: $\phi/256$.
1	0	0	Internal clock: $\phi/128$.
1	0	1	Internal clock: $\phi/32$.
1	1	0	Internal clock: $\phi/8$.
1	1	1	External clock ($P1_0/\overline{IRQ_0}$): rising or falling edge.*

Note: * The edge of the external event signal is selected by bit IEG0 in the IRQ edge select register (IEGR). For details see 3.2.3 (2), IRQ edge select register (IEGR). To count external events, set bit IRQC0 to 1 in port mode register 1 (PMR1).

2. Timer counter B (TCB)

Bit	7	6	5	4	3	2	1	0
	TCB7	TCB6	TCB5	TCB4	TCB3	TCB2	TCB1	TCB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCB is an 8-bit read-only up-counter, which is incremented by internal or external clock input. The clock source for input to this counter is selected by bits TMB2 to TMB0 in timer mode register B (TMB). The TCB value can be read by the CPU at any time.

When TCB overflows from H'FF to H'00 or to the value set in TLB, the IRRTB bit in interrupt request register 2 (IRR2) is set to 1.

TCB is allocated to the same address as timer load register B (TLB).

Upon reset, TCB is initialized to H'00.

3. Timer load register B (TLB)

Bit	7	6	5	4	3	2	1	0
	TLB7	TLB6	TLB5	TLB4	TLB3	TLB2	TLB1	TLB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

TLB is an 8-bit write-only register for setting the reload value of timer counter B (TCB).

When a reload value is set in TLB, the same value is loaded into timer counter B (TCB) as well, and TCB starts counting up from that value. When TCB overflows during operation in auto-reload mode, the TLB value is loaded in TCB. Accordingly, overflow periods can be set within the range of 1 to 256 input clocks.

The same address is allocated to TLB as to TCB.

Upon reset, TLB is initialized to H'00.

6.3.3 Timer Operation

Timer B is an 8-bit multifunction timer. It can be used as an interval timer, an auto-reload timer, or an event counter.

1. Interval timer operation

When bit TMB7 in timer mode register B (TMB) is cleared to 0, timer B functions as an 8-bit interval timer.

Upon reset, TCB is cleared to H'00 and bit TMB7 is cleared to 0, so up-counting and interval timing resume immediately after the reset. The clock input to timer B is selected from seven internal clock signals output by prescaler S, or an external clock input at pin P1₀/IRQ₀. The selection is made by bits TMB2 to TMB0 of TMB.

After the count value in TCB reaches H'FF, the next clock signal input causes timer B to overflow, setting bit IRRTB to 1 in interrupt request register 2 (IRR2). If IENTB = 1 in interrupt enable register 2 (IENR2), a CPU interrupt is requested.*

At overflow, TCB returns to H'00 and starts counting up again.

During interval timer operation (TMB7 = 0), when a value is set in timer load register B (TLB), the same value is set in TCB.

Note: * For details on interrupts, see 3.2.2, Interrupts.

2. Auto-reload timer operation

Setting bit TMB7 in TMB to 1 causes timer B to function as an 8-bit auto-reload timer. When a reload value is set in TLB, the same value is loaded into TCB, becoming the value from which TCB starts its count.

After the count value in TCB reaches H'FF, the next clock signal input causes timer B to overflow. The TLB value is then loaded into TCB, and the count continues from that value. The overflow period can be set within a range from 1 to 256 input clocks, depending on the TLB value.

The clock sources and interrupts in auto-reload mode are the same as for interval mode.

In auto-reload mode (bit TMB7 = 1), setting a new TLB value also initializes TCB.

3. Operation as event counter

Timer B can operate as an event counter, using $P1_0/\overline{IRQ_0}$ as the event input pin. External event counting is selected by setting bits TMB2 to 0 in timer register B (TMB) to all 1's (111). TCB can count either rising or falling edges of the input at pin $P1_0/\overline{IRQ_0}$.

When timer B is used to count external event input, bit IRQC0 in port mode register 1 (PMR1) should be set to 1, and bit IEN0 in interrupt enable register 1 (IENR1) should be cleared to 0 to disable interrupt requests at IRQ_0 .

6.4 Timer C

6.4.1 Overview

Timer C is an 8-bit up/down counter that increments or decrements each time a clock pulse is input. This timer has two operation modes, interval and auto reload. It can also function as an event counter.

1. Features

Features of timer C are given below.

- Choice of seven internal clock sources ($\phi/8192$, $\phi/2048$, $\phi/512$, $\phi/256$, $\phi/128$, $\phi/32$, $\phi/8$) or an external clock (can be used to count external events).
- An interrupt is requested when the counter overflows.
- Can be switched between up- and down-counting by software or hardware control.

2. Block diagram

Figure 6-4 shows a block diagram of Timer C.

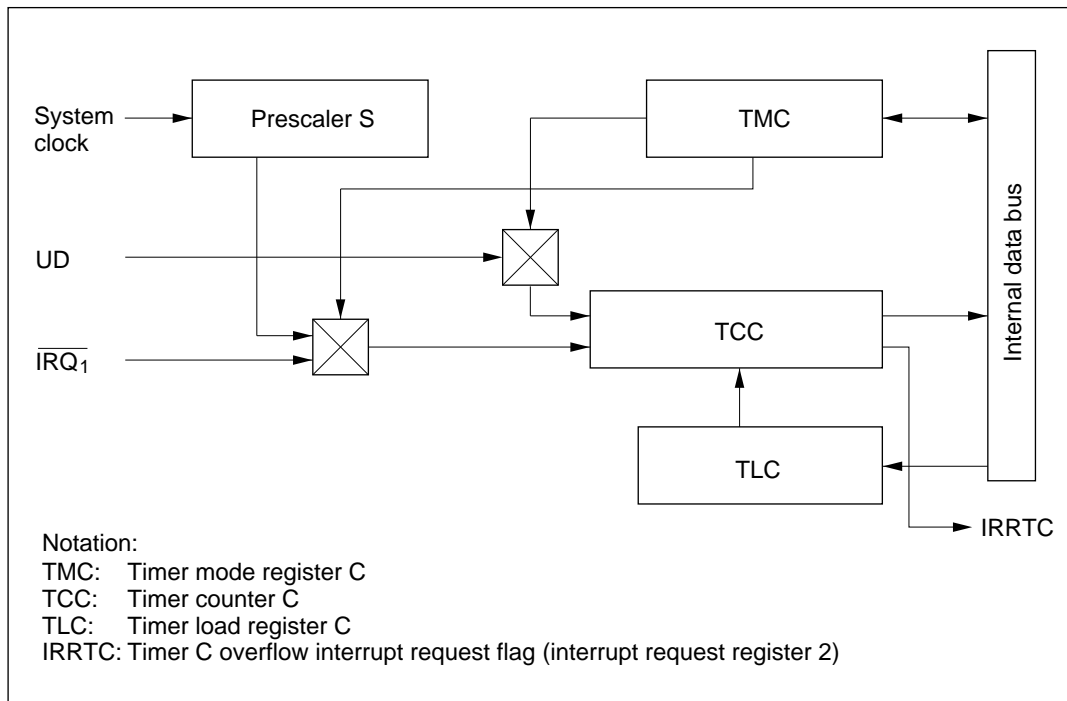


Figure 6-4 Block Diagram

3. Pin configuration

Table 6-5 shows the timer C pin configuration.

Table 6-5 Pin Configuration

Name	Abbrev.	I/O	Function
Event input pin	P1 ₁ / $\overline{\text{IRQ}}_1$	Input	Timer C event input
Up-/down-count selection pin	P9 ₇ /UD	Input	Timer C up/down control

4. Register configuration

Table 6-6 shows the register configuration of timer C.

Table 6-6 Timer C Registers

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register C	TMC	R/W	H'18	H'FFC4
Timer counter C	TCC	R	H'00	H'FFC5
Timer load register C	TLC	W	H'00	H'FFC5

6.4.2 Register Descriptions

1. Timer mode register C (TMC)

Bit	7	6	5	4	3	2	1	0
	TMC7	TMC6	TMC5	—	—	TMC2	TMC1	TMC0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/W	R/W	R/W	—	—	R/W	R/W	R/W

TMC is an 8-bit read/write register for selecting the auto-reload function, counting direction, and input clock.

Upon reset, TMC is initialized to H'18.

Bit 7: Auto-reload function select (TMC7)

Bit 7 selects the auto-reload function of timer C.

Bit 7

TMC7	Description
0	Interval timer function selected. (initial value)
1	Auto-reload function selected.

Bits 6 and 5: Counter up/down control (TMC6 and TMC5)

These bits select whether TCC operates as an up-counter, as a down-counter, or as either an up-counter or down-counter depending on the input at pin P9₇/UD.

Bit 6 TMC6	Bit 5 TMC5	Description
0	0	TCC is an up-counter. (initial value)
0	1	TCC is a down-counter.
1	*	TCC up/down control is by input at pin P9 ₇ /UD. TCC is a down-counter if UD input is high, and an up-counter if UD input is low.

Note: * Don't care.

Bits 4 and 3: Reserved bits

Bits 4 and 3 are reserved; they are always read as 1, and cannot be modified.

Bits 2 to 0: Clock select (TMC2 to TMC0)

Bits 2 to 0 select the clock input to TCC. For external clock counting, either the rising or falling edge can be selected.

Bit 2 TMC2	Bit 1 TMC1	Bit 0 TMC0	Description
0	0	0	Internal clock: $\phi/8192$. (initial value)
0	0	1	Internal clock: $\phi/2048$.
0	1	0	Internal clock: $\phi/512$.
0	1	1	Internal clock: $\phi/256$.
1	0	0	Internal clock: $\phi/128$.
1	0	1	Internal clock: $\phi/32$.
1	1	0	Internal clock: $\phi/8$.
1	1	1	External clock ($P1_1/\overline{IRQ_1}$): rising or falling edge.*

Note: * External clock edge selection is made by setting bit IEG1 in the IRQ edge select register (IEGR). For details see 3.2.3 2, IRQ edge select register (IEGR). Before setting bits TMC2 to TMC0 to all 1's (111), first set bit IRQC1 to 1 in port mode register 1 (PMR1).

2. Timer counter C (TCC)

Bit	7	6	5	4	3	2	1	0
	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCC is an 8-bit read-only up-/down-counter, which is incremented or decremented by internal or external clock input. The clock source for input to this counter is selected by bits TMC2 to TMC0 in timer mode register C (TMC). The TCC value can be read by the CPU at any time.

When TCC overflows (from H'FF to H'00 or to the value set in TLC) or underflows (from H'00 to H'FF or to the value set in TLC), the IRRTC bit in interrupt request register 2 (IRR2) is set to 1.

TCC is allocated to the same address as timer load register C (TLC).

Upon reset, TCC is initialized to H'00.

3. Timer load register C (TLC)

Bit	7	6	5	4	3	2	1	0
	TLC7	TLC6	TLC5	TLC4	TLC3	TLC2	TLC1	TLC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

TLC is an 8-bit write-only register for setting the reload value of TCC.

When a reload value is set in TLC, the same value is loaded into timer counter C (TCC) as well, and TCC starts counting up or down from that value. When TCC overflows or underflows during operation in auto-reload mode, the TLC value is loaded in TCC. Accordingly, overflow and underflow periods can be set within the range of 1 to 256 input clocks.

The same address is allocated to TLC as to TCC.

Upon reset, TLC is initialized to H'00.

6.4.3 Timer Operation

Timer C is an 8-bit multifunction timer. It can be used as an interval or auto-reload timer, or, depending on the input pin combination, as an event counter.

1. Operation as interval timer

When bit TMC7 in timer mode register C (TMC) is cleared to 0, timer C functions as an 8-bit interval timer.

Upon reset, timer counter C (TCC) is initialized to H'00 and TMC to H'18, so up-counting and interval timing resume immediately after the reset. The clock input to timer C is selected from seven internal clock signals output by prescaler S, or an external clock input at pin $P1_1/\overline{IRQ}_1$. The selection is made by bits TMC2 to TMC0 in TMC.

Either software or hardware can control whether TCC counts up or down. The selection is made by TMC bits TMC6 and TMC5.

After the count value in TCC reaches H'FF (H'00), the next clock signal input causes timer C to overflow (underflow), setting bit IRRTC to 1 in interrupt request register 2 (IRR2). If bit IENTC = 1 in interrupt enable register 2 (IENR2), a CPU interrupt is requested.*

At overflow or underflow, TCC returns to H'00 or H'FF and starts counting up or down again.

During interval timer operation (TMC7 = 0), when a value is set in timer load register C (TLC), the same value is set in TCC.

Note: * For details on interrupts, see 3.2.2, Interrupts.

2. Operation as auto-reload timer

Setting bit TMC7 in TMC to 1 causes timer C to function as an 8-bit auto-reload timer. When a reload value is set in TLC, the same value is loaded into TCC, becoming the value from which TCC starts its count.

After the count value in TCC reaches H'FF (H'00), the next clock signal input causes timer C to overflow (or underflow). The TLC value is then loaded into TCC, and the count continues from that value. The overflow (underflow) period can be set within a range from 1 to 256 input clocks, depending on the TLC value.

The clock sources, up/down control, and interrupts in auto-reload mode are the same as for interval mode.

In auto-reload mode (bit TMC7 = 1), setting a new TLC value also initializes TCC.

3. Operation as event counter

Timer C can operate as an event counter, using $P1_1/\overline{IRQ_1}$ as the event input pin. External event counting is selected by setting bits TMC2 to TMC0 in timer register C (TMC) to all 1's (111). TCC can count either rising or falling edges of the input at pin $P1_1/\overline{IRQ_1}$.

When timer C is used to count external event input, bit IRQC1 in port mode register 1 (PMR1) should be set to 1, and bit IEN1 in interrupt enable register 1 (IENR1) should be cleared to 0 to disable IRQ_1 interrupt requests.

4. TCC up/down control by hardware

The counting direction of timer C can be controlled by input at pin $P9_7/UD$. When bit TMC6 in TMC is set to 1, high-level input at the UD pin selects down-counting, while low-level input selects up-counting.

When using input at pin UD for this control function, set the UP/DOWN bit in port mode register 2 (PMR2) to 1.

6.5 Timer D

6.5.1 Overview

Timer D is an 8-bit event counter, which is incremented by input of an external event signal. Either rising or falling edges of the external event signal can be counted.

1. Features

Features of timer D are given below.

- Choice of rising or falling edge for external event counting.
- An interrupt is requested when the counter overflows.

2. Block diagram

Figure 6-5 shows a block diagram of timer D

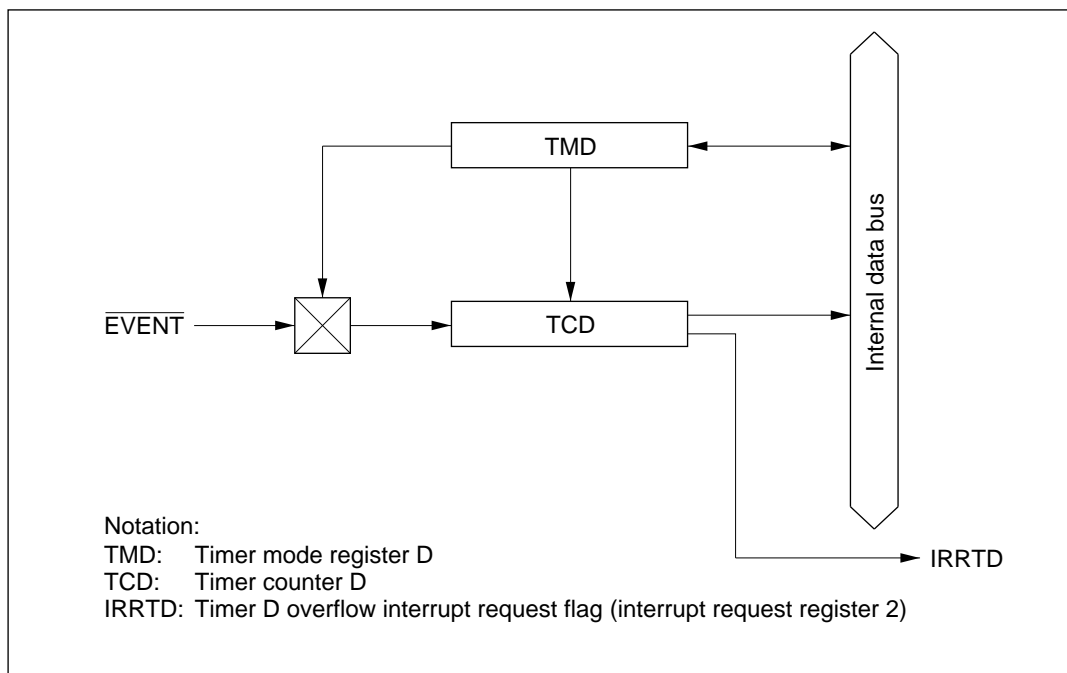


Figure 6-5 Block Diagram

3. Pin configuration

Table 6-7 shows the timer D pin configuration.

Table 6-7 Pin Configuration

Name	Abbrev.	I/O	Function
Event input pin	P1 ₆ /EVENT	Input	Timer D event input

4. Register configuration

Table 6-8 shows the register configuration of timer D.

Table 6-8 Timer D Registers

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register D	TMD	R/W*	H'7E	H'FFC6
Timer counter D	TCD	R	H'00	H'FFC7

Note: * Writing to bit 7 of TMD is possible only when writing 1 to clear the counter.

6.5.2 Register Descriptions

1. Timer mode register D (TMD)

Bit	7	6	5	4	3	2	1	0
	CLR	—	—	—	—	—	—	EDG
Initial value	0	1	1	1	1	1	1	0
Read/Write	W	—	—	—	—	—	—	R/W

TMD is an 8-bit read/write register for clearing timer counter D (TCD), and for selecting whether input at the external event pin is sensed at the rising or falling edge.

Bit 7: Counter clear (CLR)

Bit 7 initializes TCD to H'00.

Bit 7

CLR	Description
0	TCD continues operating. (initial value)
1	TCD is initialized to H'00 (after which this bit is automatically cleared to 0).

Note: It is only possible to write 1 to clear the counter. Writing 0 has no effect on counter operation.

Bits 6 to 1: Reserved bits

Bits 6 to 1 are reserved; they are always read as 1, and cannot be modified.

Bit 0: Edge select (EDG)

Bit 0 selects the rising or falling edge of input at external event pin $P1_6/\overline{EVENT}$.

Bit 0

EDG	Description
0	TCD counts falling edges of input at pin $P1_6/\overline{EVENT}$. (initial value)
1	TCD counts rising edges of input at pin $P1_6/\overline{EVENT}$.

2. Timer counter D (TCD)

Bit	7	6	5	4	3	2	1	0
	TCD7	TCD6	TCD5	TCD4	TCD3	TCD2	TCD1	TCD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCD is an 8-bit read-only up-counter, which is incremented by external clock input at pin $P1_6/\overline{EVENT}$. The input clock edge is selected by the EDG bit in timer mode register D (TMD). The TCD value can be read by the CPU at any time.

When TCD overflows from H'FF to H'00, the IRRTD bit in interrupt request register 2 (IRR2) is set to 1.

Upon reset, TCD is initialized to H'00.

6.5.3 Timer Operation

Timer D operates on an external clock input at pin P1₆/EVENT, used as an event input pin. The rising or falling edge of this input is selected by the EDG bit in timer mode register D (TMD).

After the count value in TCD reaches H'FF, the next clock signal input causes timer D to overflow, setting bit IRRTD in interrupt request register 2 (IRR2) to 1. If bit IENTD = 1 in interrupt enable register 2 (IENR2), a CPU interrupt is requested.*

At overflow, TCD returns to H'00 and starts counting up again.

TCD can be cleared by setting the CLR bit to 1 in TMD.

To use external event input, the EVENT bit in port mode register 1 (PMR1) must be set to 1.

Note: * For details on interrupts, see 3.2.2, Interrupts.

6.6 Timer E

6.6.1 Overview

Timer E is an 8-bit up-counter that increments each time a clock pulse is input. This timer has two operation modes, interval and auto reload. In addition, it can output a square wave with a 50% duty cycle, using overflow signals or signals from prescaler S.

1. Features

Features of timer E are given below.

- Choice of eight internal clock sources ($\phi/8192$, $\phi/4096$, $\phi/2048$, $\phi/512$, $\phi/256$, $\phi/128$, $\phi/32$, $\phi/8$).
- An interrupt is requested when the counter overflows.
- Prescaler signals can provide a fixed-frequency output with a 50% duty cycle.

When $\phi = 4$ MHz, output is 1.95 kHz or 3.9 kHz.

When $\phi = 2$ MHz, output is 0.98 kHz or 1.95 kHz.

- Overflow signals can produce square wave output of any frequency with a 50% duty cycle.

2. Block diagram

Figure 6-6 shows a block diagram of timer E.

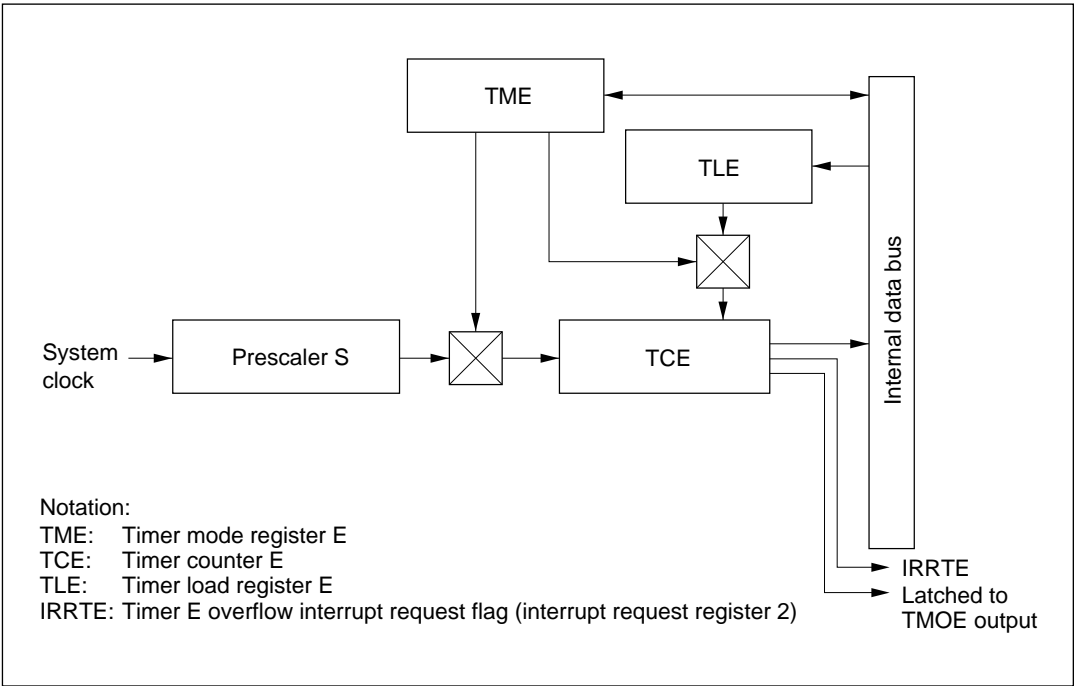


Figure 6-6 Block Diagram

3. Pin configuration

Table 6-9 shows the timer E pin configuration.

Table 6-9 Pin Configuration

Name	Abbrev.	I/O	Function
Timer E waveform output pin	P1 ₅ / $\overline{\text{IRQ}}_5$ /TMOE	Output	Timer E output

4. Register configuration

Table 6-10 shows the register configuration of timer E.

Table 6-10 Timer E Registers

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register E	TME	R/W	H'78	H'FFC8
Timer counter E	TCE	R	H'00	H'FFC9
Timer load register E	TLE	W	H'00	H'FFC9
Port mode register 4	PMR4	R/W	H'0F	H'FFEE

6.6.2 Register Descriptions

1. Timer mode register E (TME)

Bit	7	6	5	4	3	2	1	0
	TME7	—	—	—	—	TME2	TME1	TME0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

TME is an 8-bit read/write register for selecting the auto-reload function and input clock.

Upon reset, TME is initialized to H'78.

Bit 7: Auto-reload function select (TME7)

Bit 7 selects the auto-reload function of timer E.

Bit 7 TME7	Description
0	Interval timer function selected. (initial value)
1	Auto-reload function selected.

Bits 6 to 3: Reserved bits

Bits 6 to 3 are reserved; they are always read as 1, and cannot be modified.

Bits 2 to 0: Clock select (TME2 to TME0)

Bits 2 to 0 select the clock input to TCE.

Bit 2 TME2	Bit 1 TME1	Bit 0 TME0	Description
0	0	0	Internal clock: $\varnothing/8192$. (initial value)
0	0	1	Internal clock: $\varnothing/4096$.
0	1	0	Internal clock: $\varnothing/2048$.
0	1	1	Internal clock: $\varnothing/512$.
1	0	0	Internal clock: $\varnothing/256$.
1	0	1	Internal clock: $\varnothing/128$.
1	1	0	Internal clock: $\varnothing/32$.
1	1	1	Internal clock: $\varnothing/8$.

2. Timer counter E (TCE)

Bit	7	6	5	4	3	2	1	0
	TCE7	TCE6	TCE5	TCE4	TCE3	TCE2	TCE1	TCE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCE is an 8-bit read-only up-counter, which is incremented by internal clock input. The clock source for input to this counter is selected by bits TME2 to TME0 in timer mode register E (TME). The TCE value can be read by the CPU at any time.

When TCE overflows from H'FF to H'00 or to the value set in TLE, the IRRTE bit in interrupt request register 2 (IRR2) is set to 1.

TCE is allocated to the same address as timer load register E (TLE).

Upon reset, TCE is initialized to H'00.

3. Timer load register E (TLE)

Bit	7	6	5	4	3	2	1	0
	TLE7	TLE6	TLE5	TLE4	TLE3	TLE2	TLE1	TLE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

TLE is an 8-bit write-only register for setting the reload value of TCE.

When a reload value is set in TLE, the same value is loaded into timer counter E (TCE) as well, and TCE starts counting up from that value. When TCE overflows during operation in auto-reload mode, the TLE value is loaded in TCE. Accordingly, overflow periods can be set within the range of 1 to 256 input clocks.

The same address is allocated to TLE as to TCE.

Upon reset, TLE is initialized to H'00.

4. Port mode register 4 (PMR4)

Bit	7	6	5	4	3	2	1	0
	TEO	TEO ON	FREQ	VRFR	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

PMR4 is an 8-bit read/write register, for switching functions of pin P1₅/ $\overline{\text{IRQ}}_5$ /TMOE and for controlling waveform output from pin TMOE.

Upon reset, PMR4 is initialized to H'0F.

Bit 7: Timer E output function select (TEO)

Bit 6: Timer E output on/off (TEO ON)

Bit 5: Fixed frequency select (FREQ)

Bit 4: Variable frequency select (VRFR)

Functions of pin $P1_5/\overline{IRQ}_5/TMOE$ are switched as follows, according to the values in bits 7 to 4 of PMR4 and in bit $IRQC5$ of port mode register 1 (PMR1).

PMR1	PMR4				Description	
Bit 5 IRQC5	Bit 7 TEO	Bit 6 TEO ON	Bit 5 FREQ	Bit 4 VRFR	Pin Function	Pin State
0	0	0	0	0	$P1_5$ pin	Standard I/O port (initial value)
0	0	*	*	*	$P1_5$ pin	Standard I/O port
0	1	0	*	*	TMOE output pin (off)	Low-level output
0	1	1	0	0	TMOE output pin (on)	Fixed-frequency output: ($\phi/2048$) 1.95 kHz ($\phi = 4$ MHz) 0.98 kHz ($\phi = 2$ MHz)
0	1	1	1	0	TMOE output pin (on)	Fixed-frequency output: ($\phi/1024$) 3.9 kHz ($\phi = 4$ MHz) 1.95 kHz ($\phi = 2$ MHz)
0	1	1	*	1	TMOE output pin (on)	Variable-frequency output: toggled by timer E overflow
1	*	*	*	*	\overline{IRQ}_5 input pin	External interrupt input

Note: * Don't care.

Bits 3 to 0: Reserved bits

Bits 3 to 0 are reserved; they are always read as 1, and cannot be modified.

6.6.3 Timer Operation

Timer E is an 8-bit up-counter that is incremented each time a clock pulse is input. It functions as an interval or auto-reload timer. It can also output a square wave having a 50% duty cycle. Each of these operation modes is explained below.

1. Interval timer operation

When bit TME7 in timer mode register E (TME) is cleared to 0, timer E functions as an 8-bit interval timer.

Upon reset, timer counter E (TCE) is reset to H'00 and bit TME7 is cleared to 0, so up-counting and interval timing resume immediately after the reset. The clock input to timer E is selected from eight internal clock signals output by prescaler S. The selection is made by bits TME2 to TME0 in TME.

After the count value in TCE reaches H'FF, the next clock signal input causes timer E to overflow, setting bit IRRTE to 1 in interrupt request register 2 (IRR2). If bit IENTE = 1 in interrupt enable register 2 (IENR2), a CPU interrupt is requested.*

At overflow, TCE returns to H'00, and starts counting up again.

During interval timer operation (TME7 = 0), when a value is set in timer load register E (TLE), the same value is set in TCE.

Note: * For details on interrupts, see 3.2.2, Interrupts.

2. Auto-reload timer operation

Setting bit TME7 in TME to 1 causes timer E to function as an 8-bit auto-reload timer. When a reload value is set in TLE, the same value is loaded into TCE, becoming the value from which TCE starts its count.

After the count value in TCE reaches H'FF, the next clock signal input causes timer E to overflow. The TLE value is then loaded into TCE, and the count continues from that value. The overflow period can be set within a range from 1 to 256 input clocks, depending on the TLE value.

The clock sources and interrupts in auto-reload mode are the same as for interval mode.

In auto-reload mode (bit TME7 = 1), setting a new TLE value also initializes TCE.

3. Square wave output

A 50% duty square wave can be output at pin $P1_5/\overline{IRQ}_5/TMOE$ if this function is selected in port mode register 4 (PMR4) and bit $IRQC5$ in port mode register 1 (PMR1). When bit $VRFR = 0$ in PMR4, the square wave has a fixed frequency designated in the $FREQ$ bit. For the frequencies that can be output, see 6.6.2 (4), Port mode register 4 (PMR4).

When bit $VRFR = 1$, timer E overflow generates a toggle output alternating between low and high level (see figure 6-7). The overflow period is selected in timer load register E (TLE), with timer E operating in auto-reload mode (bit $TME7 = 1$). The operating clock can be selected by means of bits $TME2$ to $TME0$. These settings can give a waveform output of any desired frequency within the range shown in table 6-11.

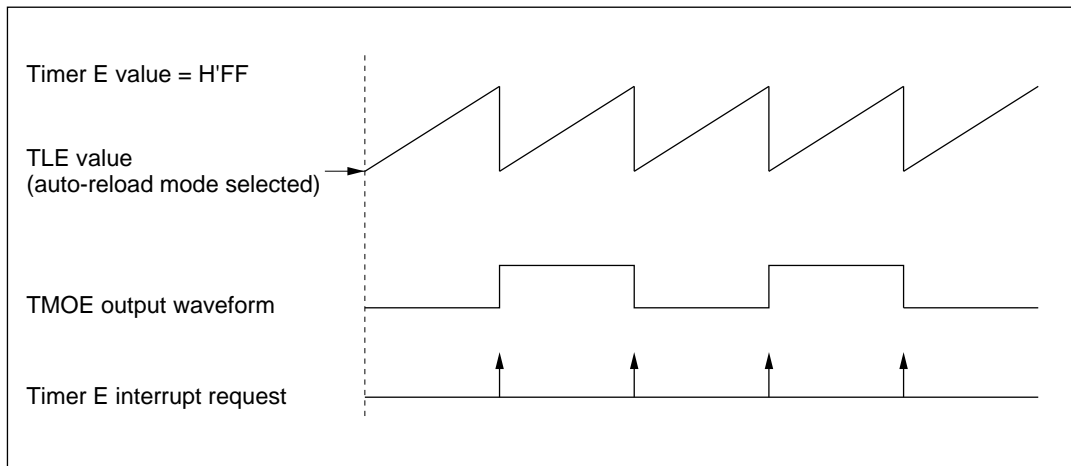


Figure 6-7 Square Wave Output Triggered by Timer E Overflow

Table 6-11 Frequencies of Output Waveforms Triggered by Timer E Overflow

Internal Clock	Output Waveform ($\phi = 2$ MHz)			
	1 Count (TLE = H'FF) $\times 2$		256 Counts (TLE = H'00) $\times 2$	
	Count Time	Output Frequency	Count Time	Output Frequency
$\phi/8$ (250 kHz)	8 μ s	125 kHz	2024 μ s	488.3 Hz
$\phi/32$ (62.5 kHz)	32 μ s	31.25 kHz	8192 μ s	122.1 Hz
$\phi/128$ (15.62 kHz)	128 μ s	7.8125 kHz	32.768 ms	30.5 Hz
$\phi/256$ (7.8125 kHz)	256 μ s	3.9063 kHz	65.536 ms	15.3 Hz
$\phi/512$ (3.9062 kHz)	512 μ s	1.9531 kHz	131.072 ms	7.63 Hz
$\phi/2048$ (976.5 Hz)	2.048 ms	488.3 Hz	524.288 ms	1.91 Hz
$\phi/4096$ (488.2 Hz)	4.096 ms	244.1 Hz	1048.576 ms	0.95 Hz
$\phi/8192$ (244.1 Hz)	8.192 ms	122.1 Hz	2097.152 ms	0.477 Hz

Internal Clock	Output Waveform ($\phi = 4$ MHz)			
	1 Count (TLE = H'FF) $\times 2$		256 Counts (TLE = H'00) $\times 2$	
	Count Time	Output Frequency	Count Time	Output Frequency
$\phi/8$ (500 kHz)	4 μ s	250 kHz	1024 μ s	976.6 Hz
$\phi/32$ (125 kHz)	16 μ s	62.5 kHz	4096 μ s	244.1 Hz
$\phi/128$ (31.25 kHz)	64 μ s	15.625 kHz	16.384 ms	61.0 Hz
$\phi/256$ (15.625 kHz)	128 μ s	7.8125 kHz	32.768 ms	30.5 Hz
$\phi/512$ (7.8125 kHz)	256 μ s	3.9063 kHz	65.536 ms	15.3 Hz
$\phi/2048$ (1.963 Hz)	1.024 ms	976.6 Hz	262.144 ms	3.8 Hz
$\phi/4096$ (976.52 Hz)	2.048 ms	488.3 Hz	524.288 ms	1.91 Hz
$\phi/8192$ (488.2 Hz)	4.096 ms	244.1 Hz	1048.576 ms	0.95 Hz

6.7 Interrupts

Timer A to E interrupts are requested when a timer overflows or underflows. Each timer is assigned its own vector address. The priority of interrupts is in the order of timer A (high) to timer E (low). Further details are given in 3.2.2, Interrupts, table 3-2, Interrupt Sources.

When timers A to E overflow, the corresponding bit IRRTA to IRRTE in interrupt request register 2 (IRR2) is set to 1. These interrupt flags are not cleared even if the interrupt is accepted. They must be cleared to 0 by software in the interrupt handler routine.

Interrupts may be enabled or disabled independently for each timer by means of bits IENTA to IENTE in interrupt enable register 2 (IENR2).

For further details see 3.2.3, Interrupt Control Registers.

6.8 Application Notes

Even when the EVENT bit in port mode register 1 (PMR1) designates the P1₆ usage of pin P1₆/ $\overline{\text{EVENT}}$, reading the P1₆ pin may cause timer D to increment. When using timer D, be sure to clear timer counter D (TCD) by means of the CLR bit in timer mode register D (TMD).

Section 7 14-Bit PWM

7.1 Overview

The H8/3614 and H8/3613 have an on-chip 14-bit pulse width modulator (PWM), which can be used as a D/A converter by connecting a low-pass filter.

Note: The H8/3612 does not have the PWM function.

7.1.1 Features

Features of the 14-bit PWM are as follows.

- Choice of two conversion periods
A conversion period of $32768/\phi$, with a minimum modulation width of $2/\phi$, or a conversion period of $16384/\phi$, with a minimum modulation width of $1/\phi$, can be chosen.
- Pulse division method for less ripple

7.1.2 Block Diagram

Figure 7-1 shows a block diagram of the 14-bit PWM.

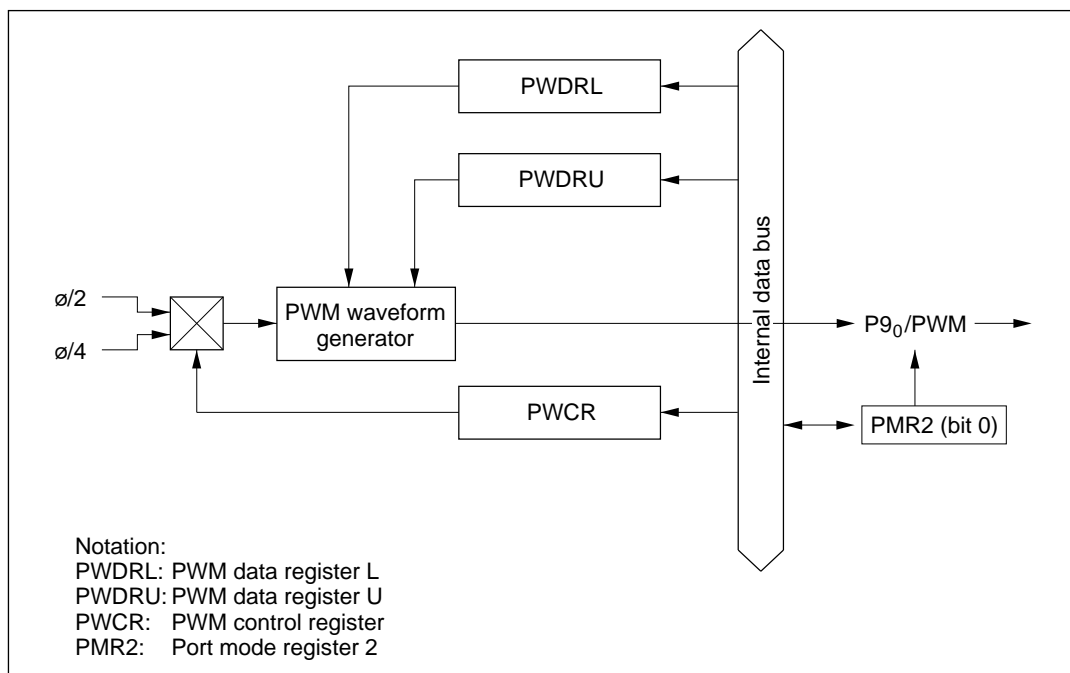


Figure 7-1 Block Diagram of 14-Bit PWM

7.1.3 Pin Configuration

Table 7-1 shows the output pin assigned to the 14-bit PWM.

Table 7-1 Pin Configuration

Name	Abbrev.	I/O	Function
PWM waveform output pin	PWM	Output	PWM waveform output

7.1.4 Register Configuration

Table 7-2 shows the register configuration of the 14-bit PWM.

Table 7-2 Register Configuration

Name	Abbrev.	R/W	Initial Value	Address
PWM control register	PWCR	W	H'FE	H'FFCC
PWM data register U	PWDRU	W	H'C0	H'FFCD
PWM data register L	PWDRL	W	H'00	H'FFCE

7.2 Register Descriptions

7.2.1 PWM Control Register (PWCR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PWCR0
Initial value	1	1	1	1	1	1	1	0
Read/Write	—	—	—	—	—	—	—	W

PWCR is an 8-bit write-only register for input clock selection.

Upon reset, PWCR is initialized to H'FE.

Bits 7 to 1: Reserved bits

Bits 7 to 1 are reserved; they are always read as 1, and cannot be modified.

Bit 0: Clock select (PWCR0)

Bit 0 selects the clock supplied to the 14-bit PWM. This bit is for writing only; it is always read as 1.

Bit 0

PWCR0 Description

0	The input clock is $\phi/2$ ($t\phi = 2/\phi$). The conversion period is $16384/\phi$, (initial value) with a minimum modulation width of $1/\phi$.
1	The input clock is $\phi/4$ ($t\phi = 4/\phi$). The conversion period is $32768/\phi$, with a minimum modulation width of $2/\phi$.

Notation:

$t\phi$: Period of PWM input clock

7.2.2 PWM Data Registers U and L (PWDRU, PWDRL)

Bit	7	6	5	4	3	2	1	0
PWDRU	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDRU1	PWDRU0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Bit	7	6	5	4	3	2	1	0
PWDRL	PWDRL7	PWDRL6	PWDRL5	PWDRL4	PWDRL3	PWDRL2	PWDRL1	PWDRL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PWDRU and PWDRL form a 14-bit write-only register, with the upper 6 bits assigned to PWDRU and the lower 8 bits to PWDRL. The value written to PWDRU and PWDRL gives the total high-level width of one PWM waveform cycle.

When 14-bit data is written to PWDRU and PWDRL, the register contents are latched in the PWM waveform generator, updating the PWM waveform generation data. The 14-bit data should always be written in the following sequence, first to PWDRL and then to PWDRU.

1. Write the lower 8 bits to PWDRL.
2. Write the upper 6 bits to PWDRU.

PWDRU and PWDRL are write-only registers. If they are read, all bits are read as 1.

Upon reset, PWDRU and L are initialized to H'C000.

7.3 Operation

When using the 14-bit PWM, set the registers in the following sequence.

1. Set bit PWM in port mode register 2 (PMR2) to 1 so that pin P9₀/PWM is designated for PWM output.
2. Set bit PWCR0 in the PWM control register (PWCR) to select a conversion period of either 32768/ϕ (PWCR0 = 1) or 16384/ϕ (PWCR0 = 0).
3. Set the output waveform data in PWM data registers U and L (PWDRU/L). Be sure to write in the correct sequence, first PWDRL then PWDRU. When data is written to PWDRU, the data in these registers will be latched in the PWM waveform generator, updating PWM waveform generation in synchronization with internal signals.

One conversion period consists of 64 pulses, as shown in figure 7-2. The total of the high-level pulse widths during this period (T_H) corresponds to the data in PWDRU and PWDRL. This relation can be represented as follows.

$$T_H = (\text{data value in PWDRU and PWDRL} + 64) \times t_{\phi}/2$$

where t_{ϕ} is the PWM input clock period, either 2/ϕ (bit PWCR0 = 0) or 4/ϕ (bit PWCR0 = 1).

If the data value in PWDRU and PWDRL is between H'3FC0 and H'3FFF, the PWM output level will be high.

Example: Settings in order to obtain a conversion period of 8,192 μs:

When bit PWCR0 = 0, the conversion period is 16384/ϕ, so ϕ must be 2 MHz. In this case $t_{fn} = 128 \mu s$, with 1/ϕ (resolution) = 0.5 μs.

When bit PWCR0 = 1, the conversion period is 32768/ϕ, so ϕ must be 4 MHz. In this case $t_{fn} = 128 \mu s$, with 2/ϕ (resolution) = 0.5 μs.

Accordingly, for a conversion period of 8,192 μs, the system clock frequency (ϕ) must be 2 MHz or 4 MHz.

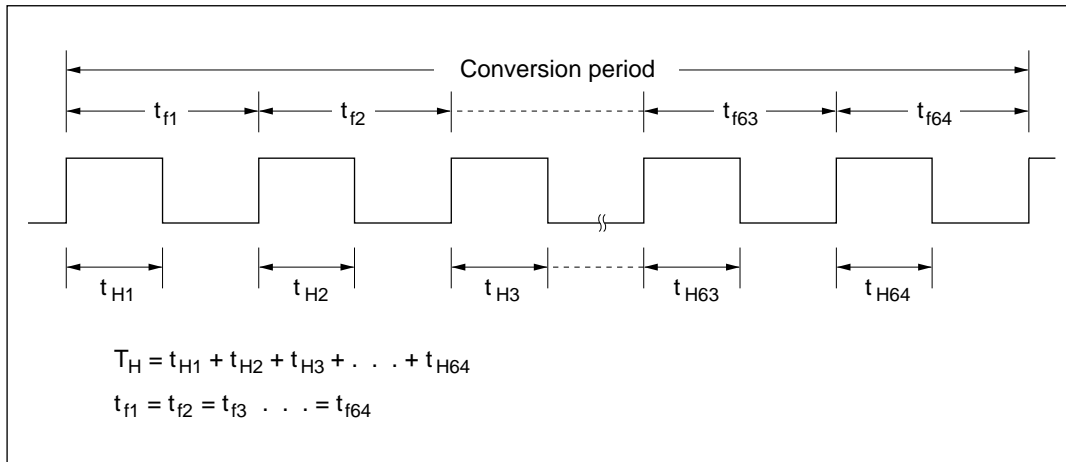


Figure 7-2 PWM Output Waveform

Section 8 SCI1

8.1 Overview

Serial communication interface 1 (SCI1) is for clock-synchronous serial transfer of 8-bit or 16-bit data.

8.1.1 Features

SCI1 features are as follows.

- Choice of 8-bit or 16-bit data transfer
- Choice of eight internal clock sources ($\phi/1024$, $\phi/256$, $\phi/64$, $\phi/32$, $\phi/16$, $\phi/8$, $\phi/4$, $\phi/2$) or an external clock
- Interrupts requested at completion of transfer or when error occurs

8.1.2 Block Diagram

Figure 8-1 shows a block diagram of SCI1.

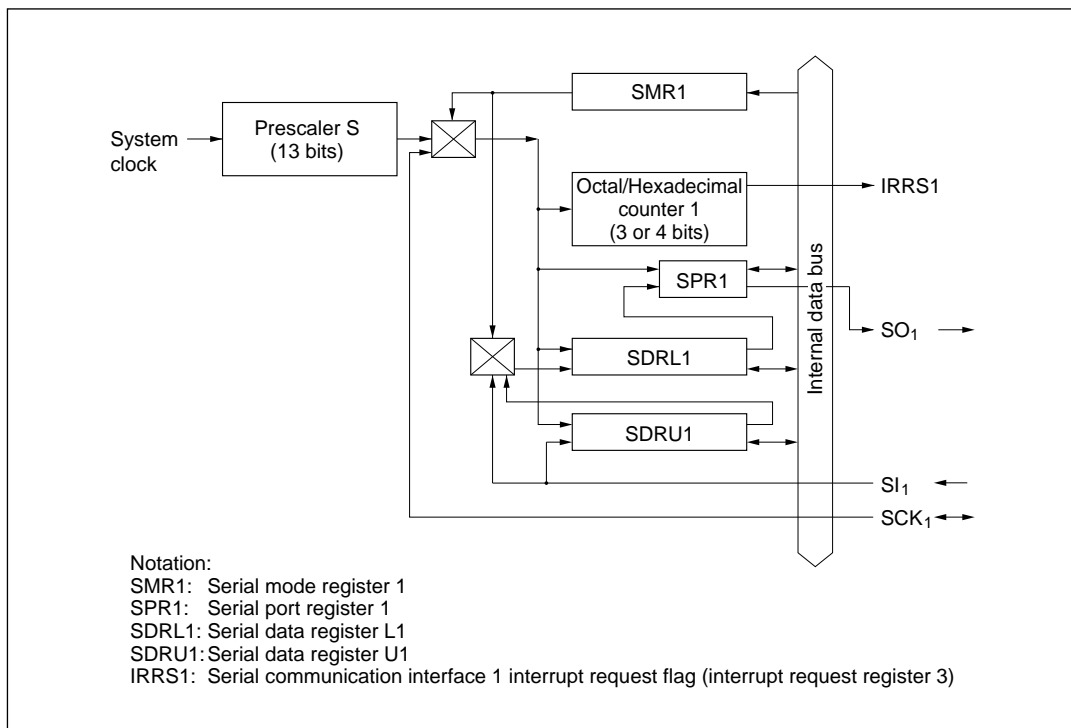


Figure 8-1 Block Diagram of SCI1

8.1.3 Pin Configuration

Table 8-1 shows the SCI1 pin configuration.

Table 8-1 Pin Configuration

Name	Abbrev.	I/O	Function
SCI1 clock pin	P9 ₁ /SCK ₁	I/O	SCI1 clock I/O pin
SCI1 data input pin	P9 ₂ /SI ₁	Input	SCI1 received data input pin
SCI1 data output pin	P9 ₃ /SO ₁	Output	SCI1 transmit data output pin

8.1.4 Register Configuration

Table 8-2 shows the SCI1 register configuration.

Table 8-2 SCI1 Registers

Name	Abbrev.	R/W	Initial Value	Address
Serial mode register 1	SMR1	W	H'80	H'FFB0
Serial data register U1	SDRU1	R/W	Not fixed	H'FFB1
Serial data register L1	SDRL1	R/W	Not fixed	H'FFB2
Serial port register 1	SPR1	R/W	Not fixed	H'FFB3
Port mode register 2	PMR2	R/W	H'00	H'FFEC
Port mode register 3	PMR3	R/W	H'97	H'FFED

8.2 Register Descriptions

8.2.1 Serial Mode Register 1 (SMR1)

Bit	7	6	5	4	3	2	1	0
	—	SMR16	SMR15	SMR14	SMR13	SMR12	SMR11	SMR10
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	W	W	W	W	W	W	W

SMR1 is an 8-bit write-only register, for selecting the operation mode and the prescaler divider ratio. Another function is to initialize the internal state of the serial interface, which happens at each write access to SMR1.

When SMR1 is written to, serial clock supply to serial data registers U1 and L1 (SDRU1, SDRL1) and to the octal/hexadecimal counter is stopped, and the octal/hexadecimal counter is reset to H'00. Accordingly, writing to the serial mode register while the serial interface is operating will abort data transmission or reception, and IRRS1 flag will be set to 1 in interrupt request register 3 (IRR3).

Upon reset, SMR1 is initialized to H'80.

Bit 7: Reserved bit

Bit 7 is reserved; it is always read as 1, and cannot be modified.

Bits 6 to 4: Operation mode select (SMR16 to SMR14)

Bits 6 to 4 select the SCI1 operation mode.

Bit 6 SMR16	Bit 5 SMR15	Bit 4 SMR14	Description
0	0	0	Continuous clock output mode (initial value)
	SMR15, SMR14 set to value other than 00		8-bit transfer mode
1	0	0	Continuous clock output mode
	SMR15, SMR14 set to value other than 00		16-bit transfer mode

Bits 3 to 0: Clock select (SMR13 to SMR10)

Bits 3 to 0 select the clock supplied to SCI1.

Bit 3 SMR13	Bit 2 SMR12	Bit 1 SMR11	Bit 0 SMR10	Pin SCK ₁	Clock Source	Prescaler Divider Ratio	Serial Clock Period (μs)	
							ø = 4 MHz	ø = 2 MHz
0	0	0	0	SCK ₁ output	Prescaler S	ø/1024 (initial value)	256	512
			1	SCK ₁ output	Prescaler S	ø/256	64	128
		1	0	SCK ₁ output	Prescaler S	ø/64	16	32
			1	SCK ₁ output	Prescaler S	ø/32	8	16
	1	0	0	SCK ₁ output	Prescaler S	ø/16	4	8
			1	SCK ₁ output	Prescaler S	ø/8	2	4
		1	0	SCK ₁ output	Prescaler S	ø/4	1	2
			1	SCK ₁ output	Prescaler S	ø/2	—	1
1	0	0	0	Not used	—	—	—	—
	⋮	⋮	⋮					
	1	1	0					
	1	1	1	SCK ₁ input	External clock	—	—	—

8.2.2 Serial Data Register U1 (SDRU1)

Bit	7	6	5	4	3	2	1	0
	SDRU17	SDRU16	SDRU15	SDRU14	SDRU13	SDRU12	SDRU11	SDRU10
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Not fixed

SDRU1 is an 8-bit read/write register. It is used as the data register for the upper 8 bits in 16-bit transfer (SDRL1 is used for the lower 8 bits).

Data written to SDRU1 is output to SDRL1 starting from the least significant bit (LSB), in synchronization with the falling edge of the serial clock. This data is then replaced by LSB-first data input at pin SI1, synchronized with the rising edge of the serial clock. In this way data is shifted in the direction from the most significant bit (MSB) toward the LSB.

SDRU1 must be written or read only after data transmission or reception is complete.

If this register is read or written while a data transfer is in progress, the data contents are not guaranteed.

The SDRU1 value upon reset is not fixed.

8.2.3 Serial Data Register L1 (SDRL1)

Bit	7	6	5	4	3	2	1	0
	SDRL17	SDRL16	SDRL15	SDRL14	SDRL13	SDRL12	SDRL11	SDRL10
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Not fixed

SDRL1 is an 8-bit read/write register. It is used as the data register in 8-bit transfer, and as the data register for the lower 8 bits in 16-bit transfer (SDRU1 is used for the upper 8 bits).

In 8-bit transfer, data written to SDRL1 is output from pin SO1 starting from the least significant bit (LSB), in synchronization with the falling edge of the serial clock. This data is then replaced by LSB-first data input at pin SI1, synchronized with the rising edge of the serial clock. In this way data is shifted in the direction from the most significant bit (MSB) toward the LSB.

In 16-bit transfer, operation is the same as for 8-bit transfer, except that input data is fed in via SDRU1.

SDRL1 must be written or read only after data transmission or reception is complete. If this register is read or written while a data transfer is in progress, the data contents are not guaranteed.

The SDRL1 value upon reset is not fixed.

8.2.4 Serial Port Register 1 (SPR1)

Bit	7	6	5	4	3	2	1	0
	SO1 LAST BIT	—	—	—	—	—	—	—
Initial value	*	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

Note: * Not fixed

SPR1 is an 8-bit read/write register, bit 7 of which is connected to the last output stage of SDRL1.

The SPR1 value upon reset is not fixed.

Bit 7: Extended data bit (SO1 LAST BIT)

Bit 7 holds the last bit of transmitted data after transmission ends.

Output from pin SO1 can be altered by software by modifying this bit either before or after transmission.

If this bit is written during data transmission, the data contents are not guaranteed.

Bit 7**SO1 LAST BIT Description**

0	Output from pin SO ₁ is low. (initial value)
1	Output from pin SO ₁ is high.

Bits 6 to 0: Reserved bits

Bits 6 to 0 are reserved: they are always read as 1, and cannot be modified.

8.2.5 Port Mode Register 2 (PMR2)

Bit	7	6	5	4	3	2	1	0
	UP/ DOWN	SO2	SI2	SCK2	SO1	SI1	SCK1	PWM
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMR2 is an 8-bit read/write register, for switching the port 9 pin functions. Bits 3 to 1, in combination with SMR1, set the SCI1 operation mode.

Upon reset, PMR2 is initialized to H'00.

Bits 3 to 1 are explained here. For bits 7 to 4 and bit 0, see 5.7.2 (1), Port Mode Register 2 (PMR2).

Bit 3: Pin P9₃/SO₁ function switch (SO1)

Bit 3 selects whether pin P9₃/SO₁ functions as a P9₃ input/output pin or as the SO₁ output pin.

Bit 3**SO1 Description**

0	Pin P9 ₃ /SO ₁ functions as P9 ₃ I/O pin. (initial value)
1	Pin P9 ₃ /SO ₁ functions as SO ₁ output pin. Setting bit SCK1 to 1 and clearing bit SI1 to 0 puts SCI1 in transmit mode.

Bit 2: Pin P9₂/SI₁ function switch (SI1)

Bit 2 selects whether pin P9₂/SI₁ functions as a P9₂ input/output pin or as the SI₁ output pin.

Bit 2

SI1	Description
0	Pin P9 ₂ /SI ₁ functions as P9 ₂ I/O pin. (initial value)
1	Pin P9 ₂ /SI ₁ functions as SI ₁ output pin. Setting bit SCK1 to 1 and clearing bit SO1 to 0 puts SCI1 in receive mode.

Bit 1: Pin P9₁/SCK₁ function switch (SCK1)

Bit 1 selects whether pin P9₁/SCK₁ functions as a P9₁ input/output pin or as the SCK₁ input/output pin.

Bit 1

SCK1	Description
0	Pin P9 ₁ /SCK ₁ functions as P9 ₁ I/O pin. (initial value)
1	Pin P9 ₁ /SCK ₁ functions as SCK ₁ I/O pin. The direction of clock I/O and the prescaler divider ratio are set in serial mode register 1 (SMR1).

8.2.6 Port Mode Register 3 (PMR3)

Bit	7	6	5	4	3	2	1	0
	—	SO2 PMOS	CS	—	SO1 PMOS	—	—	—
Initial value	1	0	0	1	0	1	1	1
Read/Write	—	R/W	R/W	—	R/W	—	—	—

PMR3 is an 8-bit read/write register, for enabling the PMOS transistors of SCI1 and SCI2 data output pins (pins SO₁ and SO₂), and for controlling SCI2 chip select output (pin SI₂/ $\overline{\text{CS}}$).

Upon reset, PMR3 is initialized to H'97.

Bit 3 is explained here. For bits 6 and 5, see 9.2.5, Port Mode Register 3 (PMR3).

Bit 3: Pin SO₁ PMOS on/off (SO1PMOS)

Bit 3 enables or disables the PMOS buffer transistor of pin P9₃/SO₁.

Bit 3

SO1PMOS	Description
0	The PMOS transistor of pin P9 ₃ /SO ₁ is enabled: CMOS output. (initial value)
1	The PMOS transistor of pin P9 ₃ /SO ₁ is disabled: NMOS open-drain output.

8.3 Operation

8.3.1 Overview

SCI1 sends and receives data in synchronization with clock pulses.

SCI1 operation modes are set by bits 6 to 4 of serial mode register 1 (SMR1) and bits 3 to 1 of port mode register 2 (PMR2) in combination, as shown in table 8-3.

Table 8-3 SCI1 Operation Mode Setting

SMR1			PMR2			Operation Mode
SMR16	SMR15	SMR14	PMR23	PMR22	PMR21	
*	*	*	0	0	0	Serial communication disabled
*	0	0	0	0	1	Continuous clock output mode
0	SMR15, SMR14 set to value other than 00		1	0	1	8-bit transmit mode
			0	1	1	8-bit receive mode
			1	1	1	8-bit transmit/receive mode
1	SMR15, SMR14 set to value other than 00		1	0	1	16-bit transmit mode
			0	1	1	16-bit receive mode
			1	1	1	16-bit transmit/receive mode

Note: * Don't care.

Pin SCK₁ and the serial clock are controlled by writing data to SMR1.

SDRU1 and SDRL1 are used to write transmit data and to hold received data; these registers can be written and read by software. Data in these registers is shifted in synchronization with the serial clock, for input and output at pins SI₁ and SO₁.

SCI1 operation starts with a dummy read of SMR1. The octal/hexadecimal counter is cleared to H'0 by this dummy read, and starts counting anew from the falling edge of the serial clock (pin SCK₁), being incremented by 1 at each rising edge of the serial clock. If 8 or 16 serial clock cycles are input and the counter overflows, or if data transmission or reception is aborted, the octal/hexadecimal counter is cleared to H'0. At the same time bit IRRS1 in interrupt request register 3 (IRR3) is set to 1.

For more details on interrupts, see 3.2.2, Interrupts.

8.3.2 Data Transfer Format

Figure 8-2 shows the synchronous data transfer format. Data can be sent and received in lengths of 8 bits or 16 bits. Data is sent and received starting from the least significant bit, in LSB-first format. Transmit data is output from one falling edge of the serial clock until the next falling edge. Receive data is latched at the rising edge of the serial clock.

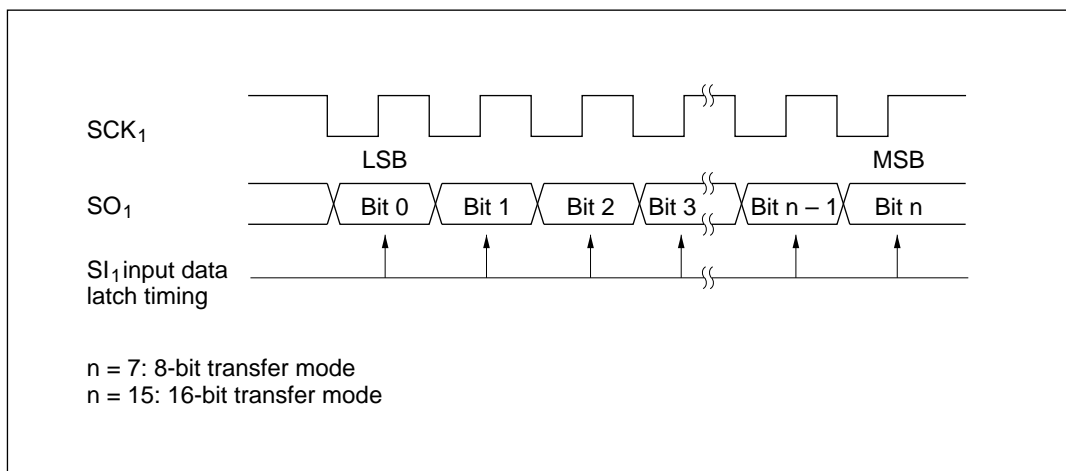


Figure 8-2 Synchronous Data Transfer Format

8.3.3 Clock

Eight internal clock sources or an external clock may be selected as the serial clock. When an internal clock is used, pin SCK₁ is the clock output pin.

8.3.4 Data Transmit/Receive

- Initializing SCI1

Before data is sent or received, first SCI1 must be initialized by software. This is done by writing the desired transfer conditions in serial mode register 1 (SMR1).

- Transmitting

A transmit operation is carried out as follows.

- 1 Set bit SO1 in port mode register 2 (PMR2) to 1, making pin P9₃/SO₁ the SO₁ output pin. Also set bit SCK1 in PMR2 to 1, making pin P9₁/SCK₁ the SCK₁ I/O pin. If necessary, set the SO1PMOS bit in PMR3 for NMOS open-drain output at pin SO₁.

- 2 Set bit SMR16 in SMR1 to 1 or 0, and set bits SMR15 and SMR14 to a value other than 00, designating 8- or 16-bit transfer mode. Select the serial clock with bits SMR13 to SMR10. Writing data to SMR1 initializes the internal state of SCI1.
- 3 Write transmit data in serial data register L1 (SDRL1) and serial data register U1 (SDRU1), as follows.
 8-bit transfer mode: SDRL1
 16-bit transfer mode: Upper byte in SDRU1, lower byte in SDRL1
- 4 Execute a dummy read of SMR1. SCI1 starts operating, and outputs the transmit data at pin SO₁.
- 5 After data transmission is complete, bit IRRS1 in interrupt request register 3 (IRR3) is set to 1.

When an internal clock source is used, a serial clock is output from pin SCK₁ in synchronization with the transmit data. After data transmission is complete, the serial clock is not output until the next dummy read of SMR1. During this time, pin SO₁ continues to output the value of the last bit transmitted.

When an external clock source is used, data is transmitted in synchronization with the serial clock input at pin SCK₁. After data transmission is complete, if the serial clock continues to be input, transmission resumes.

Between transmissions, the output value of pin SO₁ can be changed by rewriting bit 7 (SO1 LAST BIT) in serial port register 1 (SPR1).

Executing a dummy read of SMR1 during transmission will cause a transmit error, setting bit IRRS1 in IRR3 to 1.

- Receiving

A receive operation is carried out as follows.

- 1 Set bit SI1 in port mode register 2 (PMR2) to 1, making pin P9₂/SI₁ the SI₁ input pin. Also set bit SCK1 in PMR2 to 1, making pin P9₁/SCK₁ the SCK₁ I/O pin.
- 2 Set bit SMR16 in serial mode register 1 (SMR1) to 1 or 0, and set bits SMR15 and SMR14 to a value other than 00, designating 8- or 16-bit transfer mode. Select the serial clock with bits SMR13 to SMR10. Writing data to SMR1 initializes the internal state of SCI1.
- 3 Execute a dummy read of SMR1. SCI1 starts operating, and receive data is input at pin SI₁.
- 4 After data reception is complete, bit IRRS1 in interrupt request register 3 (IRR3) is set to 1.

- 5 Read the received data from SDRL1 and SDRU1, as follows.

8-bit transfer mode: SDRL1

16-bit transfer mode: Upper byte in SDRU1, lower byte in SDRL1

When an internal clock source is used, a dummy read of SMR1 immediately starts a data receive operation. The serial clock is output from pin SCK₁.

When an external clock source is used, after the dummy read of SMR1, data is received in synchronization with the serial clock input at pin SCK₁. After data reception is complete, if the serial clock continues to be input, reception resumes.

Executing a dummy read of SMR1 during reception will cause a receive error, setting bit IRRS1 in IRR3 to 1.

- Simultaneous transmit/receive

A simultaneous transmit/receive operation is carried out as follows.

- 1 Set bits SO1, SI1, and SCK1 in PMR2 to 1, designating the SO₁ output pin, SI₁ pin, and SCK₁ pin functions. If necessary, set the SO1PMOS bit in PMR3 for NMOS open-drain output at pin SO₁.
- 2 Set bit SMR16 in SMR1 to 1 or 0, and set bits SMR15 and SMR14 to a value other than 00, designating 8- or 16-bit transfer mode. Select the serial clock with bits SMR13 to SMR10. Writing data to SMR1 initializes the internal state of SCI1.
- 3 Write transmit data in SDRL1 and SDRU1, as follows.
8-bit transfer mode: SDRL1
16-bit transfer mode: Upper byte in SDRU1, lower byte in SDRL1
- 4 Execute a dummy read of SMR1. SCI1 starts operating: transmit data is output at pin SO₁, and receive data is input at pin SI₁.
- 5 After data transmission and reception are complete, bit IRRS1 in IRR3 is set to 1.
- 6 Read the received data from SDRL1 and SDRU1.
8-bit transfer mode: SDRL1
16-bit transfer mode: Upper byte in SDRU1, lower byte in SDRL1

In simultaneous data transmit/receive, the transmit operation and receive operation described in 8.3.4 sections 2 and 3 take place at the same time. See those sections for further details.

During a transmit/receive operation, a dummy read of SMR1 will result in a transmit/receive error, setting bit IRRS1 in IRR3 to 1.

8.3.5 SCI1 State Transitions

SCI1 has three internal states, as shown in figure 8-3.

In the serial start pending state, the internal state of the serial communication interface is initialized. In this state, the serial communication interface does not operate even if a serial clock signal is input. Executing a dummy read of SMR1 changes this state to the serial clock pending state.

In the serial clock pending state, when a serial clock signal is input the octal/hexadecimal counter starts counting up and the serial data register starts shifting, entering the transfer state. If continuous clock output mode has been selected, however, SCI1 outputs the clock signal continuously and does not enter the transfer state.

In the transfer state, when 8 or 16 transfer clock cycles are input, or if an SMR1 dummy read is executed, the octal/hexadecimal counter is reset to H'0, and SCI1 enters the serial clock pending state. Writing to SMR1 in the transfer state will reset the octal/hexadecimal counter to H'0 and change to the serial start pending state. In transitions from the transfer state to another state, the resetting of the octal/hexadecimal counter to H'0 sets bit IRRS1 in IRR3 to 1.

If an internal clock source is selected, a dummy read of SMR1 starts output of the serial clock, which stops after 8 or 16 clock output cycles.

After writing to SMR1 in the serial clock pending state or transfer state, it is necessary to write to SMR1 again in order to initialize the initial state of the serial communication interface. Writing to SMR1 changes the state to the serial start pending state.

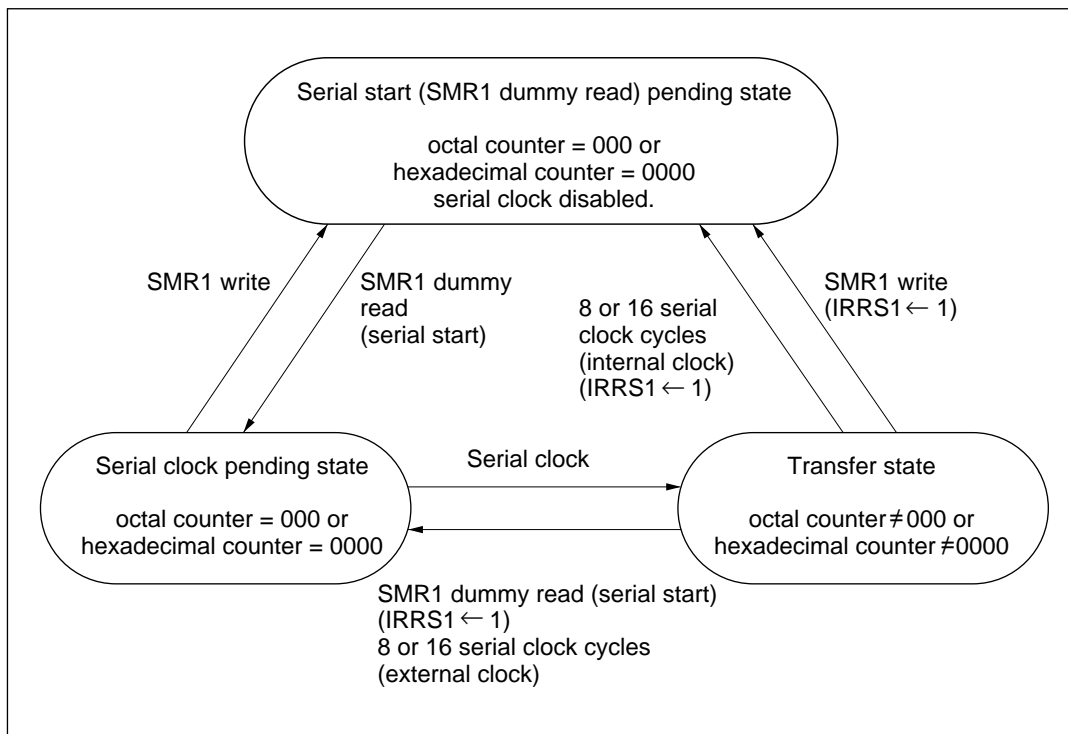


Figure 8-3 SCI1 State Transitions

8.3.6 Serial Clock Error Detection

In the transfer state, if an extraneous pulse is superimposed on the normal serial clock signal due to external noise, SCI1 may function incorrectly. Serial clock errors can be detected by means of the procedure shown in figure 8-4.

In the serial clock pending state, if more than the normal 8 or 16 serial clock cycles are mistakenly input, SCI1 changes from the transfer state to the serial clock pending state and then back to the transfer state. After bit IRRS1 in interrupt request register 3 (IRR3) is cleared to 0, writing a value in serial mode register 1 (SMR1) changes the state to serial start pending, and bit IRRS1 is again set to 1.

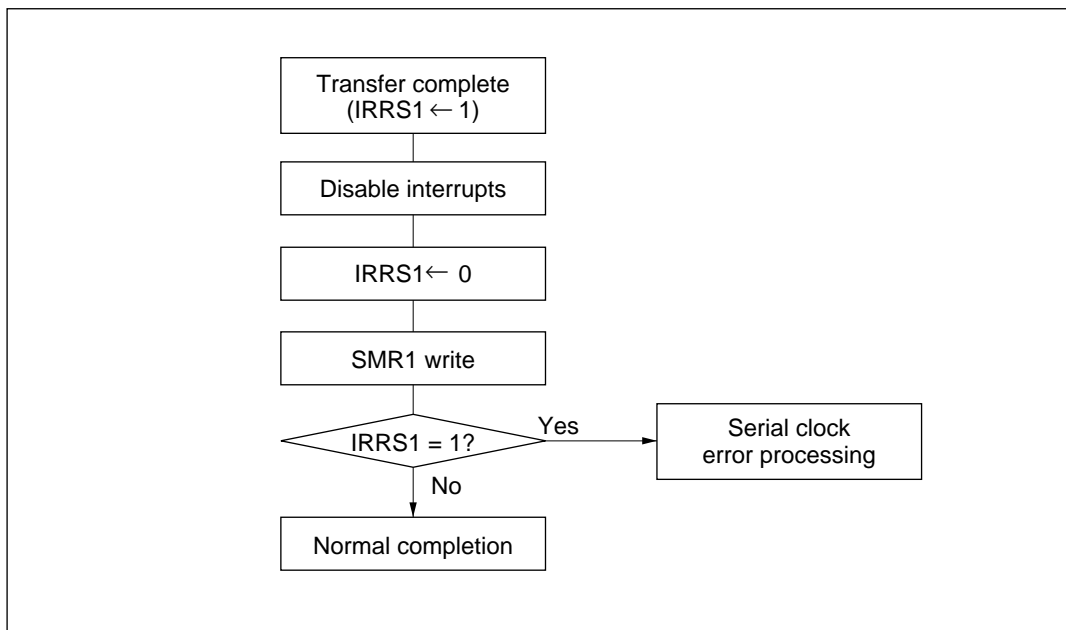


Figure 8-4 Procedure for Detecting Serial Clock Errors

8.3.7 Interrupts

SCI1 can generate interrupts for completion of transfer and for transmit/receive errors. These interrupts are assigned to the same vector address.

When an SCI1 transfer is complete, or when a transmit/receive error occurs before the transfer is complete, bit IRRS1 in interrupt request register 3 (IRR3) is set to 1. SCI1 interrupt requests can be enabled or disabled in bit IENS1 of interrupt enable register 3 (IENR3).

For further details, see 3.2.2, Interrupts.

Section 9 SCI2

9.1 Overview

Serial communication interface 2 (SCI2) has a 32-byte data buffer, for synchronous serial transfer of up to 32 bytes of data in one operation.

9.1.1 Features

SCI2 features are as follows.

- Automatic transfer of up to 32 bytes of data
- Choice of internal clock sources ($\phi/8$, $\phi/4$, $\phi/2$) or an external clock
- Interrupts requested at completion of transfer or when error occurs

9.1.2 Block Diagram

Figure 9-1 shows a block diagram of SCI2.

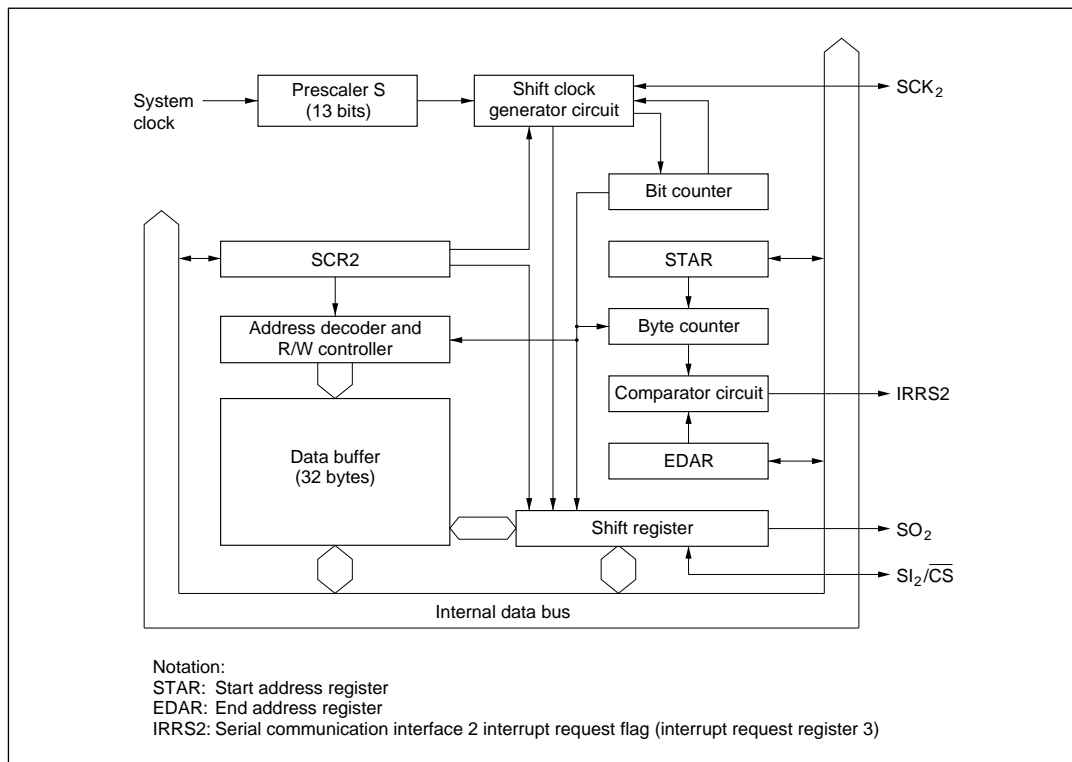


Figure 9-1 Block Diagram of SCI2

9.1.3 Pin Configuration

Table 9-1 shows the SCI2 pin configuration.

Table 9-1 Pin Configuration

Name	Abbrev.	I/O	Function
SCI2 clock pin	SCK ₂	I/O	SCI2 clock input/output
SCI2 data input pin	SI ₂	Input	SCI2 receive data input
SCI2 data output pin	SO ₂	Output	SCI2 transmit data output
SCI2 chip select output pin	$\overline{\text{CS}}$	Output	SCI2 chip select output

Note: Functions of pins P9₄/SCK₂, P9₅/SI₂/ $\overline{\text{CS}}$, and P9₆/SO₂ are switched in port mode register 2 (PMR2) and port mode register 3 (PMR3). For PMR2, see 5.7.2 (1), Port mode register 2 (PMR2).

9.1.4 Register Configuration

Table 9-2 shows the SCI2 register configuration.

Table 9-2 SCI2 Registers

Name	Abbrev.	R/W	Initial Value	Address
32-byte data buffer	—	R/W	Not fixed	H'FF80 to H'FF9F
Start address register	STAR	R/W	H'E0	H'FFA0
End address register	EDAR	R/W	H'E0	H'FFA1
Serial control register 2	SCR2	R/W	H'E0	H'FFA2
Status register	STSR	R/W	H'E0/H'E8	H'FFA3
Port mode register 2	PMR2	R/W	H'00	H'FFEC
Port mode register 3	PMR3	R/W	H'97	H'FFED

9.2 Register Descriptions

9.2.1 Start Address Register (STAR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	STA4	STA3	STA2	STA1	STA0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

STAR is an 8-bit read/write register, for designating the transfer start address in the memory area from H'FF80 to H'FF9F allocated to the 32-byte data buffer.

The 32 bytes from H'00 to H'1F designated by the lower 5 bits of STAR (bits STA4 to STA0) correspond to addresses H'FF80 to H'FF9F.

Data is sent or received continuously using the area defined in STAR and in the end address register (EDAR).

Bits 7 to 5 are reserved; they are always read as 1, and cannot be modified.

Upon reset, STAR is initialized to H'E0.

9.2.2 End Address Register (EDAR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	EDA4	EDA3	EDA2	EDA1	EDA0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

EDAR is an 8-bit read/write register, for designating the transfer end address in the memory area from H'FF80 to H'FF9F allocated to the 32-byte data buffer.

The 32 bytes from H'00 to H'1F designated by the lower 5 bits of EDAR (bits EDA4 to EDA0) correspond to addresses H'FF80 to H'FF9F.

Data is sent or received continuously using the area defined in STAR and EDAR. If the same value is designated in both STAR and EDAR, only one byte of data is transferred.

Bits 7 to 5 are reserved; they are always read as 1, and cannot be modified.

Upon reset, EDAR is initialized to H'E0.

9.2.3 Serial Control Register 2 (SCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	I/O	GAP2	GAP1	PS1	PS0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

SCR2 is an 8-bit read/write register, for selecting whether SCI2 transmits or receives, for gap insertion during continuous transfer, and for serial clock selection.

Upon reset, SCR2 is initialized to H'E0.

Bits 7 to 5: Reserved bits

Bits 7 to 5 are reserved; they are always read as 1, and cannot be modified.

Bit 4: Transmit/receive select (I/O)

Bit 4 selects SCI2 transmit or receive mode.

Bit 4

I/O	Description
0	SCI2 is in receive mode. (initial value)
1	SCI2 is in transmit mode.

Bits 3 and 2: Gap insertion (GAP2 to GAP1)

When data is transmitted or received continuously, gaps can be inserted at data divisions by holding the serial clock high for a length of time designated by bits 3 and 2. Bits 3 and 2 are valid when an internal clock source is selected as the serial clock (PS1 and 0 ≠ 11).

Data divisions may be placed every 8 bits or 16 bits; this is selected in bit GIT in the status register (STSR).

Bit 3 GAP2	Bit 2 GAP1	Description
0	0	Serial clock keeps the same duty cycle even at data divisions. (initial value)
0	1	Serial clock high level extended by one clock cycle at data divisions.
1	0	Serial clock high level extended by two clock cycles at data divisions.
1	1	Serial clock high level extended by eight clock cycles at data divisions.

Bits 1 and 0: Transfer clock select (PS1 to PS0)

Bits 1 and 0 select one of three internal clock sources or an external clock.

PS1	PS0	Pin SCK ₂	Clock Source	Prescaler Divider Ratio	Serial Clock Period		
					ø = 4 MHz	ø = 2 MHz	ø = 1 MHz
0	0	SCK ₂ output	Prescaler S	ø/2 (initial value) *	1 µs	2 µs	2 µs
0	1	SCK ₂ output	Prescaler S	ø/4	1 µs	2 µs	4 µs
1	0	SCK ₂ output	Prescaler S	ø/8	2 µs	4 µs	8 µs
1	1	SCK ₂ input	External clock	—	—	—	—

Note: * Can be set, but operation is not guaranteed.

9.2.4 Status Register (STSR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	SO ₂ LAST BIT	OVR	WT	GIT	STF
Initial value	1	1	1	0	*1	0	0	0
Read/Write	—	—	—	R/W	R/W*2	R/W*2	R/W	R/W

- Notes: 1. Not fixed
2. Cleared to 0 by write operation to STSR.

STSR is an 8-bit register indicating the SCI2 operation state, error status, etc. Writing to this register during data transmission may cause misoperation.

Upon reset, STSR is initialized to H'E0 or H'E8.

Bits 7 to 5: Reserved bits

Bits 7 to 5 are reserved; they are always read as 1, and cannot be modified.

Bit 4: Extended data bit (SO₂ LAST BIT)

Bit 4 holds the last bit of transmitted data after transmission ends.

Output from pin SO₂ can be altered by software by modifying this bit either before or after transmission.

Note that, if STF is cleared to 0 during transmission to effect a forcible termination, the transmit data is changed when the write is performed.

Bit 4

SO2 LAST BIT	Description	
0	Output from pin SO ₂ is low.	(initial value)
1	Output from pin SO ₂ is high.	

Bit 3: Overrun flag (OVR)

If the amount of data transferred exceeds the buffer size setting, or if an extraneous pulse is superimposed on the normal serial clock due to external noise, SCI2 overruns and bit 3 is set to 1. The initial value is not fixed.

Bit 3

OVR	Description	
0	[Clear conditions] When STSR is written to.	
1	[Set conditions] When overrun occurs.	

Bit 2: Waiting flag (WT)

If an attempt is made to execute a read or write instruction to the 32-byte buffer during a serial data transfer, the instruction is ignored, and bit 2 is set to 1 along with bit IRRS2 in interrupt request register 3 (IRR3).

Bit 2

WT	Description	
0	[Clear conditions] When STSR is written to.	(initial value)
1	[Set conditions] When a read/write to the 32-byte buffer is attempted during serial transfer.	

Bit 1: Gap interval flag (GIT)

Bit 1 designates whether the extended serial clock high-level interval designated in bits GAP2 and GAP1 in serial control register 2 (SCR2) occurs every 8 bits or every 16 bits. This setting is valid only for internal clock operation.

Bit 1

GIT	Description	
0	Gap specified by GAP2 and GAP1 is inserted every 16 bits.	(initial value)
1	Gap specified by GAP2 and GAP1 is inserted every 8 bits.	

Bit 0: Start/busy flag (STF)

Setting bit 0 to 1 starts an SCI2 transfer operation. This bit stays at 1 during the transfer, and is cleared to 0 after the transfer is complete. It can therefore be used as a busy flag as well. Clearing this bit to 0 during a transfer aborts the transfer, initializing SCI2. The contents of the 32-byte data buffer and of registers other than STSR are unchanged when this happens. When this bit is set to 1 to start a transfer, the transfer begins from the data indicated by STAR.

Bit 0

STF	Explanation
0	[Read access] (initial value) Indicates transfer not in progress. [Write access] Stops transfer.
1	[Read access] Indicates transfer in progress. [Write access] Starts transfer.

9.2.5 Port Mode Register 3 (PMR3)

Bit	7	6	5	4	3	2	1	0
	—	SO2 PMOS	CS	—	SO1 PMOS	—	—	—
Initial value	1	0	0	1	0	1	1	1
Read/Write	—	R/W	R/W	—	R/W	—	—	—

PMR3 is an 8-bit read/write register, for enabling the PMOS transistors of SCI1 and SCI2 data output pins (pin P9₃/SO₁ and pin P9₆/SO₂), and for controlling SCI2 chip select output (pin SI₂/CS).

Upon reset, PMR3 is initialized to H'97.

For bit 3, see 8.2.6, Port Mode Register 3 (PMR3).

Bit 7: Reserved bit

Bit 7 is reserved; it is always read as 1, and cannot be modified.

Bit 6: Pin SO₂ PMOS on/off (SO2PMOS)

Bit 6 enables or disables the PMOS buffer transistor of pin P9₆/SO₂.

Bit 6**SO2PMOS Description**

0	PMOS transistor of pin P9 ₆ /SO ₂ is enabled: CMOS output. (initial value)
1	PMOS transistor of pin P9 ₆ /SO ₂ is disabled: NMOS open-drain output.

Bit 5: Chip select output select (CS)

In combination with bit SI2 in port mode register 2 (PMR2), bit 5 selects the \overline{CS} output function of pin P9₅/SI₂/ \overline{CS} . The \overline{CS} output pin function is valid in transmit mode.

PMR2 PMR3**Bit 5 Bit 5****SI2 CS Description**

0	*	Pin P9 ₅ /SI ₂ / \overline{CS} functions as P9 ₅ I/O pin. (initial value)
1	0	Pin P9 ₅ /SI ₂ / \overline{CS} functions as SI ₂ input pin.
	1	Pin P9 ₅ /SI ₂ / \overline{CS} functions as \overline{CS} output pin.

Note: * Don't care.

Bits 4 and 2 to 0: Reserved bits

These bits are reserved; they are always read as 1, and cannot be modified.

9.3 Operation

9.3.1 Overview

SCI2 has a 32-byte data buffer, making possible continuous transfer of up to 32 bytes of data with one operation. SCI2 transmits and receives data in synchronization with clock pulses.

Selection of transmit or receive mode and of the serial clock is made in serial control register 2 (SCR2).

The start address register (STAR) and end address register (EDAR) designate the area within the 32-byte data buffer for holding transfer data. The address range from H'FF80 to H'FF9F is allocated to this data buffer. The start and end positions of the transfer data area are indicated in the lower 5 bits of STAR and EDAR.

After parameters have been set in port mode register 2 (PMR2), port mode register 3 (PMR3), SCR2, STAR, and EDAR, then when the STF bit of the status register (STSR) is set to 1, SCI2 begins a transfer operation. STF remains set to 1 during the transfer, and is cleared to 0 when the transfer is complete. The STF bit can therefore be used as a busy flag. Clearing the STF bit to 0 during a transfer stops the transfer operation and initializes SCI2. The contents of the data buffer and of other registers are unchanged in this case.

During a transfer, the CPU cannot read or write the data buffer. If a write instruction is issued it is ignored; it has the same effect as a NOP instruction except that it takes more states. Read access during a transfer yields H'FF.

When the transfer is complete, or if a data buffer read or write is attempted during the transfer, bit IRRS2 in interrupt request register 3 (IRR3) is set to 1. In case of an overrun error or a data buffer read or write during the transfer, bit OVR or WT of STSR is set to 1.

Note: If the start address is set to a value higher than the end address, the result is as shown in figure 9-2. The data transfer wraps around from address H'FF9F to address H'FF80 and continues to the end address.

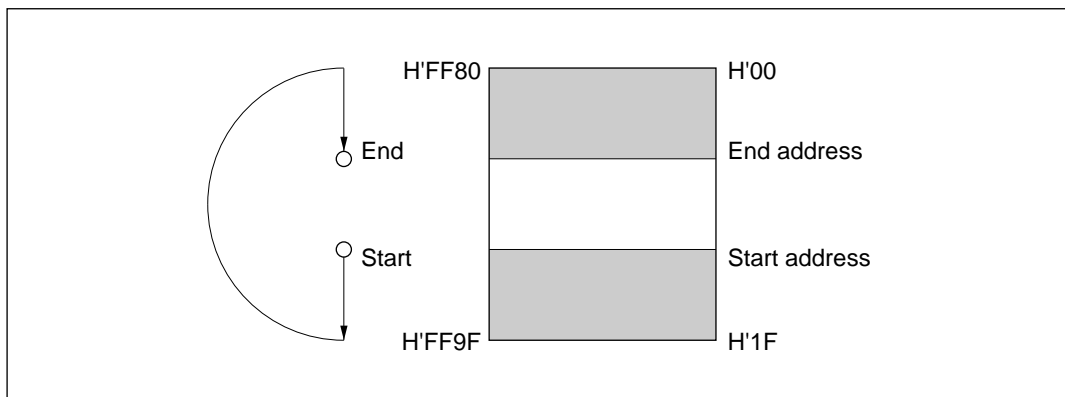


Figure 9-2 Operation When Start Address Exceeds End Address

9.3.2 Clock

Three internal clock sources or an external clock may be selected as the serial clock. When an internal clock is selected, pin SCK_2 becomes the clock output pin.

9.3.3 Data Transfer Format

Figure 9-3 shows the SCI2 data transfer format. Data is sent and received starting from the least significant bit, in LSB-first format. Transmit data is output from one falling edge of the serial clock until the next falling edge. Receive data is latched at the rising edge of the clock.

When SCI2 operates on an internal clock and is in transmit mode, a gap may be inserted at data divisions (every 8 bits or 16 bits). During this gap, the serial clock stays at the high level for a designated number of clock cycles (see figures 9-4 to 9-6).

The \overline{CS} output remains low during the gap.

Gap insertion and the length of the gap are designated in bits GAP2 and GAP1 in serial control register 2 (SCR2). Bit GIT in the status register (STSR) designates whether gaps occur at 8-bit or 16-bit intervals.

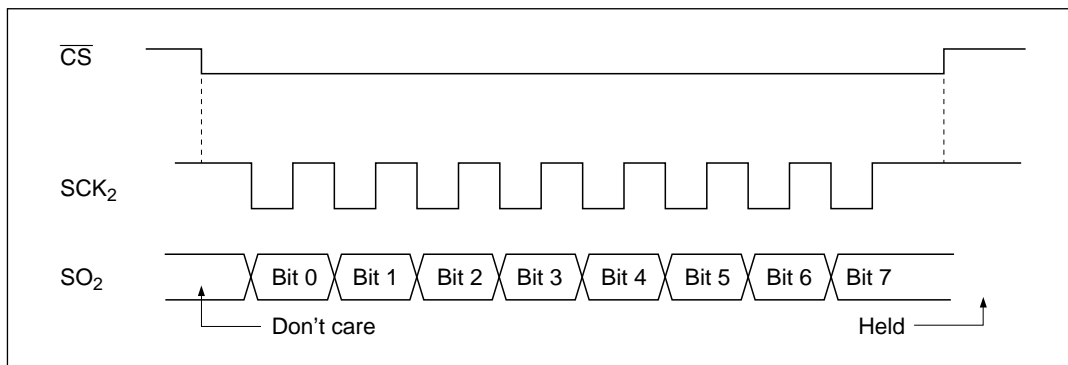


Figure 9-3 Synchronous Data Transfer Format

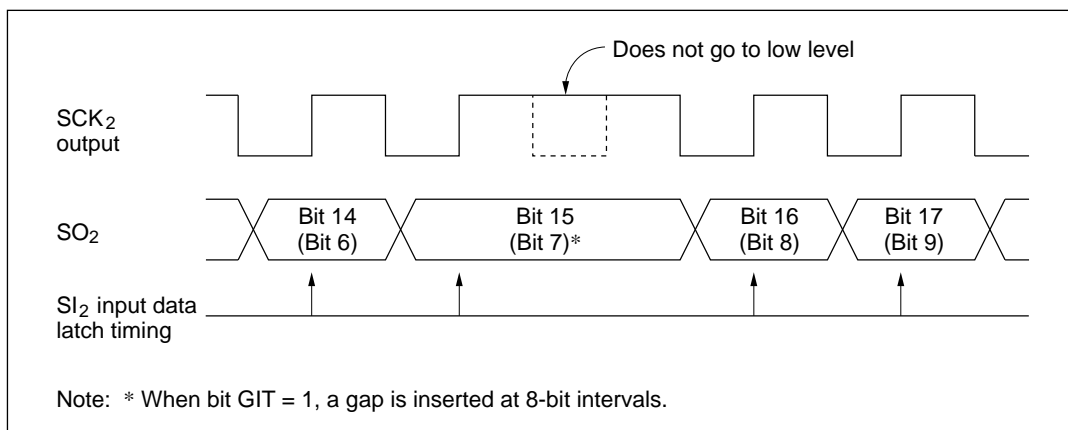


Figure 9-4 1-Clock Gap Insertion (Bits GAP2 and GAP1 = 01)

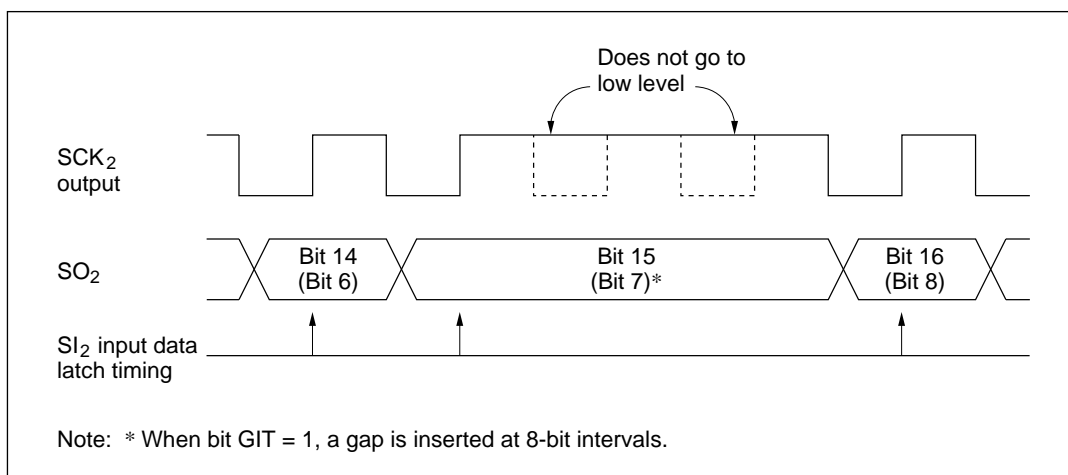


Figure 9-5 2-Clock Gap Insertion (Bits GAP2 and GAP1 = 10)

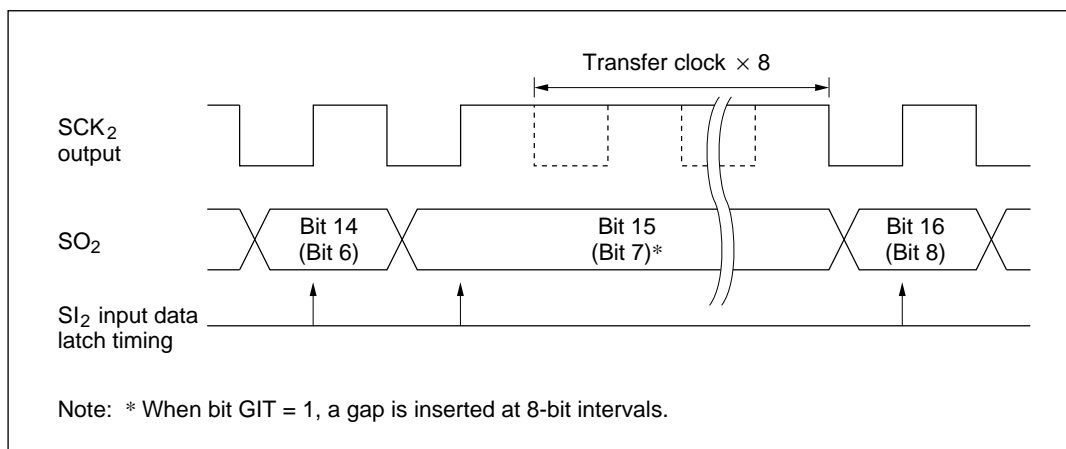


Figure 9-6 8-Clock Gap Insertion (Bits GAP2 and GAP1 = 11)

9.3.4 Data Transmit/Receive

- Initializing SCI2

Before data is sent or received, first SCI2 must be initialized by software. This involves clearing bit STF in the status register (STSR) to 0, then selecting pin functions and transfer modes in port mode register 2 (PMR2), port mode register 3 (PMR3), the start address register (STAR), the end address register (EDAR), and serial control register 2 (SCR2).

- Transmitting

A transmit operation is carried out as follows.

- 1 Set bit SO2 in port mode register 2 (PMR2) to 1, making pin P9₆/SO₂ the SO₂ output pin. If necessary, set the SO2PMOS bit and CS bit in PMR3 for NMOS open-drain output at pin SO₂ and for chip select output at pin P9₅/SI₂/ $\overline{\text{CS}}$.
- 2 Write transmit data in the 32-byte data buffer (H'FF80 to H'FF9F).
- 3 Set the transfer start address in the lower 5 bits of STAR.
- 4 Set the transfer end address in the lower 5 bits of EDAR.
- 5 In SCR2, select transmit mode (bit I/O = 1), the serial clock, and gap insertion (internal clock operation only).
- 6 Select the data gap interval with bit GIT of STRS, then set bit STF to 1. Setting bit STF starts the transmit operation.

- 7 After data transmission is complete, bit IRRS2 in interrupt request register 3 (IRR3) is set to 1, and bit STF in STSR is cleared to 0.

If an internal clock source is used, a serial clock is output from pin SCK₂ in synchronization with the transmit data. After data transmission is completed, the serial clock is not output until bit STF is again set. During this time, pin SO₂ continues to output the value of the last bit transmitted.

When an external clock source is used, data is transmitted in synchronization with the serial clock input at pin SCK₂. After data transmission is completed, further transmission does not take place even if the serial clock continues to be input; pin SO₂ continues to output the value of the last bit transmitted.

Between transmissions, the output value of pin SO₂ can be changed by rewriting bit SO2 LAST BIT in STSR.

An attempt to read or write the data buffer during transmission will cause bit IRRS2 in IRR3 to be set to 1. Bit WT in STSR will also be set to 1.

- Receiving

A receive operation is carried out as follows.

- 1 Set bit SI2 in port mode register 2 (PMR2) to 1, making pin P9₅/SI₁/CS the SI₂ input pin.
- 2 Allocate an area to hold the received data in the 32-byte data buffer and set the start address in the lower 5 bits of the start address register (STAR).
- 3 Set the transfer end address in the lower 5 bits of the end address register (EDAR).
- 4 In serial control register 2 (SCR2), select receive mode (bit I/O = 0) and the serial clock.
- 5 Set bit STF of the status register (STSR) to 1, starting the receive operation.
- 6 After receiving is completed, bit IRRS2 in interrupt request register 3 (IRR3) is set to 1, and bit STF is cleared to 0.
- 7 Read the received data from the data buffer.

If an internal clock source is used, setting bit STF to 1 in STSR immediately starts a data receive operation. The serial clock is output from pin SCK₂.

When an external clock source is used, after bit STF is set, data is received in synchronization with the clock input at pin SCK₂. After receiving is completed, no further receive operations take place until bit STF is again set, even if the serial clock continues to be input.

An attempt to read or write the data buffer during receiving will cause bit IRRS2 in IRR3 and bit WT in STSR to be set to 1. Bit OVR in STSR is set to 1 if an overrun error occurs.

When SCI2 operates on an internal clock and is in transmit mode, a gap may be inserted at data divisions (every 8 bits or 16 bits). During this gap, serial clock stays at the high level for a designated number of clock cycles (see figures 9-4 through 9-6).

Gap insertion and the length of the gap are designated in bits GAP2 and GAP1 of SCR2. Bit GIT of STSR designates whether gaps occur at 8-bit or 16-bit intervals.

9.4 Interrupts

SCI2 can generate interrupts when a transfer is completed and when the data buffer is read or written during a transfer. These interrupts are assigned to the same vector address.

When the above conditions occur, bit IRRS2 in interrupt request register 3 (IRR3) is set to 1. SCI2 interrupt requests can be enabled or disabled in bit IENS2 of interrupt enable register 3 (IENR3). For further details, see 3.2.2, Interrupts.

When an overrun error occurs, or when a read or write of the data buffer is attempted during a transfer, the OVR or WT bit in the status register (STSR) is set to 1. These bits can be used to determine the cause of the error.

9.5 Application Notes

1. Do not write to any register during a transfer (while bit STF of STSR is set to 1), since this can cause misoperation.
2. When receiving, set bit SI2 in port mode register 2 (PMR2) to 1 and clear bit CS in port mode register 3 (PMR3) to 0 to select the SI₂ pin function. If bit CS = 1 and bit SI2 = 1, selecting the $\overline{\text{CS}}$ pin function, incorrect data will be received.

Section 10 A/D Converter

10.1 Overview

The H8/3614 Series includes on-chip a resistance-ladder type successive-approximation A/D converter, which can convert up to eight channels of analog input.

10.1.1 Features

The A/D converter has the following features.

- 8-bit resolution
- Eight input channels
- Conversion time: 14.8 μ s per channel (min, at $f_{osc} = 8.38$ MHz)
- Built-in sample-and-hold function
- Interrupt requested on completion of A/D conversion

10.1.2 Block Diagram

Figure 10-1 shows a block diagram of the A/D converter.

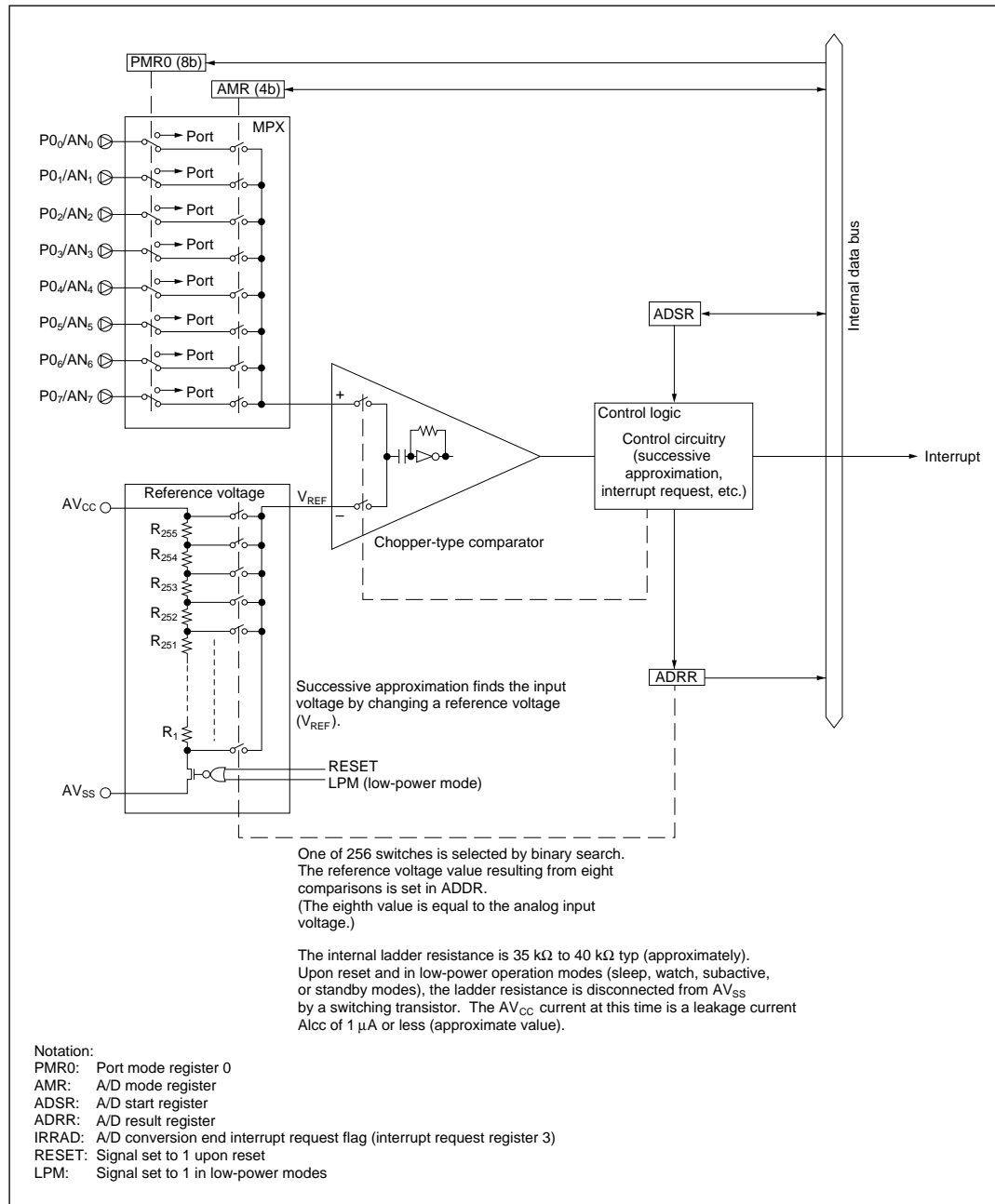


Figure 10-1 Block Diagram of A/D Converter

10.1.3 Pin Configuration

Table 10-1 shows the A/D converter pin configuration.

Table 10-1 Pin Configuration

Name	Abbrev.	I/O	Function
Analog power supply pin	AV _{CC}	Input	Analog power supply and reference voltage
Analog ground pin	AV _{SS}	Input	Analog ground and reference voltage
Analog input pin 0	AN ₀	Input	Analog input channel 0
Analog input pin 1	AN ₁	Input	Analog input channel 1
Analog input pin 2	AN ₂	Input	Analog input channel 2
Analog input pin 3	AN ₃	Input	Analog input channel 3
Analog input pin 4	AN ₄	Input	Analog input channel 4
Analog input pin 5	AN ₅	Input	Analog input channel 5
Analog input pin 6	AN ₆	Input	Analog input channel 6
Analog input pin 7	AN ₇	Input	Analog input channel 7

10.1.4 Register Configuration

Table 10-2 shows the A/D converter register configuration.

Table 10-2 Register Configuration

Name	Abbrev.	R/W	Initial Value	Address
A/D mode register	AMR	R/W	H'78	H'FFBC
A/D start register	ADSR	R/W	H'7F	H'FFBE
A/D result register	ADRR	R	Not fixed	H'FFBD
Port mode register 0	PMR0	W	H'00	H'FFEF

10.2 Register Descriptions

10.2.1 A/D Result Register (ADRR)

Bit	7	6	5	4	3	2	1	0
	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
Initial value	*	*	*	*	*	*	*	*
Read/Write	R	R	R	R	R	R	R	R

Note: * Not fixed

ADRR is an 8-bit read-only register for holding the result of analog-to-digital conversion.

ADRR can be read by the CPU at any time, but the ADRR value during A/D conversion is not fixed.

After A/D conversion is complete, the conversion result is stored in ADRR as 8-bit data; this data is held in ADRR until the next conversion operation starts.

ADRR is not cleared on reset.

10.2.2 A/D Mode Register (AMR)

Bit	7	6	5	4	3	2	1	0
	AMR7	—	—	—	—	AMR2	AMR1	AMR0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

AMR is an 8-bit read/write register for selecting the A/D conversion speed and analog input pin.

Writing to AMR should be done with the A/D start flag (ADSF) cleared to 0 in the A/D start register (ADSR).

Upon reset, AMR is initialized to H'78.

Bit 7: Clock select (AMR7)

Bit 7 sets the A/D conversion speed.*1

Bit 7 AMR7	Conversion Period*2	$\phi = 2\text{ MHz}$	$\phi = 4.19\text{ MHz}$	
0	$62/\phi$	$31\text{ }\mu\text{s}$	$14.8\text{ }\mu\text{s}$	(initial value)
1	$31/\phi$	$15.5\text{ }\mu\text{s}$	—*1	

- Notes: 1. Operation is not guaranteed if the conversion time is less than $14.8\text{ }\mu\text{s}$. Set bit 7 for a value of at least $14.8\text{ }\mu\text{s}$.
2. A/D conversion starts after a value of 1 is written to ADSF. The conversion period starts when the start flag is set and ends when it is reset upon completion of conversion. The actual time during which sample and hold are repeated is called the conversion interval (see figure 10-2).

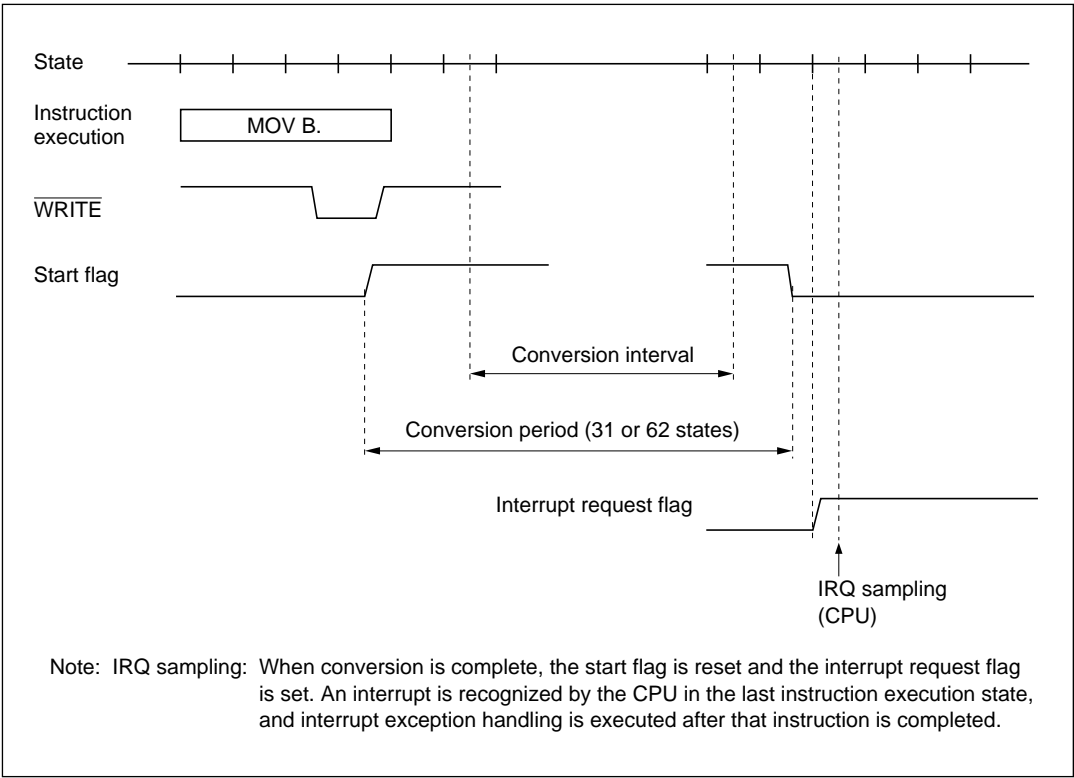


Figure 10-2 Internal Operation of A/D Converter

Bits 6 to 3: Reserved bits

Bits 6 to 3 are reserved; they are always read as 1, and cannot be modified.

Bits 2 to 0: Channel select (AMR2 to AMR0)

Bits 2 to 0 select the analog input channel.

Settings are also required in port mode register 0 (PMR0). See 10.2.4, Port Mode Register 0 (PMR0).

Bit 2 AMR2	Bit 1 AMR1	Bit 0 AMR0	Analog Input Channel
0	0	0	AN ₀ (initial value)
0	0	1	AN ₁
0	1	0	AN ₂
0	1	1	AN ₃
1	0	0	AN ₄
1	0	1	AN ₅
1	1	0	AN ₆
1	1	1	AN ₇

10.2.3 A/D Start Register (ADSR)

Bit	7	6	5	4	3	2	1	0
	ADSF	—	—	—	—	—	—	—
Initial value	0	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

The A/D start register (ADSR) is an 8-bit read/write register for starting and stopping A/D conversion.

A/D conversion is started by writing 1 to the A/D start flag (ADSF). When conversion is complete, the converted data is set in the A/D result register (ADRR), and at the same time ADSF is cleared to 0.

Bit 7: A/D start flag (ADSF)

Bit 7 is for controlling and confirming the start and end of A/D conversion.

Bit 7

ADSF	Description
0	[Read access] (initial value) Indicates that A/D conversion has been completed or stopped. [Write access] Stops A/D conversion.
1	[Read access] Indicates A/D conversion in progress. [Write access] Starts A/D conversion.

Bits 6 to 0: Reserved bits

Bits 6 to 0 are reserved; they are always read as 1, and cannot be modified.

10.2.4 Port Mode Register 0 (PMR0)

Bit	7	6	5	4	3	2	1	0
	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PMR0 is an 8-bit write-only register for designating whether each of the port 0 pins is used as a general-purpose input pin or as an analog input channel to the A/D converter. Designation is made separately for each pin.

Upon reset, PMR0 is initialized to H'00.

Bit n	Description
ANn	
0	Pin P0 _n /AN _n is used for general-purpose input. (initial value)
1	Pin P0 _n /AN _n is an analog input channel.

(n = 0 to 7)

10.3 Operation

The A/D converter operates by successive approximations, and yields its conversion result as 8-bit data.

A/D conversion begins when software sets the A/D start flag (bit ADSF) to 1. Bit ADSF keeps a value of 1 during A/D conversion, and is cleared to 0 automatically when conversion is complete.

The completion of conversion also sets bit IRRAD in interrupt request register 3 (IRR3) to 1. An A/D conversion end interrupt is requested if bit IENAD in interrupt enable register 3 (IENR3) is set to 1.

If the conversion time or input channel needs to be changed in the A/D mode register (AMR) during A/D conversion, bit ADSF should first be cleared to 0, stopping the conversion operation, in order to avoid misoperation.

10.4 Interrupts

When A/D conversion is complete (ADSF changes from 1 to 0), bit IRRAD in interrupt request register 3 (IRR3) is set to 1.

A/D conversion end interrupts can be enabled or disabled by means of bit IENAD in interrupt enable register 3 (IENR3).

For further details see 3.2.2, Interrupts.

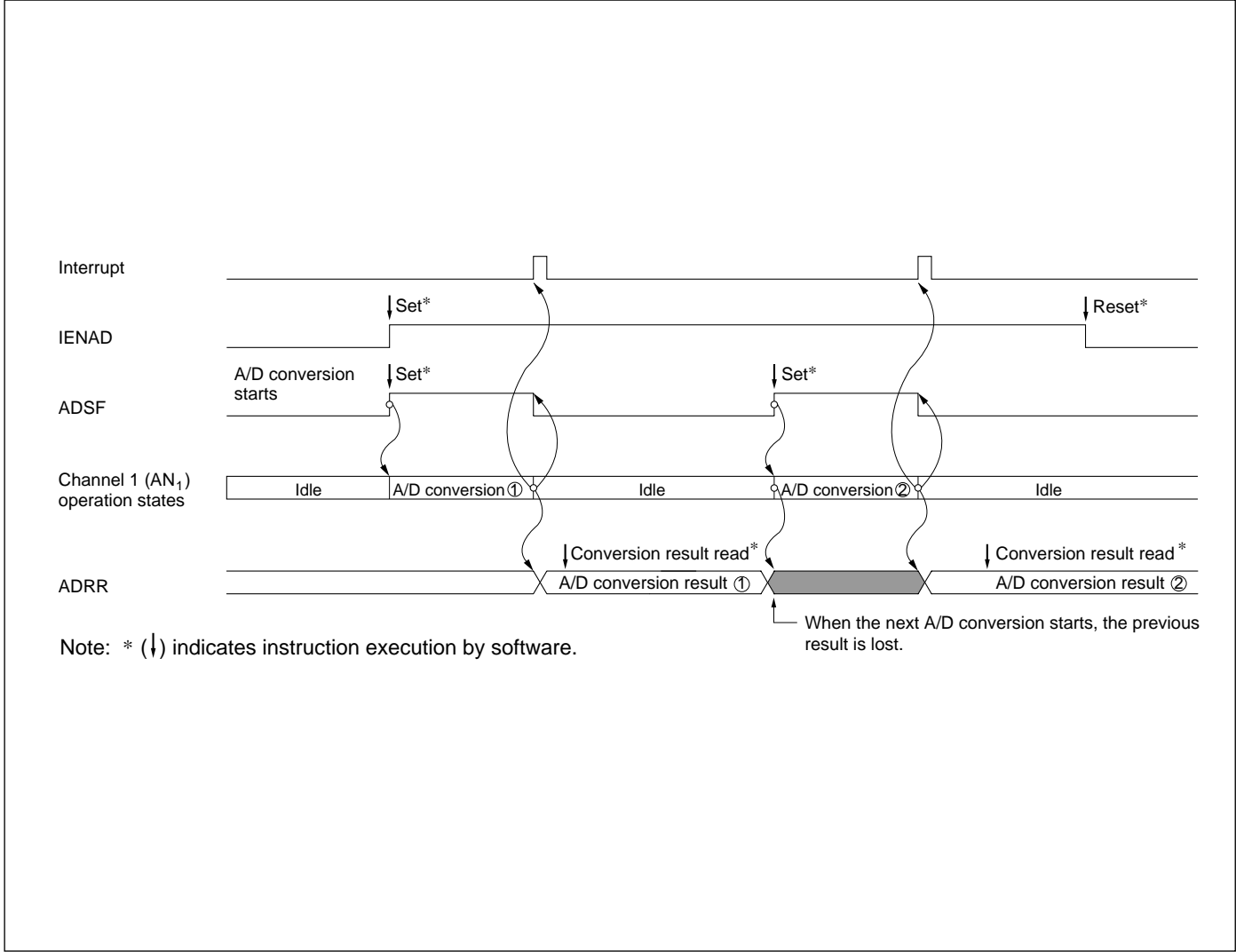
10.5 Typical Use

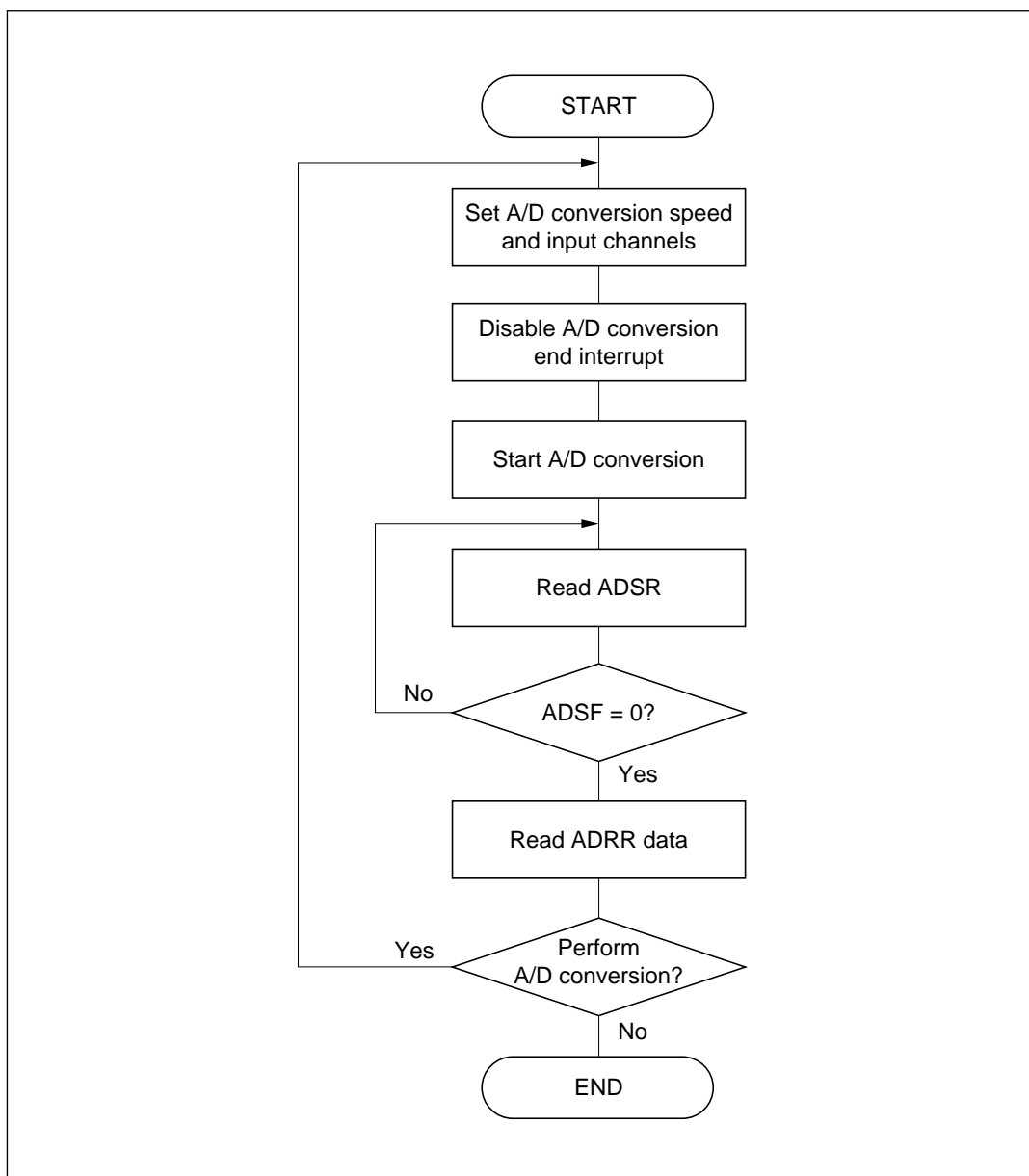
An example of how the A/D converter can be used is given below, using channel 1 (AN₁) as the analog input channel. Figure 13-3 shows the operation timing for this example.

1. Bits AMR2 to AMR0 of the A/D mode register (AMR) are set to 001, and bits AN7 to AN0 of port mode register 0 (PMR0) are set to 00000010, making AN₁ the analog input channel. The interrupt request is cleared by setting bit IRRAD to 0, A/D interrupts are enabled by setting bit IENAD to 1, and A/D conversion is started by setting bit ADSF to 1.
2. When A/D conversion is complete, bit IRRAD is set to 1, and the A/D conversion results are sent to the A/D result register (ADRR). At the same time ADSF is cleared to 0, and the A/D converter goes to the idle state.
3. Bit IENAD = 1, so an A/D conversion end interrupt is requested.
4. The A/D interrupt handling routine starts.
5. The A/D conversion result is read and processed.
6. The A/D interrupt handling routine ends.

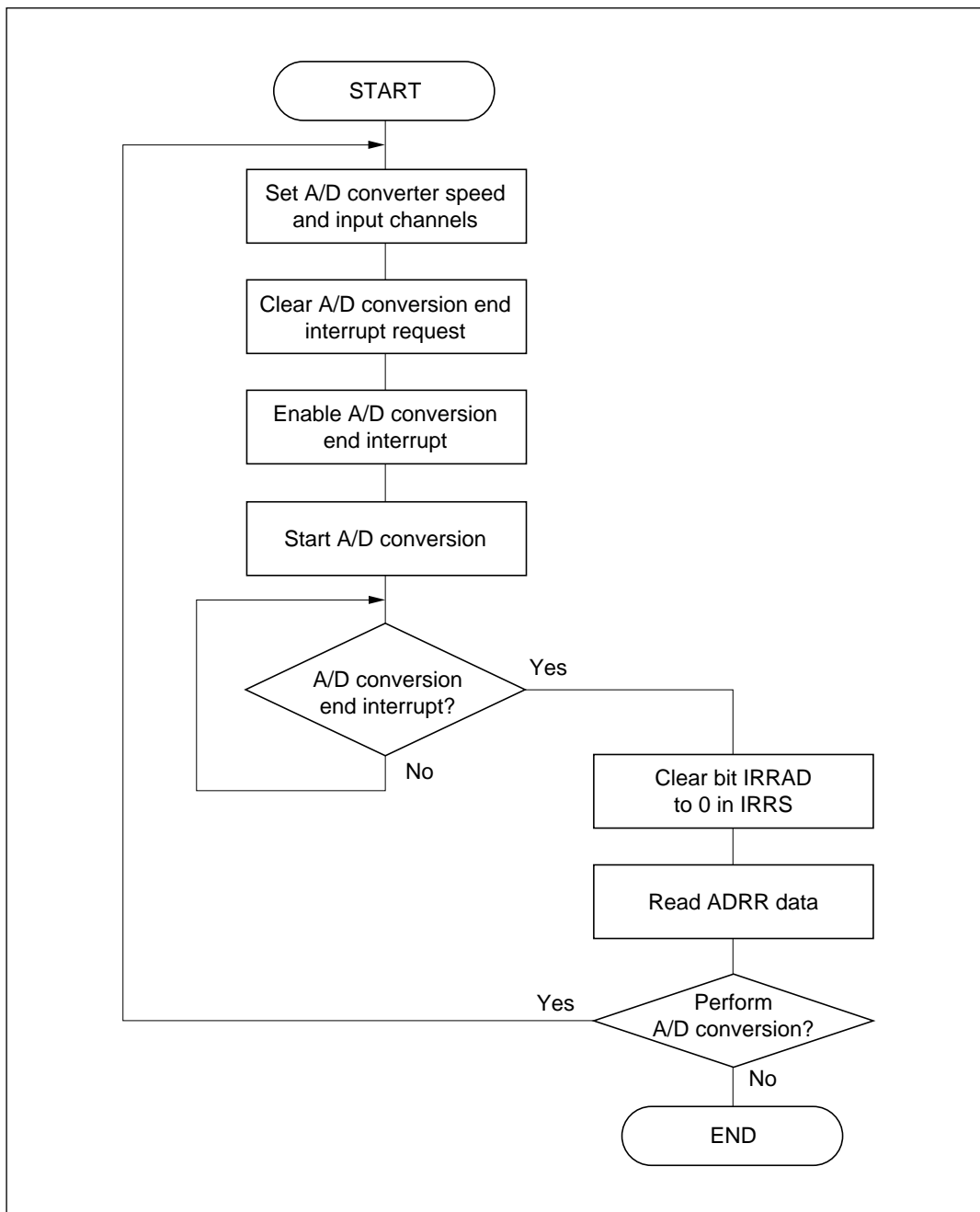
If ADSF is set to 1 again afterward, A/D conversion starts and steps 2 through 6 take place.

Figures 10-4 and 10-5 show flow charts of procedures for using the A/D converter.





**Figure 10-4 Flow Chart of Procedure for Using A/D Converter (1)
(Polling by Software)**



**Figure 10-5 Flow Chart of Procedure for Using A/D Converter (2)
(Interrupts Used)**

10.6 Application Notes

1. Data in the A/D result register (ADRR) should be read only when the A/D start flag (ADSF) in the A/D start register (ADSR) is cleared to 0.
2. Changing a digital input signal at a nearby pin during A/D conversion may adversely affect conversion accuracy.
3. The pin selected as an analog input channel in the A/D mode register (AMR) must also be designated as an analog input channel in port mode register 0 (PMR0).

Section 11 RAM

11.1 Overview

The H8/3612 has 512 bytes of high-speed static RAM on-chip. The H8/3613 and H8/3614 have 1024 bytes. The RAM is connected to the CPU by a 16-bit data bus, allowing high-speed two-state access for both byte data and word data.

11.1.1 Block Diagram

Figure 11-1 shows a block diagram of the on-chip RAM.

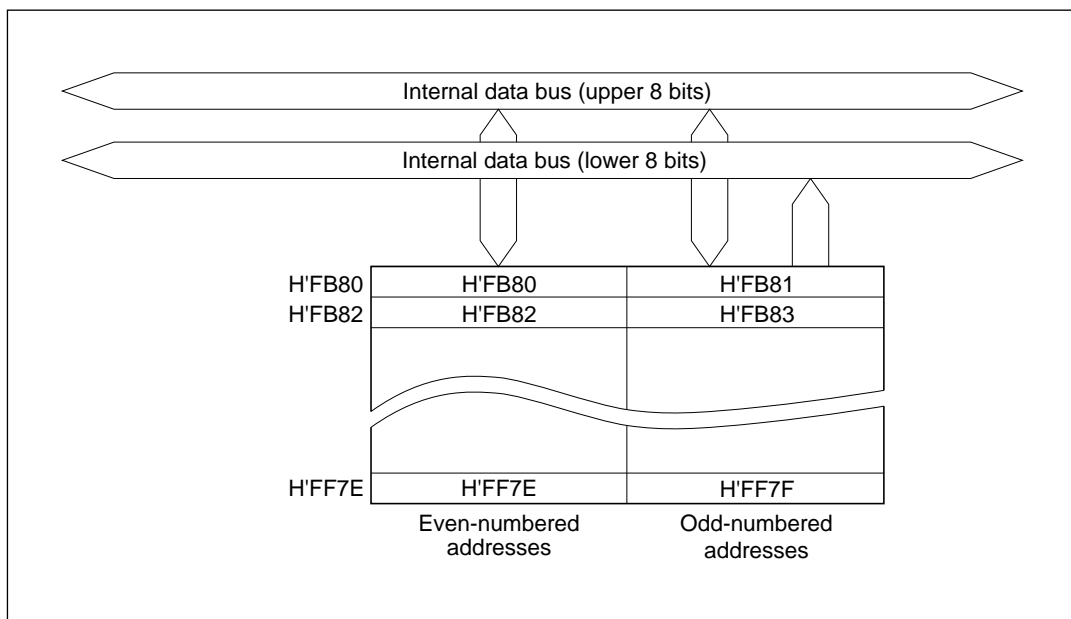


Figure 11-1 RAM Block Diagram (H8/3614)

Section 12 ROM

12.1 Overview

The H8/3612 has 16 kbytes of on-chip mask ROM. The H8/3613 has 24 kbytes. The H8/3614 has 32 kbytes. The ROM is connected to the CPU by a 16-bit data bus, allowing high-speed two-state access for both byte data and word data. ZTAT™ versions of the H8/3614 have 32 kbytes of PROM.

12.1.1 Block Diagram

Figure 12-1 shows a block diagram of the on-chip ROM.

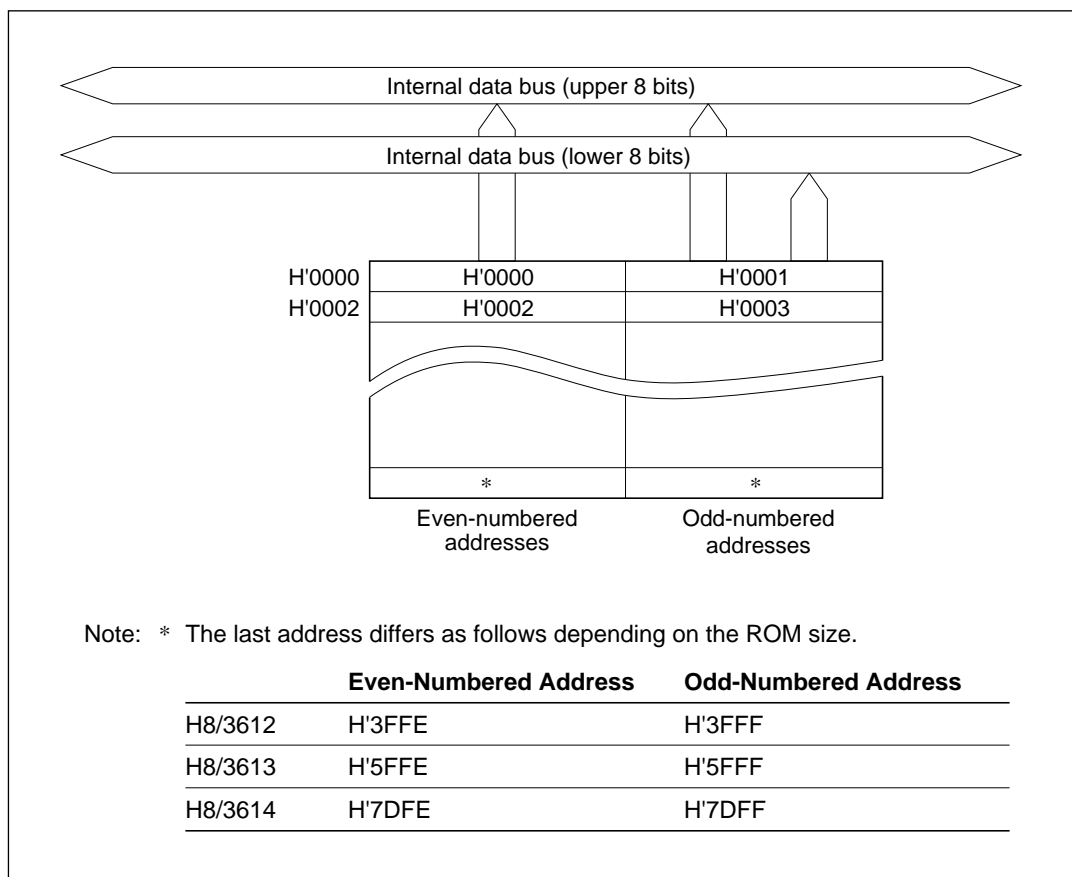


Figure 12-1 ROM Block Diagram

12.2 PROM Mode

12.2.1 Setting to PROM Mode

If the on-chip ROM is PROM, setting the chip to PROM mode stops operations as a microcontroller and allows the PROM to be programmed in the same way as the HN27C256H. Table 12-1 shows how to select PROM mode.

Table 12-1 Selection of PROM Mode

Pin Name	Abbrev.	Setting
Test pin	TEST	High level
Mode pin	MD ₀ (P4 ₀)	Low level
Mode pin	MD ₁ (P4 ₁)	
Mode pin	MD ₂ (P1 ₇)	High level

12.2.2 Socket Adapter Pin Arrangement and Memory Map

A standard PROM programmer can be used to program the PROM. A socket adapter is required for conversion to 28 pins, as listed in table 12-2.

Figure 12-2 shows the pin-to-pin wiring of the socket adapter. Figure 12-3 shows a memory map.

Table 12-2 Socket Adapter

Package	Socket Adapter
64-pin QFP (FP-64A)	HS3614ESH01H
64-pin SDIP (DP-64S)	HS3614ESS01H

H8/3614			EPROM Socket	
FP-64A	DP-64S	Pin	Pin	HN27C256H
10	18	RES	V _{PP}	1
42	50	P9 ₀	EO ₀	11
43	51	P9 ₁	EO ₁	12
44	52	P9 ₂	EO ₂	13
45	53	P9 ₃	EO ₃	15
46	54	P9 ₄	EO ₄	16
47	55	P9 ₅	EO ₅	17
48	56	P9 ₆	EO ₆	18
49	57	P9 ₇	EO ₇	19
26	34	P2 ₀	EA ₀	10
25	33	P2 ₁	EA ₁	9
24	32	P2 ₂	EA ₂	8
23	31	P2 ₃	EA ₃	7
22	30	P2 ₄	EA ₄	6
21	29	P2 ₅	EA ₅	5
20	28	P2 ₆	EA ₆	4
19	27	P2 ₇	EA ₇	3
50	58	PA ₀	EA ₈	25
17	25	P1 ₆	EA ₉	24
52	60	PA ₂	EA ₁₀	21
53	61	PA ₃	EA ₁₁	23
54	62	PA ₄	EA ₁₂	2
55	63	PA ₅	EA ₁₃	26
56	64	PA ₆	EA ₁₄	27
57	1	PA ₇	CEN	20
51	59	PA ₁	OEN	22
29	37	P4 ₃	V _{CC}	28
30	38	P4 ₂	V _{CC}	28
18	26	P1 ₇	V _{CC}	28
31	39	P4 ₁	V _{SS}	14
32	40	P4 ₀	V _{SS}	14
33, 58	41, 2	V _{CC} , AV _{CC}	V _{CC}	28
7, 3	15, 11	V _{SS} , AV _{SS}	V _{SS}	14
4, 6	12, 14	TEST, X1	V _{CC}	28
8	16	OSC1	V _{SS}	14

Note: Pins not indicated above should be left open.

Figure 12-2 Socket Adapter Pin Correspondence

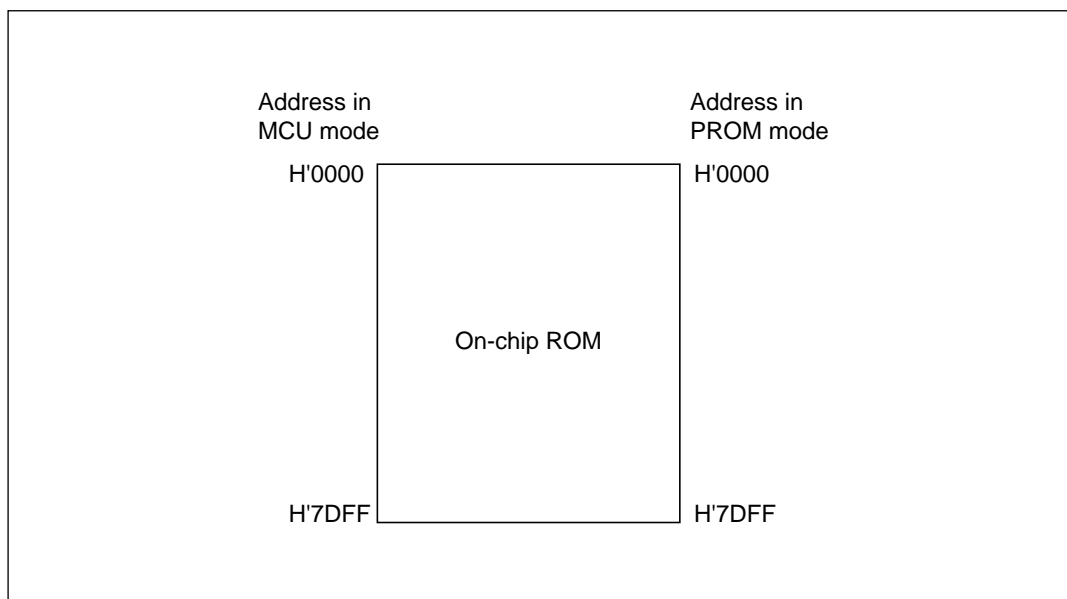


Figure 12-3 Memory Map in PROM Mode

12.3 Programming

The write, verify, and other sub-modes of PROM mode are selected as shown in table 12-3.

Table 12-3 Sub-Mode Selection in PROM Mode

Mode	Pin					
	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{CC}	EO_7 to EO_0	EA_{14} to EA_0
Write	L	H	V_{PP}	V_{CC}	Data input	Address input
Verify	H	L	V_{PP}	V_{CC}	Data output	Address input
Programming disabled	H	H	V_{PP}	V_{CC}	High impedance	Address input

Notation:

L: Low level

H: High level

V_{PP} : V_{PP} level

V_{CC} : V_{CC} level

The specifications for writing and reading the on-chip PROM are identical to those for the standard HN27C256H EPROM.

12.3.1 Writing and Verifying

An efficient, high-speed programming method is provided for writing and verifying the PROM data. This method achieves high speed without voltage stress on the device and without lowering the reliability of written data. H'FF data is written in unused address areas.

The basic flow of this high-speed programming method is shown in figure 12-4. Table 12-4 and table 12-5 give the electrical characteristics in programming mode. Figure 12-5 shows a write/verify timing diagram.

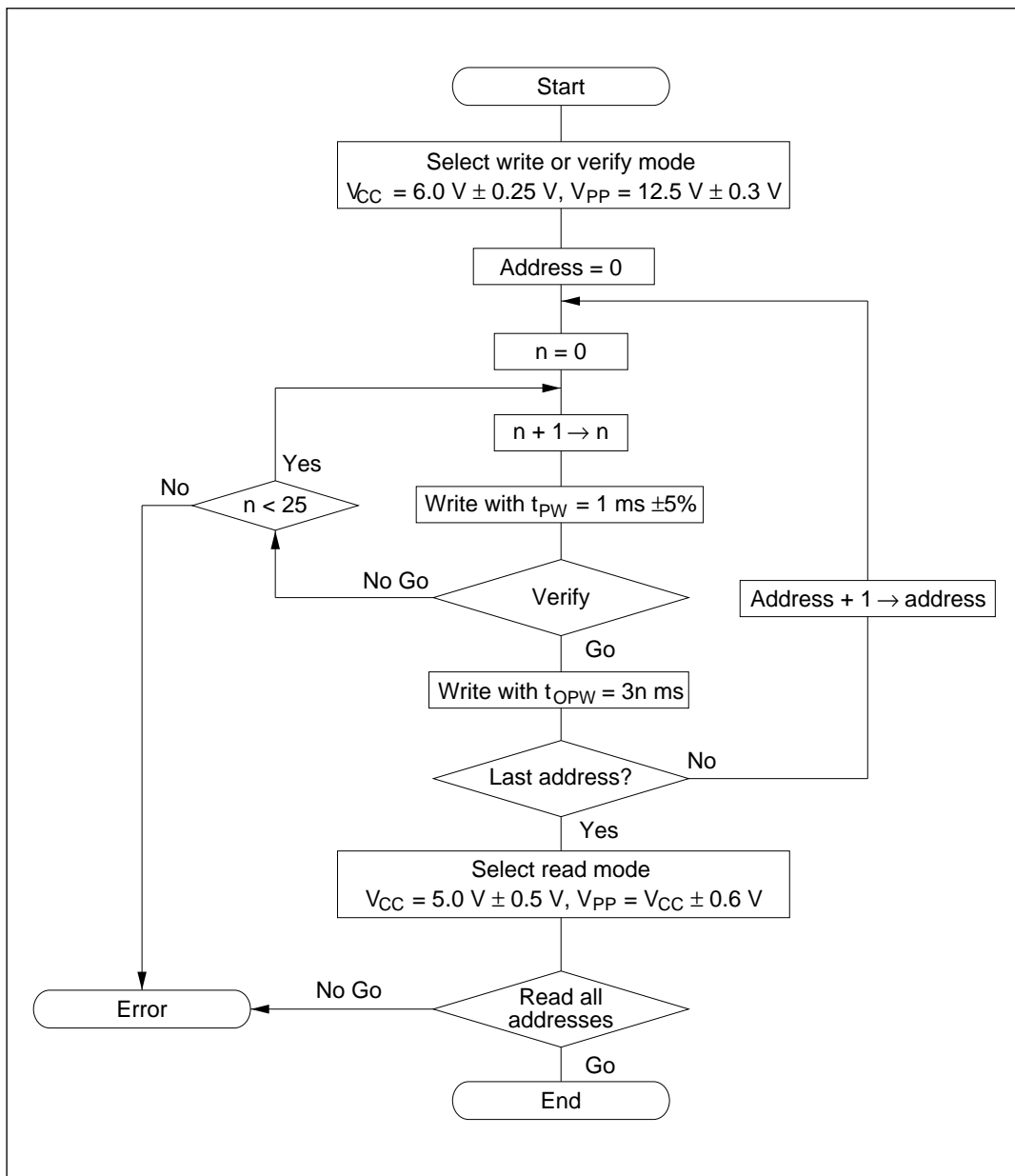


Figure 12-4 High-Speed Programming Flowchart

Table 12-4 DC Characteristics(Conditions: $V_{CC} = 6.0 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input high-level voltage	\overline{EA}_{14} to EA_0 , EO_7 to EO_0 , \overline{OE} , \overline{CE}	V_{IH}	2.4	—	$V_{CC} + 0.3 \text{ V}$		
Input low-level voltage	\overline{EA}_{14} to EA_0 , EO_7 to EO_0 , \overline{OE} , \overline{CE}	V_{IL}	-0.3	—	0.8	V	
Output high-level voltage	EO_7 to EO_0	V_{OH}	2.4	—	—	V	$I_{OH} = -200 \mu\text{A}$
Output low-level voltage	EO_7 to EO_0	V_{OL}	—	—	0.45	V	$I_{OL} = 1.6 \text{ mA}$
Input leakage current	EO_7 to EO_0 , \overline{EA}_{14} to EA_0 , \overline{OE} , \overline{CE}	$ I_{LI} $	—	—	2	μA	$V_{IN} = 5.25 \text{ V}/0.5 \text{ V}$
V_{CC} current		I_{CC}	—	—	40	mA	
V_{PP} current		I_{PP}	—	—	40	mA	

Table 12-5 AC Characteristics(Conditions: $V_{CC} = 6.0 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	μs	Figure 12-5*
\overline{OE} setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
Data output disable time	t_{DF}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
Programming pulse width	t_{PW}	0.95	1.0	1.05	ms	
\overline{CE} pulse width for overwrite programming	t_{OPW}	2.85	—	78.75	ms	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
Data output delay time	t_{OE}	0	—	500	ns	

Notes: * Input pulse level: 0.8 to 2.2 V
Input rise time/fall time $\leq 20 \text{ ns}$
Timing reference levels Input: 1.0 V, 2.0 V
Output: 0.8 V, 2.0 V

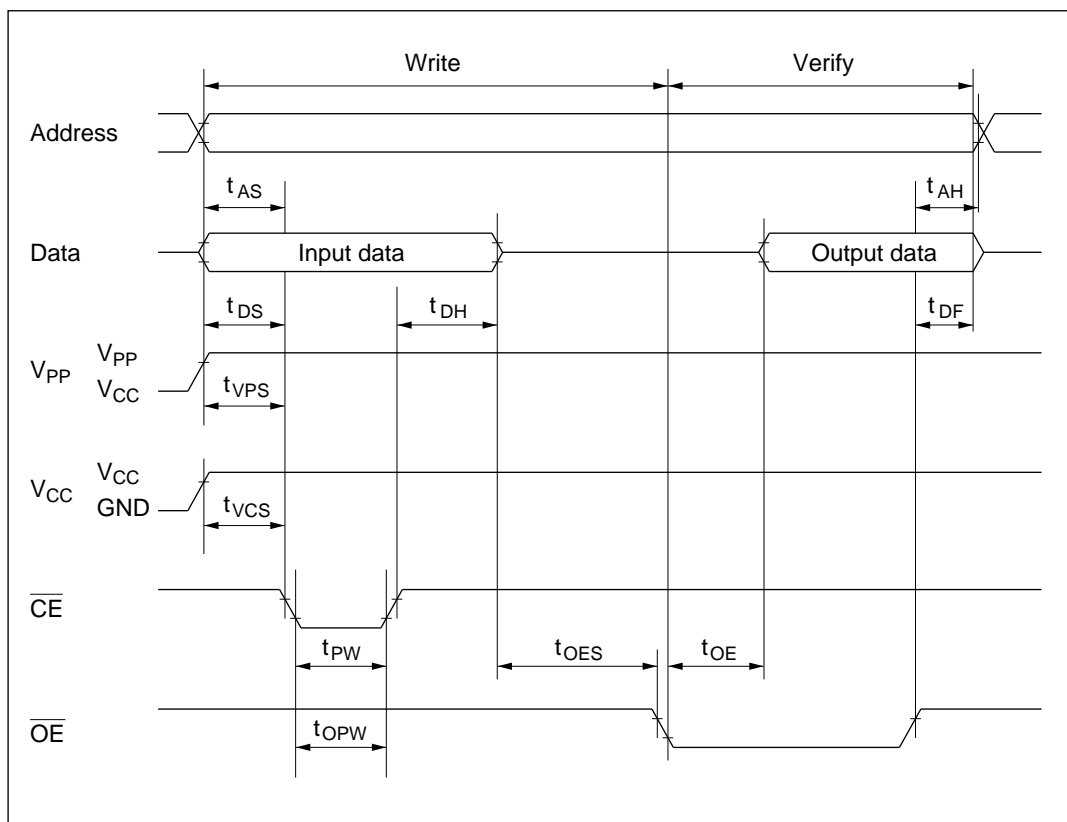


Figure 12-5 PROM Write/Verify Timing

12.3.2 Precautions When Writing

1. Use the specified programming voltage and timing.

The programming voltage in PROM mode (V_{PP}) is 12.5 V. Use of a higher voltage can permanently damage the chip. Be especially careful with respect to PROM programmer overshoot.

Setting the PROM programmer to Hitachi specifications for the HN27C256H or to Intel specifications will result in a correct V_{PP} of 12.5 V.

2. Make sure the index marks on the PROM programmer socket, socket adapter, and chip are properly aligned. If they are not, the chip may be destroyed by excessive current flow. Before programming, be sure the chip is properly mounted in the PROM programmer.
3. Avoid touching the socket adapter or chip during programming, since this may cause contact faults and write errors.

12.3.3 Reliability of Written Data

An effective way to assure the data holding characteristics of the programmed chips is to bake them at 150°C, then screen them for data errors. This procedure quickly eliminates chips with PROM memory cells prone to early data retention failure.

Figure 12-6 shows a flowchart of this screening procedure.

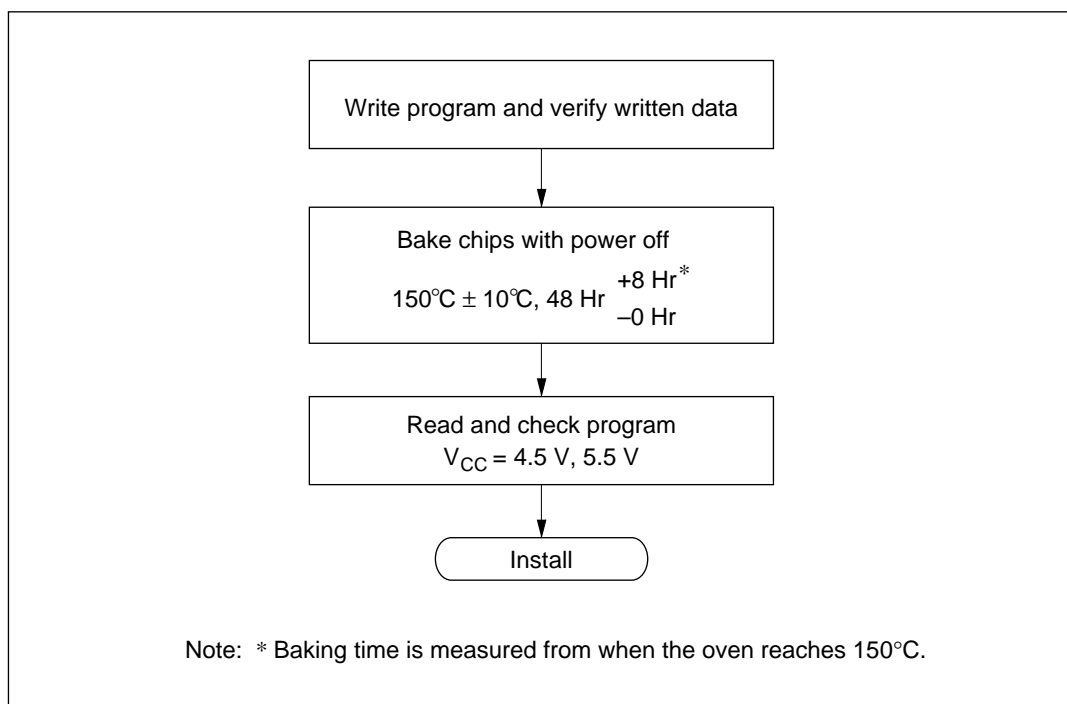


Figure 12-6 Recommended Screening Procedure

If write errors occur repeatedly while the same PROM programmer is being used, stop programming and check for problems in the PROM programmer and socket adapter, etc.

Please notify your Hitachi representative of any problems occurring during programming or in screening after high-temperature baking.

Section 13 Electrical Specifications

13.1 Absolute Maximum Ratings

Table 13-1 gives the absolute maximum ratings for the H8/3614 Series.

Table 13-1 Absolute Maximum Ratings (Provisional Values)

Item	Symbol	Rating	Unit	Notes
Supply voltage	V_{CC}	−0.3 to +7.0	V	1, 2
Programming voltage	V_{PP}	−0.3 to +14.0	V	1, 2, 3
Analog supply voltage	AV_{CC}	−0.3 to +7.0	V	1, 2
Analog input voltage	AV_{IN}	−0.3 to $AV_{CC} + 0.3$	V	1, 2
Pin voltage	V_T	−0.3 to $V_{CC} + 0.3$	V	1, 2
Operating temperature	T_{op}	−20 to +75	°C	1, 2
Storage temperature	T_{stg}	−55 to +125	°C	1, 2

Notes: 1. Operation in excess of these absolute maximum ratings may result in permanent damage to the LSI. Normally the LSI should be operated within the conditions given under electrical characteristics on the following pages, so as to avoid malfunction and assure maximum reliability.

2. All voltages are based on V_{SS} as a reference voltage.

3. Applies to the ZTAT™ version.

13.2 HD6473614 Electrical Characteristics

13.2.1 HD6473614 DC Characteristics

Table 13-2 gives the allowable current values of the HD6473614. Table 13-3 gives the DC characteristics.

Table 13-2 Allowable Output Current Values

Conditions: $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^{\circ}\text{C}$

Item	Symbol	Rating	Unit	Notes
Allowable input current (into LSI)	I_O	2	mA	1, 2
Allowable output current (from LSI)	$-I_O$	2	mA	2, 3
Allowable output current (from LSI)	$-I_O$	20	mA	3, 4
Total allowable input current (into LSI)	ΣI_O	50	mA	5
Total allowable output current (from LSI)	$-\Sigma I_O$	150	mA	6

Notes: 1. Allowable input current means the maximum current that can flow from each I/O pin to V_{SS} .
2. Applies to standard pins.
3. Allowable output current means the maximum current that can flow from V_{CC} to each I/O pin.
4. Applies to PMOS open-drain pins.
5. Total allowable input current means the sum of current that can flow at one time from all I/O pins to V_{SS} .
6. Total allowable output current means the sum of current that can flow from V_{CC} to all I/O pins.

Table 13-3 DC Characteristics

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Input high voltage	V_{IH}	\overline{RES}		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
		$\overline{IRQ_0}$ to $\overline{IRQ_5}$						
		SCK_1 , SCK_2	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	$0.9 V_{CC}$	—	$V_{CC} + 0.3$		
		SI_1 , SI_2						
		\overline{EVENT} , UD	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
		OSC_1		$V_{CC} - 0.5$	—	$V_{CC} + 0.3$	V	
			$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$		
		$P0_0$ to $P0_7$ $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_7	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
		$P4_0$ to $P4_5$	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	\overline{RES}		-0.3	—	$0.2 V_{CC}$	V	
		SCK_1 , SCK_2						
		$\overline{IRQ_0}$ to $\overline{IRQ_5}$	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	-0.3	—	$0.1 V_{CC}$		
		SI_1 , SI_2						
		\overline{EVENT} , UD	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	
		OSC_1		-0.3	—	0.5	V	
			$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	-0.3	—	0.3		
		$P0_1$ to $P0_7$ $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_7	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	
		$P4_0$ to $P4_5$	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	

Note: Connect the TEST pin to V_{SS} .

Table 13-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Output high voltage	V_{OH}	P1 ₀ to P1 ₅ P2 ₀ to P2 ₇ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PWM SO1, SO ₂ SCK ₁ , SCK ₂ PA ₀ to PA ₇	$-I_{OH} = 1.0$ mA	$V_{CC} - 1.0$	—	—	V	
			$-I_{OH} = 0.5$ mA	$V_{CC} - 0.5$	—	—		
			$V_{CC} = 2.7$ to 5.5 V $-I_{OH} = 0.3$ mA	$V_{CC} - 0.5$	—	—		
		P4 ₀ to P4 ₅	$-I_{OH} = 15$ mA	$V_{CC} - 3.0$	—	—	V	
			$-I_{OH} = 10$ mA	$V_{CC} - 2.0$	—	—		
			$-I_{OH} = 4$ mA	$V_{CC} - 1.0$	—	—		
Output low voltage	V_{OL}	P1 ₀ to P1 ₅ P2 ₀ to P2 ₇ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PWM SO ₁ , SO ₂ SCK ₁ , SCK ₂ PA ₀ to PA ₇	$V_{CC} = 4.0$ to 5.5 V $I_{OL} = 1.6$ mA	—	—	0.4	V	
			$V_{CC} = 2.7$ to 5.5 V $I_{OL} = 0.5$ mA	—	0.4	—	V	Reference value
Input leakage current	$ I_{IL} $	\overline{RES}	$V_{IN} = 0$ to V_{CC}			40	μA	

Table 13-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
I/O leakage current	$ I_{IL} $	TEST SCK ₁ , SCK ₂ SI ₁ , SI ₂ IRQ ₀ to IRQ ₅ EVENT, UD OSC ₁ P0 ₀ to P0 ₇ P1 ₀ to P1 ₆ P2 ₀ to P2 ₇ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PA ₀ to PA ₇	$V_{IN} = 0$ to V_{CC}	—	—	1	μA	
		P4 ₀ to P4 ₅ P1 ₇	$V_{IN} = 0.0$ to V_{CC}	—	—	2	μA	
Input capacitance	C_{IN}	Input pins and I/O pins other than power source pin	$f = 1$ MHz, $V_{IN} = 0$ V $T_a = 25^\circ\text{C}$	—	—	20	pF	
		P1 ₆ /EVENT		—	—	35		
		RES		—	—	70		

Table 13-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Current dissipation when CPU operating in active mode	I_{OPE}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	17	—	mA	Reference value 1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	9	—		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	6	—		
Current dissipation during reset in active mode	I_{RES}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	6	9	mA	1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	3	5		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	1.5	—		
Current dissipation in sleep mode	I_{SLEEP}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	2.5	3.5	mA	1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	1.5	2.0		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	1.0	—		
Current dissipation in subactive mode	I_{SUB}	V_{CC}	$V_{CC} = 2.7$ V 32 kHz crystal oscillator used	—	6	20	μA	
				—	11	—	μA	2
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	16	—	μA	Reference value
				—	22	—	μA	2
Current dissipation in watch mode	I_{WATCH}	V_{CC}	$V_{CC} = 2.7$ V 32 kHz crystal oscillator used	—	3.2	6	μA	
				—	3.8	—	μA	2
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	10	—	μA	Reference value
				—	12	—	μA	2
Current dissipation in standby mode	I_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	—	—	10	μA	

Table 13-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
RAM data retention voltage in standby mode	V_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	2	—	—	V	

Notes: 1. Does not include current flowing to output buffer.
 2. Reference value when 47 μF bypass capacitor is connected between V_{CC} and V_{SS} .

13.2.2 HD6473614 AC Characteristics

Table 13-4 gives the control signal timing of the HD6473614. Table 13-5 gives the serial interface timing.

Table 13-4 Control Signal Timing

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Clock pulse generator frequency	f_{OSC}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	2	—	8.4	MHz	
				2	—	4.2		
Clock cycle time	t_{CYC}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	119	—	500	ns	Figure 13-1
				238	—	500		
Instruction cycle time	ϕ		$V_{CC} = 2.7$ to 5.5 V	238	—	1000	ns	
				476	—	1000		
Subclock pulse generator frequency	f_x	X ₁ , X ₂	$V_{CC} = 2.7$ to 5.5 V	—	32.768	—	kHz	
Subclock cycle time	t_{subcyc}	X ₁ , X ₂	$V_{CC} = 2.7$ to 5.5 V	—	30.5	—	μs	
Subactive instruction cycle time	ϕ_{SUB}		$V_{CC} = 2.7$ to 5.5 V	—	244.14	—	μs	
Oscillator settling time (crystal oscillator)	t_{rc}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	40	ms	
				—	—	60		
Oscillator settling time (ceramic oscillator)	t_{rc}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ms	
				—	—	40		
Oscillator settling time	t_{rc}	X ₁ , X ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	2	s	
External clock pulse width (high)	t_{CPH}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	40	—	—	ns	Figure 13-1
				100	—	—		
External clock pulse width (low)	t_{CPL}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	40	—	—	ns	
				100	—	—		
External clock rise time	t_{CPr}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ns	
				—	—	20		
External clock fall time	t_{CPf}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ns	
				—	—	20		

Table 13-4 Control Signal Timing (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
RES pin pulse width (low)	t_{REL}	RES	$V_{CC} = 2.7$ to 5.5 V	10	—	—	\emptyset	Figure 13-2
\overline{IRQ} pin pulse width (high)	t_{IH}	\overline{IRQ}_0 to \overline{IRQ}_5	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset \emptyset_{SUB}	Figure 13-3
\overline{IRQ} pin pulse width (low)	t_{IL}	\overline{IRQ}_0 to \overline{IRQ}_5	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset \emptyset_{SUB}	
EVENT pin pulse width (high)	t_{EVH}	EVENT	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	Figure 13-4
EVENT pin pulse width (low)	t_{EVL}	EVENT	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	
UD pin minimum change width	t_{UDH} t_{UDL}	UD	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	Figure 13-5

Table 13-5 Serial Interface Timing

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Output transfer clock cycle time	t_{scyc}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	Figure 13-6
Output transfer clock pulse width (high)	t_{SCKH}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	
Output transfer clock pulse width (low)	t_{SCKL}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	
Output transfer clock rise time	t_{SCKr}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Output transfer clock fall time	t_{SCKf}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Input transfer clock cycle time	t_{scyc}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	1	—	—	\emptyset	
Input transfer clock pulse width (high)	t_{SCKH}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	

Table 13-5 Serial Interface Timing (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Input transfer clock pulse width (low)	t_{SCKL}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	Figure 13-6
Input transfer clock rise time	t_{SCKr}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Input transfer clock fall time	t_{SCKf}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Serial output data delay time	t_{dSO}	SO ₁ , SO ₂		—	—	200	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	350		
Serial input data setup time	t_{sSI}	SI ₁ , SI ₂		230	—	—	ns	
			$V_{CC} = 2.7$ to 5.5 V	470	—	—		
Serial input data hold time	t_{hSI}	SI ₁ , SI ₂		230	—	—	ns	
			$V_{CC} = 2.7$ to 5.5 V	470	—	—		
Transfer hold time	t_{SCK2}	SCK ₂	When pin SCK ₂ is input pin	0.2	—	40	μs	Figure 13-7
			When pin SCK ₂ is input pin $V_{CC} = 2.7$ to 5.5 V	0.4	—	40		
			When pin SCK ₂ is output pin $V_{CC} = 2.7$ to 5.5 V	—	—	1	t_{scyc}	
Transfer end acknowledge time	t_{CS}	\overline{CS}	$V_{CC} = 2.7$ to 5.5 V	3	—	4	\emptyset	

13.2.3 HD6473614 A/D Converter Characteristics

Table 13-6 gives the HD6473614 A/D converter characteristics.

Table 13-6 A/D Converter Characteristics

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Analog supply voltage	AV_{CC}	AV_{CC}		$V_{CC} - 0.3$	V_{CC}	$V_{CC} + 0.3$	V	
Analog input voltage	AV_{IN}	AN_0 to AN_7		AV_{SS}	—	AV_{CC}	V	
Analog current	AI_{CC}	AV_{CC}	$AV_{CC} = 5$ V	—	—	200	μA	
	AI_{STOP}		Reset and power-down mode	—	—	10	μA	
Analog input capacitance	C_{AIN}	AN_0 to AN_7		—	—	30	pF	
Allowable signal source impedance	R_{AIN}	AN_0 to AN_7		—	—	10	$\text{k}\Omega$	
Resolution				—	—	8	Bit	
Absolute precision			$V_{CC} = AV_{CC} = 5$ V	—	—	± 2.5	LSB	
			$V_{CC} = AV_{CC} = 4.0$ to 5.5 V	—	± 2.5	—		Reference value
Conversion time				31	15.5	14.8	μs	

13.3 HD6433613 and HD6433614 Electrical Characteristics

13.3.1 HD6433613 and HD6433614 DC Characteristics

Table 13-7 gives the allowable current values of the HD6433613 and HD6433614. Table 13-8 gives the DC characteristics.

Table 13-7 Allowable Output Current Values

Conditions: $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^{\circ}\text{C}$

Item	Symbol	Rating	Unit	Notes
Allowable input current (into LSI)	I_O	2	mA	1, 2
Allowable output current (from LSI)	$-I_O$	2	mA	2, 3
Allowable output current (from LSI)	$-I_O$	20	mA	3, 4
Total allowable input current (into LSI)	ΣI_O	50	mA	5
Total allowable output current (from LSI)	$-\Sigma I_O$	150	mA	6

Notes: 1. Allowable input current means the maximum current that can flow from each I/O pin to V_{SS} .
2. Applies to standard pins.
3. Allowable output current means the maximum current that can flow from V_{CC} to each I/O pin.
4. Applies to PMOS open-drain pins.
5. Total allowable input current means the sum of current that can flow at one time from all I/O pins to V_{SS} .
6. Total allowable output current means the sum of current that can flow from V_{CC} to all I/O pins.

Table 13-8 DC Characteristics

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Input high voltage	V_{IH}	\overline{RES}		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
		$\overline{IRQ_0}$ to $\overline{IRQ_5}$						
		SCK_1 , SCK_2	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.9 V_{CC}$	—	$V_{CC} + 0.3$		
		SI_1 , SI_2						
		\overline{EVENT} , \overline{UD}	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
		OSC_1		$V_{CC} - 0.5$	—	$V_{CC} + 0.3$	V	
			$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$		
		$P0_0$ to $P0_7$ $P1_0$ to $P1_6$ $P2_0$ to $P2_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_7	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
		$P4_0$ to $P4_5$ $P1_7$	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	\overline{RES}		-0.3	—	$0.2 V_{CC}$	V	
		SCK_1 , SCK_2						
		$\overline{IRQ_0}$ to $\overline{IRQ_5}$	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.1 V_{CC}$		
		SI_1 , SI_2						
		\overline{EVENT} , \overline{UD}	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	
		OSC_1		-0.3	—	0.5	V	
			$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	0.3		
		$P0_0$ to $P0_7$ $P1_0$ to $P1_6$ $P2_0$ to $P2_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_7	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	
		$P4_0$ to $P4_5$ $P1_7$	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	

Note: Connect the TEST pin to V_{SS} .

Table 13-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Output high voltage	V_{OH}	P1 ₀ to P1 ₅ P2 ₀ to P2 ₇	$-I_{OH} = 1.0$ mA	$V_{CC} - 1.0$	—	—	V	
		P8 ₀ to P8 ₇ P9 ₀ to P9 ₇	$-I_{OH} = 0.5$ mA	$V_{CC} - 0.5$	—	—		
		PWM SO ₁ , SO ₂ PA ₀ to PA ₇	$V_{CC} = 2.7$ to 5.5 V $-I_{OH} = 0.3$ mA	$V_{CC} - 0.5$	—	—		
		P4 ₀ to P4 ₅	$-I_{OH} = 15$ mA	$V_{CC} - 3.0$	—	—	V	
			$-I_{OH} = 10$ mA	$V_{CC} - 2.0$	—	—		
			$-I_{OH} = 4$ mA	$V_{CC} - 1.0$	—	—		
Output low voltage	V_{OL}	P1 ₀ to P1 ₅ P2 ₀ to P2 ₇ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PWM SO ₁ , SO ₂ PA ₀ to PA ₇	$V_{CC} = 4.0$ to 5.5 V $I_{OL} = 1.6$ mA	—	—	0.4	V	
			$V_{CC} = 2.7$ to 5.5 V $I_{OL} = 0.5$ mA	—	0.4	—	V	Reference value
Input leakage current	$ I_{IL} $	\overline{RES}	Mask ROM version: $V_{IN} = 0$ to V_{CC}	—	—	1	μA	

Table 13-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
I/O leakage current	$ I_{IL} $	TEST SCK ₁ , SCK ₂ SI ₁ , SI ₂ IRQ ₀ to IRQ ₅ EVENT, UD OSC ₁ P0 ₀ to P0 ₇ P1 ₀ to P1 ₆ P2 ₀ to P2 ₇ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PA ₀ to PA ₇	$V_{IN} = 0$ to V_{CC}	—	—	1	μA	
		P4 ₀ to P4 ₇ P1 ₇	$V_{IN} = 0$ to V_{CC}	—	—	2	μA	
Pull-up MOS current	$-I_p$	P1 ₀ to P1 ₆ P2 ₀ to P2 ₇	$V_{CC} = 5$ V, $V_{IN} = 0$ V	50	—	300	μA	Reference value
		P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PA ₀ to PA ₇	$V_{CC} = 2.7$ V, $V_{IN} = 0$ V	—	25	—		
Input capacitance	C_{IN}	Input pins other than power source pin	$f = 1$ MHz, $V_{IN} = 0$ V $T_a = 25^\circ\text{C}$	—	—	15	pF	
		P1 ₇		—	—	30		

Table 13-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Current dissipation when CPU operating in active mode	I_{OPE}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	15	—	mA	Reference value 1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	8	—		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	5	—		
Current dissipation during reset in active mode	I_{RES}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	5	8	mA	1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	2.5	4		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	1.3	—		
Current dissipation in sleep mode	I_{SLEEP}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	2	3	mA	1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	1	1.5		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	0.6	—		
Current dissipation in subactive mode	I_{SUB}	V_{CC}	$V_{CC} = 2.5$ V 32 kHz crystal oscillator used	—	5	20	μA	
				—	9	—	μA	2
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	13	—	μA	Reference value
				—	20	—	μA	2
Current dissipation in watch mode	I_{WATCH}	V_{CC}	$V_{CC} = 2.5$ V 32 kHz crystal oscillator used	—	2.2	5	μA	
				—	2.8	—	μA	2
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	6	—	μA	Reference value
				—	8	—	μA	2
Current dissipation in standby mode	I_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	—	—	5	μA	

Table 13-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^{\circ}\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
RAM data retention voltage in standby mode	V_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	2	—	—	V	

Notes: 1. Does not include current flowing to pull-up MOS or output buffer.
 2. Reference value when 47 μF bypass capacitor is connected between V_{CC} and V_{SS} .

13.3.2 HD6433613 and HD6433614 AC Characteristics

Table 13-9 gives the control signal timing of the HD6433613 and HD6433614. Table 13-10 gives the serial interface timing.

Table 13-9 Control Signal Timing

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Clock pulse generator frequency	f_{OSC}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	2	—	8.4	MHz	
				2	—	4.2		
Clock cycle time	t_{CYC}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	119	—	500	ns	Figure 13-1
				238	—	500		
Instruction cycle time	\varnothing		$V_{CC} = 2.7$ to 5.5 V	238	—	1000	ns	
				476	—	1000		
Subclock pulse generator frequency	f_x	X ₁ , X ₂	$V_{CC} = 2.5$ to 5.5 V	—	32.768	—	kHz	
Subclock cycle time	t_{subcyc}	X ₁ , X ₂	$V_{CC} = 2.5$ to 5.5 V	—	30.5	—	μs	
Subactive instruction cycle time	\varnothing_{SUB}		$V_{CC} = 2.5$ to 5.5 V	—	244.14	—	μs	
Oscillator setting time (crystal oscillator)	t_{rc}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	40	ms	
				—	—	60		
Oscillator setting time (ceramic oscillator)	t_{rc}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ms	
				—	—	40		
Oscillator settling time	t_{rc}	X ₁ , X ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	2	s	
External clock pulse width (high)	t_{CPH}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	40	—	—	ns	Figure 13-1
				100	—	—		
External clock pulse width (low)	t_{CPL}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	40	—	—	ns	
				100	—	—		
External clock rise time	t_{CPr}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ns	
				—	—	20		
External clock fall time	t_{CPf}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ns	
				—	—	20		

Table 13-9 Control Signal Timing (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
$\overline{\text{RES}}$ pin pulse width (low)	t_{REL}	$\overline{\text{RES}}$	$V_{CC} = 2.7$ to 5.5 V	10	—	—	\emptyset	Figure 13-2
$\overline{\text{IRQ}}$ pin pulse width (high)	t_{IH}	$\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_5$	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset \emptyset_{SUB}	Figure 13-3
$\overline{\text{IRQ}}$ pin pulse width (low)	t_{IL}	$\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_5$	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset \emptyset_{SUB}	
EVENT pin pulse width (high)	t_{EVH}	$\overline{\text{EVENT}}$	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	Figure 13-4
EVENT pin pulse width (low)	t_{EVL}	$\overline{\text{EVENT}}$	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	
UD pin minimum change width	t_{UDH} t_{UDL}	UD	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	Figure 13-5

Table 13-10 Serial Interface Timing

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Output transfer clock cycle timing	t_{scyc}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	Figure 13-6
Output transfer clock pulse width (high)	t_{SCKH}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	
Output transfer clock pulse width (low)	t_{SCKL}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	
Output transfer clock rise time	t_{SCKr}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Output transfer clock fall time	t_{SCKf}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Input transfer clock cycle timing	t_{scyc}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	1	—	—	\emptyset	
Input transfer clock pulse width (high)	t_{SCKH}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	

Table 13-10 Serial Interface Timing (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Input transfer clock pulse width (low)	t_{SCKL}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	Figure 13-6
Input transfer clock rise time	t_{SCKr}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Input transfer clock fall time	t_{SCKf}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Serial output data delay time	t_{dSO}	SO ₁ , SO ₂		—	—	200	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	350		
Serial input data setup time	t_{sSI}	SI ₁ , SI ₂		230	—	—	ns	
			$V_{CC} = 2.7$ to 5.5 V	470	—	—		
Serial input data hold time	t_{hSI}	SI ₁ , SI ₂		230	—	—	ns	
			$V_{CC} = 2.7$ to 5.5 V	470	—	—		
Transfer hold time	t_{SCK2}	SCK ₂	When pin SCK ₂ is input pin	0.2	—	40	μs	Figure 13-7
			When pin SCK ₂ is input pin $V_{CC} = 2.7$ to 5.5 V	0.4	—	40		
			When pin SCK ₂ is output pin $V_{CC} = 2.7$ to 5.5 V	—	—	1	t_{scyc}	
Transfer end acknowledge time	t_{CS}	\overline{CS}	$V_{CC} = 2.7$ to 5.5 V	3	—	4	\emptyset	

13.3.3 HD6433613 and HD6433614 A/D Converter Characteristics

Table 13-11 gives the HD6433613 and HD6433614 A/D converter characteristics.

Table 13-11 A/D Converter Characteristics

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Analog supply voltage	AV_{CC}	AV_{CC}		$V_{CC} - 0.3$	V_{CC}	$V_{CC} + 0.3$	V	
Analog input voltage	AV_{IN}	AN_0 to AN_7		AV_{SS}	—	AV_{CC}	V	
Analog current	AI_{CC}	AV_{CC}	$AV_{CC} = 5$ V	—	—	200	μA	
	AI_{STOP}		Reset and power-down mode	—	—	10	μA	
Analog input capacitance	C_{AIN}	AN_0 to AN_7		—	—	30	pF	
Allowable signal source impedance	R_{AIN}	AN_0 to AN_7		—	—	10	$\text{k}\Omega$	
Resolution				—	—	8	Bit	
Absolute precision			$V_{CC} = AV_{CC} = 5$ V	—	—	± 2.5	LSB	
			$V_{CC} = AV_{CC} = 4.0$ to 5.5 V	—	± 2.5	—		Reference value
Conversion time				31	15.5	14.8	μS	

13.4 HD6433612 Electrical Characteristics

13.4.1 HD6433612 DC Characteristics

Table 13-12 gives the allowable output current values of the HD6433612. Table 13-13 gives the DC characteristics.

Table 13-12 Allowable Output Current Values

Conditions: $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Rating	Unit	Notes
Allowable input current (into LSI)	I_O	2	mA	1, 2
Allowable output current (from LSI)	$-I_O$	2	mA	2, 3
Allowable output current (from LSI)	$-I_O$	20	mA	3, 4
Total allowable input current (into LSI)	ΣI_O	50	mA	5
Total allowable output current (from LSI)	$-\Sigma I_O$	150	mA	6

Notes: 1. Allowable input current means the maximum current that can flow from each I/O pin to V_{SS} .
2. Applies to standard pins.
3. Allowable output current means the maximum current that can flow from V_{CC} to each I/O pin.
4. Applies to PMOS open-drain pins.
5. Total allowable input current means the sum of current that can flow at one time from all I/O pins to V_{SS} .
6. Total allowable output current means the sum of current that can flow from V_{CC} to all I/O pins.

Table 13-13 DC Characteristics

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Input high voltage	V_{IH}	\overline{RES}		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
		$\overline{IRQ_0}$ to $\overline{IRQ_5}$						
		SCK_1, SCK_2	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.9 V_{CC}$	—	$V_{CC} + 0.3$		
		SI_1, SI_2						
		\overline{EVENT}, UD	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
		OSC_1		$V_{CC} - 0.5$	—	$V_{CC} + 0.3$	V	
			$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$		
		$P0_0$ to $P0_7$ $P1_0$ to $P1_6$ $P2_0$ to $P2_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_7	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
		$P4_0$ to $P4_5$ $P1_7$	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	\overline{RES}		-0.3	—	$0.2 V_{CC}$	V	
		SCK_1, SCK_2						
		$\overline{IRQ_0}$ to $\overline{IRQ_5}$	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.1 V_{CC}$		
		SI_1, SI_2						
		\overline{EVENT}, UD	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	
		OSC_1		-0.3	—	0.5	V	
			$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	0.3		
		$P0_0$ to $P0_7$ $P1_0$ to $P1_6$ $P2_0$ to $P2_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_7	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	
		$P4_0$ to $P4_5$ $P1_7$	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	

Note: Connect the TEST pin to V_{SS} .

Table 13-13 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Output high voltage	V_{OH}	P1 ₀ to P1 ₅ P2 ₀ to P2 ₇	$-I_{OH} = 1.0$ mA	$V_{CC} - 1.0$	—	—	V	
		P8 ₀ to P8 ₇ P9 ₀ to P9 ₇	$-I_{OH} = 0.5$ mA	$V_{CC} - 0.5$	—	—		
		SO ₁ , SO ₂ SCK ₁ , SCK ₂ PA ₀ to PA ₇	$V_{CC} = 2.7$ to 5.5 V $-I_{OH} = 0.3$ mA	$V_{CC} - 0.5$	—	—		
		P4 ₀ to P4 ₅	$-I_{OH} = 15$ mA	$V_{CC} - 3.0$	—	—	V	
			$-I_{OH} = 10$ mA	$V_{CC} - 2.0$	—	—		
			$-I_{OH} = 4$ mA	$V_{CC} - 1.0$	—	—		
Output low voltage	V_{OL}	P1 ₀ to P1 ₅ P2 ₀ to P2 ₇ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇	$V_{CC} = 4.0$ to 5.5 V $I_{OL} = 1.6$ mA	—	—	0.4	V	
		SO ₁ , SO ₂ SCK ₁ , SCK ₂ PA ₀ to PA ₇	$V_{CC} = 2.7$ to 5.5 V $I_{OL} = 0.5$ mA	—	0.4	—	V	Reference value
Input leakage current	$ I_{IL} $	RES	Mask ROM version: $V_{IN} = 0$ to V_{CC}	—	—	1	μA	

Table 13-13 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
I/O leakage current	$ I_{IL} $	TEST SCK ₁ , SCK ₂ SI ₁ , SI ₂ IRQ ₀ to IRQ ₅ EVENT, UD OSC ₁ P0 ₀ to P0 ₇ P1 ₀ to P1 ₆ P2 ₀ to P2 ₇ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PA ₀ to PA ₇	$V_{IN} = 0.0$ to V_{CC}	—	—	1	μA	
		P4 ₀ to P4 ₅ P1 ₇	$V_{IN} = 0.0$ to V_{CC}	—	—	2	μA	
Pull-up MOS current	$-I_p$	P1 ₀ to P1 ₆ P2 ₀ to P2 ₇ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PA ₀ to PA ₇	$V_{CC} = 5$ V, $V_{IN} = 0$ V	50	—	300	μA	
			$V_{CC} = 2.7$ V, $V_{IN} = 0$ V	—	25	—		Reference value
Input capacitance	C_{IN}	Input pins and I/O pins other than power source pin	$f = 1$ MHz, $V_{IN} = 0$ V $T_a = 25^\circ\text{C}$	—	—	15	pF	
		P1 ₇		—	—	30		

Table 13-13 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Current dissipation when CPU operating in active mode	I_{OPE}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	15	—	mA	Reference value 1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	8	—		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	5	—		
Current dissipation during reset in active mode	I_{RES}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	5	8	mA	1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	2.5	4		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	1.3	—		
Current dissipation in sleep mode	I_{SLEEP}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	2	3	mA	1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	1	1.5		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	0.6	—		
Current dissipation in subactive mode	I_{SUB}	V_{CC}	$V_{CC} = 2.5$ V 32 kHz crystal oscillator used	—	5	20	μA	
				—	9	—	μA	2
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	13	—	μA	Reference value
				—	20	—	μA	2
Current dissipation in watch mode	I_{WATCH}	V_{CC}	$V_{CC} = 2.5$ V 32 kHz crystal oscillator used	—	2.2	5	μA	
				—	2.8	—	μA	2
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	6	—	μA	Reference value
				—	8	—	μA	2
Current dissipation in standby mode	I_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	—	—	5	μA	

Table 13-13 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^{\circ}\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
RAM data retention voltage in standby mode	V_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	2	—	—	V	

Notes: 1. Does not include current flowing to pull-up MOS or output buffer.
2. Reference value when 47 μF bypass capacitor is connected between V_{CC} and V_{SS} .

13.4.2 HD6433612 AC Characteristics

Table 13-14 gives the control signal timing of the HD6433612. Table 13-15 gives the serial interface timing.

Table 13-14 Control Signal Timing

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Clock pulse generator frequency	f_{OSC}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	2	—	8.4	MHz	
				2	—	4.2		
Clock cycle time	t_{CYC}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	119	—	500	ns	Figure 13-1
				238	—	500		
Instruction cycle time	ϕ		$V_{CC} = 2.7$ to 5.5 V	238	—	1000	ns	
				476	—	1000		
Subclock pulse generator frequency	f_x	X ₁ , X ₂	$V_{CC} = 2.5$ to 5.5 V	—	32.768	—	kHz	
Subclock cycle time	t_{subcyc}	X ₁ , X ₂	$V_{CC} = 2.5$ to 5.5 V	—	30.5	—	μs	
Subactive instruction cycle time	ϕ_{SUB}		$V_{CC} = 2.5$ to 5.5 V	—	244.14	—	μs	
Oscillator setting time (crystal oscillator)	t_{rc}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	40	ms	
				—	—	60		
Oscillator setting time (ceramic oscillator)	t_{rc}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ms	
				—	—	40		
Oscillator settling time	t_{rc}	X ₁ , X ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	2	s	
External clock pulse width (high)	t_{CPH}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	40	—	—	ns	Figure 13-1
				100	—	—		
External clock pulse width (low)	t_{CPL}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	40	—	—	ns	
				100	—	—		
External clock rise time	t_{CPr}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ns	
				—	—	20		
External clock fall time	t_{CPf}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ns	
				—	—	20		

Table 13-14 Control Signal Timing (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
$\overline{\text{RES}}$ pin pulse width (low)	t_{REL}	$\overline{\text{RES}}$	$V_{CC} = 2.7$ to 5.5 V	10	—	—	\emptyset	Figure 13-2
$\overline{\text{IRQ}}$ pin pulse width (high)	t_{IH}	$\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_5$	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset \emptyset_{SUB}	Figure 13-3
$\overline{\text{IRQ}}$ pin pulse width (low)	t_{IL}	$\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_5$	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset \emptyset_{SUB}	
EVENT pin pulse width (high)	t_{EVH}	EVENT	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	Figure 13-4
EVENT pin pulse width (low)	t_{EVL}	EVENT	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	
UD pin minimum change width	t_{UDH} t_{UDL}	UD	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	Figure 13-5

Table 13-15 Serial Interface Timing

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Output transfer clock cycle timing	t_{scyc}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	2	—	—	\emptyset	Figure 13-6
Output transfer clock pulse width (high)	t_{SCKH}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	
Output transfer clock pulse width (low)	t_{SCKL}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	
Output transfer clock rise time	t_{SCKr}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Output transfer clock fall time	t_{SCKf}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Input transfer clock cycle timing	t_{scyc}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	1	—	—	\emptyset	
Input transfer clock pulse width (high)	t_{SCKH}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	

Table 13-15 Serial Interface Timing (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Input transfer clock pulse width (low)	t_{SCKL}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	Figure 13-6
Input transfer clock rise time	t_{SCKr}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Input transfer clock fall time	t_{SCKf}	SCK ₁ , SCK ₂		—	—	60	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	80		
Serial output data delay time	t_{dSO}	SO ₁ , SO ₂		—	—	200	ns	
			$V_{CC} = 2.7$ to 5.5 V	—	—	350		
Serial input data setup time	t_{sSI}	SI ₁ , SI ₂		230	—	—	ns	
			$V_{CC} = 2.7$ to 5.5 V	470	—	—		
Serial input data hold time	t_{hSI}	SI ₁ , SI ₂		230	—	—	ns	
			$V_{CC} = 2.7$ to 5.5 V	470	—	—		
Transfer hold time	t_{SCK2}	SCK ₂	When pin SCK ₂ is input pin	0.2	—	40	μs	Figure 13-7
			When pin SCK ₂ is input pin $V_{CC} = 2.7$ to 5.5 V	0.4	—	40		
			When pin SCK ₂ is output pin $V_{CC} = 2.7$ to 5.5 V	—	—	1	t_{scyc}	
Transfer end acknowledge time	t_{CS}	\overline{CS}	$V_{CC} = 2.7$ to 5.5 V	3	—	4	ø	

13.4.3 HD6433612 A/D Converter Characteristics

Table 13-16 gives the HD6433612 A/D converter characteristics.

Table 13-16 A/D Converter Characteristics

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Analog supply voltage	AV_{CC}	AV_{CC}		$V_{CC} - 0.3$	V_{CC}	$V_{CC} + 0.3$	V	
Analog input voltage	AV_{IN}	AN_0 to AN_7		AV_{SS}	—	AV_{CC}	V	
Analog current	AI_{CC}	AV_{CC}	$AV_{CC} = 5$ V	—	—	200	μA	
	AI_{STOP}		Reset and power-down mode	—	—	10	μA	
Analog input capacitance	C_{AIN}	AN_0 to AN_7		—	—	30	pF	
Allowable signal source impedance	R_{AIN}	AN_0 to AN_7		—	—	10	$\text{k}\Omega$	
Resolution				—	—	8	Bit	
Absolute precision			$V_{CC} = AV_{CC} = 5$ V	—	—	± 2.5	LSB	
			$V_{CC} = AV_{CC} = 4.0$ to 5.5 V	—	± 2.5	—		Reference value
Conversion time				31	15.5	14.8	μS	

13.5 Operational Timing

This section provides the following timing diagrams (figures 13-1 to 13-8).

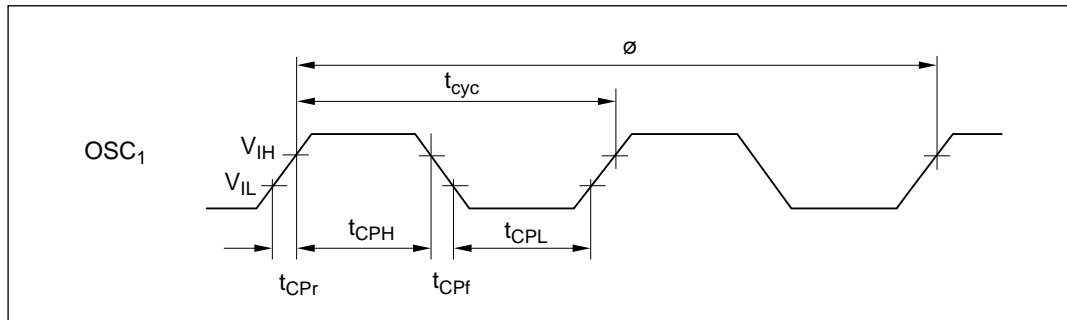


Figure 13-1 System Clock Input Timing

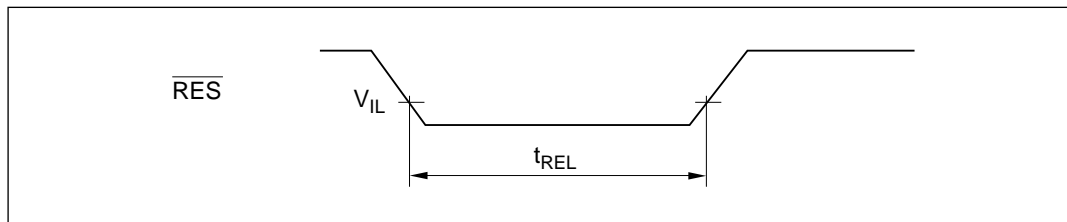


Figure 13-2 $\overline{\text{RES}}$ Pin Pulse Width (low)

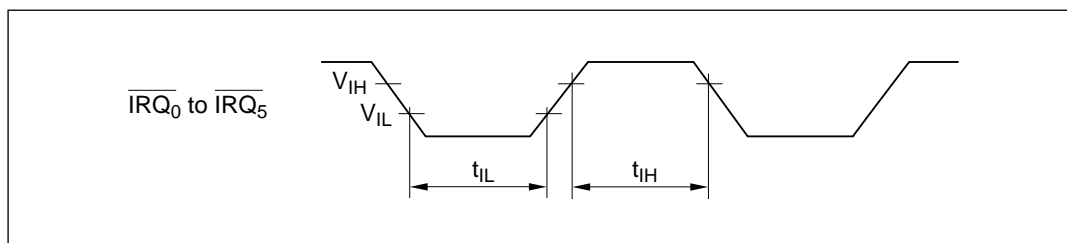


Figure 13-3 $\overline{\text{IRQ}}$ Pin Input Timing

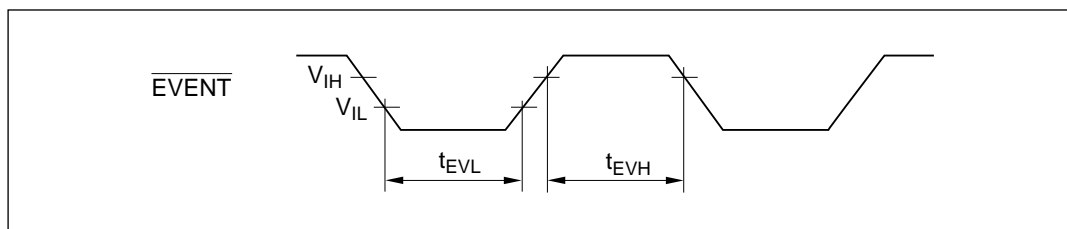


Figure 13-4 $\overline{\text{EVENT}}$ Pin Minimum Pulse Width

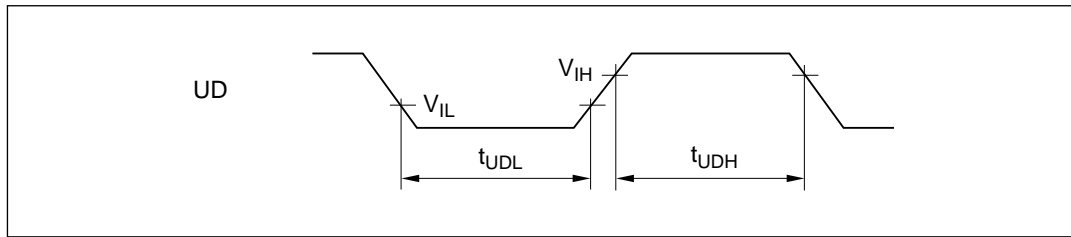


Figure 13-5 UD Pin Minimum Change Width

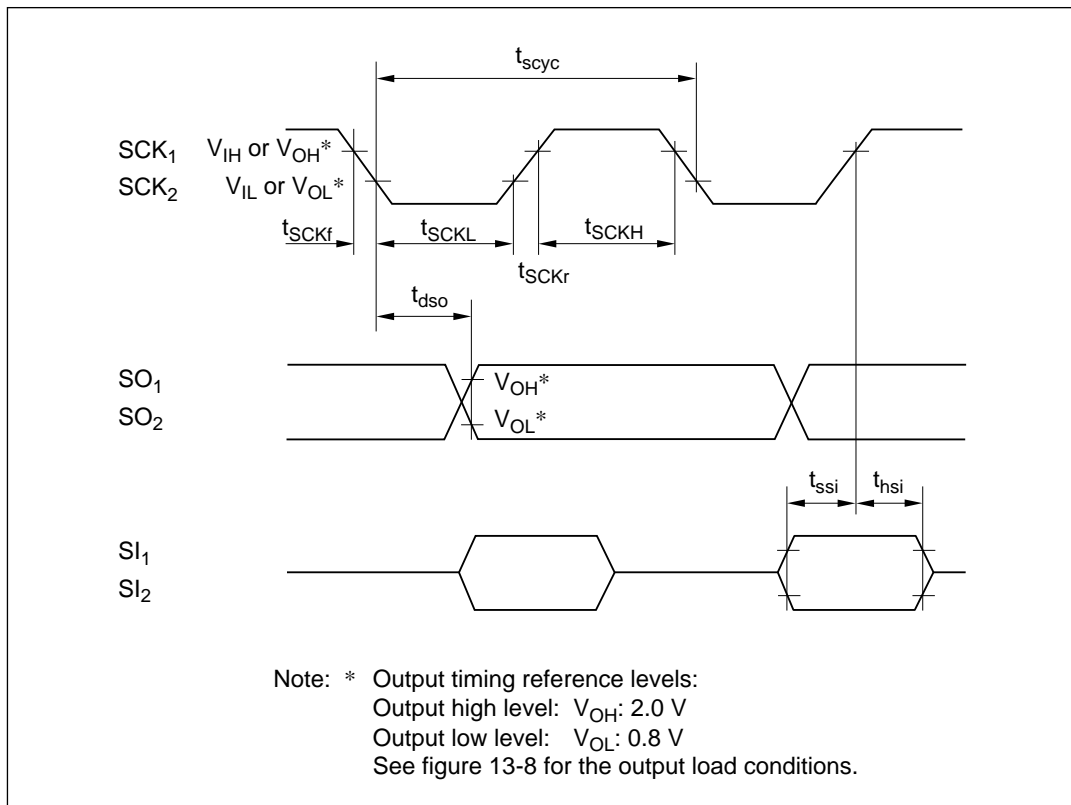


Figure 13-6 SCI I/O Timing

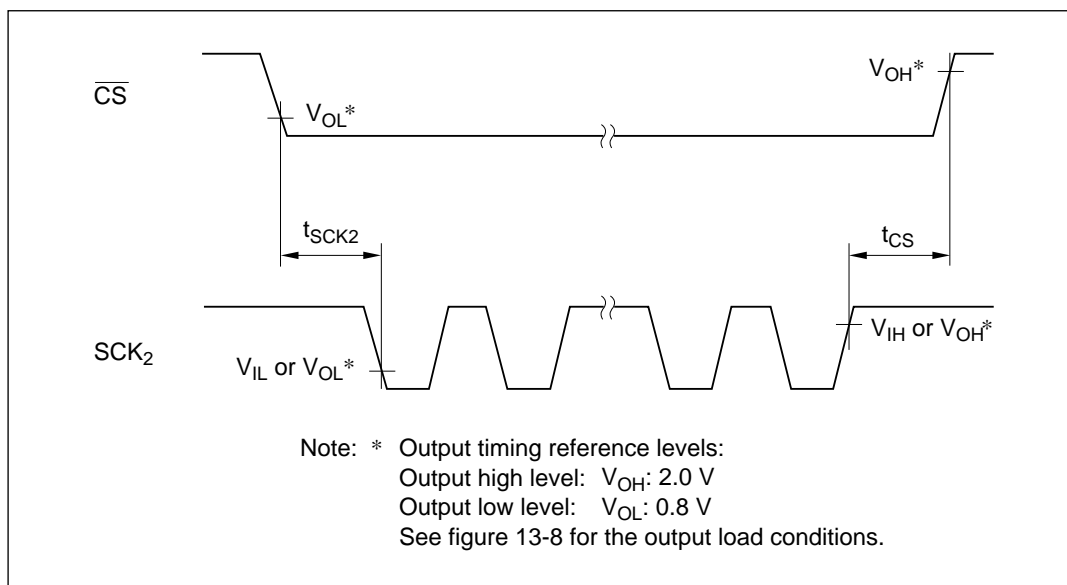


Figure 13-7 Serial Communication Interface 2 Chip Select Timing

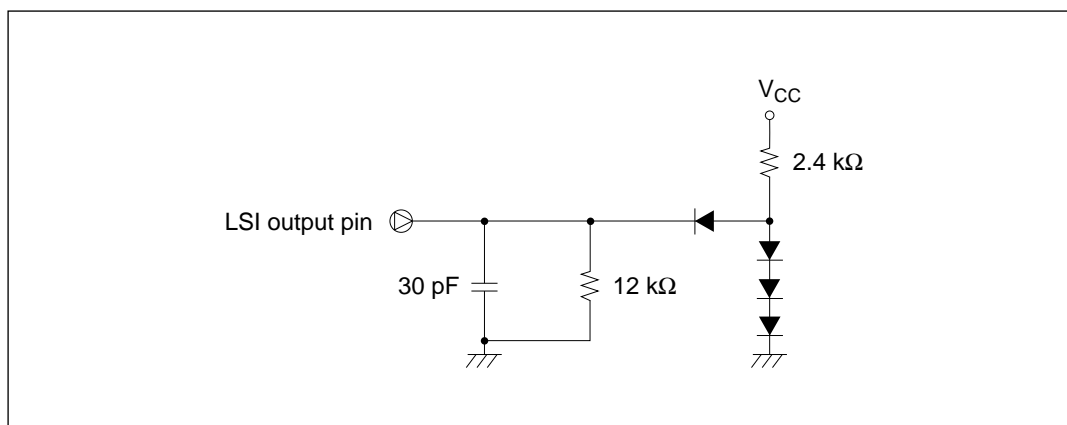


Figure 13-8 Output Load Conditions

13.6 Differences in Electrical Characteristics between Mask ROM and ZTAT™ Versions

Table 13-17 shows the difference in electrical characteristics between the HD6473614 and HD6433612/HD6433613/HD6433614.

Table 13-17 Differences in Electrical Characteristics between Mask ROM and ZTAT™ Versions

Item	Symbol	Applicable Pins	Test Conditions	Mask ROM Version			ZTAT™ Version			Unit
				Min	Typ	Max	Min	Typ	Max	
Operation range in subactive mode		V _{CC}		2.5	—	5.5	2.7	—	5.5	V
Input leakage current	I _{IL}	$\overline{\text{RES}}$		—	—	1	—	—	40	μA
Input capacitance	C _{IN}	P16/ $\overline{\text{EVENT}}$		—	—	15	—	—	35	pF
		P17		—	—	30	—	—	20	
		$\overline{\text{RES}}$		—	—	15	—	—	70	
Current dissipation when CPU operating in active mode	I _{OPE}	V _{CC}	V _{CC} = 5 V, f _{OSC} = 8 MHz	—	15	—	—	17	—	mA
			V _{CC} = 5 V, f _{OSC} = 4 MHz	—	8	—	—	9	—	
			V _{CC} = 3 V, f _{OSC} = 4 MHz	—	5	—	—	6	—	
Current dissipation during reset in active mode	I _{RES}	V _{CC}	V _{CC} = 5 V, f _{OSC} = 8 MHz	—	5	8	—	6	9	mA
			V _{CC} = 5 V, f _{OSC} = 4 MHz	—	2.5	4	—	3	5	
			V _{CC} = 3 V, f _{OSC} = 4 MHz	—	1.3	—	—	1.5	—	
Current dissipation in sleep mode	I _{SLEEP}	V _{CC}	V _{CC} = 5 V, f _{OSC} = 8 MHz	—	2	3	—	2.5	3.5	
			V _{CC} = 5 V, f _{OSC} = 4 MHz	—	1	1.5	—	1.5	2	
			V _{CC} = 3 V, f _{OSC} = 4 MHz	—	0.6	—	—	1	—	

Table 13-17 Differences in Electrical Characteristics between Mask ROM and ZTAT™ Versions (cont)

Item	Symbol	Applicable Pins	Test Conditions	Mask ROM Version			ZTAT™ Version			Unit
				Min	Typ	Max	Min	Typ	Max	
Current dissipation in subactive mode	I _{SUB}	V _{CC}	V _{CC} = 2.5 V (no bypass capacitor)	—	5	20				μA
			V _{CC} = 2.5 V (47 μF bypass capacitor)	—	9	—				
			V _{CC} = 2.7 V (no bypass capacitor)				—	6	20	
			V _{CC} = 2.7 V (47 μF bypass capacitor)				—	11	—	
			V _{CC} = 5 V (no bypass capacitor)	—	13	—	—	16	—	
			V _{CC} = 5 V (47 μF bypass capacitor)	—	20	—	—	22	—	
Current dissipation in watch mode	I _{WATCH}	V _{CC}	V _{CC} = 2.5 V (no bypass capacitor)	—	2.2	5				μA
			V _{CC} = 2.5 V (47 μF bypass capacitor)	—	2.8	—				
			V _{CC} = 2.7 V (no bypass capacitor)				—	3.2	6	
			V _{CC} = 2.7 V (47 μF bypass capacitor)				—	3.8	—	
			V _{CC} = 5 V (no bypass capacitor)	—	6	—	—	10	—	
			V _{CC} = 5 V (47 μF bypass capacitor)	—	8	—	—	12	—	
Current dissipation in standby mode	I _{STBY}	V _{CC}		—	—	5	—	—	10	μA

Appendix A CPU Instruction Set

A.1 Instruction Set List

Operation Notation

Rd8/16	General register (destination) (8 or 16 bits)
Rs8/16	General register (source) (8 or 16 bits)
Rn8/16	General register (8 or 16 bits)
CCR	Condition code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#xx:3/8/16	Immediate data (3, 8, or 16 bits)
d:8/16	Displacement (8 or 16 bits)
@aa:8/16	Absolute address (8 or 16 bits)
+	Addition
−	Subtraction
×	Multiplication
÷	Division
^	AND logical
∨	OR logical
⊕	Exclusive OR logical
→	Move
—	Inverse logic

Condition Code Notation

Symbol

↑	Modified according to the instruction result
*	Not fixed (value not guaranteed)
0	Always cleared to 0
—	Not affected by the instruction execution result

A.2 Operation Code Map

Table A-1 is a map of the operation codes contained in the first byte of the instruction code (bits 15 to 8 of the first instruction word).

Some pairs of instructions have identical first bytes. These instructions are differentiated by the first bit of the second byte (bit 7 of the first instruction word).

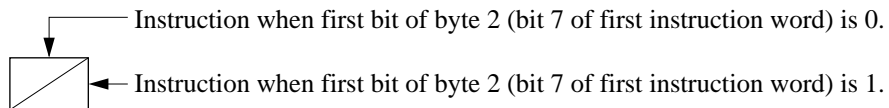


Table A-1 Operation Code Map

LO HI	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SLEEP*2	STC	LDC	ORC	XORC	ANDC	LDC	ADD		INC	ADDS	MOV		ADDX	DAA
1	SHLL SHAL	SHLR SHAR	ROTXL ROTL	ROTXR ROTR	OR	XOR	AND	NOT NEG	SUB		DEC	SUBS	CMP		SUBX	DAS
2	MOV															
3																
4	BRA	BRN	BHI	BLS	BCC	BCS	BNE	BEQ	BVC	BVS	BPL	BMI	BGE	BLT	BGT	BLE
5	MULXU	DIVXU			RTS	BSR	RTE			JMP					JSR	
6	BSET	BNOT	BCLR	BTST				BST BIST	MOV*1							
7					BOR BIOR	BXOR BIXOR	BAND BIAND	BLD BILD			MOV			EEPMOV	Bit manipulation instruction	
8	ADD															
9	ADDX															
A	CMP															
B	SUBX															
C	OR															
D	XOR															
E	AND															
F	MOV															

Note: 1. The PUSH and POP instructions are identical in machine language to MOV instructions.
 2. Do not use the SLEEP instruction.

A.3 Number of States Required for Execution

Table A-2 Instruction Set

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (Bytes)										Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@ (d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@ (d:8, PC)	@@aa	I								
												I	H	N	Z	V	C		
MOV.B #xx:8, Rd	B	#xx:8 → Rd8	2									—	—	↑	↑	0	—	2	
MOV.B Rs, Rd	B	Rs8 → Rd8		2								—	—	↑	↑	0	—	2	
MOV.B @Rs, Rd	B	@Rs16 → Rd8			2							—	—	↑	↑	0	—	4	
MOV.B @(d:16, Rs), Rd	B	@(d:16, Rs16)→ Rd8				4						—	—	↑	↑	0	—	6	
MOV.B @Rs+, Rd	B	@Rs16 → Rd8 Rs16+1 → Rs16					2					—	—	↑	↑	0	—	6	
MOV.B @aa:8, Rd	B	@aa:8 → Rd8						2				—	—	↑	↑	0	—	4	
MOV.B @aa:16, Rd	B	@aa:16 → Rd8						4				—	—	↑	↑	0	—	6	
MOV.B Rs, @Rd	B	Rs8 → @Rd16			2							—	—	↑	↑	0	—	4	
MOV.B Rs, @(d:16, Rd)	B	Rs8 → @(d:16, Rd16)				4						—	—	↑	↑	0	—	6	
MOV.B Rs, @-Rd	B	Rd16-1 → Rd16 Rs8 → @Rd16					2					—	—	↑	↑	0	—	6	
MOV.B Rs, @aa:8	B	Rs8 → @aa:8						2				—	—	↑	↑	0	—	4	
MOV.B Rs, @aa:16	B	Rs8 → @aa:16						4				—	—	↑	↑	0	—	6	
MOV.W #xx:16, Rd	W	#xx:16 → Rd	4									—	—	↑	↑	0	—	4	
MOV.W Rs, Rd	W	Rs16 → Rd16		2								—	—	↑	↑	0	—	2	
MOV.W @Rs, Rd	W	@Rs16 → Rd16			2							—	—	↑	↑	0	—	4	
MOV.W @(d:16, Rs), Rd	W	@(d:16, Rs16) → Rd16				4						—	—	↑	↑	0	—	6	
MOV.W @Rs+, Rd	W	@Rs16 → Rd16 Rs16+2 → Rs16					2					—	—	↑	↑	0	—	6	
MOV.W @aa:16, Rd	W	@aa:16 → Rd16						4				—	—	↑	↑	0	—	6	
MOV.W Rs, @Rd	W	Rs16 → @Rd16			2							—	—	↑	↑	0	—	4	
MOV.W Rs, @(d:16, Rd)	W	Rs16 → @(d:16, Rd16)				4						—	—	↑	↑	0	—	6	
MOV.W Rs, @-Rd	W	Rd16-2 → Rd16 Rs16 → @Rd16					2					—	—	↑	↑	0	—	6	
MOV.W Rs, @aa:16	W	Rs16 → @aa:16						4				—	—	↑	↑	0	—	6	
POP Rd	W	@SP → Rd16 SP+2 → SP					2					—	—	↑	↑	0	—	6	
PUSH Rs	W	SP-2 → SP Rs16 → @SP					2					—	—	↑	↑	0	—	6	

Table A-2 Instruction Set (cont)

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (Bytes)										Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@ (d:16, Rn)	@ -Rn/@Rn+	@aa:8/16	@ (d:8, PC)	@ @aa	I								
												I	H	N	Z	V	C		
EEPMOV	—	if R4L≠0 then Repeat @R5 → @R6 R5+1 → R5 R6+1 → R6 R4L-1 → R4L Until R4L=0 else next;									4	—	—	—	—	—	—	[4]	
ADD.B #xx:8, Rd	B	Rd8+#xx:8 → Rd8	2									—	↑	↑	↑	↑	↑	2	
ADD.B Rs, Rd	B	Rd8+Rs8 → Rd8		2								—	↑	↑	↑	↑	↑	2	
ADD.W Rs, Rd	W	Rd16+Rs16 → Rd16		2								—	[1]	↑	↑	↑	↑	2	
ADDX.B #xx:8, Rd	B	Rd8+#xx:8 +C → Rd8	2									—	↑	↑	[2]	↑	↑	2	
ADDX.B Rs, Rd	B	Rd8+Rs8 +C → Rd8		2								—	↑	↑	[2]	↑	↑	2	
ADDS.W #1, Rd	W	Rd16+1 → Rd16		2								—	—	—	—	—	—	2	
ADDS.W #2, Rd	W	Rd16+2 → Rd16		2								—	—	—	—	—	—	2	
INC.B Rd	B	Rd8+1 → Rd8		2								—	—	↑	↑	↑	—	2	
DAA.B Rd	B	Rd8 decimal adjust → Rd8	2									—	*	↑	↑	*	[3]	2	
SUB.B Rs, Rd	B	Rd8-Rs8 → Rd8		2								—	↑	↑	↑	↑	↑	2	
SUB.W Rs, Rd	W	Rd16-Rs16 → Rd16		2								—	[1]	↑	↑	↑	↑	2	
SUBX.B #xx:8, Rd	B	Rd8-#xx:8-C → Rd8	2									—	↑	↑	[2]	↑	↑	2	
SUBX.B Rs, Rd	B	Rd8-Rs8-C → Rd8		2								—	↑	↑	[2]	↑	↑	2	
SUBS.W #1, Rd	W	Rd16-1 → Rd16		2								—	—	—	—	—	—	2	
SUBS.W #2, Rd	W	Rd16-2 → Rd16		2								—	—	—	—	—	—	2	
DEC.B Rd	B	Rd8-1 → Rd8		2								—	—	↑	↑	↑	—	2	
DAS.B Rd	B	Rd8 decimal adjust → Rd8	2									—	*	↑	↑	*	—	2	
NEG.B Rd	B	0-Rd → Rd		2								—	↑	↑	↑	↑	↑	2	
CMP.B #xx:8, Rd	B	Rd8-#xx:8	2									—	↑	↑	↑	↑	↑	2	
CMP.B Rs, Rd	B	Rd8-Rs8		2								—	↑	↑	↑	↑	↑	2	
CMP.W Rs, Rd	W	Rd16-Rs16		2								—	[1]	↑	↑	↑	↑	2	

Table A-2 Instruction Set (cont)

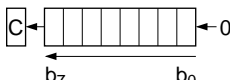
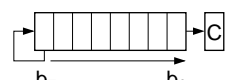
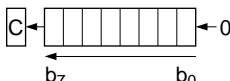
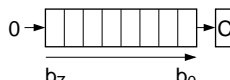

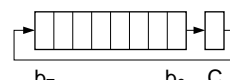
Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (Bytes)										Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@ (d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@ (d:8, PC)	@ @aa	I	I	H	N	Z	V	C		
MULXU.B Rs, Rd	B	$Rd8 \times Rs8 \rightarrow Rd16$		2									—	—	—	—	—	—	14
DIVXU.B Rs, Rd	B	$Rd16 \div Rs8 \rightarrow Rd16$ (RdH: remainder, RdL: quotient)		2									—	—	[5]	[6]	—	—	14
AND.B #xx:8, Rd	B	$Rd8 \wedge \#xx:8 \rightarrow Rd8$	2										—	—	↓	↓	0	—	2
AND.B Rs, Rd	B	$Rd8 \wedge Rs8 \rightarrow Rd8$		2									—	—	↓	↓	0	—	2
OR.B #xx:8, Rd	B	$Rd8 \vee \#xx:8 \rightarrow Rd8$	2										—	—	↓	↓	0	—	2
OR.B Rs, Rd	B	$Rd8 \vee Rs8 \rightarrow Rd8$		2									—	—	↓	↓	0	—	2
XOR.B #xx:8, Rd	B	$Rd8 \oplus \#xx:8 \rightarrow Rd8$	2										—	—	↓	↓	0	—	2
XOR.B Rs, Rd	B	$Rd8 \oplus Rs8 \rightarrow Rd8$		2									—	—	↓	↓	0	—	2
NOT.B Rd	B	$\overline{Rd} \rightarrow Rd$		2									—	—	↓	↓	0	—	2
SHAL.B Rd	B			2									—	—	↓	↓	↓	↓	2
SHAR.B Rd	B			2									—	—	↓	↓	0	↓	2
SHLL.B Rd	B			2									—	—	↓	↓	0	↓	2
SHLR.B Rd	B			2									—	—	0	↓	0	↓	2
ROTXL.B Rd	B			2									—	—	↓	↓	0	↓	2
ROTXR.B Rd	B			2									—	—	↓	↓	0	↓	2

Table A-2 Instruction Set (cont)

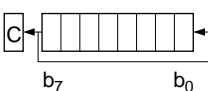
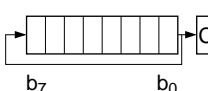
Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (Bytes)										Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	I								
			I	H	N	Z	V	C											
ROTL.B Rd	B			2								—	—	↕	↕	0	↕	2	
ROTR.B Rd	B			2								—	—	↕	↕	0	↕	2	
BSET #xx:3, Rd	B	(#xx:3 of Rd8) ← 1		2								—	—	—	—	—	—	2	
BSET #xx:3, @Rd	B	(#xx:3 of @Rd16) ← 1			4							—	—	—	—	—	—	8	
BSET #xx:3, @aa:8	B	(#xx:3 of @aa:8) ← 1						4				—	—	—	—	—	—	8	
BSET Rn, Rd	B	(Rn8 of Rd8) ← 1		2								—	—	—	—	—	—	2	
BSET Rn, @Rd	B	(Rn8 of @Rd16) ← 1			4							—	—	—	—	—	—	8	
BSET Rn, @aa:8	B	(Rn8 of @aa:8) ← 1						4				—	—	—	—	—	—	8	
BCLR #xx:3, Rd	B	(#xx:3 of Rd8) ← 0		2								—	—	—	—	—	—	2	
BCLR #xx:3, @Rd	B	(#xx:3 of @Rd16) ← 0			4							—	—	—	—	—	—	8	
BCLR #xx:3, @aa:8	B	(#xx:3 of @aa:8) ← 0						4				—	—	—	—	—	—	8	
BCLR Rn, Rd	B	(Rn8 of Rd8) ← 0		2								—	—	—	—	—	—	2	
BCLR Rn, @Rd	B	(Rn8 of @Rd16) ← 0			4							—	—	—	—	—	—	8	
BCLR Rn, @aa:8	B	(Rn8 of @aa:8) ← 0						4				—	—	—	—	—	—	8	
BNOT #xx:3, Rd	B	(#xx:3 of Rd8) ← (#xx:3 of Rd8)		2								—	—	—	—	—	—	2	
BNOT #xx:3, @Rd	B	(#xx:3 of @Rd16) ← (#xx:3 of @Rd16)			4							—	—	—	—	—	—	8	
BNOT #xx:3, @aa:8	B	(#xx:3 of @aa:8) ← (#xx:3 of @aa:8)						4				—	—	—	—	—	—	8	
BNOT Rn, Rd	B	(Rn8 of Rd8) ← (Rn8 of Rd8)		2								—	—	—	—	—	—	2	
BNOT Rn, @Rd	B	(Rn8 of @Rd16) ← (Rn8 of @Rd16)			4							—	—	—	—	—	—	8	
BNOT Rn, @aa:8	B	(Rn8 of @aa:8) ← (Rn8 of @aa:8)						4				—	—	—	—	—	—	8	

Table A-2 Instruction Set (cont)

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (Bytes)									Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	I							
			I	H	N	Z	V	C										
BTST #xx:3, Rd	B	(#xx:3 of Rd8) → Z		2								—	—	—	↑	—	—	2
BTST #xx:3, @Rd	B	(#xx:3 of @Rd16) → Z			4							—	—	—	↑	—	—	6
BTST #xx:3, @aa:8	B	(#xx:3 of @aa:8) → Z						4				—	—	—	↑	—	—	6
BTST Rn, Rd	B	(Rn8 of Rd8) → Z		2								—	—	—	↑	—	—	2
BTST Rn, @Rd	B	(Rn8 of @Rd16) → Z			4							—	—	—	↑	—	—	6
BTST Rn, @aa:8	B	(Rn8 of @aa:8) → Z						4				—	—	—	↑	—	—	6
BLD #xx:3, Rd	B	(#xx:3 of Rd8) → C		2								—	—	—	—	—	↑	2
BLD #xx:3, @Rd	B	(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↑	6
BLD #xx:3, @aa:8	B	(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↑	6
BILD #xx:3, Rd	B	(#xx:3 of Rd8) → C		2								—	—	—	—	—	↑	2
BILD #xx:3, @Rd	B	(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↑	6
BILD #xx:3, @aa:8	B	(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↑	6
BST #xx:3, Rd	B	C → (#xx:3 of Rd8)		2								—	—	—	—	—	—	2
BST #xx:3, @Rd	B	C → (#xx:3 of @Rd16)			4							—	—	—	—	—	—	8
BST #xx:3, @aa:8	B	C → (#xx:3 of @aa:8)						4				—	—	—	—	—	—	8
BIST #xx:3, Rd	B	\overline{C} → (#xx:3 of Rd8)		2								—	—	—	—	—	—	2
BIST #xx:3, @Rd	B	\overline{C} → (#xx:3 of @Rd16)			4							—	—	—	—	—	—	8
BIST #xx:3, @aa:8	B	\overline{C} → (#xx:3 of @aa:8)						4				—	—	—	—	—	—	8
BAND #xx:3, Rd	B	$C \wedge (\#xx:3 \text{ of Rd8}) \rightarrow C$		2								—	—	—	—	—	↑	2
BAND #xx:3, @Rd	B	$C \wedge (\#xx:3 \text{ of @Rd16}) \rightarrow C$			4							—	—	—	—	—	↑	6
BAND #xx:3, @aa:8	B	$C \wedge (\#xx:3 \text{ of @aa:8}) \rightarrow C$						4				—	—	—	—	—	↑	6
BIAND #xx:3, Rd	B	$C \wedge (\#xx:3 \text{ of Rd8}) \rightarrow C$		2								—	—	—	—	—	↑	2
BIAND #xx:3, @Rd	B	$C \wedge (\#xx:3 \text{ of @Rd16}) \rightarrow C$			4							—	—	—	—	—	↑	6
BIAND #xx:3, @aa:8	B	$C \wedge (\#xx:3 \text{ of @aa:8}) \rightarrow C$						4				—	—	—	—	—	↑	6
BOR #xx:3, Rd	B	$C \vee (\#xx:3 \text{ of Rd8}) \rightarrow C$		2								—	—	—	—	—	↑	2
BOR #xx:3, @Rd	B	$C \vee (\#xx:3 \text{ of @Rd16}) \rightarrow C$			4							—	—	—	—	—	↑	6
BOR #xx:3, @aa:8	B	$C \vee (\#xx:3 \text{ of @aa:8}) \rightarrow C$						4				—	—	—	—	—	↑	6
BIOR #xx:3, Rd	B	$C \vee (\#xx:3 \text{ of Rd8}) \rightarrow C$		2								—	—	—	—	—	↑	2
BIOR #xx:3, @Rd	B	$C \vee (\#xx:3 \text{ of @Rd16}) \rightarrow C$			4							—	—	—	—	—	↑	6

Table A-2 Instruction Set (cont)

Mnemonic	Operand Size	Operation	Branching Condition	Addressing Mode/ Instruction Length (Bytes)									Condition Code						No. of States
				#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	I							
													I	H	N	Z	V	C	
BIOR #xx:3, @aa:8	B	$C \vee (\#xx:3 \text{ of } @aa:8) \rightarrow C$							4				—	—	—	—	—	↑	6
BXOR #xx:3, Rd	B	$C \oplus (\#xx:3 \text{ of } Rd8) \rightarrow C$			2								—	—	—	—	—	↑	2
BXOR #xx:3, @Rd	B	$C \oplus (\#xx:3 \text{ of } @Rd16) \rightarrow C$				4							—	—	—	—	—	↑	6
BXOR #xx:3, @aa:8	B	$C \oplus (\#xx:3 \text{ of } @aa:8) \rightarrow C$							4				—	—	—	—	—	↑	6
BIXOR #xx:3, Rd	B	$C \oplus (\#xx:3 \text{ of } Rd8) \rightarrow C$			2								—	—	—	—	—	↑	2
BIXOR #xx:3, @Rd	B	$C \oplus (\#xx:3 \text{ of } @Rd16) \rightarrow C$				4							—	—	—	—	—	↑	6
BIXOR #xx:3, @aa:8	B	$C \oplus (\#xx:3 \text{ of } @aa:8) \rightarrow C$							4				—	—	—	—	—	↑	6
BRA d:8 (BT d:8)	—	$PC \leftarrow PC + d:8$								2			—	—	—	—	—	—	4
BRN d:8 (BF d:8)	—	$PC \leftarrow PC + 2$								2			—	—	—	—	—	—	4
BHI d:8	—	If condition is true then $PC \leftarrow PC + d:8$ else next;	$C \vee Z = 0$							2			—	—	—	—	—	—	4
BLS d:8	—		$C \vee Z = 1$							2			—	—	—	—	—	—	4
BCC d:8 (BHS d:8)	—		$C = 0$							2			—	—	—	—	—	—	4
BCS d:8 (BLO d:8)	—		$C = 1$							2			—	—	—	—	—	—	4
BNE d:8	—		$Z = 0$							2			—	—	—	—	—	—	4
BEQ d:8	—		$Z = 1$							2			—	—	—	—	—	—	4
BVC d:8	—		$V = 0$							2			—	—	—	—	—	—	4
BVS d:8	—		$V = 1$							2			—	—	—	—	—	—	4
BPL d:8	—		$N = 0$							2			—	—	—	—	—	—	4
BMI d:8	—		$N = 1$							2			—	—	—	—	—	—	4
BGE d:8	—		$N \oplus V = 0$							2			—	—	—	—	—	—	4
BLT d:8	—		$N \oplus V = 1$							2			—	—	—	—	—	—	4
BGT d:8	—		$Z \vee (N \oplus V) = 0$							2			—	—	—	—	—	—	4
BLE d:8	—		$Z \vee (N \oplus V) = 1$							2			—	—	—	—	—	—	4
JMP @Rn	—	$PC \leftarrow Rn16$				2							—	—	—	—	—	—	4
JMP @aa:16	—	$PC \leftarrow aa:16$							4				—	—	—	—	—	—	6
JMP @@aa:8	—	$PC \leftarrow @@aa:8$									2		—	—	—	—	—	—	8
BSR d:8	—	SP-2 → SP PC → @SP PC ← PC+d:8								2			—	—	—	—	—	—	6

Table A-2 Instruction Set (cont)

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (Bytes)									Condition Code						No. of States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	I							
JSR @Rn	—	SP-2 → SP PC → @SP PC ← Rn16			2							—	—	—	—	—	—	6
JSR @aa:16	—	SP-2 → SP PC → @SP PC ← aa:16						4				—	—	—	—	—	—	8
JSR @@aa:8	—	SP-2 → SP PC → @SP PC ← @aa:8								2		—	—	—	—	—	—	8
RTS	—	PC ← @SP SP+2 → SP									2	—	—	—	—	—	—	8
RTE	—	CCR ← @SP SP+2 → SP PC ← @SP SP+2 → SP									2	↑	↑	↑	↑	↑	↑	10
SLEEP	—	Transit to sleep mode.									2	—	—	—	—	—	—	2
LDC #xx:8, CCR	B	#xx:8 → CCR	2									↑	↑	↑	↑	↑	↑	2
LDC Rs, CCR	B	Rs8 → CCR		2								↑	↑	↑	↑	↑	↑	2
STC CCR, Rd	B	CCR → Rd8		2								—	—	—	—	—	—	2
ANDC #xx:8, CCR	B	CCR ∧ #xx:8 → CCR	2									↑	↑	↑	↑	↑	↑	2
ORC #xx:8, CCR	B	CCR ∨ #xx:8 → CCR	2									↑	↑	↑	↑	↑	↑	2
XORC #xx:8, CCR	B	CCR ⊕ #xx:8 → CCR	2									↑	↑	↑	↑	↑	↑	2
NOP	—	PC ← PC+2									2	—	—	—	—	—	—	2

- Notes: [1] Set to 1 when there is a carry or borrow from bit 11; otherwise cleared to 0.
[2] If the result is zero, the previous value of the flag is retained; otherwise the flag is cleared to 0.
[3] Set to 1 if decimal adjustment produces a carry; otherwise cleared to 0.
[4] The number of states required for execution is 4n+9 (n = value of R4L).
[5] Set to 1 if the divisor is negative; otherwise cleared to 0.
[6] Set to 1 if the divisor is zero; otherwise cleared to 0.

Appendix B On-Chip Registers

B.1 On-Chip Registers (1)

Addr. (Last Byte)	Register Name	Bit Names								Module Name
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'A0	STAR	—	—	—	STA4	STA3	STA2	STA1	STA0	SCI2
H'A1	EDAR	—	—	—	EDA4	EDA3	EDA2	EDA1	EDA0	
H'A2	SCR2	—	—	—	I/O	GAP2	GAP1	PS1	PS0	
H'A3	STSR	—	—	—	SO2 LAST BIT	OVR	WT	GIT	STF	
H'A4 to H'AF	—	Not used								—
H'B0	SMR1	—	SMR16	SMR15	SMR14	SMR13	SMR12	SMR11	SMR10	SCI1
H'B1	SDRU1	SDRU17	SDRU16	SDRU15	SDRU14	SDRU13	SDRU12	SDRU11	SDRU10	
H'B2	SDRL1	SDRL17	SDRL16	SDRL15	SDRL14	SDRL13	SDRL12	SDRL11	SDRL10	
H'B3	SPR1	SO1 LAST BIT	—	—	—	—	—	—	—	
H'B4	—	—	—	—	—	—	—	—	—	—
H'B5	—	—	—	—	—	—	—	—	—	
H'B6	—	—	—	—	—	—	—	—	—	
H'B7	—	—	—	—	—	—	—	—	—	
H'B8	—	—	—	—	—	—	—	—	—	
H'B9	—	—	—	—	—	—	—	—	—	
H'BA	—	—	—	—	—	—	—	—	—	
H'BB	—	—	—	—	—	—	—	—	—	
H'BC	AMR	AMR7	—	—	—	—	AMR2	AMR1	AMR0	A/D converter
H'BD	ADRR	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	
H'BE	ADSR	ADSF	—	—	—	—	—	—	—	
H'BF	—	—	—	—	—	—	—	—	—	

Notation: SCI1: Serial communication interface 1
SCI2: Serial communication interface 2

B.1 On-Chip Registers (1) (cont)

Addr. (Last Byte)	Register Name	Bit Names								Module Name
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'C0	TMA	—	—	—	—	TMA3	TMA2	TMA1	TMA0	Timer A
H'C1	TCA	TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0	
H'C2	TMB	TMB7	—	—	—	—	TMB2	TMB1	TMB0	Timer B
H'C3	TLB/TCB	TLB7/ TCB7	TLB6/ TCB6	TLB5/ TCB5	TLB4/ TCB4	TLB3/ TCB3	TLB2/ TCB2	TLB1/ TCB1	TLB0/ TCB0	
H'C4	TMC	TMC7	TMC6	TMC5	—	—	TMC2	TMC1	TMC0	Timer C
H'C5	TLC/TCC	TLC7/ TCC7	TLC6/ TCC6	TLC5/ TCC5	TLC4/ TCC4	TLC3/ TCC3	TLC2/ TCC2	TLC1/ TCC1	TLC0/ TCC0	
H'C6	TMD	CLR	—	—	—	—	—	—	EDG	Timer D
H'C7	TCD	TCD7	TCD6	TCD5	TCD4	TCD3	TCD2	TCD1	TCD0	
H'C8	TME	TME7	—	—	—	—	TME2	TME1	TME0	Timer E
H'C9	TLE/TCE	TLE7/ TCE7	TLE6/ TCE6	TLE5/ TCE5	TLE4/ TCE4	TLE3/ TCE3	TLE2/ TCE2	TLE1/ TCE1	TLE0/ TCE0	
H'CA	—	—	—	—	—	—	—	—	—	14-bit PWM
H'CB	—	—	—	—	—	—	—	—	—	
H'CC	PWCR*	—	—	—	—	—	—	—	PWCR0	
H'CD	PWDRU*	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDRU1	PWDRU0	
H'CE	PWDRL*	PWDRL7	PWDRL6	PWDRL5	PWDRL4	PWDRL3	PWDRL2	PWDRL1	PWDRL0	
H'CF	—	—	—	—	—	—	—	—	—	I/O ports
H'D0	PDR0	PDR0 ₇	PDR0 ₆	PDR0 ₅	PDR0 ₄	PDR0 ₃	PDR0 ₂	PDR0 ₁	PDR0 ₀	
H'D1	PDR1	—	—	PDR1 ₅	PDR1 ₄	PDR1 ₃	PDR1 ₂	PDR1 ₁	PDR1 ₀	
H'D2	PDR2	PDR2 ₇	PDR2 ₆	PDR2 ₅	PDR2 ₄	PDR2 ₃	PDR2 ₂	PDR2 ₁	PDR2 ₀	
H'D3	—	—	—	—	—	—	—	—	—	
H'D4	PDR4	—	—	PDR4 ₅	PDR4 ₄	PDR4 ₃	PDR4 ₂	PDR4 ₁	PDR4 ₀	
H'D5	—	—	—	—	—	—	—	—	—	
H'D6	—	—	—	—	—	—	—	—	—	
H'D7	—	—	—	—	—	—	—	—	—	
H'D8	PDR8	PDR8 ₇	PDR8 ₆	PDR8 ₅	PDR8 ₄	PDR8 ₃	PDR8 ₂	PDR8 ₁	PDR8 ₀	
H'D9	PDR9	PDR9 ₇	PDR9 ₆	PDR9 ₅	PDR9 ₄	PDR9 ₃	PDR9 ₂	PDR9 ₁	PDR9 ₀	
H'DA	PDRA	PDRA ₇	PDRA ₆	PDRA ₅	PDRA ₄	PDRA ₃	PDRA ₂	PDRA ₁	PDRA ₀	
H'DB	—	—	—	—	—	—	—	—	—	
H'DC	—	—	—	—	—	—	—	—	—	
H'DD	—	—	—	—	—	—	—	—	—	
H'DE	—	—	—	—	—	—	—	—	—	
H'DF	—	—	—	—	—	—	—	—	—	

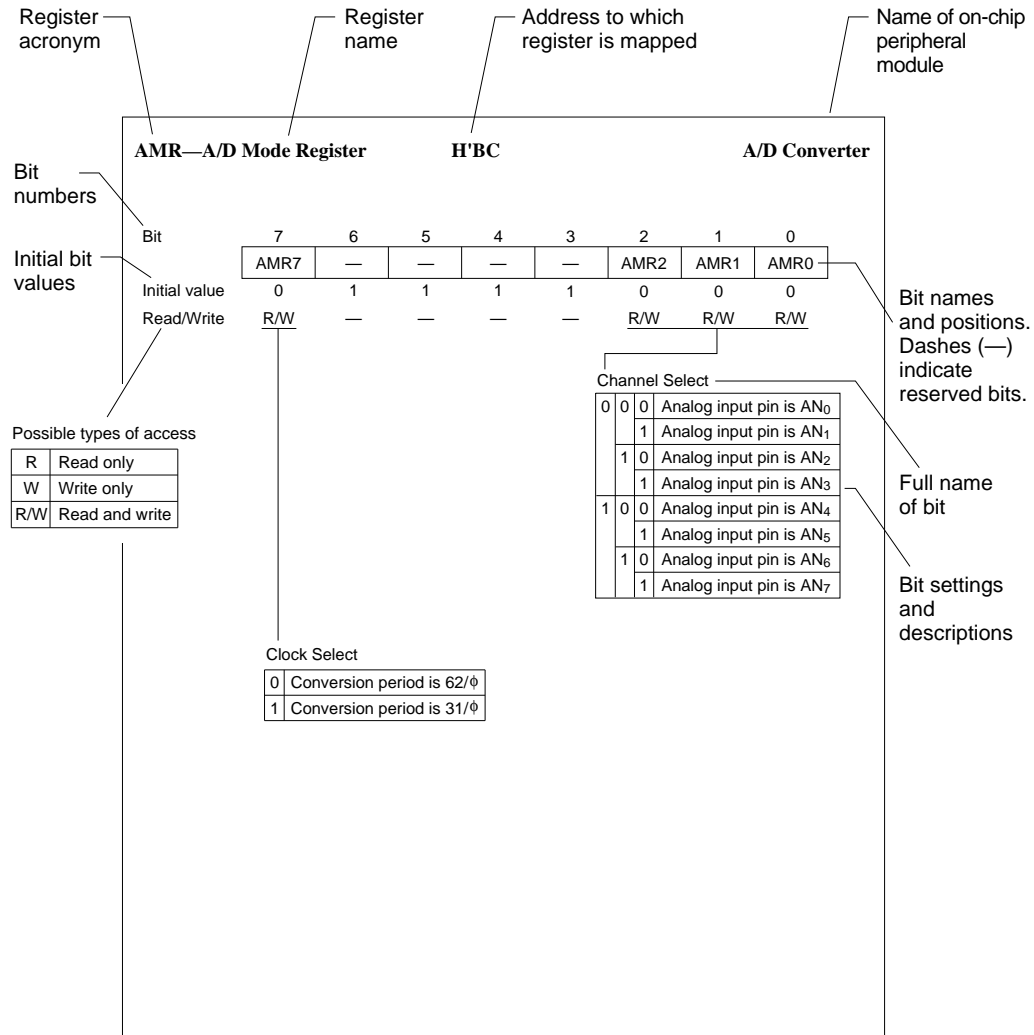
Note: * Not usable in the H8/3612.

B.1 On-Chip Registers (1) (cont)

Addr. (Last Byte)	Register Name	Bit Names								Module Name
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'E0	—	—	—	—	—	—	—	—	—	I/O ports
H'E1	PCR1	—	—	PCR1 ₅	PCR1 ₄	PCR1 ₃	PCR1 ₂	PCR1 ₁	PCR1 ₀	
H'E2	PCR2	PCR2 ₇	PCR2 ₆	PCR2 ₅	PCR2 ₄	PCR2 ₃	PCR2 ₂	PCR2 ₁	PCR2 ₀	
H'E3	—	—	—	—	—	—	—	—	—	
H'E4	—	—	—	—	—	—	—	—	—	
H'E5	—	—	—	—	—	—	—	—	—	
H'E6	—	—	—	—	—	—	—	—	—	
H'E7	—	—	—	—	—	—	—	—	—	
H'E8	PCR8	PCR8 ₇	PCR8 ₆	PCR8 ₅	PCR8 ₄	PCR8 ₃	PCR8 ₂	PCR8 ₁	PCR8 ₀	System control
H'E9	PCR9	PCR9 ₇	PCR9 ₆	PCR9 ₅	PCR9 ₄	PCR9 ₃	PCR9 ₂	PCR9 ₁	PCR9 ₀	
H'EA	PCRA	PCRA ₇	PCRA ₆	PCRA ₅	PCRA ₄	PCRA ₃	PCRA ₂	PCRA ₁	PCRA ₀	
H'EB	PMR1	NOISE CANCEL	EVENT	IRQC5	IRQC4	IRQC3	IRQC2	IRQC1	IRQC0	
H'EC	PMR2	UP/ DOWN	SO2	SI2	SCK2	SO1	SI1	SCK1	PWM*	
H'ED	PMR3	—	SO2 PMOS	CS	—	SO1 PMOS	—	—	—	
H'EE	PMR4	TEO	TEO ON	FREQ	VRFR	—	—	—	—	
H'EF	PMR0	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	
H'F0	SYSCR1	SSBY	STS2	STS1	STS0	LSON	—	—	—	System control
H'F1	SYSCR2	—	—	—	—	DTON	—	—	—	
H'F2	IEGR	—	—	—	IEG4	—	—	IEG1	IEG0	
H'F3	IENR1	—	—	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0	
H'F4	IENR2	—	—	IENDT	IENTE	IENDT	IENTC	IENTB	IENTA	
H'F5	IENR3	IENAD	—	—	—	—	—	IENS2	IENS1	
H'F6	IRR1	—	—	IRRI5	IRRI4	IRRI3	IRRI2	IRRI1	IRRI0	
H'F7	IRR2	—	—	IRRDT	IRRTE	IRRTD	IRRTC	IRRTB	IRRTA	
H'F8	IRR3	IRRAD	—	—	—	—	—	IRRS2	IRRS1	
H'F9	—	—	—	—	—	—	—	—	—	
H'FA	—	—	—	—	—	—	—	—	—	
H'FB	—	—	—	—	—	—	—	—	—	
H'FC	—	—	—	—	—	—	—	—	—	
H'FD	—	—	—	—	—	—	—	—	—	
H'FE	—	—	—	—	—	—	—	—	—	
H'FF	—	—	—	—	—	—	—	—	—	

Note: * Not usable in the H8/3612.

B.2 On-Chip Registers (2)



STAR—Start Address Register**H'A0****SCI2**

Bit	7	6	5	4	3	2	1	0
	—	—	—	STA4	STA3	STA2	STA1	STA0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Designates transfer starting address
in address space H'FF80 to H'FF9F.

EDAR—End Address Register**H'A1****SCI2**

Bit	7	6	5	4	3	2	1	0
	—	—	—	EDA4	EDA3	EDA2	EDA1	EDA0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Designates transfer end address
in address space H'FF80 to H'FF9F.

SCR2—Serial Control Register 2**H'A2****SCI2**

Bit	7	6	5	4	3	2	1	0
	—	—	—	I/O	GAP2	GAP1	PS1	PS0
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Transmit/Receive Select

0	Receive mode
1	Transmit mode

Gap Insertion

0	0	No gap insertion
0	1	1-clock gap insertion
1	0	2-clock gap insertion
1	1	8-clock gap insertion

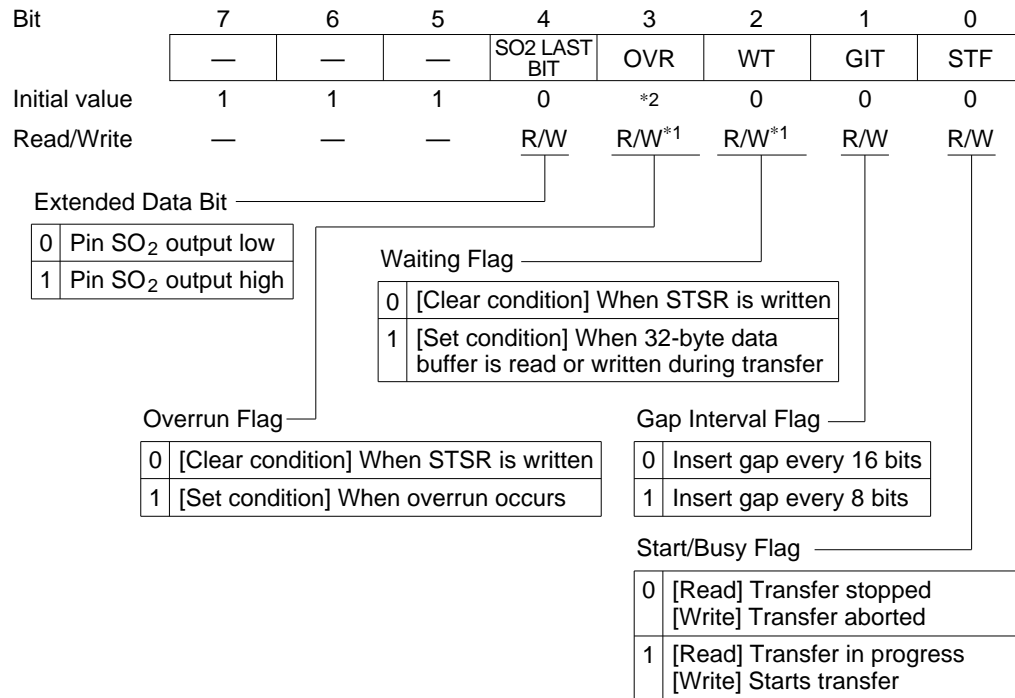
Transfer Clock Select

0	0	$\phi/2$, SCK ₂ is output pin
0	1	$\phi/4$, SCK ₂ is output pin
1	0	$\phi/8$, SCK ₂ is output pin
1	1	External clock, SCK ₂ is input pin

STSR—Status Register

H'A3

SCI2



- Notes:
1. Cleared to 0 by write operation to STSR.
 2. Not fixed

SMR1—Serial Mode Register 1 **H'B0** **SCI1**

Bit	7	6	5	4	3	2	1	0
	—	SMR16	SMR15	SMR14	SMR13	SMR12	SMR11	SMR10
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	W	W	W	W	W	W	W

Operation Mode Select

0	0	0	Clock continuous output mode
	Not 00		8-bit transfer mode
1	0	0	Clock continuous output mode
	Not 00		16-bit transfer mode

Clock Select

0	0	0	0	0/1024, SCK ₁ is output pin			
			1	0/256, SCK ₁ is output pin			
			1	0	0/64, SCK ₁ is output pin		
				1	0/32, SCK ₁ is output pin		
			1	0	0	0/16, SCK ₁ is output pin	
				1	0/8, SCK ₁ is output pin		
			1	0	0/4, SCK ₁ is output pin		
				1	0/2, SCK ₁ is output pin		
			1	0	0	0	Not used
				1	Not used		
			1	0	Not used		
				1	Not used		
			1	0	Not used		
				1	Not used		
			1	0	Not used		
				1	External clock, SCK ₁ is input pin		

SDRU1—Serial Data Register U1 **H'B1** **SCI1**

Bit	7	6	5	4	3	2	1	0
	SDRU17	SDRU16	SDRU15	SDRU14	SDRU13	SDRU12	SDRU11	SDRU10
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Used to set transmit data and store received data.
8-bit transfer mode: not used
16-bit transfer mode: upper 8 bits of data register

Note: * Not fixed

SDRL1—Serial Data Register L1**H'B2****SCI1**

Bit	7	6	5	4	3	2	1	0
	SDRL17	SDRL16	SDRL15	SDRL14	SDRL13	SDRL12	SDRL11	SDRL10
Initial value	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Used to set transmit data and store received data.
 8-bit transfer mode: data register
 16-bit transfer mode: lower 8 bits of data register

Note: * Not fixed

SPR1—Serial Port Register 1**H'B3****SCI1**

Bit	7	6	5	4	3	2	1	0
	SO1 LAST BIT	—	—	—	—	—	—	—
Initial value	*	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

Extended Data Bit

0	Pin SO ₁ output low
0	Pin SO ₁ output high

Note: * Not fixed

AMR—A/D Mode Register**H'BC****A/D Converter**

Bit	7	6	5	4	3	2	1	0
	AMR7	—	—	—	—	AMR2	AMR1	AMR0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W
	Clock Select				Channel Select			
	0	Conversion period is 62/ø				0	0	0
	1	Conversion period is 31/ø				0	1	0
						1	0	0
						1	0	1
						1	1	0
						1	1	1
						1	0	0
						1	0	1
						1	1	0
						1	1	1

ADRR—A/D Result Register**H'BD****A/D Converter**

Bit	7	6	5	4	3	2	1	0
	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
Initial value	*	*	*	*	*	*	*	*
Read/Write	R	R	R	R	R	R	R	R
	A/D Conversion Result							

Note: * Not fixed

ADSR—A/D Start Register**H'BE****A/D Converter**

Bit	7	6	5	4	3	2	1	0
	ADSF	—	—	—	—	—	—	—
Initial value	0	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

A/D Start Flag

0	[Read] A/D conversion stopped or complete [Write] A/D conversion aborted
1	[Read] A/D conversion in progress [Write] Starts A/D conversion

TMA—Timer Mode Register A**H'C0****Timer A**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	TMA3	TMA2	TMA1	TMA0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Clock Select

0	0	0	0	Input source PSS, $\emptyset/8192$
			1	Input source PSS, $\emptyset/4096$
		1	0	Input source PSS, $\emptyset/2048$
			1	Input source PSS, $\emptyset/512$
	1	0	0	Input source PSS, $\emptyset/256$
			1	Input source PSS, $\emptyset/128$
		1	0	Input source PSS, $\emptyset/32$
			1	Input source PSS, $\emptyset/8$
1	0	0	0	Input source PSW, 2 s
			1	Input source PSW, 1 s
		1	0	Input source PSW, 0.5 s
			1	Input source PSW, 125 ms
	1	0	0	PSW and TCA reset
			1	
		1	0	
			1	

TCA—Timer Counter A

H'C1

Timer A

Bit	7	6	5	4	3	2	1	0
	TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Count Value

TMB—Timer Mode Register B

H'C2

Timer B

Bit	7	6	5	4	3	2	1	0
	TMB7	—	—	—	—	TMB2	TMB1	TMB0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

Clock Select

0	0	0	Internal clock, \varnothing /8192
	1		Internal clock, \varnothing /2048
1	0		Internal clock, \varnothing /512
	1		Internal clock, \varnothing /256
1	0	0	Internal clock, \varnothing /128
	1		Internal clock, \varnothing /32
1	0		Internal clock, \varnothing /8
	1		External clock, choice of rising or falling edge

Auto Reload Function Select

0	Interval timer
1	Auto-reload timer

TCB—Timer Counter B**H'C3****Timer B**

Bit	7	6	5	4	3	2	1	0
	TCB7	TCB6	TCB5	TCB4	TCB3	TCB2	TCB1	TCB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Count Value

TLB—Timer Load Register B**H'C3****Timer B**

Bit	7	6	5	4	3	2	1	0
	TLB7	TLB6	TLB5	TLB4	TLB3	TLB2	TLB1	TLB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Reload Value Setting

TMC—Timer Mode Register C**H'C4****Timer C**

Bit	7	6	5	4	3	2	1	0
	TMC7	TMC6	TMC5	—	—	TMC2	TMC1	TMC0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/W	R/W	R/W	—	—	R/W	R/W	R/W

Clock Select

0	0	0	Internal clock, $\varnothing/8192$
1	1	1	Internal clock, $\varnothing/2048$
1	0	0	Internal clock, $\varnothing/512$
1	1	1	Internal clock, $\varnothing/256$
1	0	0	Internal clock, $\varnothing/128$
1	1	1	Internal clock, $\varnothing/32$
1	0	0	Internal clock, $\varnothing/8$
1	1	1	External clock, choice of rising or falling edge

Count-Up/Down Control

0	0	Up-counter
1	1	Down-counter
1	*	Hardware control via pin P9 ₇ /UD. High is down, low is up.

Auto-Reload Function Select

0	Interval timer
1	Auto-reload timer

Note: * Don't care.

TCC—Timer Counter C**H'C5****Timer C**

Bit	7	6	5	4	3	2	1	0
	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Count Value

TLC—Timer Load Register C**H'C5****Timer C**

Bit	7	6	5	4	3	2	1	0
	TLC7	TLC6	TLC5	TLC4	TLC3	TLC2	TLC1	TLC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Reload Value Setting

TMD—Timer Mode Register D**H'C6****Timer D**

Bit	7	6	5	4	3	2	1	0
	CLR	—	—	—	—	—	—	EDG
Initial value	0	1	1	1	1	1	1	0
Read/Write	W	—	—	—	—	—	—	R/W

Edge Select

0	Incremented at falling edge of $\overline{\text{EVENT}}$ pin input
1	Incremented at rising edge of $\overline{\text{EVENT}}$ pin input

Counter Clear

0	After this bit is set to 1 and TCD is initialized, it is automatically cleared by hardware.
1	TCD is initialized to H'00.

TCD—Timer Counter D**H'C7****Timer D**

Bit	7	6	5	4	3	2	1	0
	TCD7	TCD6	TCD5	TCD4	TCD3	TCD2	TCD1	TCD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Count Value

TME—Timer Mode Register E**H'C8****Timer E**

Bit	7	6	5	4	3	2	1	0
	TME7	—	—	—	—	TME2	TME1	TME0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W	—	—	—	—	R/W	R/W	R/W

Auto-Reload Function Select		Clock Select	
0	Interval timer	0 0 0	Internal clock, $\phi/8192$
1	Auto-reload timer	1 1	Internal clock, $\phi/4096$
		1 0	Internal clock, $\phi/2048$
		1 1	Internal clock, $\phi/512$
		1 0 0	Internal clock, $\phi/256$
		1 1	Internal clock, $\phi/128$
		1 0	Internal clock, $\phi/32$
		1 1	Internal clock, $\phi/8$

TCE—Timer Counter E**H'C9****Timer E**

Bit	7	6	5	4	3	2	1	0
	TCE7	TCE6	TCE5	TCE4	TCE3	TCE2	TCE1	TCE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Count Value			
-------------	--	--	--

TLE—Timer Load Register E**H'C9****Timer E**

Bit	7	6	5	4	3	2	1	0
	TLE7	TLE6	TLE5	TLE4	TLE3	TLE2	TLE1	TLE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Reload Value Setting			
----------------------	--	--	--

PWCR—PWM Control Register**H'CC****14-bit PWM**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PWCR0
Initial value	1	1	1	1	1	1	1	0
Read/Write	—	—	—	—	—	—	—	W

Clock Select

0	The input clock is $\phi/2$. The conversion period is $16384/\phi$, with a minimum modulation width of $1/\phi$.
1	The input clock is $\phi/4$. The conversion period is $32768/\phi$, with a minimum modulation width of $2/\phi$.

Note: Not usable in the H8/3612.

PWDRU—PWM Data Register U**H'CD****14-bit PWM**

Bit	7	6	5	4	3	2	1	0
	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDRU1	PWDRU0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Upper 6 Bits of Data for PWM Waveform Generation

Note: Not usable in the H8/3612.

PWDRL—PWM Data Register L**H'CE****14-bit PWM**

Bit	7	6	5	4	3	2	1	0
	PWDRL7	PWDRL6	PWDRL5	PWDRL4	PWDRL3	PWDRL2	PWDRL1	PWDRL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Lower 8 Bits of Data for PWM Waveform Generation

Note: Not usable in the H8/3612.

PDR0—Port Data Register 0**H'D0****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	PDR0 ₇	PDR0 ₆	PDR0 ₅	PDR0 ₄	PDR0 ₃	PDR0 ₂	PDR0 ₁	PDR0 ₀
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

PDR1—Port Data Register 1**H'D1****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	—	—	PDR1 ₅	PDR1 ₄	PDR1 ₃	PDR1 ₂	PDR1 ₁	PDR1 ₀
Initial value	— *	— *	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Pins P1₆ and P1₇ are input-only pins; whenever they are read, the pin level is read out.

PDR2—Port Data Register 2**H'D2****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	PDR2 ₇	PDR2 ₆	PDR2 ₅	PDR2 ₄	PDR2 ₃	PDR2 ₂	PDR2 ₁	PDR2 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR4—Port Data Register 4**H'D4****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	—	—	PDR4 ₅	PDR4 ₄	PDR4 ₃	PDR4 ₂	PDR4 ₁	PDR4 ₀
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

PDR8—Port Data Register 8**H'D8****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	PDR8 ₇	PDR8 ₆	PDR8 ₅	PDR8 ₄	PDR8 ₃	PDR8 ₂	PDR8 ₁	PDR8 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR9—Port Data Register 9**H'D9****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	PDR9 ₇	PDR9 ₆	PDR9 ₅	PDR9 ₄	PDR9 ₃	PDR9 ₂	PDR9 ₁	PDR9 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDRA—Port Data Register A**H'DA****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	PDRA ₇	PDRA ₆	PDRA ₅	PDRA ₄	PDRA ₃	PDRA ₂	PDRA ₁	PDRA ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCR1—Port Control Register 1**H'E1****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	—	—	PCR1 ₅	PCR1 ₄	PCR1 ₃	PCR1 ₂	PCR1 ₁	PCR1 ₀
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Port 1 I/O Select

0	Input port
1	Output port

PCR2—Port Control Register 2**H'E2****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	PCR2 ₇	PCR2 ₆	PCR2 ₅	PCR2 ₄	PCR2 ₃	PCR2 ₂	PCR2 ₁	PCR2 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 2 I/O Select

0	Input port
1	Output port

PCR8—Port Control Register 8**H'E8****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	PCR8 ₇	PCR8 ₆	PCR8 ₅	PCR8 ₄	PCR8 ₃	PCR8 ₂	PCR8 ₁	PCR8 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 8 I/O Select

0	Input port
1	Output port

PCR9—Port Control Register 9**H'E9****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	PCR9 ₇	PCR9 ₆	PCR9 ₅	PCR9 ₄	PCR9 ₃	PCR9 ₂	PCR9 ₁	PCR9 ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 9 I/O Select

0	Input port
1	Output port

PCRA—Port Control Register A**H'EA****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	PCRA ₇	PCRA ₆	PCRA ₅	PCRA ₄	PCRA ₃	PCRA ₂	PCRA ₁	PCRA ₀
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

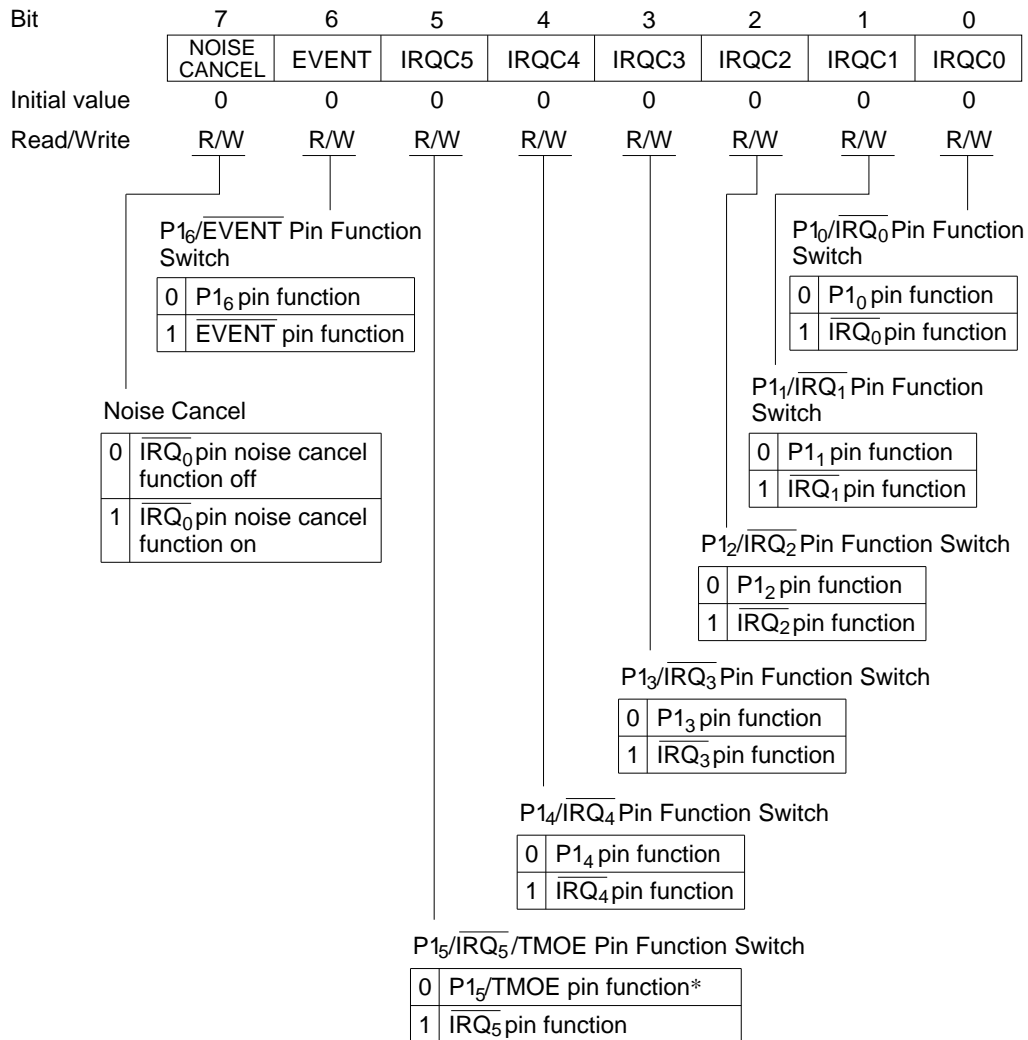
Port A I/O Select

0	Input port
1	Output port

PMR1—Port Mode Register 1

H'EB

I/O Ports

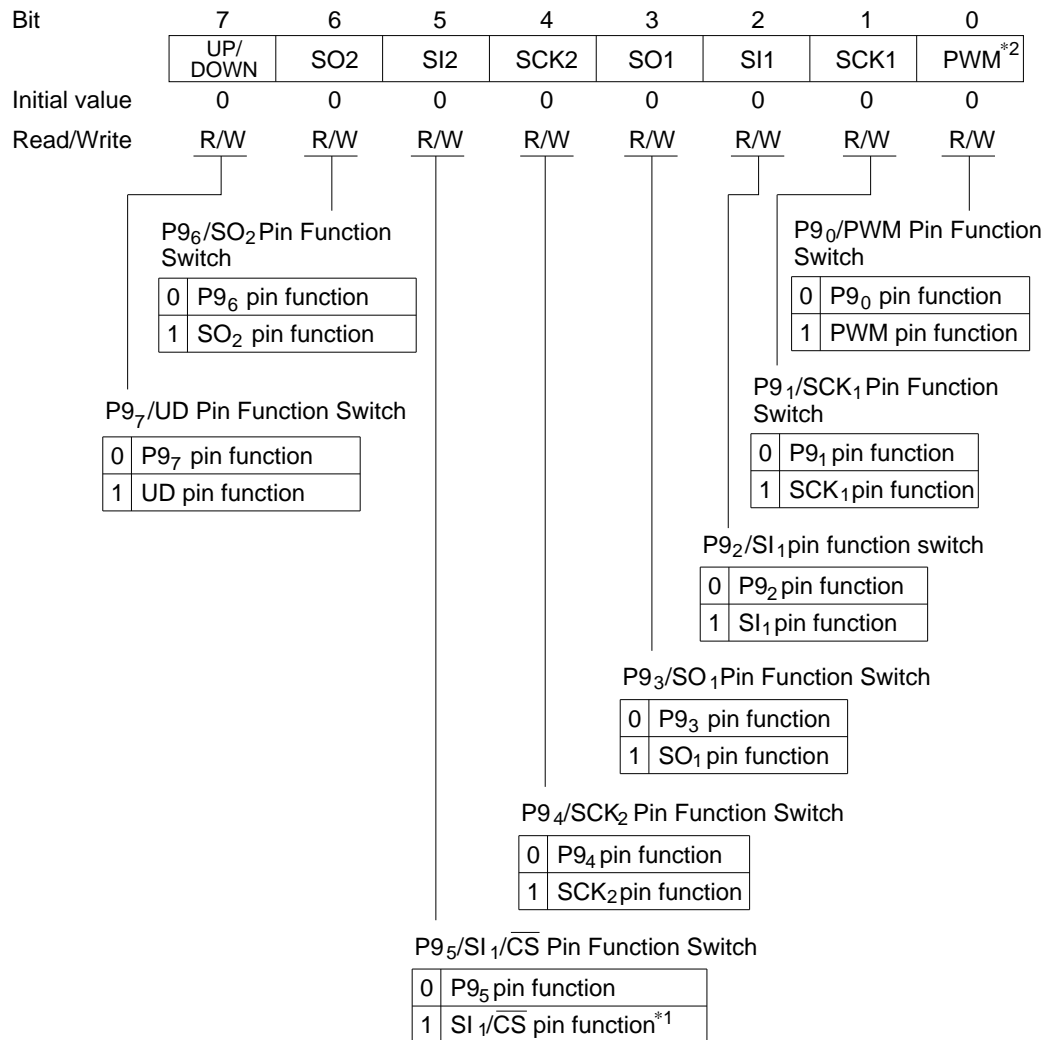


Note: * For the switching between P1₅ and TMOE pin functions see under PMR4.

PMR2—Port Mode Register 2

H'EC

I/O Ports



- Notes: 1. For the switching between SI₁ and $\overline{\text{CS}}$ pin functions see under PMR3.
2. Not usable (both read- and write-disabled) in the H8/3612.

PMR3—Port Mode Register 3

H'ED

I/O Ports

Bit	7	6	5	4	3	2	1	0
	—	SO2 PMOS	CS	—	SO1 PMOS	—	—	—
Initial value	1	0	0	1	0	1	1	1
Read/Write	—	R/W	R/W	—	R/W	—	—	—

SO₁ Pin PMOS On/Off

0	SO ₁ pin PMOS buffer on. CMOS output.
1	SO ₁ pin PMOS off. NMOS open-drain output.

Chip Select Output Select

PMR2 SI2	PMR3 CS	P9 ₅ /SI ₂ / $\overline{\text{CS}}$ pin function switch
0	0	P9 ₅ pin function
	1	
1	0	SI ₂ pin function
	1	$\overline{\text{CS}}$ pin function

SO₂ Pin PMOS On/Off

0	SO ₂ pin PMOS buffer on. CMOS output.
1	SO ₂ pin PMOS off. NMOS open-drain output.

PMR4—Port Mode Register 4**H'EE****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	TEO	TEO ON	FREQ	VRFR	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Timer E Output Control

PMR1	PMR4				P1 ₅ /IRQ ₅ /TMOE Pin Function Switch	Pin Status
IRQC5	TEO	TEO ON	FREQ	VRFR		
0	0	*	*	*	P1 ₅ pin function	Standard I/O port
0	1	0	*	*	TMOE pin function (off)	Low-level output
0	1	1	0	0	TMOE pin function (on)	Fixed-frequency output: $\phi/2048$
0	1	1	1	0	TMOE pin function (on)	Fixed-frequency output: $\phi/1024$
0	1	1	*	1	TMOE pin function (on)	Variable-frequency output: output toggles at each timer E overflow
1	*	*	*	*	IRQ ₅ pin function	External interrupt input

Note: * Don't care.

PMR0—Port Mode Register 0**H'EF****I/O Ports**

Bit	7	6	5	4	3	2	1	0
	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Analog Input Select

0	POn input pin
1	ANn input pin

(n = 7 to 0)

SYSCR1—System Control Register 1
H'F0
System Control

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	LSON	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W ^{*1}	R/W	R/W	R/W	R/W	R/W	—	—

Standby Timer Select

0	0	0	Wait time = 8,192 states
0	0	1	Wait time = 16,384 states
0	1	0	Wait time = 32,768 states
0	1	1	Wait time = 65,536 states
1	*3	*3	Wait time = 131,072 states

Low-Speed on Flag ^{*2}

0	CPU runs on system clock (\emptyset)
1	CPU runs on subclock (\emptyset_{SUB})

Standby

0	Sleep mode entered after SLEEP instruction is executed.
1	Standby mode or watch mode entered after SLEEP instruction is executed.

- Notes:
1. Write is enabled in active mode only.
 2. This relates to the transitions between operation modes, so functioning depends on the combination of this bit with other control bits and interrupts. For details see 3.3, System Modes.
 3. Don't care.

SYSCR2—System Control Register 2
H'F1
System Control

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	DTON	—	—	—
Initial value	1	1	1	1	0	1	0	0
Read/Write	—	—	—	—	W*	—	R/W	R/W

Direct Transfer On Flag

0	In subactive mode, watch mode is entered when a SLEEP instruction is executed.
1	In subactive mode, if LSON bit = 0, active mode is entered via watch mode when a SLEEP instruction is executed.

Note: * Write is enabled in subactive mode only.

IEGR—IRQ Edge Select Register**H'F2****System Control**

Bit	7	6	5	4	3	2	1	0
	—	—	—	IEG4	—	—	IEG1	IEG0
Initial value	1	1	1	0	1	1	0	0
Read/Write	—	—	—	R/W	—	—	R/W	R/W

IRQ₄ Input Edge Select

0	Falling edge detected.
1	Rising edge detected.

IRQ₀ Input Edge Select

0	Falling edge detected.
1	Rising edge detected.

IRQ₁ Input Edge Select

0	Falling edge detected.
1	Rising edge detected.

IENR1—Interrupt Enable Register 1**H'F3****System Control**

Bit	7	6	5	4	3	2	1	0
	—	—	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

IRQ₅ Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

IRQ₄ Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

IRQ₃ Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

IRQ₂ Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

IRQ₁ Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

IRQ₀ Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

IENR2—Interrupt Enable Register 2**H'F4****System Control**

Bit	7	6	5	4	3	2	1	0
	—	—	IENDT	IENTE	IENDT	IENTC	IENTB	IENTA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DTON Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Timer E Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Timer D Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Timer C Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Timer B Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

Timer A Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

IENR3—Interrupt Enable Register 3**H'F5****System Control**

Bit	7	6	5	4	3	2	1	0
	IENAD	—*	—	—	—	—	IENS2	IENS1
Initial value	0	0	1	1	1	1	0	0
Read/Write	R/W	—	—	—	—	—	R/W	R/W

A/D Conversion Complete Interrupt Enable

0	Interrupts disabled.
1	Interrupts enabled.

SCI1 Interrupt Enable

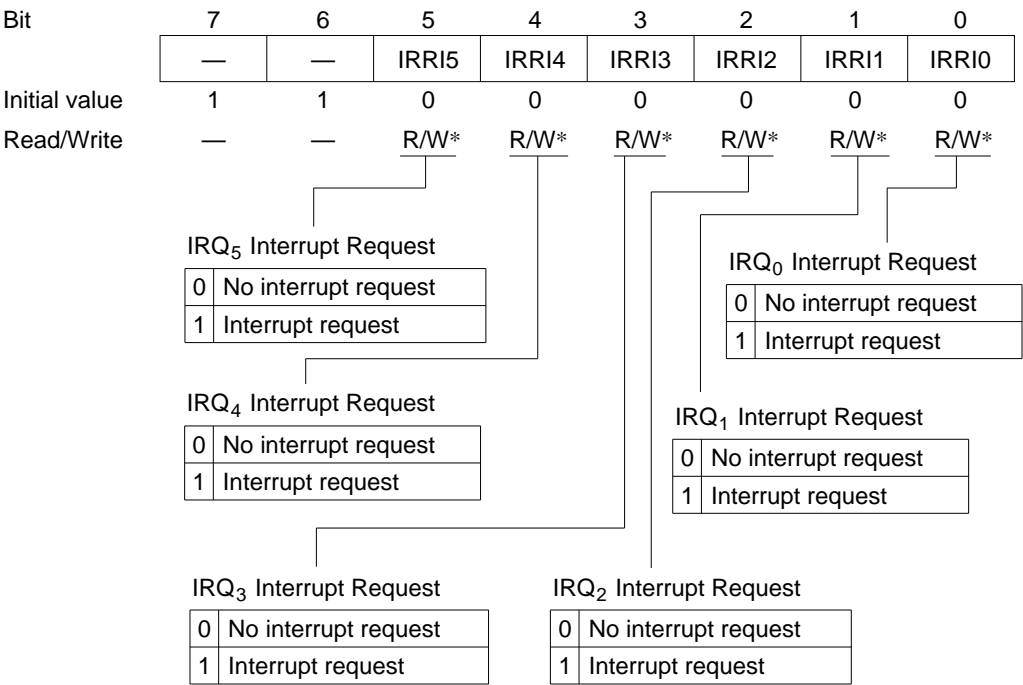
0	Interrupts disabled.
1	Interrupts enabled.

SCI2 Interrupt Enable

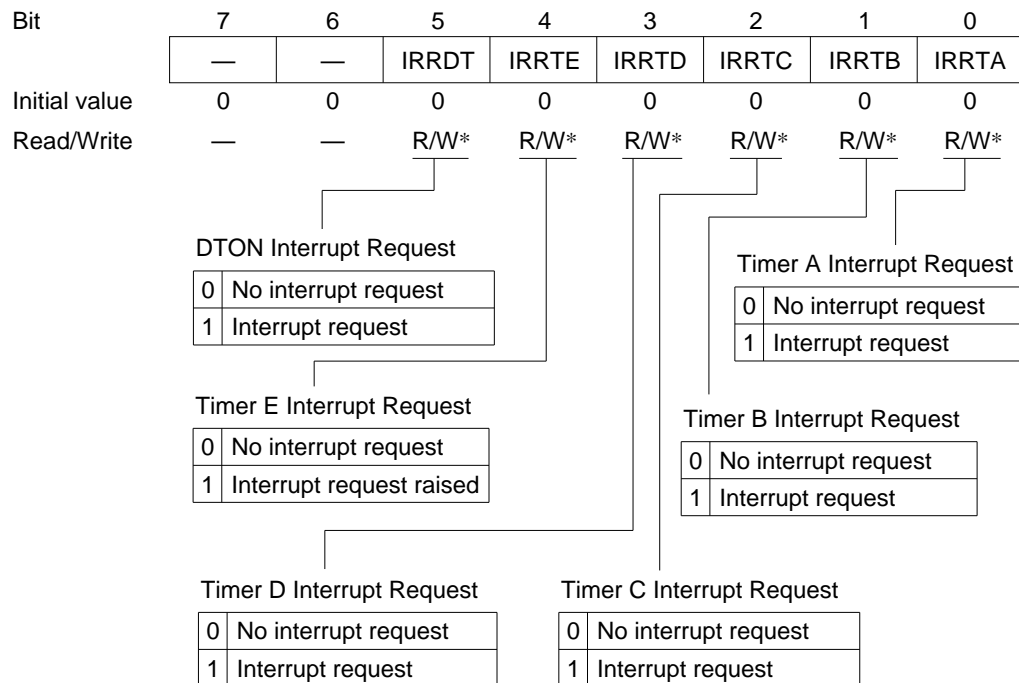
0	Interrupts disabled.
1	Interrupts enabled.

Note: * Read- and write-enabled. Always write 0 in this bit.

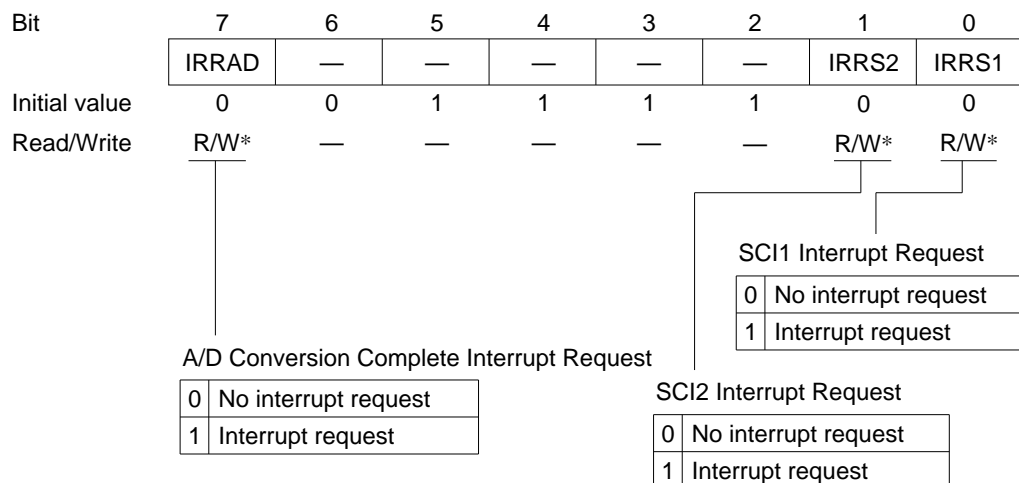
IRR1—Interrupt Request Register 1 **H'F6** **System Control**



Note: * Only 0 can be written, to clear the flag.

IRR2—Interrupt Request Register 2**H'F7****System Control**

Note: * Only 0 can be written, to clear the flag.

IRR3—Interrupt Request Register 3**H'F8****System Control**

Note: * Only 0 can be written, to clear the flag.

Appendix C I/O Port Block Diagrams

C.1 Port 0 Block Diagram

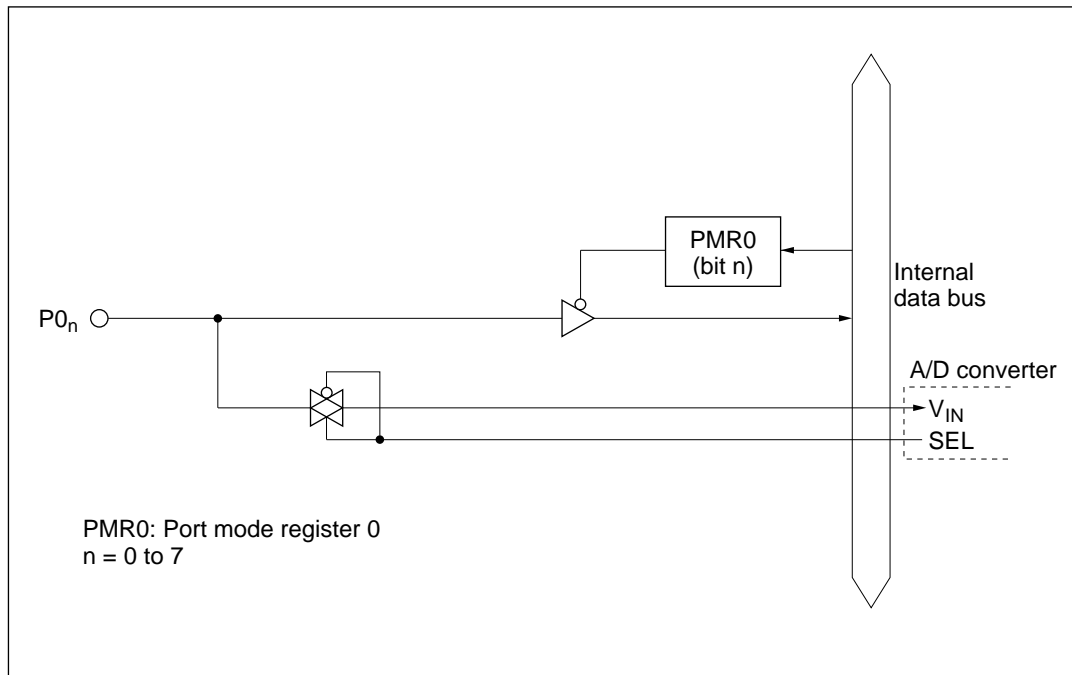


Figure C-1 Port 0 Block Diagram

C.2 Port 1 Block Diagram

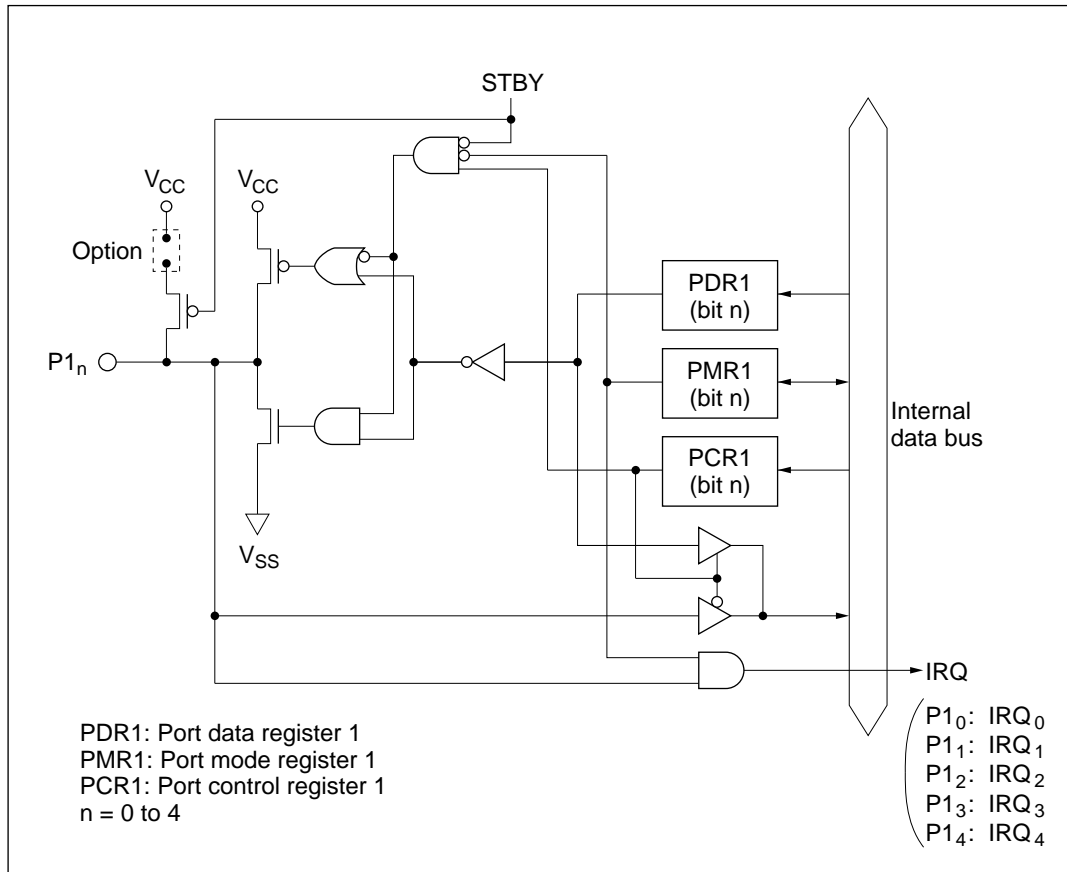


Figure C-2 (a) Port 1 Block Diagram (Pins $P1_0$ to $P1_4$)

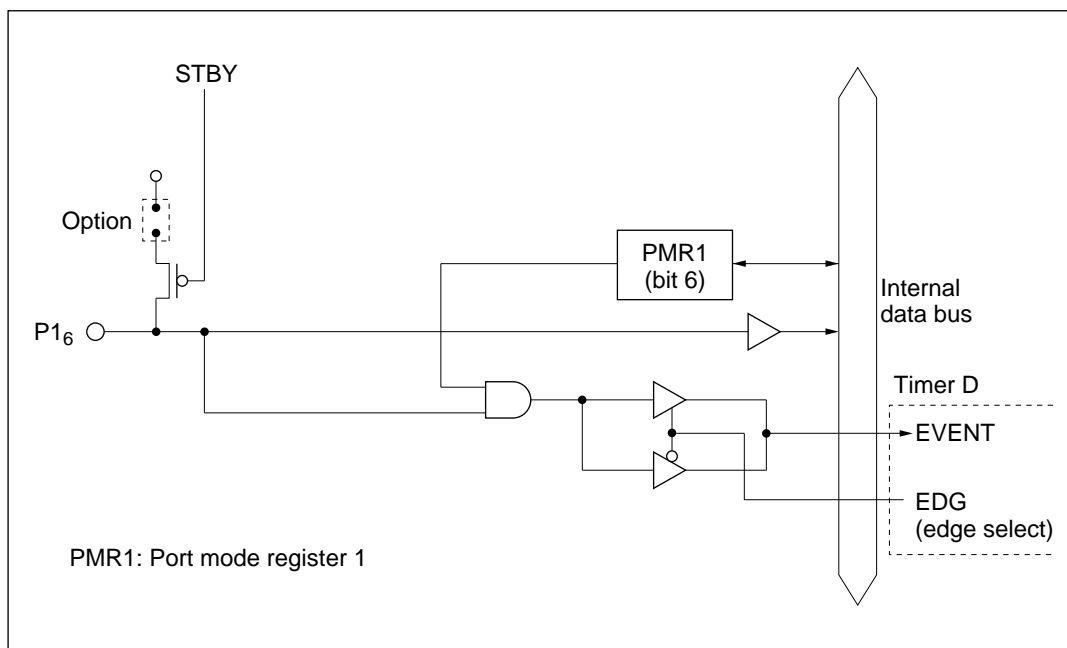


Figure C-2 (c) Port 1 Block Diagram (Pin P1₆)

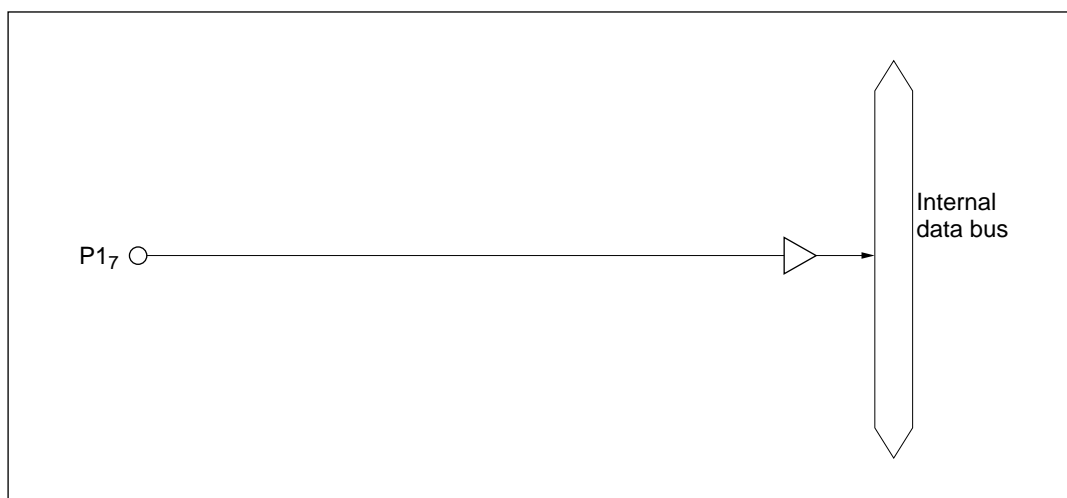


Figure C-2 (d) Port 1 Block Diagram (Pin P1₇)

C.3 Port 2 Block Diagram

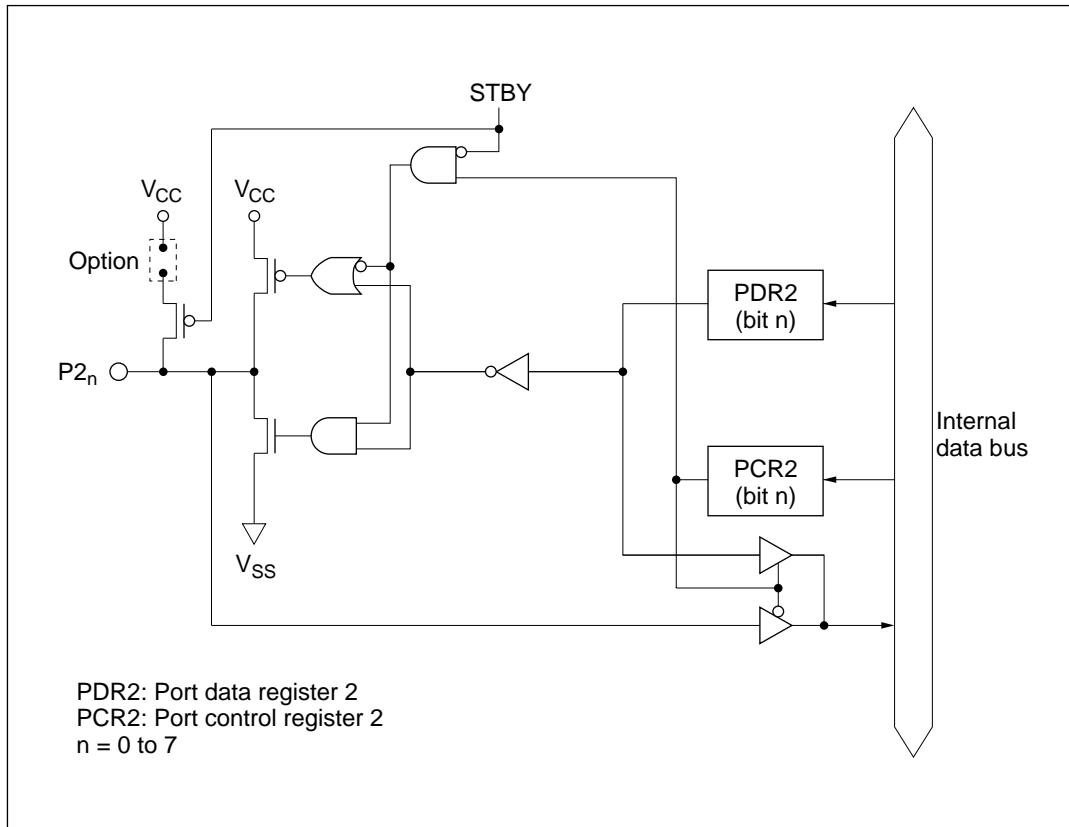


Figure C-3 Port 2 Block Diagram

C.4 Port 4 Block Diagram

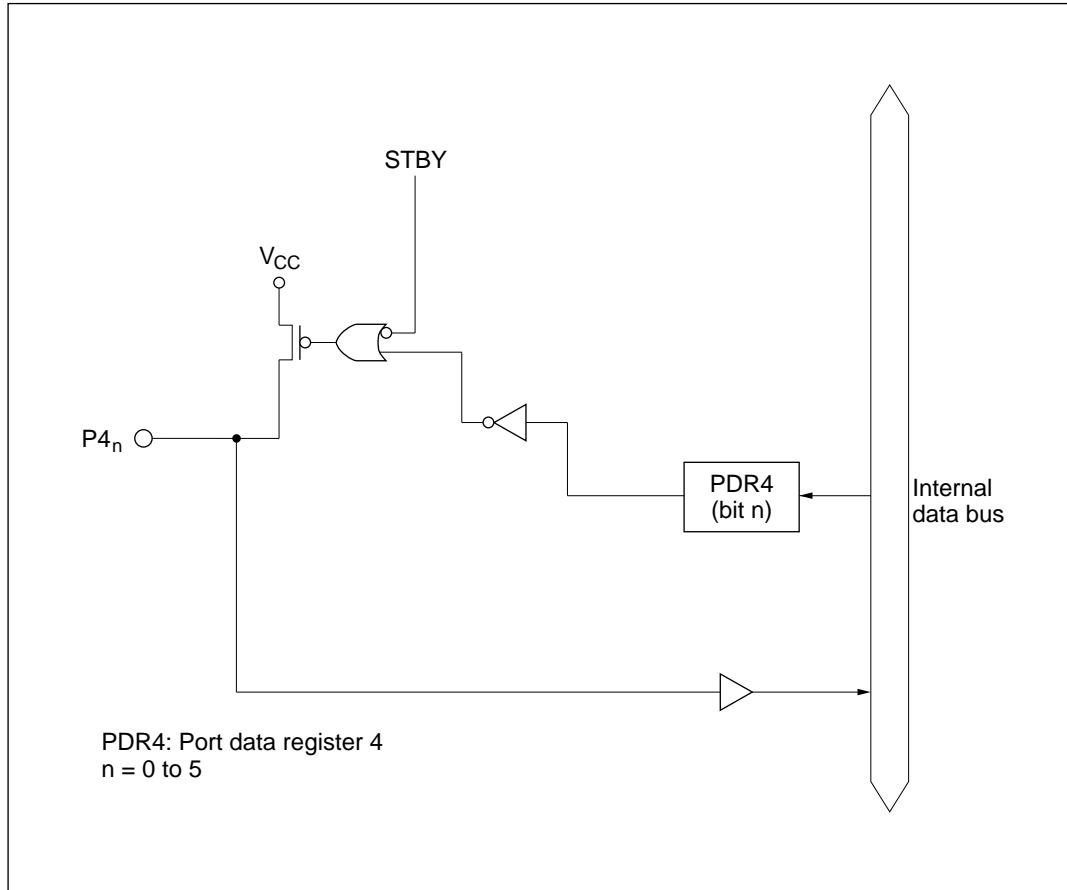


Figure C-4 Port 4 Block Diagram

C.5 Port 8 Block Diagram

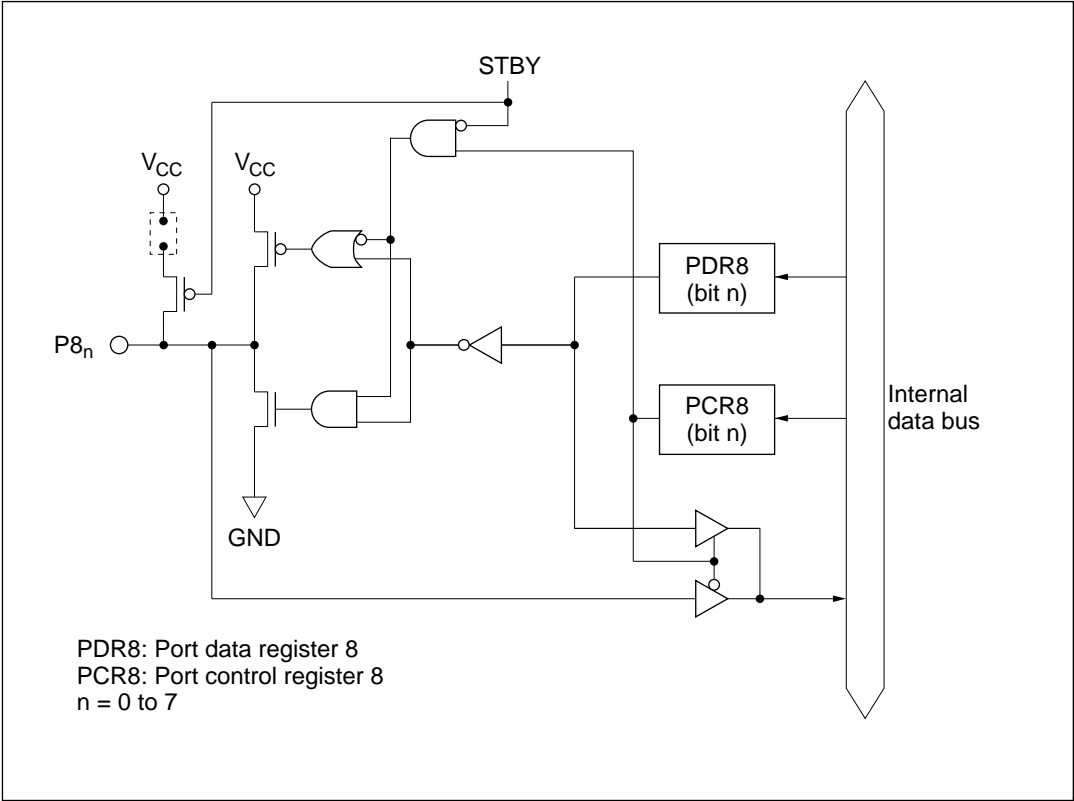


Figure C-5 Port 8 Block Diagram

C.6 Port 9 Block Diagram

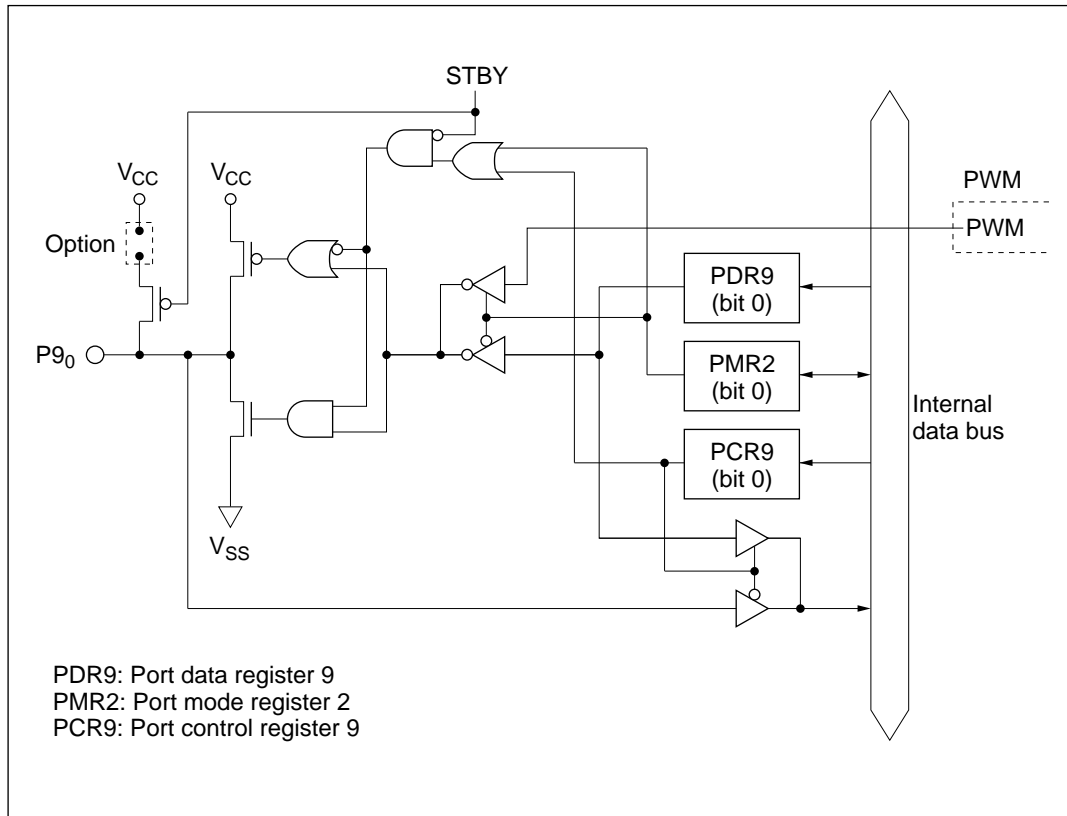


Figure C-6 (a) Port 9 Block Diagram (Pin P9₀)

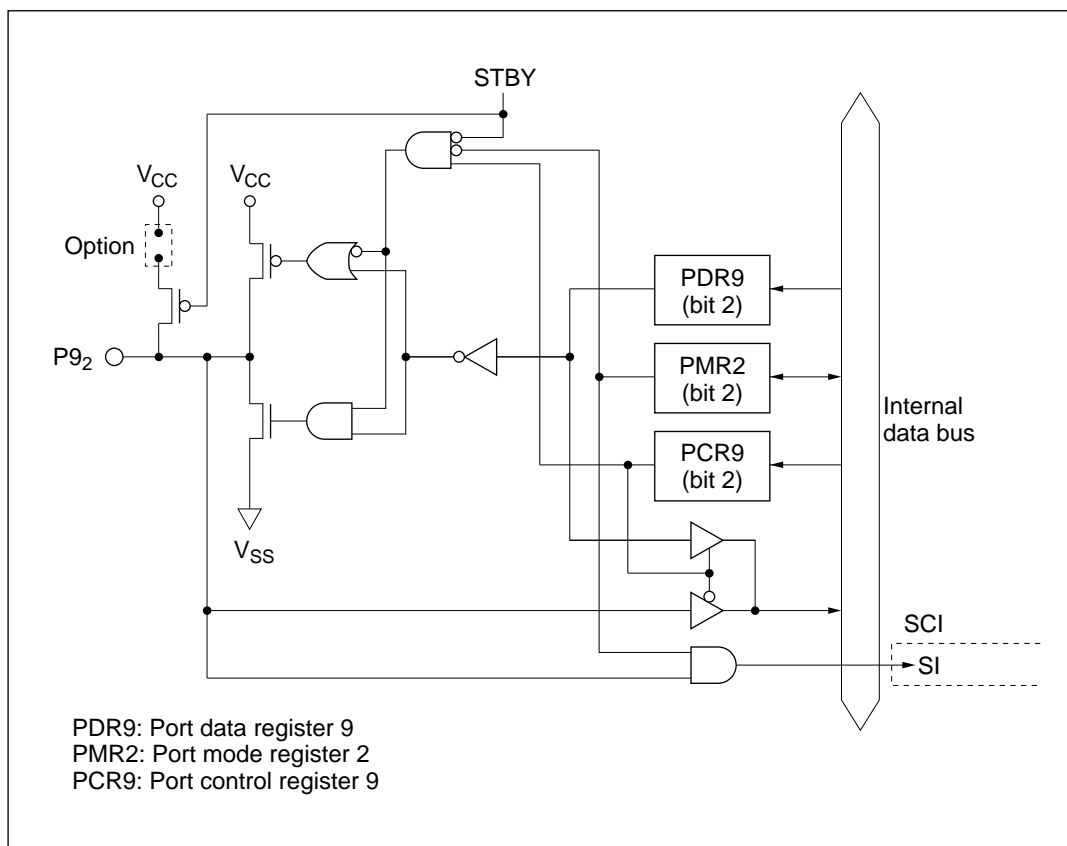


Figure C-6 (c) Port 9 Block Diagram (Pin P9₂)

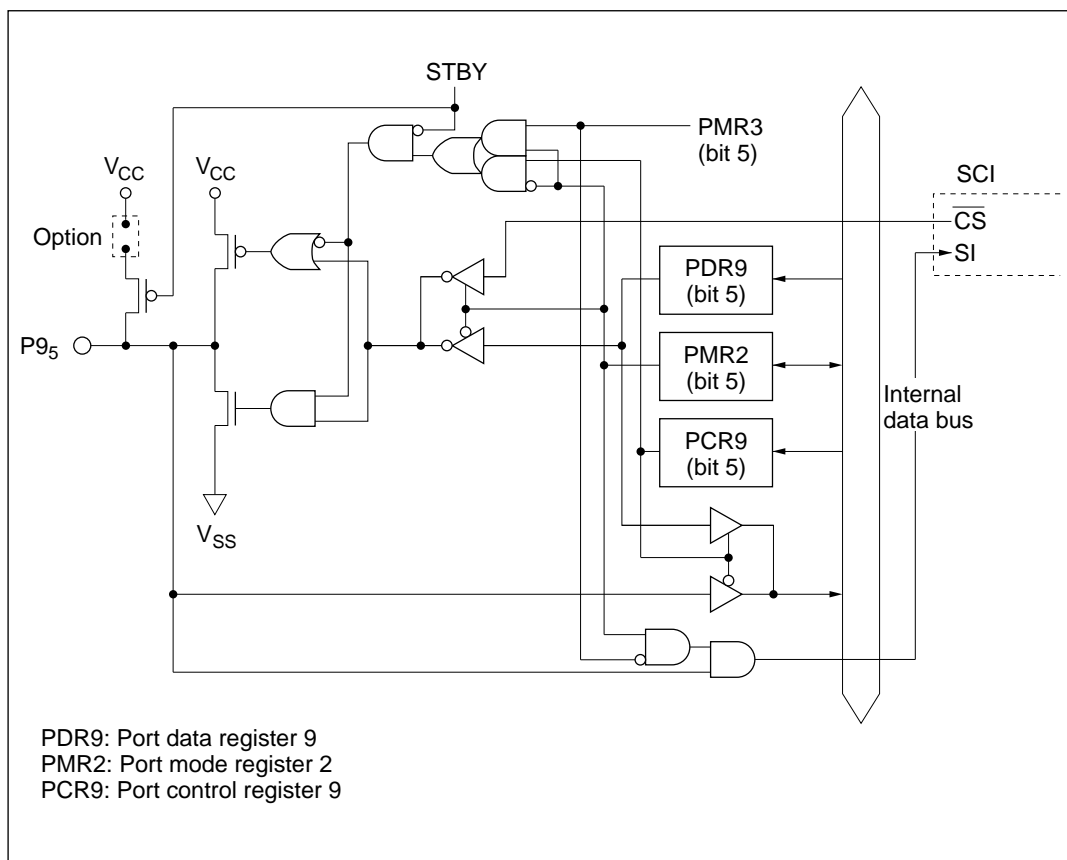


Figure C-6 (e) Port 9 Block Diagram (Pin P9₅)

C.7 Port A Block Diagram

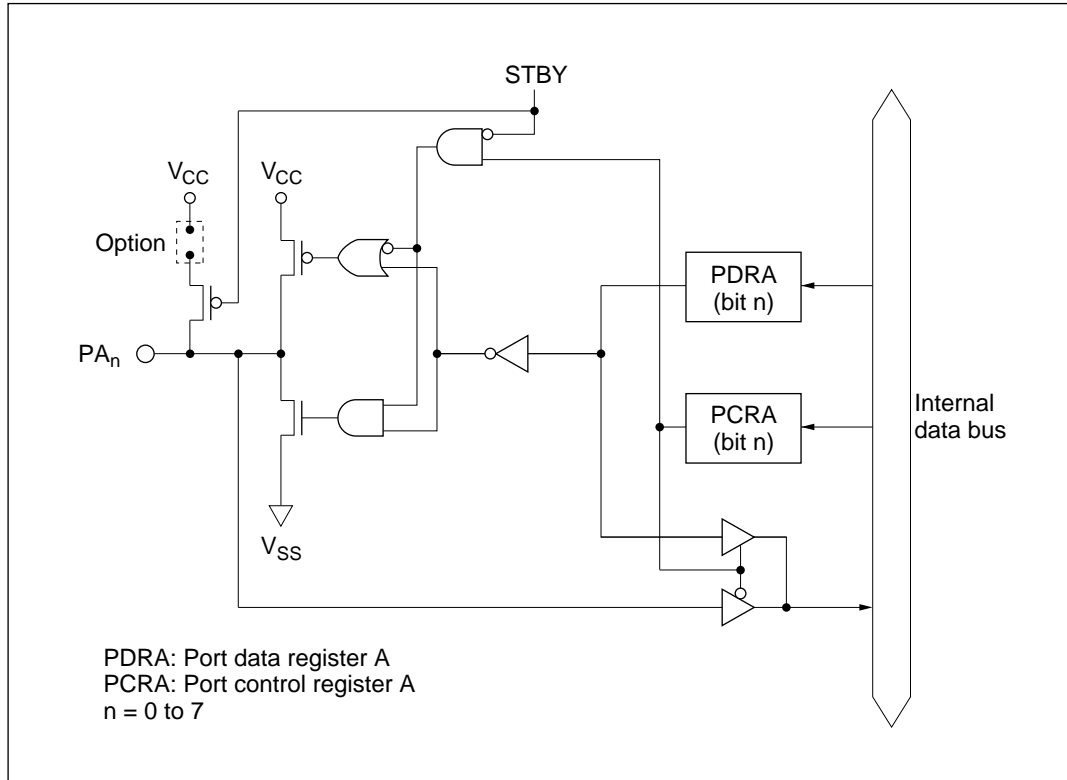


Figure C-7 Port A Block Diagram

Appendix D Port States in Each Processing State

Table D-1 Port States

Port Pins	Reset	Mode				
		Sleep	Standby	Watch	Subactive	Active
P0 ₇ to P0 ₀	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Input port
P1 ₇	Hi-z	Hi-z	Hi-z	Hi-z	Hi-z	Input port
P1 ₆	Hi-z or pull-up	Hi-z or pull-up	Hi-z	Hi-z	Hi-z	Input port
P1 ₅ to P1 ₀	Hi-z or pull-up	prev. state	Hi-z	Hi-z	Hi-z	I/O port
P4 ₅ to P4 ₀	Hi-z	prev. state	Hi-z	Hi-z	Hi-z	I/O port
P2 ₇ to P2 ₀	Hi-z or pull-up	prev. state	Hi-z	Hi-z	Hi-z	I/O port
P8 ₇ to P8 ₀	Hi-z or pull-up	prev. state	Hi-z	Hi-z	Hi-z	I/O port
P9 ₇ to P9 ₀	Hi-z or pull-up	prev. state	Hi-z	Hi-z	Hi-z	I/O port
PA ₇ , to PA ₀	Hi-z or pull-up	prev. state	Hi-z	Hi-z	Hi-z	I/O port

Notation:

Hi-z: High-impedance state

Prev. state: Input pins are in high-impedance state. Output pins hold their previous output.

Hi-z or pull-up: Standard ports for which the pull-up MOS mask option is chosen are in pull-up state; ports without the pull-up MOS option are in high-impedance state.

- Notes:
1. When pull-up MOS is chosen as a mask option with standard ports, the pull-ups are always on in active mode and sleep mode, regardless of the port control register (PCR) and port data register (PDR) settings. The pull-ups are off in power-down modes other than sleep mode.
 2. The input gates of pins selected for peripheral function input remain on even in power-down modes. This means the input levels must be fixed in order to avoid increased power dissipation.

Appendix E List of Mask Options

HD6433612, HD6433613, and HD6433614

Please indicate the selected specifications by marking the appropriate box (with an × or √ mark). The shaded boxes cannot be selected.

(1) I/O Options

B: With MOS pull-up

C: No MOS pull-up

Date of order	, 19	
Company		
Address		
Name		
ROM code name		
LSI model no.	<input type="checkbox"/> HD6433612	<input type="checkbox"/> HD6433613
	<input type="checkbox"/> HD6433614	

Pin	I/O	I/O option	
		B	C
P1 ₀ /IRQ ₀	I/O		
P1 ₁ /IRQ ₁	I/O		
P1 ₂ /IRQ ₂	I/O		
P1 ₃ /IRQ ₃	I/O		
P1 ₄ /IRQ ₄	I/O		
P1 ₅ /TMOE/IRQ ₅	I/O		
P1 ₆ /EVENT	I		
P1 ₇	I		
P2 ₀	I/O		
P2 ₁	I/O		
P2 ₂	I/O		
P2 ₃	I/O		
P2 ₄	I/O		
P2 ₅	I/O		
P2 ₆	I/O		
P2 ₇	I/O		

Pin	I/O	I/O option	
		B	C
P8 ₀	I/O		
P8 ₁	I/O		
P8 ₂	I/O		
P8 ₃	I/O		
P8 ₄	I/O		
P8 ₅	I/O		
P8 ₆	I/O		
P8 ₇	I/O		
P9 ₀ /PWM*	I/O		
P9 ₁ /SCK ₁	I/O		
P9 ₂ /SI ₁	I/O		
P9 ₃ /SO ₁	I/O		
P9 ₄ /SCK ₂	I/O		
P9 ₅ /SI ₂	I/O		
P9 ₆ /SO ₂	I/O		
P9 ₇ /UD	I/O		
PA ₀	I/O		
PA ₁	I/O		
PA ₂	I/O		
PA ₃	I/O		
PA ₄	I/O		
PA ₅	I/O		
PA ₆	I/O		
PA ₇	I/O		

(2) P4₀ to P4₅ are PMOS open-drain pins.

(3) Package

<input type="checkbox"/> FP-64A
<input type="checkbox"/> DP-64S

(4) Oscillator at OSC₁ and OSC₂

<input type="checkbox"/> Crystal oscillator	f _{OSC} =	MHz
<input type="checkbox"/> Ceramic oscillator	f _{OSC} =	MHz
<input type="checkbox"/> External clock	f _{OSC} =	MHz

(5) Oscillator at X₁ and X₂

<input type="checkbox"/> Used	f _x = 32.768 kHz
<input type="checkbox"/> Not used	X ₁ = V _{CC}

Note: * The H8/3612 does not have a pulse width modulator.

Notes: 1. The wide temperature range specification and I specification are special specifications. There is no J specification for these products. Please contact your local Hitachi representative for details.
2. ROM data submitted in an EPROM must be written starting from address H'0000 in accordance with the memory map of the particular microcontroller. For data outside the ROM area on the memory map use H'FF.

Appendix F Package Dimensions

Figures F-1 and F-2 show the external dimensions of the FP-64A and DP-64S packages, respectively, for H8/3614 Series.

Unit: mm

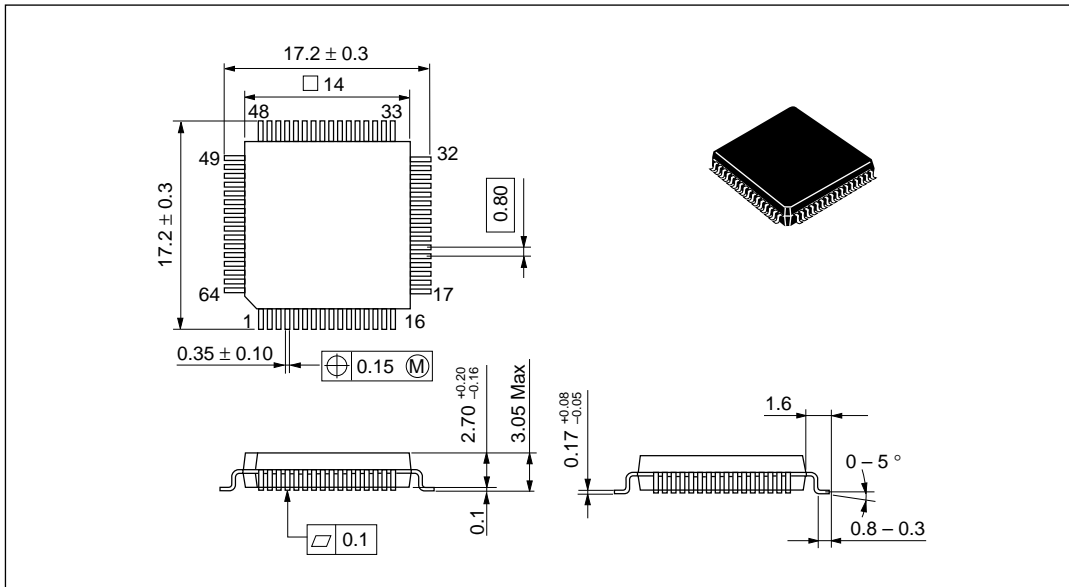


Figure F-1 External Dimensions (FP-64A)

Unit: mm

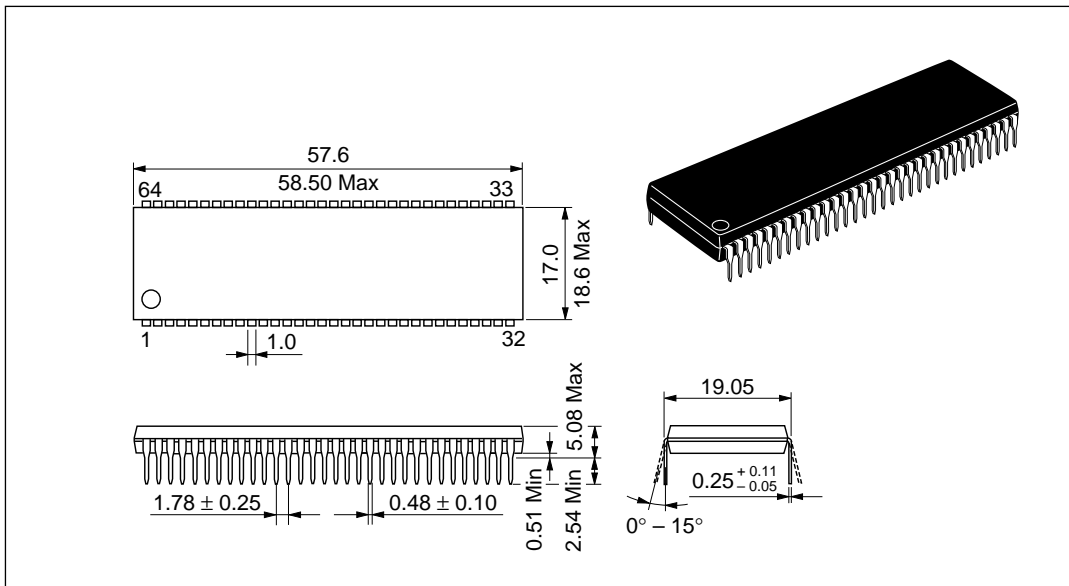


Figure F-2 External Dimensions (DP-64S)

