Hitachi America, Ltd.

Application Note

H8/510

Amelia Lam

H8/510 PWM Waveform generation

INTRODUCTION

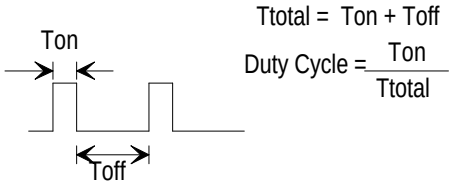


Fig. 1 PWM waveform

Pulse Width Modulation is typically used in stepping motor control, tone generation, disk recording or even A/D conversion application. It is expressed in terms of duty cycle, which is the period of T_{on} as a percentage of the T_{total} (Fig. 1). Here T_{on} is the duration that has positive pulse voltage, and Toff is the duration that has zero voltage. And Ttotal is the sum of Ton + Toff.

Hence by varying the duty cycle, the power of the signal will be modulated. This in turn is controls the speed of the stepping motor in the hard disk drive or the automotive engine environment, or controls the loudness of the tone generation to a speaker. The on-chip timer in the H8/510 device can be used to generate the pulse width modulated signal. This appnote is to discuss how the PWM is implemented, the result is also tested on an 8Ω speaker which generates different tone according to the preassigned duty cycle.

H8/510 MICROCONTROLLER

Hitachi's H8/510 is a CMOS microcomputer with 16-bit architecture. The on-chip peripheral modules include Timers, Serial Communication Interface (SCI), Refresh Controller, Bus Controller, A/D converter and I/O ports. Although there are three timers to provide input capture and output compare functions, there is not a designated timer to perform Pulse Width Modulation as in the H8/53X device. However, this feature can be implemented with the on-chip 8-bit Timer using match A and match B condition.

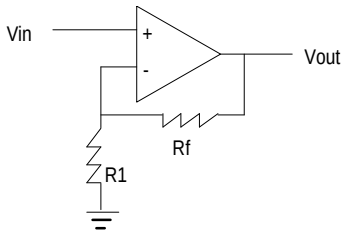
In this demo, the clock source to the 8-bit timer is chosen as $\phi/64$ while the system clock is running at 9.834MHz. Therefore, the timer is incremented every 6.5μs since the period of the prescaled clock is

$$1 / 9.834\text{MHz} \div 64$$

Both output compare match A and output compare match B are used so that the timer output (TMO) will change to the specified logic level on each match condition. The Time Constant Registers A & B (TCORA & TCORB) are programmed with values in order to produce the desired Ton and Toff.

HARDWARE CONSIDERATION

The TMO is connected to a speaker so that the variation in the duty cycle can be exemplified by the variation in the tones generated. The one used in this demo is an 8Ω, 0.2W speaker. For connection, an audio power amplifier LM386 is placed in between the speaker and the TMO to avoid the excessive loading by the speaker itself. A 5K resistor is placed in the feedback loop so that when coupled with the 1K resistor at the inverting input, the amplifier provides a gain of 6. This is true since:



$$\text{gain (G)} = 1 + \frac{Rf}{R1}$$

The inclusion of the 4.7uF capacitor in the feedback loop is to reduce the dc offset. The complete circuit is shown in Fig. 2

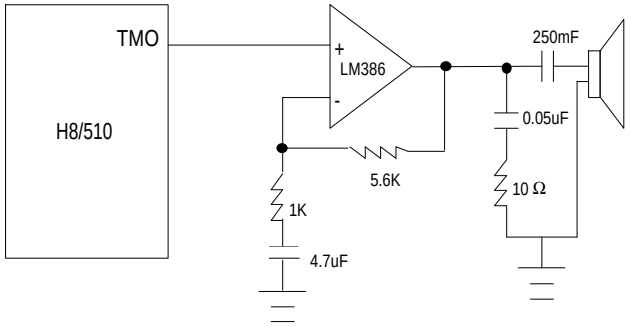


Fig. 2 Connection between speaker and H8/510

SOFTWARE CONSIDERATION

The program has labels designated for five duty cycles as follows:

D20:	20%
D40	40%
D50	50%
D60	60%
D80	80%

The logic level is set to one when match B condition occurs and the logic level is returned to zero when match A occurs. Hence the output select bit 3-0 of TCSR is programmed as 1001 respectively. On the other hand, the timer counter is cleared depending on the duty cycle assigned. Normally, it will be cleared on compare match A condition if TCORA has a larger value than TCORB. The two bits to control the counter clearing are CCLR1 & CCLR0 of the TCR.

The program is designed in such a way that the duty cycle starts off from 20% and increases as the shown in the sequence above. Each duty cycle will cause the speaker to generate a tone which lasts about 5 seconds. After that, the speaker will be turned off for another 5s and then genearte a different tone for 5s and so on.

The interrupt request on the Compare match A & B are enabled by setting the CMIEA & CMIEB bits to one. On each interrupt, the compare match flag (CMFA or CMFB) is cleared for the next match condition.

DUTY CYCLE CALCULATION

The frequency of the tone is fixed at 2000Hz which thus has a period of 500µs. For a 20% duty cycle, Ton will be 100µs and Toff will be 400µs. As each timer counter is updated at a rate of 6.5µs, Ton requires a total count of:

Count (Ton) = 100 ÷ 6.5 ≈ 15 (0FH)

Count (Toff) = 400 ÷ 6.5 ≈ 62 (3EH)

Therefore the value 0FH is programmed into TCORA and 4DH (3E + 0F) is programmed into TCORB to allow a waveform of 20% duty cycle to be generated. Similiar calculation is applied to the rest of the other cycles. Refer to Fig. 3 for the information on how the match condition is used in varying duty cycles.

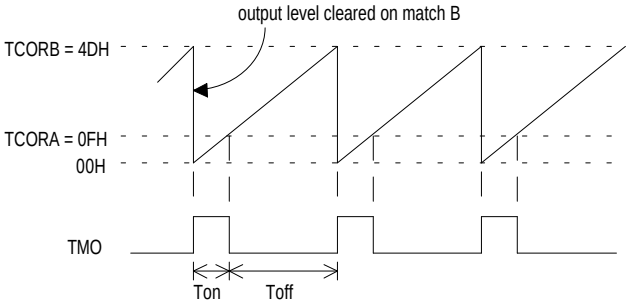


Fig. 3 Timer output on match condition

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APPENDIX A

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Command line:  c:\devtool\h8mri\ASMH85.EXE -o 510pwm.obj -l 510pwm.src
Line Address
                                          ; This program is to generate the PWM pulse from one of the H8/510
                                         ; FRT Timers.  The code will be debugged from the H8/510 eval board.
                                         ; The system clock for this eval board is running at 9.834MHz
                                         ;
                                         ; Program : 510pwm.doc
                                        ; Date : 12/1/93
                                         ; By : Amelia Lam
                                         ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                                                 .SECTION        CODE1,TEXT,LOCATE=H'1000
     000000C4       TCNT      .EQU      H'C4
     000000C0       TCR       .EQU      H'C0
     000000C1       TCSR      .EQU      H'C1
     000000C2       TCORA     .EQU      H'C2
     000000C3       TCORB     .EQU      H'C3
     00000002       IPRC      .EQU      H'02
                                         ; To initialize the 510 FRT
                                         ;;;;;;;;;;;;;;;;;;;;;;;;;;
     00001000 04 00 8F   TINI:  LDC.B     #H'00,TP            ; set the stack pointer
     00001003 5F 22 30          MOV.W     #H'2230,SP
     00001006 04 00 8D          LDC.B     #H'00,DP
     00001009 04 00 8C          LDC.B     #H'00,EP
     0000100C 0C 06 00 88       LDC.W     #H'0600,SR
     00001010 04 FF 8B          LDC.B     #H'FF,BR
     00001013 05 02 06 70       MOV.B     #H'70,@IPRC:8
     00001017 04 FE 8B          LDC.B     #H'FE,BR
     0000101A 05 C1 06 09       MOV.B     #H'09,@TCSR:8       ; 1 to matchB, 0 to matchA
    0000101E 05 C2 06 0F D20:   MOV.B     #H'0F,@TCORA:8      ; 20% duty cycle
     00001022 05 C3 06 4D       MOV.B     #H'4D,@TCORB:8
     00001026 05 C0 06 D2       MOV.B     #H'D2,@TCR:8
     0000102A 1E 00 6A          BSR       DLY
     0000102D 05 C0 06 00       MOV.B     #H'00,@TCR:8
     00001031 1E 00 63          BSR       DLY
    00001034 05 C2 06 1F D40:   MOV.B     #H'1F,@TCORA:8      ; 40% duty cycle
     00001038 05 C3 06 4D       MOV.B     #H'4D,@TCORB:8
     0000103C 05 C0 06 D2       MOV.B     #H'D2,@TCR:8
     00001040 1E 00 54          BSR       DLY
     00001043 05 C0 06 00       MOV.B     #H'00,@TCR:8
     00001047 1E 00 4D          BSR       DLY
    0000104A 05 C2 06 4D D50:   MOV.B     #H'4D,@TCORA:8      ; 50% duty cycle
     0000104E 05 C3 06 26       MOV.B     #H'26,@TCORB:8
     00001052 05 C0 06 CA       MOV.B     #H'CA,@TCR:8        ; intr enabled, clear on A
     00001056 1E 00 3E          BSR       DLY                 ; clk source = /64
     00001059 05 C0 06 00       MOV.B     #H'00,@TCR:8
     0000105D 1E 00 37          BSR       DLY
    00001060 05 C2 06 4D D60:   MOV.B     #H'4D,@TCORA:8      ; 60% duty cycle
     00001064 05 C3 06 1F       MOV.B     #H'1F,@TCORB:8
     00001068 05 C0 06 CA       MOV.B     #H'CA,@TCR:8
     0000106C 1E 00 28          BSR       DLY
     0000106F 05 C0 06 00       MOV.B     #H'00,@TCR:8
    00001073 1E 00 21           BSR       DLY
   00001076 05 C2 06 4D  D80:   MOV.B     #H'4D,@TCORA:8      ; 80% duty cycle

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Line Address
     0000107A 05 C3 06 0F       MOV.B     #H'0F,@TCORB:8
     0000107E 05 C0 06 CA       MOV.B     #H'CA,@TCR:8
     00001082 1E 00 12          BSR       DLY
     00001085 05 C0 06 00       MOV.B     #H'00,@TCR:8
     00001089 1E 00 0B          BSR       DLY
     0000108C 10 10 1E   COUNT: JMP       @D20
                                         ; Compare match interrupt
                                         ;;;;;;;;;;;;;;;;;;;;;;;;
     0000108F 05 C1 D6   MATA:  BCLR.B    #6,@TCSR:8           ; clear CMFA bit
     00001092 0A                RTE
     00001093 05 C1 D7   MATB:  BCLR.B    #7,@TCSR:8          ; clear CMFB bit
     00001096 0A                RTE
     00001097 54 08      DLY:   MOV.B     #8,R4               ; delay for 5s
     00001099 5B FF FF   DLY1:  MOV.W     #H'ffFF,R3
    0000109C 0C 00 01 33 DLY2:  SUB.W     #1,R3
     000010A0 0C 00 01 BB       DIVXU.W   #1,R3
     000010A4 0C 00 01 AB       MULXU.W   #1,R3
     000010A8 26 F2             BNE       DLY2
     000010AA 0C 00 01 34       SUB.W     #1,R4
     000010AE 26 E9             BNE       DLY1
     000010B0 19                RTS
                                         ; To set up the interrupt vector
                                         ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                                        .SECTION        TABLE1,DATA,LOCATE=H'0000
                                         .ORG    H'0000
     00000000 00 00 10 00                .DATA.L TINI
                                        .ORG    H'00C0
```

```
93   000000C0 00 00 10 8F     CMIA      .DATA.L MATA
94   000000C4 00 00 10 93     CMIB      .DATA.L MATB
95
96                                          .END

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                  Cross Reference

Label            Value         References

CMIA            000000C0      -93
CMIB            000000C4      -94
COUNT        0000108C       -63
D20               0000101E        -32  63
D40               00001034       -38
D50               0000104A       -44
D60               00001060       -50
D80               00001076        -56
DLY               00001097        35  37  41  43  47  49  53  55  59  61  -74
DLY1              00001099        -75  81
DLY2             0000109C      -76  79
IPRC              00000002       -17  28
MATA           0000108F       -68  93
MATB           00001093       -71  94
TCNT             00000C4        -12
TCORA         000000C2      -15  32  38  44  50  56
TCORB         000000C3      -16  33  39  45  51  57
TCR               000000C0       -13  34  36  40  42  46  48  52  54  58  60
TCSR            000000C1       -14  31  68  71
TINI                00001000       -22  90

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                  Section Table

Section      Attribute   Size              Start

CODE1        ABS-TEXT     00B1              00001000
TABLE1       ABS-DATA    00C8            00000000


 Errors: 0, Warnings: 0
```


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