Hitachi America, Ltd.

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Application Engineering
TechNote

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Interfacing PSRAM devices to the H8/3003

PSRAMs combine the desirable characteristics of DRAMs (low cost and high density) and SRAMS (simpler circuit interface through direct addressing). Just like DRAMs, they require periodic refresh cycles through a dedicated input pin (RFSH-), but not through the RAS- and CAS- signals.

The Refresh Controller module of the H8/3003 allows PSRAMs to be easily connected to external memory area 3 of the microcontroller via the chip select line CS3-, and provides the refresh signal through a simple connection between the RFSH- pin of the H8/3003 and the corresponding pin on the memory device. Regardless of which operating mode is used, the memory data path size (either 8- or 16-bit wide) as well as the length of the access and refresh cycles can be set in the Bus Controller module registers ABWCR and ASTCR. The relationship between memory area 3 settings in the ABWCR and ASTCR, access cycles, and refresh cycles is indentical to the DRAM case, and is illustrated in table 7-4 in the H8/3003 Hardware Manual. Figures 1 and 2 show generic connections between the H8/3003 and PSRAMs for both 8-bit and 16-bit data modes. Please note that some PSRAMs have separate OE- and RFSH- pins; in this case, the RD- line from the H8/3003 should be connected to the OE- pin, and the RFSH- line should be tied directly to the RFSH- pin of the device. Also, if the memory space allocated to the PSRAM is less than the size of memory area 3, or if the PSRAM memory shares memory area 3 with another device, additional decode logic is needed.

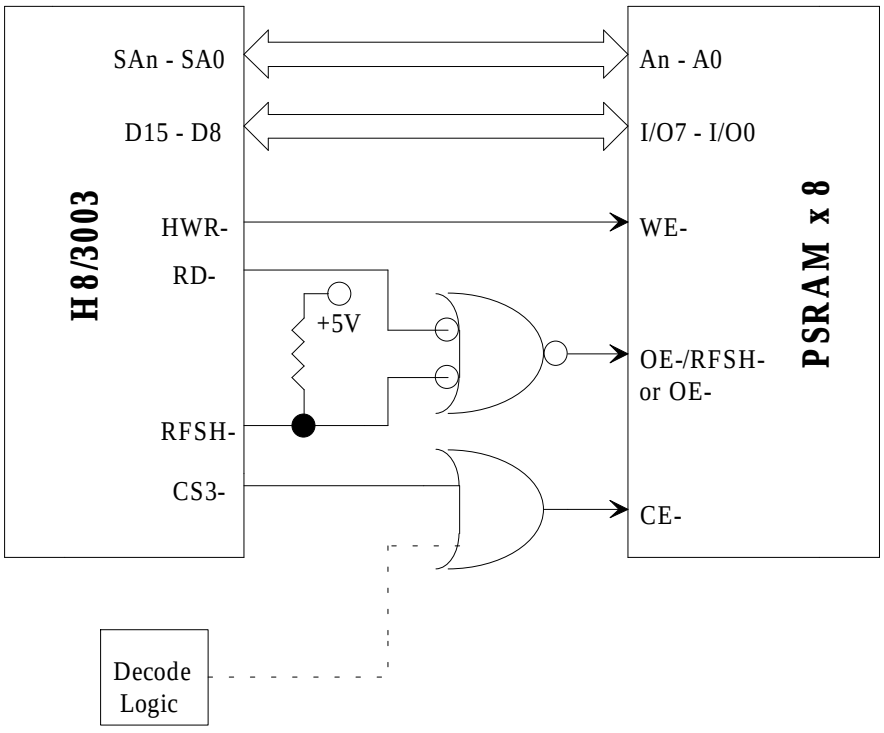

Figure 1. PSRAM connection in the byte access mode.

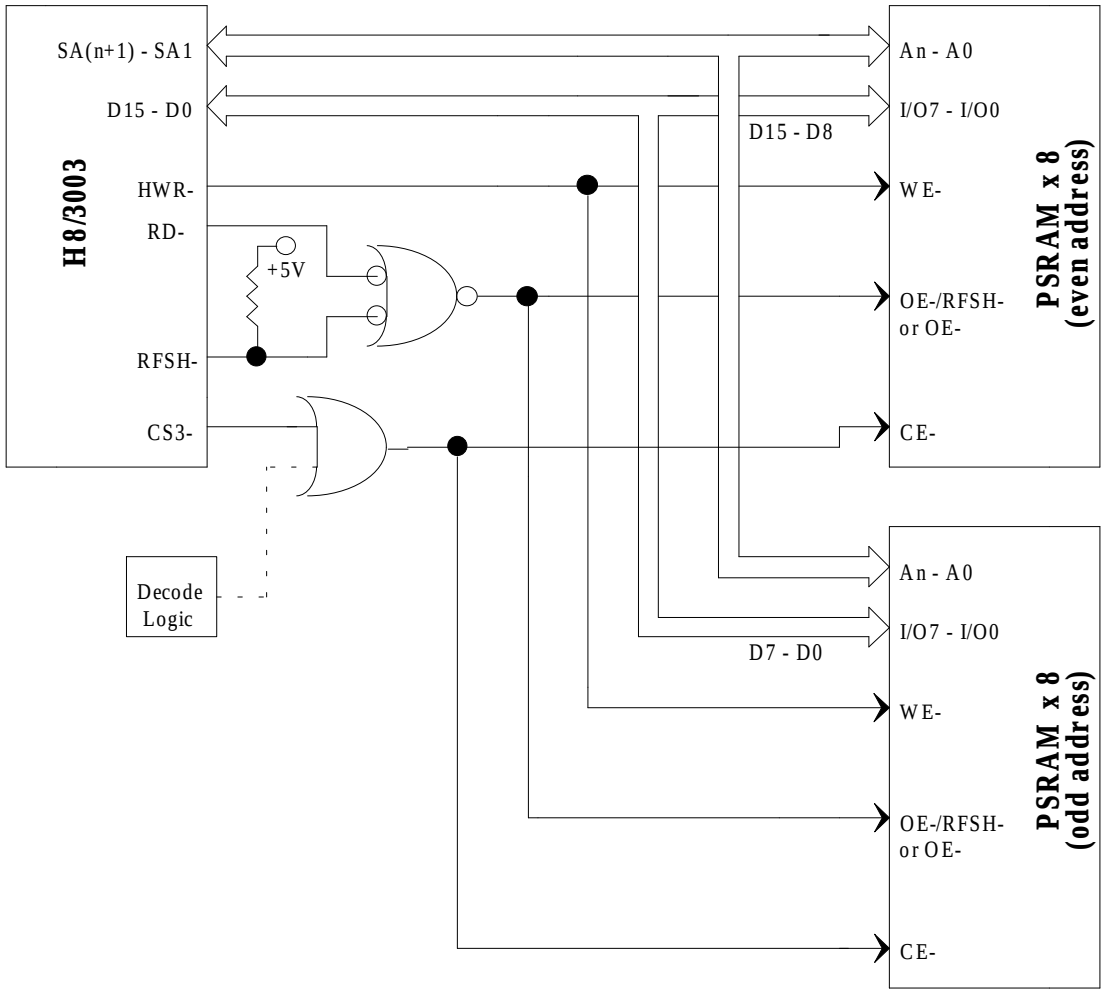

Figure 2. PSRAM connection in the word access mode.

Note: If the H8/3003 interface to PSRAMs is preset for word accesses (as in figure 2 above) and the user software re-configures it for byte accesses, transfers will only occur via D15 - 8, and only the PSRAM containing the even address locations will be used. Consequently, data will be stored only at even locations.

In order to be able to perform PSRAM accesses, the refresh controller module of the H8/3003 must be correctly initialized. This is achieved by setting bits 6, 5, and 2 to 1, and clearing bits 5 and 0 of the Refresh Control Register (RFSHCR), as illustrated in the figure below. Please refer to AE-0043 or to the H8/3003 Hardware Manual for a detailed functional description of each bit.

7	6	5	4	3	2	1	0
SRFMD	PSRAME	DRAME	CAS/WE	M9/M8	RFSHE	Res.	RCYCE
1 or 0	1	0	X	X	1	1	0

In addition, bits 5 - 3 of the Refresh Timer Control/Status Register (RTMCSR) must be programmed for the desired refresh counter clock frequency; for each refresh clock period, the Refresh Timer Counter Register (RTCNT) will be incremented by 1. The Refresh Time Constant Register (RTCOR) should be loaded with the desired compare-match value that determines the time interval between refresh cycles. The flowchart shown on the next page indicates the proper initialization sequence. Note that once bits 6 or 5 of RFSHCR are set, bits 0, 2, 3, and 4 as well as RTMCSR, RTCOR, and RTCNT are write-disabled.

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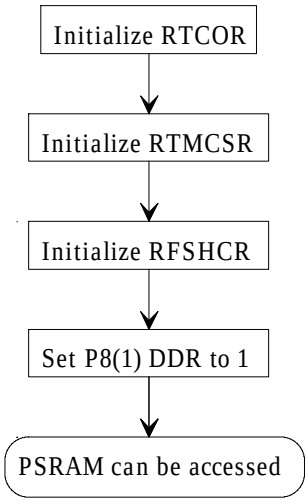

Figure 3. PSRAM initialization sequence.

When the H8/3003 enters the software standby mode, a self-refresh process can be initiated for PSRAMs that support this function. Bit 7 (SRFMD) of RFSHCR, when set, will cause the chip select line CS3- to turn high and the refresh output signal RFSH- to go low when the microcontroller enters the software standby mode. If these conditions last for more than 8 us, then the PSRAM device(s) will enter the self-refresh mode.

The table below shows a list of available and recommended Hitachi PSRAM parts that the user can interface to the H8/3003.

Part Number	Size	Refresh
HM65256B Series	32K x 8	via OE- pin
HM658128A Series	128K x 8	via RFSH- pin
HM658512 Series	512K x 8	via OE-/RFSH- pin

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