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Application Engineering
TechNote

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Enabling DMA end-of-transfer interrupts on the H8/300H

All members of the 16-bit H8/300H family feature an on-chip DMA controller providing fast and direct data transfers between memory and I/O locations or between memory locations without CPU involvement. A maximum of 8 DMA channels can operate simultaneously in memory-to-I/O transfer mode, and a maximum of 4 DMA channels can operate simultaneoulsy in memory-to-memory operation mode (on the H8/3003). For each DMA mode of operation, an end-of-transfer interrupt (DEND) may be requested upon a byte (or word) transfer completion or, if the block transfer DMA mode is used, upon transfer completion of a memory block of data. In order to ensure proper operation, the user must adhere to a sequenced setup procedure for each DMA mode of operation, as shown in the hardware manuals. However, extra care must be exercised when enabling the end-of-transfer interrupts in each mode of operation.

The Data Transfer Control Register (DTCR) in the memory-to-I/O modes, and its counterpart in memory-to-memory modes (DTCRA), contain 2 control bits that determine a DMA-end interrupt is correctly issued. These are the data transfer enable (DTE) bit, and the data transfer interrupt enable (DTIE) bit. The function of the DTE bit is to enable or disable data transfer, and the function of the DTIE bit is to enable or disable a DEND interrupt at the end of the transfer. According to the setup procedure for each DMA transfer type outlined in the H8/3003 hardware manual, the DTE bit should be cleared and the DTIE bit should be set (thus enabling a DEND interrupt at end-of-transfer) by writing the DTCR (or DTCRA) register in one write cycle. This step must be undertaken **although the DTE bit has an initialization value of 0.**

If, during the setup procedure, the user programs the DTCR(A) with the DTIE bit cleared to 0 (thus initially disabling end-of-transfer interrupts) and, later on in the program after a series of DMA transfers have been executed, the user decides to enable end-of-transfer interrupts by setting the DTIE bit to 1 (using the BSET instruction), an end-of-transfer DEND interrupt will be issued right away **before the DMA transfer starts.** In order to avoid this situation, 2 options are available:

1. Clear the DTE bit again as the DTIE bit is set in the same write cycle (that is, use a MOV instruction).
2. Set the DTIE bit right after the DTE bit is set, that is after the DMA transfer is enabled.

Also, the programmer must make sure that the DTCR (or DTCRA) must be read while the DTE bit is cleared **before** the DTE bit is set to start the DMA transfer. Using bit manipulation instructions to program any bits in DTCR(A) except DTIE should take care of reading the register. Alternatively, a MOV instruction can be used to write the content of DTCR into a CPU register, and then write it back to DTCR.