Hitachi America, Ltd.

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Application Engineering
TechNote

Cristian Tomescu

DMA Request and Transfer Time

The DMA Controller module of the H8/300H family of microcontrollers can be activated in 3 possible ways:

1. By internal interrupts from either the ITU (upon compare-match or input capture conditions), or the SCI (upon transmit-end or receive-end).
2. By external request via a falling edge or low level at the DREQ pin.
3. In software by register setup (auto-request).

The table below shows the activation methods, transfer direction, and the bus modes for each DMA transfer type.

TRANSFER TYPE	BUS MODE	ACTIVATION	Address or Register Length	
			SOURCE	DESTINATION
Short Address Modes	Cycle-Steal	Compare-Match, Input-Capture, or TxI	24 Bits	8 Bits
- I/O Mode		RxI	8 Bits	24 Bits
- Idle Mode - Repeat Mode		External Request	24 Bits	8 Bits
Normal Mode	Cycle-Steal	External Request	24 Bits	24 Bits
	Cycle-Steal or Burst	Auto-Request		
Block Transfer Mode	Burst	Compare-Match, Input-Capture, or External Request		

During Cycle-Steal DMA modes, only one byte (or word) of data is transferred at each request, and the CPU and DMAC share the data bus by alternating CPU cycles with DMA transfer cycles. During Burst DMA modes, a whole string of data is transferred at each request; consequently, the DMAC keeps the bus until each data block is transferred while the CPU is idling. This Tech Note will describe how to calculate the minimum time between 2 consecutive byte or word DMA transfer requests by each of the following activation sources (assuming no wait-states are added into the alternating CPU cycles).

Interrupt requests:

The minimum time between consecutive transfer requests activated by an internal interrupt, and with the DMAC operating in either the Short Address Modes or the Normal Mode, can be calculated by adding the following timing parameters:

1. The time it takes to request the DMA, i.e., the time between the interrupt-causing event and the internal interrupt request signal. If the interrupt is caused by a compare-match event, the interrupt acknowledge time between the compare-match signal and the internal interrupt request signal (IMI) is 1 Timer clock period, as can be seen in the ITU section of the H8/3003 Hardware Manual. If the interrupt is caused by an input-capture event, the acknowledge time between the input-capture pin toggling and the DMA request input-capture signal is 1 clock period, and the interval between the input-capture signal and the internal interrupt request signal is 1.5 clock periods, which makes it a total of 2.5 Timer clock periods, as can be observed from the figures in the same section in the manual. If the interrupt source is an SCI transmit or receive-end, there is no delay between the event occurrence and the interrupt request signal.
2. The DMA "latency" time, i.e., the time it takes from the transfer request until the DMA controller starts operating. The H8/3003 Hardware Manual specifies a minimum latency time of 4 T-states.
3. One DMA "dummy" cycle (Td), which lasts for 1 T-state.
4. The time it takes the DMA to read the contents of the source address. Depending upon the bus-controller settings and/or what memory area is being accessed, this process can take a minimum of either 2 or 3 T-states (assuming no wait states are induced in the cycle).

5. If the DMAC operates in the Block Transfer Mode, the time it takes the DMA to write data at the destination address must be added in the above calculation, since the interrupt request is sampled at the end of this cycle. Depending upon the bus controller settings and/or what memory area is being accessed, this process can take a minimum of either 2 or 3 T-states (again assuming no wait states are induced in this cycle).
6. Additional CPU states occurring during the following CPU cycle.

As an example, figure 1 below shows the timing between consecutive input-capture activated DMA cycles operating in the Short Address Modes performing transfers from a 16-bit 2 T-state access area to an 8-bit 3 T-state access area. The Timer as well as the DMAC is assumed to operate at the system clock frequency. The Timer is set up so that input-capture events are triggered on both edges at the input-capture pin. The minimum time between consecutive input-capture signals will be 7 T-states between the first 2 toggle actions at the input-capture pin, and 8 T-states between the following requests, assuming the inserted CPU cycle is only 2 T-states.

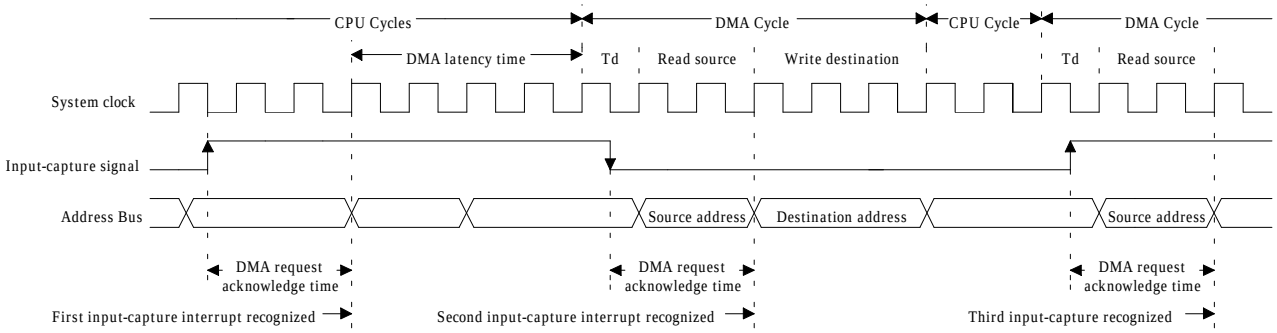

Figure 1. Timing of DMAC cycles activated by input-capture events in the Short Address Modes.

If the DMAC is set up to execute successive block transfers of one byte or word under the same conditions as in the example above, a minimum time of 10 T-states is needed between the first 2 transfer requests, and a minimum of 8 T-states between the following requests. Figure 2 below illustrates the timing for this case:

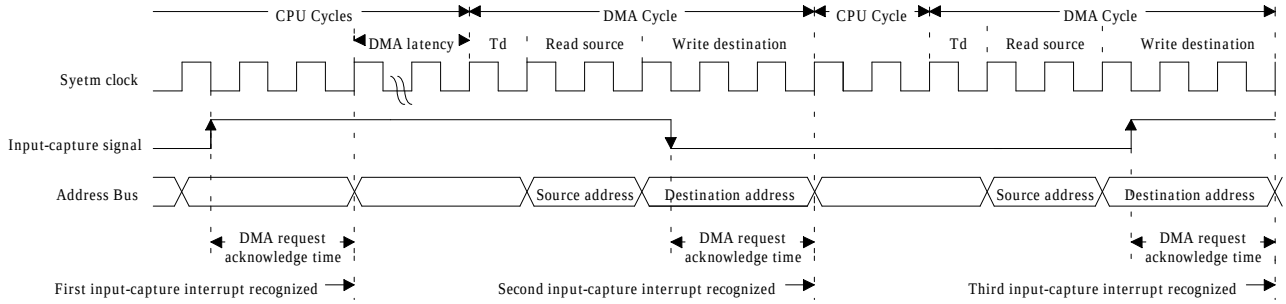

Figure 2. Timing of DMAC cycles activated by input-capture events in the Block Transfer Mode.

External requests:

The minimum time between a DMA request and the next DMA request, which are activated by a falling edge or a low-level at the DREQ pin, is calculated similarly to the case above, but with one important difference: there is no interrupt acknowledge time, as explained in point a) above. The figure depicted in the DMAC section of the H8/3003 Hardware Manual exemplifies this case for the DMA controller operating in either the Short Address Mode or the Normal Mode.

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Hitachi America, Ltd. • San Francisco Center • 2000 Sierra Point Parkway • Brisbane, CA 94005-1819 • (415) 589-8300

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