Hitachi America, Ltd.

TN-0117

Application Engineering
TechNote

June, 1995

Watchdog Timer Initialization

Hitachi's H8/510, H8/532, H8/534, H8/536, H8/538 and H8/570 contain a Watchdog Timer (WDT) circuits to reset the part in the event of a software failure or stall. The WDT register default settings initialize the timer as a interval timer, therefore, the software start-up routine must set the registers to begin WDT operation. WDT registers require a slightly different access procedure.

The H8/532 circuit issues an NMI interrupt rather than a hardware reset if the watchdog timer is allowed to overflow . Although this does not provide a true system reset, it does allow the programmer more flexibility over which peripherals are re-initialized and where program flow resumes. The NMI routine should evaluate and correct the system status. The stack pointer must be re-written to return the program counter to a known and valid location following RTE from the interrupt routine. An I/O port line can be used to issue an external reset and/or issue an external warning signal.

Procedure:

1. If required, set the RSTOE bit in the Reset Control / Status Register to enable a RESET signal output on the RES pin in the event of a WDT timer overflow (this step is not valid for the H8/532).
2. Select one of eight clock pre-scale values by writing to CKS2-CKS0 (TCSR [2:0]). The pre-scale values selects the WDT interval.
3. Set the WT/IT bit (TCSR [6]) to select watchdog mode.
4. Set the TME bit (TCSR [5]) to begin WDT operation.

Timer Counter (TCNT) and Timer Control / Status Registers (TCSR)

These registers are located on word boundaries, however, only the lower byte contains register data. The upper byte is used for password protection. A write access must be word wide. The upper 8 bits of the word must contain the access password, the lower 8 bits contain the write data. A read cycle should access only the lower byte.

To set or clear the Timer Control Status Register (TCSR), use a word operation where the upper byte contains the password H'A5. To start the WDT with an overflow interval of 13.1 ms (System Clock = 10 MHz) use the following instruction:

MOV.W #H'A565, @WDT_TCSR_W

where WDT_TCSR_W is the write address for the TCSR.

To prevent a time-out condition and subsequent RESET, the CPU must clear the TCNT before the count value overflows. The upper byte of the clear instruction must contain the password H'5A.

MOV.W #H'5A00, @WDT_TCNT_W

where WDT_TCNT_W is the write address for the TCNT.

Reset Control / Status Register

The Reset Control \ Status Register is also aligned to word boundaries. The lower byte contains two valid bits: Bit 7, WRST, is the WDT reset condition flag. Bit 6, RSTOE, is used to drive the RES pin low to reset external circuits following a time-out condition. A read cycle should be a byte wide access to the lower byte. A write cycle to set or clear a bit must be word wide. The upper byte must contain the password unique to the bit being accessed, the lower byte holds the write data.

For example:

To enable the RSTOE during initialization, use the instruction

MOV.W #H'5A40, @WDT_RSTCST_W

where WDT_RSTCSR is the write address for the RSTCSR register and H'5A is the RSTOE password.

To clear the WRST flag after a WDT overflow and reset, use the instruction:

MOV.W #H'A500,@WDT_RSTCST_W

where WDT_RSTCST_W is the write address for the RTSCSR register and H'A5 is the WRST password.

written by: Carol Jacobson, Application Engineering

Hitachi America, Ltd. Semiconductor and I.C. Division
2000 Sierra Point Parkway, Brisbane, CA 94005-1819 (415)589-8300