Hitachi Microcomputer
Technical Q & A
H8/300H Series

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Introduction

The H8/300H series microcontrollers are high-performance Hitachi-original 16-bit microcontrollers that build in the optimum peripheral equipment for industrial machinery around high-speed H8/300 CPUs that have architecture upwardly compatible with H8/300 CPUs.

The microcontroller puts a CPU, RAM, direct memory access controller (DMAC), bus controller, timers, and a serial communication interface (SCI) on a single chip, making it suitable for a wide range of applications from small to large systems.

This microcontroller technical Q&A covers the H8/3001, H8/3002, H8/3003, H8/3042 series, H8/3032 series, and H8/3048 series.

Table 0-1 H8/300H Series

Item			H8/3003	H8/3002	H8/3001	H8/3042	H8/3041	H8/3040
CPU			H8/300H	H8/300H	H8/300H	H8/300H	H8/300H	H8/300H
Memory	ROM	Mask (byte)	—	—	—	64 k	48 k	32 k
		ZTAT™*	—	—	—	Yes	—	—
	RAM (byte)		512	512	512	2 k	2 k	2 k
Address space (byte)			16 M	16 M	16 M	16 M	16 M	16 M
External data bus width (bit)			8/16	8/16	8/16	8/16	8/16	8/16
Timers	ITU (integrated timer unit)		5 ch	5 ch	5 ch	5 ch	5 ch	5 ch
	Watchdog timer		1 ch	1 ch	—	1 ch	1 ch	1 ch
DMA controller	Memory ↔ I/O		8 ch	4 ch	—	4 ch	4 ch	4 ch
	Memory ↔ memory		4 ch	2 ch	—	2 ch	2 ch	2 ch
Programmable timing pattern controller (TPC)			16 bits	16 bits	12 bits	16 bits	16 bits	16 bits
SCI (Asynchronous/clock-synchronous)			2 ch	2 ch	1 ch	2 ch	2 ch	2 ch
A/D converter	Resolution		10 bits	10 bits	10 bits	10 bits	10 bits	10 bits
	Input channel		8 ch	8 ch	4 ch	8 ch	8 ch	8 ch
	External trigger input		Yes	Yes	Yes	Yes	Yes	Yes
D/A converter	Resolution		—	—	—	8 bits	8 bits	8 bits
	Input channel		—	—	—	2 ch	2 ch	2 ch
Refresh controller			On-chip	On-chip	—	On-chip	On-chip	On-chip
Interrupts	External interrupts		9	7	4	7	7	7
	Internal Interrupts		34	30	20	30	30	30
I/O port			58	46	32	78	78	78
Package			QFP-112	QFP-100 TQFP-100	QFP-80 TQFP-80	QFP-100 TQFP-100	QFP-100 TQFP-100	QFP-100 TQFP-100
Miscellaneous			—	—	—	—	—	—

Note: ZTAT (Zero turn around time) is a trademark of Hitachi Ltd.

Table I-1 H8/300H Series (cont)

Item			H8/3048	H8/3047	H8/3044	H8/3032	H8/3031	H8/3030
CPU			H8/300H	H8/300H	H8/300H	H8/300H	H8/300H	H8/300H
Memory	ROM	Mask (byte)	128 k	96 k	32 k	64 k	32 k	16 k
		ZTAT™*	Yes	—	—	Yes	—	—
	RAM (byte)		4 k	4 k	2 k	2 k	1 k	512
Address space (byte)			16 M	16 M	16 M	1 M	1 M	1 M
External data bus width (bit)			8/16	8/16	8/16	8	8	8
Timers	ITU (integrated timer unit)		5 ch	5 ch	5 ch	5 ch	5 ch	5 ch
	Watchdog timer		1 ch	1 ch	1 ch	1 ch	1 ch	1 ch
DMA controller	Memory ↔ I/O		4 ch	4 ch	4 ch	—	—	—
	Memory ↔ memory		2 ch	2 ch	2 ch	—	—	—
Programmable timing pattern controller (TPC)			16 bits	16 bits	16 bits	16 bits	16 bits	16 bits
SCI (Asynchronous/clock-synchronous)			2 ch	2 ch	2 ch	1 ch	1 ch	1 ch
A/D converter	Resolution		10 bits	10 bits	10 bits	10 bits	10 bits	10 bits
	Input channel		8 ch	8 ch	8 ch	8 ch	8 ch	8 ch
	External trigger input		Yes	Yes	Yes	Yes	Yes	Yes
D/A converter	Resolution		8 bits	8 bits	8 bits	—	—	—
	Input channel		2 ch	2 ch	2 ch	—	—	—
Refresh controller			On-chip	On-chip	On-chip	—	—	—
Interrupts	External interrupts		7	7	7	6	6	6
	Internal Interrupts		30	30	30	21	21	21
I/O port			78	78	78	63	63	63
Package			QFP-100 TQFP-100	QFP-100 TQFP-100	QFP-100 TQFP-100	QFP-80 TQFP-80	QFP-80 TQFP-80	QFP-80 TQFP-80
Miscellaneous			Built-in smart card interface, improved low-voltage, low-power performance			—	—	—

For Users of the Microcontroller Technical Q & A

This *Microcontroller Technical Q & A* was compiled from answers to technical questions we received from Hitachi microcontroller users. We hope that it will be a useful addition to the *H8/300H series user manuals*. Before starting design of products that use microcontrollers, read through the manual to deepen your understanding of microcontroller products and re-familiarize yourself with those areas of difficulty at the design stage.

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Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-001A
Topic	The Difference Between the CCR's V Flag and C Flag		

Question

Since the CCR's V flag and C flag both flag a 1 when an operation overflows, what is the difference?

Classification—H8/300H

	Software
0	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The CCR's V flag is accessed to see if an overflow has occurred in a signed operation. In figure 1.1, which is a byte-sized operation, the flag is set to 1 when the result is smaller than the negative minimum (H'80) or larger than the positive maximum (H'7F).

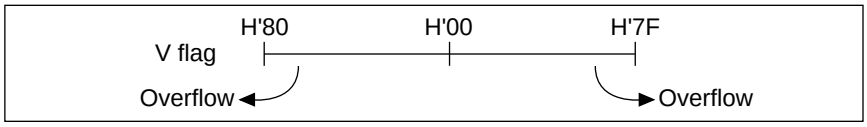


Figure 1.1 V Flag Operation

In contrast, the CCR's C flag is accessed to see if an overflow has occurred in an unsigned operation. In figure 1.2, which is a byte-sized operation, the flag is set to 1 when the result is smaller than the minimum (H'00) or larger than the maximum (H'FF).

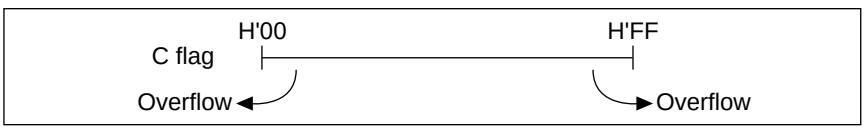


Figure 1.2 C Flag Operation

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-002A
Topic	The Relationship Between Data Size and V Flag Changes		

Question

Do the changes in the CCR's V flag vary with data size?

Classification—H8/300H	
	Software
0	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The CCR's V flag changes when an overflow is detected in the result of a signed arithmetic operation. This operation is the same for all data sizes. However, the timing of the changes in the flag varies as follows:

- Byte: When the value is smaller than H'80 or larger than H'7F.
- Word: When the value is smaller than H'8000 or larger than H'7FFF.
- Longword: When the value is smaller than H'80000000 or larger than H'7FFFFFFF.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-003A
Topic	Use of General Registers		

Question

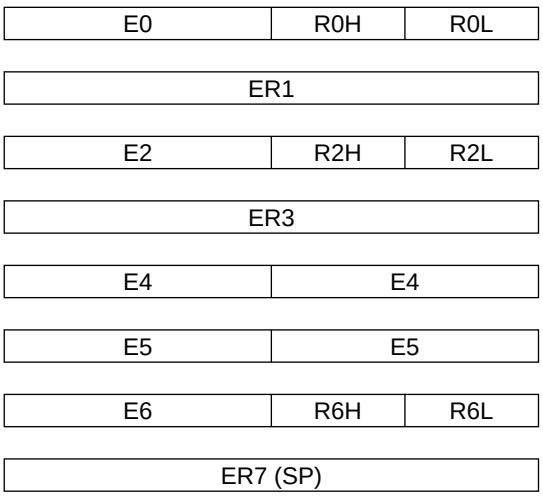
Can different general registers be used as 8-bit, 16-bit, and 32-bit registers at the same time?

Classification—H8/300H

	Software
0	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Yes. Registers can be set freely for use as shown in figure 1.3.



Note: ER7 is used as the SP without any special notice being given.

Figure 1.3 Use of General Registers

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 2.4.2, General Registers, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-004
Topic	Bus State While the CPU Is Operating		

Question

1. What is the bus state during CPU internal processing?
2. What is the bus state after $\overline{\text{DREQ}}$ is received?
3. What is the bus state after $\overline{\text{BREQ}}$ is received?

Classification—H8/300H

	Software
	Registers
0	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

See table 1.1.

Table 1.1 Bus State While the CPU Is Operating

CPU Operation	Address Bus	Data Bus
During internal CPU processing	Hold	High impedance
After $\overline{\text{DREQ}}$ is received	DMA address	DMA data
After $\overline{\text{BREQ}}$ is received	High impedance	High impedance

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See figure 6.18, External Bus Release State, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-005A
Topic	Bus Modes		

Question

Section 6.2.1 of the H8/3003 Hardware Manual says, “When even 1 bit of the ABWCR is cleared to 0, the bus mode becomes 16 bits.” Does this mean that all areas can be accessed in 16-bit mode?

Classification—H8/300H

	Software
	Registers
0	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

No. When a given bit ADWn (bus width control for area n) of the ABWCR (bus width control register) is cleared to 0, only that area whose bit is cleared can be accessed in 16-bit mode. The manual description might better read, "When even one area is set as a 16-bit accessed space, the H8/300H CPU goes into 16-bit bus mode and D15–D0 can all be used as the data bus. This means that I/O ports that are also used as the lower data bus (D7–D0) cannot be used as general ports, even in an 8-bit access space."

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See table 6.4, Address Space and Data Bus Used, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-006A
Topic	Setting the Bus Controller in Area 7		

Question

Since area 7 mixes on-chip RAM and internal I/O registers, in which areas are the bus widths and access states set by the bus controller valid?

Classification—H8/300H

	Software
	Registers
0	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

In area 7, the bus width and number of access states set by the bus controller are valid in areas other than the on-chip RAM and internal I/O registers. (The addresses of the area differ according to the product. See the manual for details.) On-chip RAM has a fixed bus width of 16-bits and a fixed number of access states of 2. The internal I/O registers can have bus widths of 8-bits or 16-bits, and have a fixed number of access states of 3.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See figure 6.2, Access Area Map for Each Operating Mode, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

When the RAME (RAM enable) bit of the SYSCR (system control register) is cleared to 0, the on-chip RAM is not valid and the settings of area 7 are followed. The CS signal outputs low in all of area 7.

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-007A
Topic	External Installation of RAM to 8-Bit Bus Areas		

Question

When RAM is externally installed in 8-bit bus space, which signal should be used to access it, $\overline{\text{HWR}}$ or $\overline{\text{LWR}}$?

Classification—H8/300H

	Software
	Registers
0	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Use the $\overline{\text{HWR}}$ signal.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See table 6.4, Address Space and Data Bus Used, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-008A-1
Topic	Changing the Number of Wait States Inserted Per Area		

Question

1. Can the wait mode be set for individual areas?
2. If not, how should the wait mode be set to change the number of access states inserted for individual areas?

Classification—H8/300H

	Software
	Registers
0	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. WMS (wait mode select) bits 1 and 0 of the WCR (wait control register), which set the wait mode, are common to all areas. For this reason, the wait mode cannot be set for individual areas.
2. The following areas, can, however, be mixed:
   - Wait disabled areas
   - Areas to which wait states are only inserted by the $\overline{\text{WAIT}}$ pin (pin wait mode 0)
   - Areas in which WC (wait count) bits 1 and 0 of the WCR are valid (programmable wait mode, pin wait mode 1, or pin auto-wait mode)

   The number of access states for individual areas can be changed by using these in combination. An example is shown below and in tables 1.2 and 1.3.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 6.3.5 (5), WSC Setting Example, in the following manuals:
- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

The bus width and the enabled/disabled state of WSC (wait state controller) operation can be set for individual areas.

Product	H8/300H	Q&A No.	QA300H-008A-2
Topic	Changing the Number of Wait States Inserted Per Area		
Answer			

Example: To set the following access states for the following areas:

- Areas 0–1: 2 states
- Area 2: 3 states
- Areas 3–4: 4 states
- Area 5: 5 states
- Areas 6–7: 6 states

Table 1.2 Changing the Number of Wait States Inserted Per Area

Area	Memory Map	Wait States from WC Bit	Enable/Disable of Wait Insertion from $\overline{\text{WAIT}}$ Pin	$\overline{\text{Waits}}$ from $\overline{\text{WAIT}}$ pin	Access States
Area 0	2-state access space	Invalid	Disable	—	2
Area 1	Wait-disabled area				
Area 2	3-state access space pin wait mode 0	Invalid	Enable	0	3
Area 3		Valid/1 state	Enable	0	4
Area 4	3-state access space pin wait mode 1				
Area 5			Enable	1	5
Area 6	3-state access space	Invalid	Enable	3	6
Area 7	pin wait mode 0				

Table 1.3 Register Settings

Register	Address	Setting							
		7							0
ASTCR (Access state control register)	H'FC	1	1	1	1	1	1	0	0
		7							0
WCER (Wait state control enable register)	H'38	0	0	1	1	1	0	0	0
		7							0
WCR	H'F9	—	—	—	—	1	0	0	1

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-009A
Topic	Receiving $\overline{\text{BREQ}}$ in Power-Down Mode		

Question

1. Can $\overline{\text{BREQ}}$ be received in sleep mode?
2. Can $\overline{\text{BREQ}}$ be received in hardware/software standby mode?

Classification—H8/300H

	Software
	Registers
0	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. Yes
2. Since both the hardware standby mode and software standby mode bring on-chip peripheral modules to a halt (including the clock), $\overline{\text{BREQ}}$ cannot be received.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-010A
Topic	Maximum Wait Time After $\overline{\text{BREQ}}$ Input		

Question

Why does it take so long between $\overline{\text{BREQ}}$ input and $\overline{\text{BACK}}$ output?

Classification—H8/300H

	Software
	Registers
0	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Because the $\overline{\text{BREQ}}$ request is held in the following cases:

1. When DMAC (DMA controller) data is being transferred in burst mode or block transfer mode.
2. When waits are inserted during accesses of external addresses.

Example: When an instruction with a word-size operand is executed with an 8-bit bus in pin wait mode 1: 1 bus cycle (3 states + inserted wait states + wait states inserted by pin) × 2.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-011A
Topic	Interrupt Sampling		

Question

When are external interrupts (NMI, IRQn) sampled?

Answer

Sampling occurs at every fall of the system clock ϕ.

Classification—H8/300H

	Software
	Registers
	Bus controller
0	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See figure 18.17, Interrupt Input Timing, in the following manuals:
- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*

See figure 20.17, Interrupt Input Timing, in the following manual:
- *H8/3042 Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-012A
Topic	Holding External Interrupts		

Question

1. Are the IRQn interrupt requests held if they are produced when the IRQnE (IRQ enable) bit of the IER (IRQ enable register), which controls external interrupts (IRQn), is cleared to 0?
2. Are IRQn interrupt requests held if they are produced when interrupts are masked with the I and UI bits of the CCR (condition code register)?

Classification—H8/300H

	Software
	Registers
	Bus controller
0	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. Yes. When the signal specified by the ISCR (IRQ sense control register) drives the IRQn pin, the IRQnF (IRQn flag) of the ISR (IRQ status register) is set to 1. This is not affected by the state of the IRQnE bit. When the IRQnE bit is set to 1 while the IRQnF is set to 1, an interrupt is requested. The IRQnF bit can be cleared with software.
2. Yes. As in the above case, IRQnF is not affected by the state of the I and UI bits. When the IRQnE and IRQnF bits are set to 1 and the interrupt mask is cleared, the interrupt is accepted.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See figure 5.2, IRQ Interrupt Block Diagram, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-013A
Topic	Receiving NMIs During NMI Processing		

Question

If the NMI has the highest priority and is always accepted, will another NMI be accepted if it is generated while the NMI interrupt processing routine is running?

Classification—H8/300H

	Software
	Registers
	Bus controller
0	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

If another NMI is generated while an NMI interrupt processing routine is running, that interrupt request is accepted superimposed over the first.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-014A
Topic	Edge Rise and Fall Times for Interrupt Pins		

Question

When an edge trigger is used for an external interrupt, what are the longest allowed rise and fall times of the edge?

Classification—H8/300H

	Software
	Registers
	Bus controller
0	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Make it no more than 2 states. More than this will produce the following effects:

1. Interrupts will not be accepted because the edge change is not detected.
2. More than one edge will be detected internally for each change in the external pin signal, so multiple interrupts will be requested.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-015A
Topic	Disable Timing for Interrupts		

Question

1. Are interrupts disabled the instant that the peripheral module's interrupt enable bit is cleared to 0?
2. When the interrupt enable bit of the IER (IRQ enable register) is cleared to 0, are interrupt instantly disabled?

Classification—H8/300H

	Software
	Registers
	Bus controller
0	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. Interrupts are disabled after the instruction that cleared the interrupt enable bit to 0 finishes executing. When an interrupt request is generated while the zeroing instruction is executing, that interrupt request is accepted after the instruction completes its execution.
2. Interrupts are disabled after the instruction that cleared the interrupt enable bit to 0 finishes executing. When an interrupt request is generated while the zeroing instruction is executing, that interrupt request is not accepted after the instruction completes its execution since the request signal is cleared simultaneously with the enable bit. However, since the IRQn flag is held, the next time the interrupt enable bit is set to 1, that interrupt is accepted.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 5.5.1, Interrupt Generation and Disable Contention, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

Also see section 1.3.2, Holding External Interrupts (QA300H-012A), in this manual.

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-016A
Topic	Exception Processing After a Reset		

Question

Are interrupts ever generated immediately following resets?

Classification—H8/300H

	Software
	Registers
	Bus controller
0	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

No. Immediately after a reset, all interrupts, including NMIs, are disabled. However, when the first instruction of a program is executed, NMIs are accepted.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 4.2.3, Interrupts After a Reset, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Product	H8/300H	Q&A No.	QA300H-017A-1
Topic	Using the Interrupt Controller		

Question

How should the two interrupt priority levels be used to make effective use of the interrupt controller?

Classification—H8/300H

	Software
	Registers
	Bus controller
0	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

By rewriting the values set in IPRA and IPRB (interrupt priority registers A and B) for every interrupt processing routine, the interrupt priority can be changed at any time. IPRA and IPRB are 1-word registers, so they are easy to manipulate. A sample program is shown in figure 1.4. See the procedures after the figure for a more concrete example on use.

```
PUSH      R0          ——— Saves content of R0
MOV.W     @IPRA, R0   ———┐ Saves IPRA value
PUSH      R0          ———┘
MOV.W     #NEW, R0    ———┐ Sets the new IPRA value to NEW
MOV.W     R0, @IPRA   ———┘
ANDC      #H'BF, CCR  ——— Clears the UI bit
  ⋮           ⋮
POP       R0          ———┐ Reverts to the saved IPRA value
MOV.W     R0, @IPRA   ———┘
POP       R0          ——— Reverts to the saved R0 value
RTE
```

Figure 1.4 Sample Program

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	H8/300H	Q&A No.	QA300H-017A-2
Topic	Using the Interrupt Controller		
Answer			

1. Procedure for setting interrupt priority:
   a. Set the UE (user bit enable) bit of the SYSCR (system control register) to 0, the I bit (interrupt mask) of the CCR (condition code register) to 1, and the CCR's UI (user bit/interrupt mask) bit to 0. In this state, only NMIs and priority 1 interrupt sources are accepted.

   b. Set the interrupt priorities for each interrupt source on the user end.

   c. Perform the following processing during the interrupt processing routines. Following the interrupt priorities set by the user, interrupts of priorities lower than the interrupt in question are masked by writing a 0 to the appropriate bits in IPRA and IPRB.

2. Figure 1.5 shows the processing procedures when the interrupt priorities set by the user are as shown in table 1.4.

Table 1.4 Interrupt Priorities

Interrupt Source	User-Set Priorities		Initial IPRA, IPRB Settings
Timer 1	5	Highest	1
Timer 2	4	↕	1
SCI 1	3	↕	1
Timer 3	2	↕	1
Timer 4	1	↕	1
SCI 2	0	Lowest	1

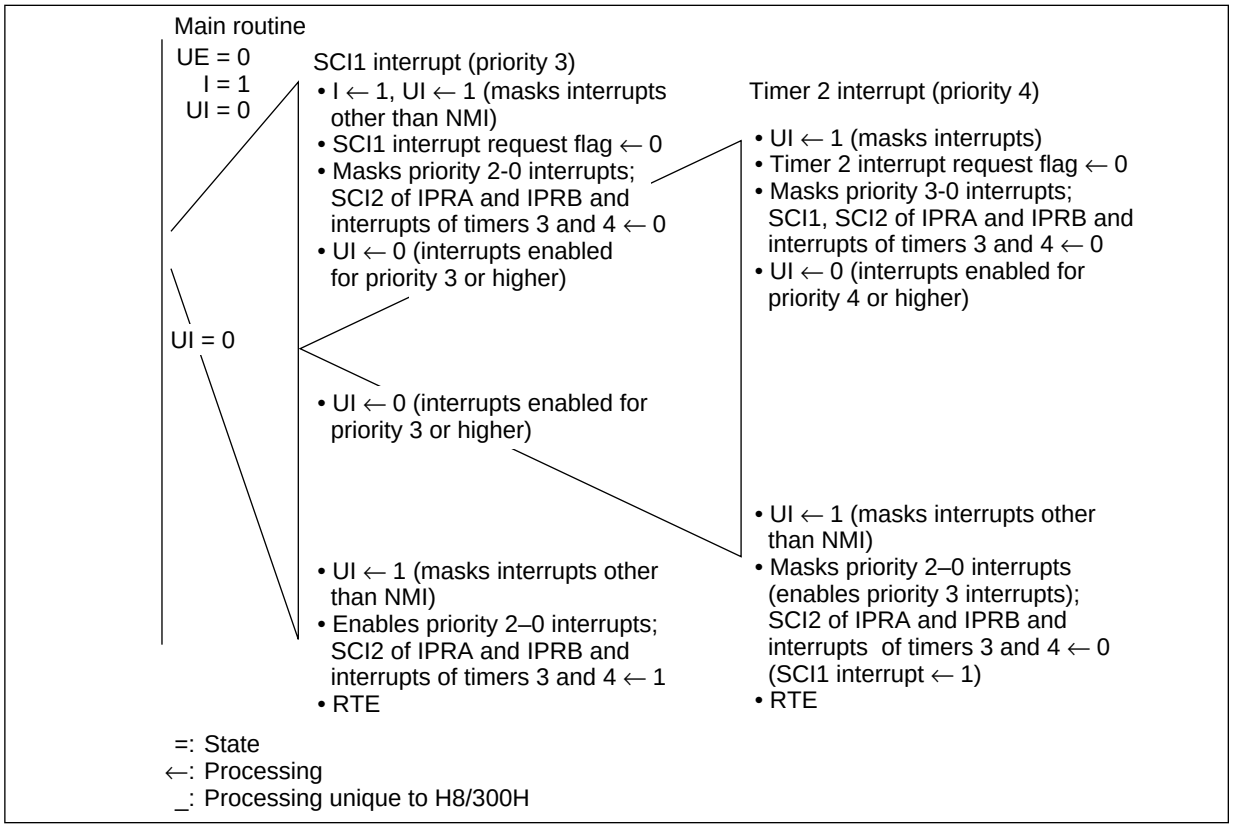


Figure 1.5 Processing Procedures

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-018A
Topic	Receiving an External IRQ1 After Returning From Hardware Standby Mode		

Question

In the hardware standby mode, I set the $\overline{\text{IRQ1}}$ pin to low and then left the hardware standby mode. Will interrupts be accepted after returning while the $\overline{\text{IRQ1}}$ pin remains low?

Classification—H8/300H

	Software
	Registers
	Bus controller
0	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Interrupts will not be accepted immediately after returning. A reset clears hardware standby mode. This initializes the IER (IRQ enable register) and IRQ1 becomes disabled (the IRQ1E (IRQ1 enable) bit of the IER = 0). Thereafter, if the IRQ1E bit of the IER is set to 1 and the I and UI bits of the CCR enable interrupts, interrupts will be accepted.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 4.2.3, Interrupts After a Reset, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-019A
Topic	Interrupt Priority Within Groups		

Question

1. When external interrupts occur simultaneously within groups with the same priority (for example, IRQ4–IRQ7) which has priority?
2. When an IRQ4 interrupt occurs during an IRQ7 interrupt processing routine, what happens? (Does IRQ4 wait or does IRQ4 processing take priority?)

Classification—H8/300H

	Software
	Registers
	Bus controller
0	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. A priority is set within the IRQ4–IRQ7 interrupt group of IRQ4 > IRQ5 > IRQ6 > IRQ7.
2. The IRQ7 is accepted first. After it is accepted, IRQ4–IRQ7 are all masked. When the I (interrupt mask) and UI (interrupt mask) bits of the CCR (condition code register) are enabled during the IRQ7 processing routine, IRQ4–IRQ7 can be accepted. When not enabled in the IRQ7 processing routine, the IRQ4 is accepted after returning from the IRQ7 processing routine.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See table 5.3, Interrupt Factors, Vector Addresses, and Interrupt Priority Ranking (1) , in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-020A
Topic	Interrupts When the Bus Is Released		

Question

Are interrupts that occur when the bus is released held?

Classification—H8/300H

	Software
	Registers
	Bus controller
0	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

They are. After the bus release ends, they are accepted after the execution of one instruction. This is the same regardless of whether they are sensed by edge or level.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	H8/300H	Q&A No.	QA300H-021A
Topic	NMI Sampling Timing and Receiving After Reset		

Question

After reset, when does sampling of the NMI signal begin?

Classification—H8/300H	
	Software
	Registers
	Bus controller
	Interrupts
0	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Sampling of the NMI signal begins simultaneously with the fall of the system clock in which the reset clear was sampled. The NMI is not accepted, however, until after the execution of the first instruction after the reset is cleared (see figure 1.6)

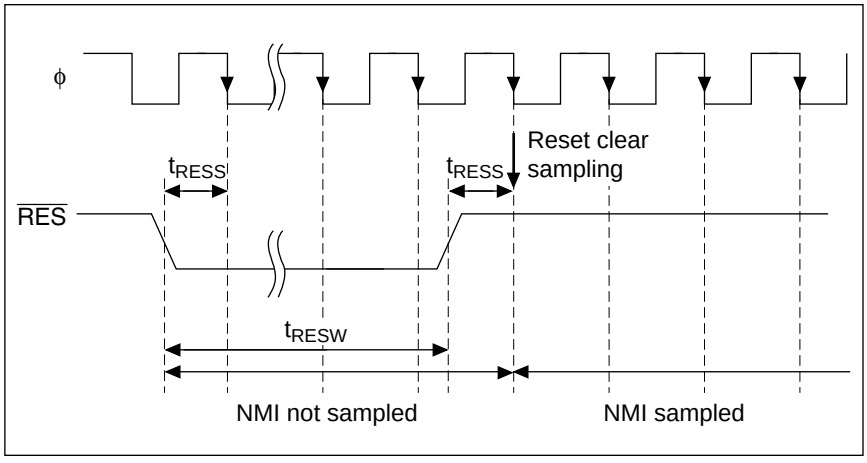


Figure 1.6 NMI Sampling Timing and Receiving After Reset

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-022A
Topic	Initializing SP After Reset		

Question

Why does the SP (stack pointer) have to be initialized immediately after a reset?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
0	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

If an interrupt is accepted before the SP is initialized, the save address when the PC (program counter) is saved by the interrupt exception processing becomes undefined. The PC could be written to a blank address, to the I/O registers and so on, which makes it impossible to read them correctly on return. This can cause run-away operation. To avoid this, initialize the SP immediately after a reset.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 4.2.3, Interrupts After a Reset, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-023A
Topic	Pin State During Power-On Reset		

Question

What pin states do I need to pay attention to during power-on resets?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
0	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

During a power-on reset, set the device to an operating mode that uses the mode pins (MD0–MD2) and keep the $\overline{\text{STBY}}$ pin high. Also remember that the ϕ output data is undefined until oscillation settles.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 3.1.1, Types of Operating Mode Selection, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-024A
Topic	$\overline{\text{RESO}}$ Pin Output From $\overline{\text{RES}}$ Pin Input		

Question

What is the $\overline{\text{RESO}}$ pin state for reset state ($\overline{\text{RES}}$ = low)?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
0	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The $\overline{\text{RESO}}$ pin is high impedance for reset state ($\overline{\text{RES}}$ = low). It does not go to reset output ($\overline{\text{RESO}}$ = low).

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-025A
Topic	Connecting $\overline{\text{RES}}$ and $\overline{\text{RESO}}$ Pins		

Question

Is there any problem with taking $\overline{\text{RESO}}$ pin low output and inputting it directly to the $\overline{\text{RES}}$ pin?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
0	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Yes. When a WDT (watchdog timer) overflow causes $\overline{\text{RESO}}$ output to be input directly to the $\overline{\text{RES}}$ pin, a reset caused by $\overline{\text{RES}}$ pin input is triggered at that moment and everything internal to the LSI, including the WDT, is initialized. This forcibly disables the $\overline{\text{RESO}}$ output as well, meaning that the $\overline{\text{RES}}$ input spec t_{RESW} ($\overline{\text{RES}}$ pin pulse width) minimum of 10 t_{cyc} cannot be satisfied and the operation of the H8/300H CPU after that point cannot be guaranteed. A buffer thus needs to be inserted to ensure that the $\overline{\text{RESO}}$ output does not find its way to the $\overline{\text{RES}}$ pin. (See figure 1.7.)

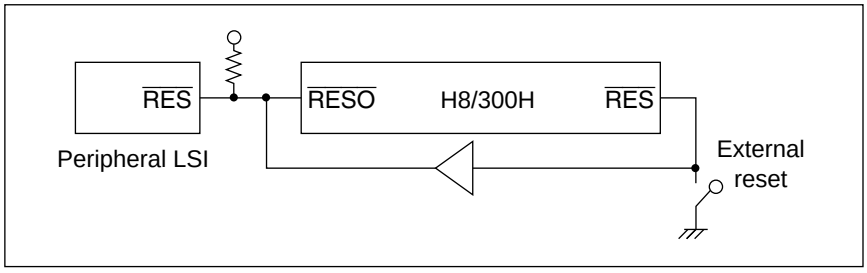


Figure 1.7 Connecting $\overline{\text{RES}}$ and $\overline{\text{RESO}}$ Pins

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-026A
Topic	Cautions for Reset Input		

Question

Are there any cautions for reset input?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
0	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

When the $\overline{\text{RES}}$ pin is made low, a reset begins, but to be sure that a reset is performed, it must be low for at least 20 ms when the power is turned on and at least 10 system clock cycles when operating. When it goes high thereafter, reset exception processing begins. If these conditions are not satisfied, operation thereafter cannot be guaranteed.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 4.2.2, Reset Sequence, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-027A
Topic	Executing Instructions When Switching to Hardware Standby Mode		

Question

What happens to executing instructions when the $\overline{\text{STBY}}$ pin goes low and the hardware standby mode is entered?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
0	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals:
- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*

See section 19.5.1, Transition to Hardware Standby Mode, in the following manual:
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-028A
Topic	Mode Pins During Hardware Standby Mode		

Question

What happens when the mode pins (MD2–MD0) are changed in hardware standby mode?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
0	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The result is abnormal hardware standby mode operation. Do not change the mode pins while in hardware standby mode. When the mode is changed to PROM mode, for example, the power consumption goes up.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-029A
Topic	Returning From Hardware Standby Mode		

Question

I know that the $\overline{\text{RES}}$ pin has to be kept low and the $\overline{\text{STBY}}$ pin changed to high to return from hardware standby mode, but how long before the $\overline{\text{STBY}}$ pin is changed to high does the $\overline{\text{RES}}$ pin have to be low?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
0	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

To return from hardware standby mode, the $\overline{\text{RES}}$ pin has to be low for 100 ns before the $\overline{\text{STBY}}$ pin is changed to high. (See figure 1.8.)

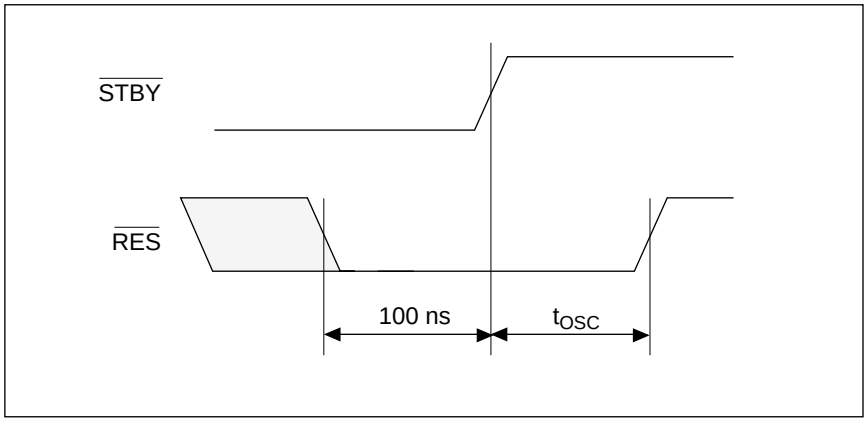


Figure 1.8 Standby Release Timing

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See Appendix E, Hardware Standby Mode Transition (Return Timing), in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Product	H8/300H	Q&A No.	QA300H-030A
Topic	Interrupt Sampling and Receiving in Sleep Mode		

Question

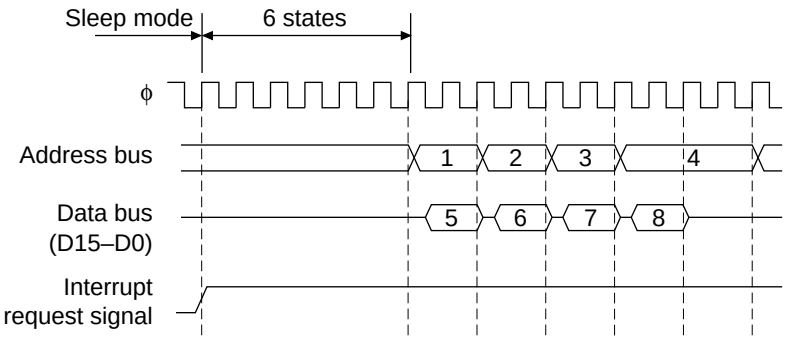
1. When are external interrupts sampled during sleep mode?
2. How many states after an interrupt is sampled is sleep mode cleared?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
0	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock.
2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.)



1: SP-2
2: SP-4
3, 4: Interrupt vector address
5, 6: Saved PC and saved CCR
7, 8: Interrupt processing routine start address (contents of vector address)
Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is external memory)

Figure 1.9 Timing of Clearing Sleep Mode by Interrupt

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

Product	H8/300H	Q&A No.	QA300H-031A
Topic	Execution Time in Software Standby Mode		

Question

How many states are needed to transition to the software standby mode using a SLEEP instruction?

Classification—H8/300H	
	Software
	Registers
	Bus controller
	Interrupts
	Resets
0	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The time required to transition to the software standby mode is the time (states) required for the SLEEP instruction to execute. When the SLEEP instruction is stated in on-chip memory, it takes 2 states; when the SLEEP instruction is in external 8-bit 3-state-access space, it takes 6 states. The figure below shows the timing for execution of the SLEEP instruction. (See figure 1.10.)

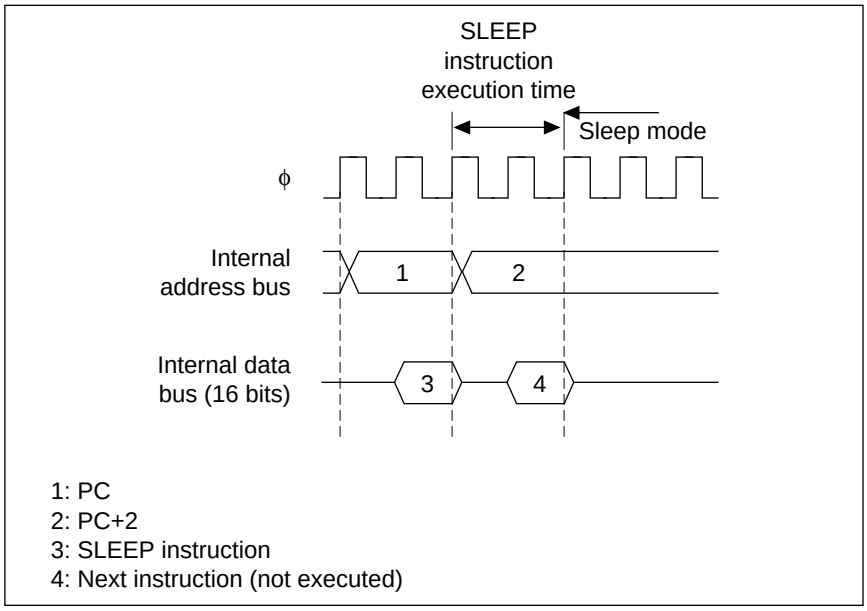


Figure 1.10 Sleep Instruction Timing

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-032A-1
Topic	Operation When an Interrupt is Requested During Execution or While Fetching a SLEEP Instruction		

Question

How does the H8/300H CPU operate when an interrupt comes in during a SLEEP instruction fetch or while a SLEEP instruction is executing?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
0	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Operation varies, depending on the time the interrupt request occurs, as shown below:

A. During SLEEP instruction fetch: The interrupt exception processing starts after the previous instruction finishes executing. The saved PC becomes the address of the SLEEP instruction. After returning from the interrupt service routine, the SLEEP instruction executes.

B. During SLEEP instruction execution (case 1): Interrupt exception processing starts without going through the sleep state. The saved PC becomes the address of the instruction after the SLEEP instruction. After returning from the interrupt service routine, the instruction after the SLEEP instruction executes.

C. During SLEEP instruction execution (case 2): The sleep mode is canceled 6 states later and the interrupt service routine starts. (See figure 1.11.)

Related Manuals

Manual Title

Other Technical Documentation

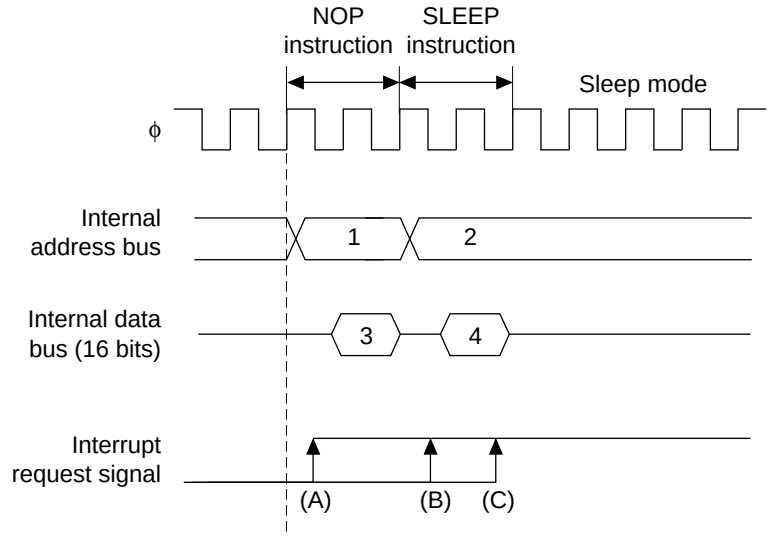
Document Name

Related Microcomputer Technical Q&A

Title

References

Product	H8/300H	Q&A No.	QA300H-032A-2
Topic	Operation When an Interrupt is Requested During Execution or While Fetching a SLEEP Instruction		
Answer			



1: SP
2: SP + 2
3: SLEEP instruction
4: Next instruction
Note: During H8/3003 (mode 2, 2-state access)

Figure 1.11 Timing When an Interrupt Request Occurs During SLEEP Instruction Fetch or Execution

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-033A
Topic	Support for the DAA (DAS) Instruction with the INC (DEC) Instruction		

Question

1. The DAA instruction can be used with an add instruction (ADD), but how about executing it after an INC instruction executes?
2. The DAS instruction can be used with a subtract instruction (SUB), but how about executing it after an DEC instruction executes?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
0	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. Execution of a DAA instruction after execution of an INC instruction is not supported, since the C and H flags do not reflect the results of the operation after INC instruction execution. To increment decimal data, execute a DAA instruction after adding 1 with the ADD instruction (ADD.B #1, Rd).
2. Execution of a DAS instruction after execution of an DEC instruction is not supported, since the C and H flags do not reflect the results of the operation after DEC instruction execution. To decrement decimal data, execute a DAS instruction after adding –1 with the ADD instruction (ADD .B #–1, Rd) and inverting the C and H flags (XORC #A0, CCR).

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Actual operation is determined by the flag state.

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-034A
Topic	BRA and BRN Instructions		

Question

1. What is the difference between BRA (BT) and JMP? Also, what does it mean for the condition to be "True"?
2. What does it mean for the BRN (BF) condition to be "False"?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
0	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. The BRA instruction can be used just like the JMP instruction, but differs in the following points:
   - It can only branch in the range +127 bytes to –128 bytes for d:8 and +32767 bytes to –32768 bytes for d:16.
   - If the relative values of objects do not change, the program can be relocated.
   - Execution states and instruction size are different.
   - Assembler format is different.

   A condition of True means that since this instruction always branches, the branch condition is always True.
2. A condition of False means that since this instruction never branches, the branch condition is always False.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	H8/300H	Q&A No.	QA300H-035A
Topic	BRN Instruction		

Question

What kind of instruction is BRN (BF)?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
0	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

BRN is a convenient instruction that replaces conditional branch instructions during debugging. It operates the same as the NOP instruction, but its size and execution time differ as described in table 1.5.

Table 1.5 The BRN Instruction

Instruction		Instruction Size (Bytes)	Instruction Execution Time (States)
BRN	d:8	2	4*
	d:16	4	6*
NOP		2	2*

Note: For a 16-bit bus/2-state access space or an instruction fetch from the on-chip ROM.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Like BRN, BRA (BT) is convenient to use during debugging.

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-036A
Topic	The SUBX Instruction		

Question

Why does the SUBX instruction (subtraction with carry) preserve the Z flag when the result of execution is 0?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
0	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The SUBX instruction is used to divide a subtraction operation into multiple subtractions. After the SUBX instruction is executed, the Z flag reflects the result of all of these operations (See figure 1.12.). It does not reflect the results of each individual SUBX instruction.

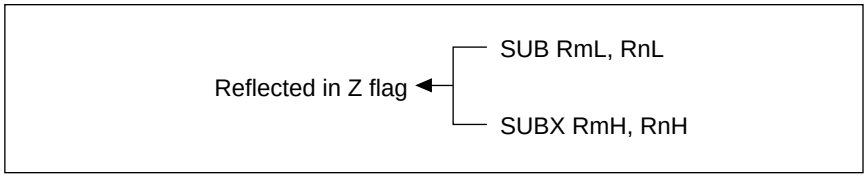


Figure 1.12 Z Flag

When the SUBX instruction results in a 0, the Z flag thus holds the result of the previous operation.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-037A
Topic	Odd Address Values During STC Instruction Execution		

Question

What is the odd address value when an STC instruction is executed and the CCR stored in an (register indirect) even address?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
0	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Undefined.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-038A
Topic	Interrupts and DMA Transfer Requests While the EEPMOV Instruction Is Executing		

Question

1. When an interrupt occurs during the execution of an EEPMOV instruction, what happens to that interrupt request?
2. What happens when a DMA transfer request occurs during the execution of an EEPMOV instruction?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
0	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. When an interrupt occurs during the execution of an EEPMOV.B instruction, the interrupt is held and accepted when the instruction finishes executing. It is handled the same as when an interrupt occurs during ordinary instruction execution. However, NMIs that occur during EEPMOV.W execution are accepted after transfer of the byte in transfer is completed. For interrupts other than NMIs, operation is the same as for EEPMOV.B.
2. The DMA transfer is executed between the read cycle and write cycle of the EEPMOV instruction.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 2.2.28 (items 1 and 2), EEPMOV, in the following manual:

- *H8/300H Series Programming Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-039A
Topic	The Difference Between EEPMOV.B and EEPMOV.W		

Question

What is the difference between EEPMOV.B and EEPMOV.W?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
0	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The transfer data size of both the EEPMOV.B and EEPMOV.W instructions is byte, but there are some differences, as described below.

- Size of register that counts the transfer bytes:
  EEPMOV.B: Byte (maximum number of transfer bytes is 255).
  EEPMOV.W: Word (maximum number of transfer bytes is 65535).
- Enable/disable of interrupt acceptance:
  EEPMOV.B: Accepted after instruction executes (all held).
  EEPMOV.W: NMI alone is accepted after transfer of byte in transfer is completed (all others held).

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 2.2.28 (1), (2) EEPMOV
- *H8/300H Series Programming Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-040A
Topic	Cautions on Stack Operation		

Question

Are there any particular cautions about stack operation to be aware of?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
0	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

On the H8/300H, the stack area is always accessed by word or longword. When the stack pointer is set to an odd number, malfunctions can result. Use the PUSH or POP instructions to stack. The initial value of SP (stack pointer) is undefined. It is initialized by the user.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 2.4.4 Inicial CPU Resistor, section 2.5.2 Memory Data Formats, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-041A
Topic	On-Chip Peripheral LSI Access When the Bus Is Released		

Question

Can external devices (bus master) access internal registers of the H8/300H when the H8/300H CPU has released the bus to an external device?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
0	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

No. Internal registers cannot be accessed from external devices.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-042A
Topic	Areas That Can Be Used as ROM by the Vector Table		

Question

1. Can the empty areas of the vector table (reserved by system or reserve) be used as ROM?
2. Can the empty areas of the I/O registers be used as ROM?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
0	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. The vector numbers reserved by the system (4–6) on the vector table cannot be used. Reserve addresses, however, can be used as ROM. Unused interrupt vector addresses on the vector table can also be used.
2. The empty areas of the I/O registers cannot be used.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Items reserved by the system are used by development tools. Addresses reserved by the system and reserve addresses are listed in the manual. Branch address areas of "memory indirect" addressing can use addresses other than those reserved by the system or those of used by the vector table.

Technical Questions and Answers

Product	H8/300H	Q&A No.	QA300H-043A
Topic	Pin State During the Oscillation Settling Time		

Question

What are the pin states during oscillation settling time after the software standby mode is cleared?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
0	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The same as in the software standby mode.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-101-1
Topic	Receiving DMAC Startup Requests		

Question

When a DMA controller startup request occurs:

1. When is the request forced to wait?

2. Is the request accepted under the following conditions?
   - During EEPMOV execution
   - During read-modify-write instruction execution
   - During DMAC cycle steal transfers.

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. The bus arbiter priority order is: external bus master > refresh controller > DMAC > CPU. This means that DMA requests are not accepted when an external bus master or refresh controller with a priority higher than the DMAC has the bus. Since the DMAC channels have the priorities (for H8/3003) shown in table 2.1, the request waits when a higher priority channel is transferring.

Table 2.1 DMAC Channel Priority

Short Address Mode	Full Address Mode	Priority
Channel 0 A Channel 0 B	Channel 0	Highest
Channel 1 A Channel 1 B	Channel 1	
Channel 2 A Channel 2 B	Channel 2	
Channel 3 A Channel 3 B	Channel 3	Lowest

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-101-2
Topic	Receiving DMAC Startup Requests		

Answer

2. During EEPMOV execution, requests are accepted between the read cycle and the write cycle. During read-modify-write instruction execution, requests are accepted between the read cycle, instruction fetch, and the write cycle. During cycle steal transfers, requests are accepted if the channel of the transfer request is higher in priority than the current channel.

References

1. BSET, BCLR, BNOT, BST and BIST are read-modify-write instructions.
2. When the wait is longer than those described above, wait states may have been inserted by a CPU bus cycle that has a DREQ request. (See figure 2.1.)

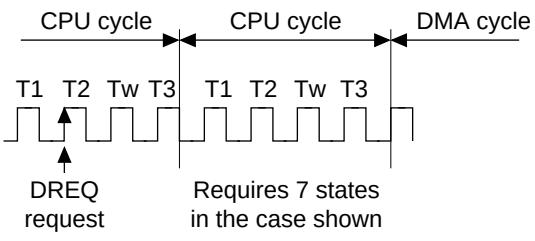


Figure 2.1 Wait State Insertion

Product	Common	Q&A No.	QA300H-102
Topic	Addresses During DMA Transfers		

Question

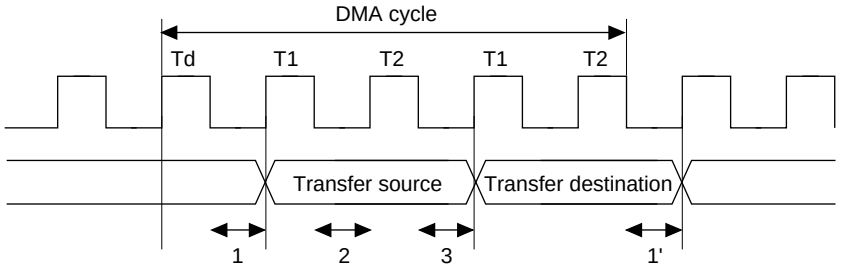
Doesn't the CPU cause problems in DMAC operation if it reads the MAR (memory address register) during DMA transfers?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Reading the MAR does not have any affect on DMA operation. However, when longword data is read, a DMA cycle can enter in between reading of the top 16-bits of data and the bottom 16-bits of data, as described in the manual. As a result, the value read may differ from the actual value. The timing at which the MAR is updated is shown in figure 2.2.



1. MAR updated at transfer source.
2. Counter updated.
3. MAR updated at transfer destination

Note: MAR also updated at transfer source at 1' (during burst transfers and in the block transfer mode).

Figure 2.2 MAR Update Timing

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

There should be no mistake in the value read so long as the bottom 16-bit (MARH, MARL) value is read with the MOV.W instruction.

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-103
Topic	$\overline{\text{TEND}}$ Signal Output Timing 1		

Question

Is the $\overline{\text{TEND}}$ signal output at every byte/word transfer?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The $\overline{\text{TEND}}$ signal is output when the startup source is an external request (using the $\overline{\text{DREQ}}$ pin). In operating modes other than block transfer mode, the $\overline{\text{TEND}}$ signal is driven low during the final transfer write cycle. For block transfers, it is low during the write cycle just before the end of a 1 block transfer. It is not output at every byte/word. (See figure 2.3.)

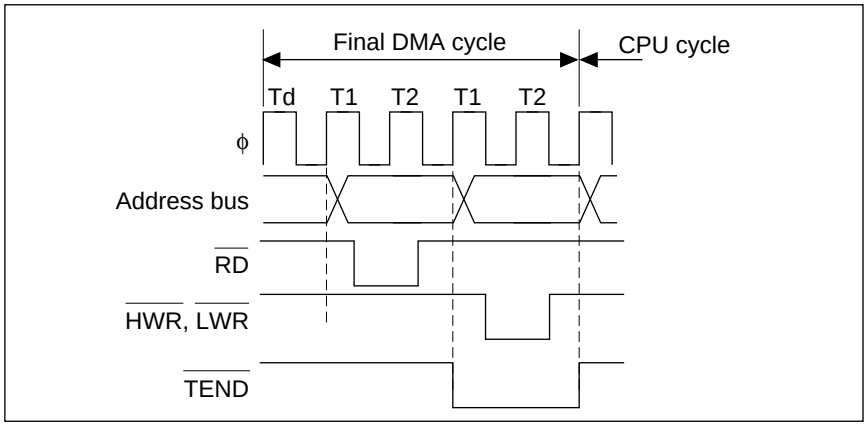


Figure 2.3 $\overline{\text{TEND}}$ Output

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-104
Topic	$\overline{\text{TEND}}$ Signal Output Timing 2		

Question

At what timing is the $\overline{\text{TEND}}$ signal output?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The $\overline{\text{TEND}}$ signal is output in the write cycle when the ETCR (transfer count register) becomes H'00. Figure 2.4 illustrates the timing.

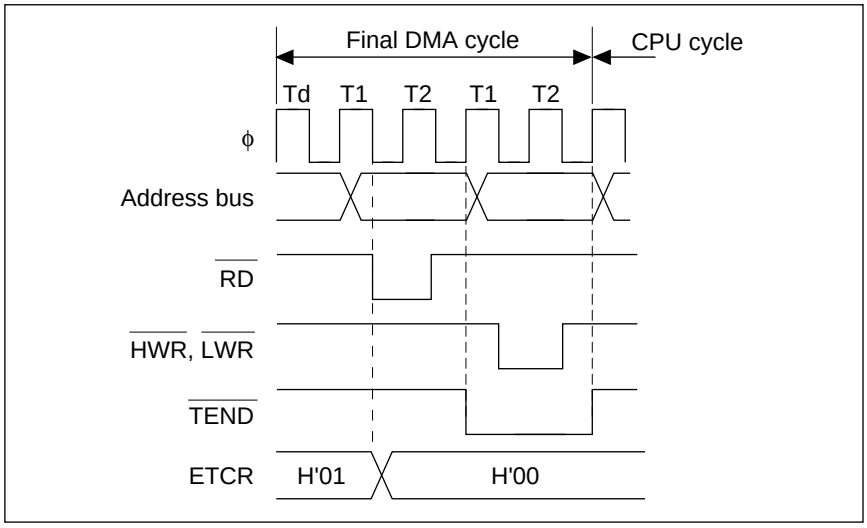


Figure 2.4 $\overline{\text{TEND}}$ Output Timing

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-105
Topic	The Relationship Between the DMAC's DTE and DTIE Bits		

Question

When the DTIE (data transfer interrupt enable) bit is 1 and the DTE (data transfer enable) bit is then cleared to 0, the manual says that an interrupt is requested of the CPU.

1. Will DMA transfer end interrupts occur continuously, as shown in figure 2.5?
2. If so, what can be done to keep interrupts from occurring?

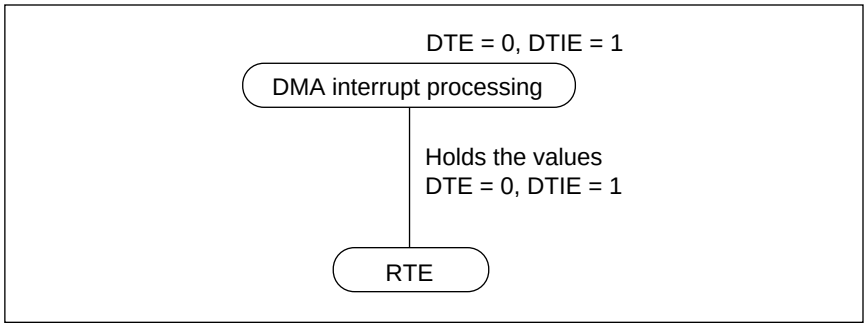


Figure 2.5 Continuous Interrupts from DTE and DTIE

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. Yes, interrupts will occur continuously.
2. If DTE = 0 and DTIE = 1 (enabling interrupts), interrupts will always be produced. To prevent this, set DTE to 1 (the BSET instruction can be used), or clear the DTIE bit to 0 (the BCLR instruction can be used).

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-106
Topic	DMAC Startup		

Question

When the DMAC is started up with an ITU compare match interrupt, what happens if the I (interrupt mask) and UI (user bit/interrupt mask) of the CCR (condition code register) are masked?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Interrupts selected as DMAC startup sources are not affected by the CPU's interrupt mask bits (I and UI bits). (See figure 2.6.)

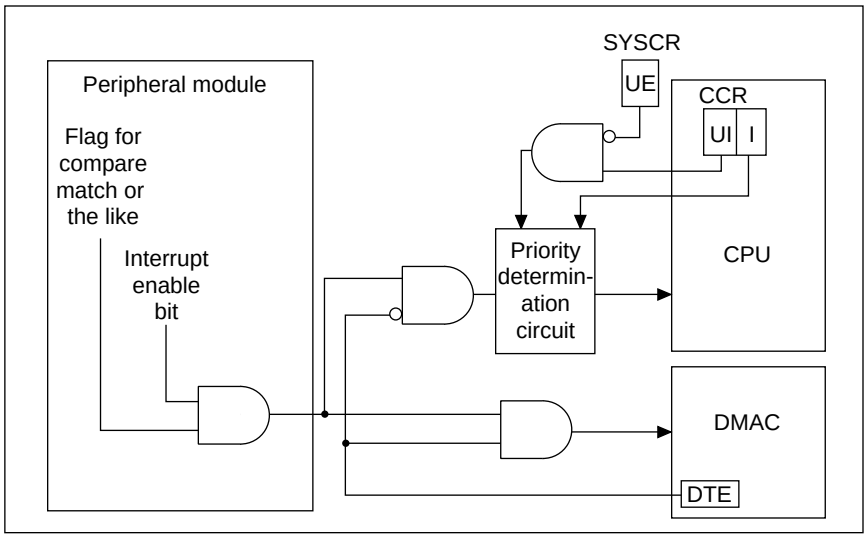


Figure 2.6 DMAC Startup

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

When an interrupt is disabled with an interrupt enable bit in a module, interrupts will not occur for either the DMAC startup request or the CPU.

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-107
Topic	The DMAC and Timer Interrupts		

Question

When the DMAC startup source has compare-matched the ITU, is an interrupt produced to the CPU of the ITU?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Interrupt requests selected as startup sources startup the DMAC when the DTE (data transfer enable) bit of the DMAC's DTCR (data transfer control register) is set to 1, and no interrupt is generated to the CPU.

When the DTE bit is 0, no startup request is generated and an interrupt goes to the CPU. An interrupt that is used as a startup source cannot simultaneously generate an interrupt to the CPU.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-108
Topic	Operation After a DMAC End Interrupt Is Generated 1		

Question

When the transfer count register becomes H'0000 while the DMAC is in use and an end interrupt is generated:

1. When is the next transfer request accepted?
2. Are transfer requests generated before the DMA transfer starts ignored?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. The next transfer request is accepted when the DTE (data transfer enable) bit is set to 1 by software. When the transfer count register reaches H'0000 and a transfer end interrupt is generated, the DTE bit of the DTCR (data transfer control register) is cleared and data transfer is disabled. To do another transfer, set the transfer count register during the end interrupt routine and then set the DTE bit to 1.
2. When the startup request is an internal interrupt, a CPU interrupt is requested when the DTE bit is 0. For more information, see the hardware manual. When the startup request is an external request, it is ignored if it is an edge.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 8.6, Cautions on Use, in the following manuals:

- *H8/3002 Hardware Manual*
- *H8/3003 Hardware Manual*
- *H8/3042 Series Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-109
Topic	Operation After a DMAC End Interrupt Is Generated 2		

Question

When the transfer count register becomes H'0000 while the DMAC is in use and the transfer ends, when is the transfer end interrupt generated?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

After the transfer ends, an interrupt request is generated and the bus is released. When the CPU captures the bus, the transfer end interrupt is performed after the executing instruction ends. (See figure 2.7.)

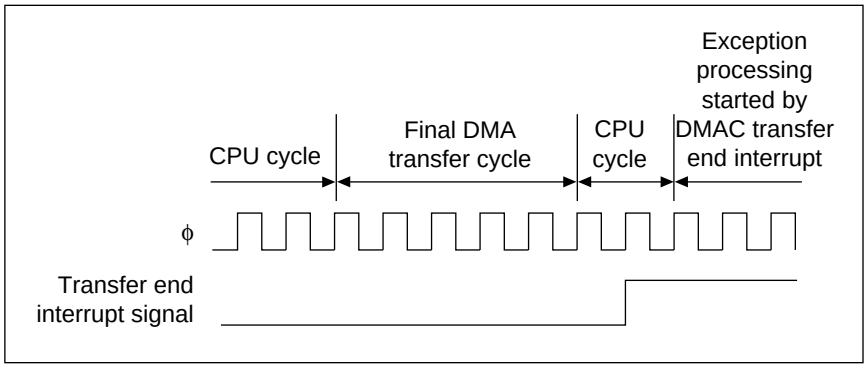


Figure 2.7 Timing at DMAC End Interrupt

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-110
Topic	DMA Transfers Started up by Serial Transfers		

Question

Can more than 256 transfers be done between memory and I/Os when SCI and DMAC are used together to send and receive?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

When the DMAC is started up by the SCI, I/O mode should be used. The maximum number of transfers allowed will then be 65,536. To transfer more data than this, data must be stored in memory and the transfer counter reset with a transfer end interrupt.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-111
Topic	Time Until DMAC Startup by the $\overline{\text{DREQ}}$ Pin		

Question

Why is 4 states the minimum time to startup the DMAC from the $\overline{\text{DREQ}}$ pin?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The delay time from the $\overline{\text{DREQ}}$ pin to the internal DMAC module is 2 states. The bus arbiter internal processing time is also 2 states. This means a minimum of 4 states (the sum of these figures) is required.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-112
Topic	Reverse Operation in the DMA Repeat Mode		

Question

What do I do to pause a DMA transfer that uses repeat mode and then start it up in the opposite direction?

Classification—H8/300H	
	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The flowchart in figure 2.8 illustrates the process.

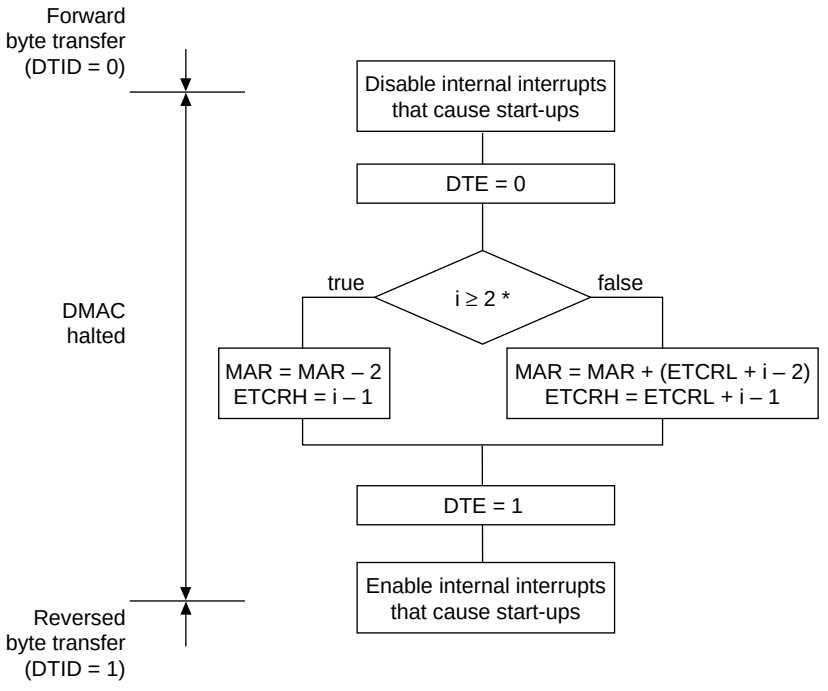


Figure 2.8 Reverse Operation in the DMA Repeat Mode

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-113
Topic	Use of Dual-Function Pins		

Question

When the DMAC is used under the following conditions, can the $\overline{\text{TEND}}/\overline{\text{CS}}$ dual-function pin be used as a $\overline{\text{CS}}$ output?

Conditions: Full-address transfer mode, external request (low level input from $\overline{\text{DREQ}}$ pin) for the startup source.

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

It cannot be used as a $\overline{\text{CS}}$ output. When external request is selected as the startup source, the $\overline{\text{TEND}}/\overline{\text{CS}}$ dual-function pin concerned becomes a $\overline{\text{TEND}}$ output pin. For more information, see the I/O Port section in the hardware manual.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

See section 9, I/O Ports, in the following manual:
- *H8/3003 Hardware Manual*

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-114
Topic	I/O Ports and the $\overline{\text{DREQ}}$ Pin		

Question

1. How should the DTE (data transfer enable) bit of the DTCR (data transfer control register) be set to use pins that are used both as $\overline{\text{DREQ}}$ pins and I/O ports as I/O ports?
2. How should dual-function pins be set for use as $\overline{\text{DREQ}}$ pins?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
0	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. They can be used as I/O ports without regard to the DTE bit.
2. To use dual-function pins as $\overline{\text{DREQ}}$ pins, clear the DDR (data direction register) of affected ports to 0. When the DDR is set to 1, port output is detected as $\overline{\text{DREQ}}$ input.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-115
Topic	PWM Mode and Interrupts		

Question

When the ITU is used in the PWM mode and interrupts are enabled, is it necessary to clear the IMFB (input capture/compare match flag B) of the TSR (timer status register) to 0 within the interrupt processing routine or is the IMFB automatically cleared when an IMIB interrupt is generated?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
0	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The IMFB flag must be cleared to 0 within the interrupt processing routine. The timing when the flag is cleared by the program is shown in figure 2.9.

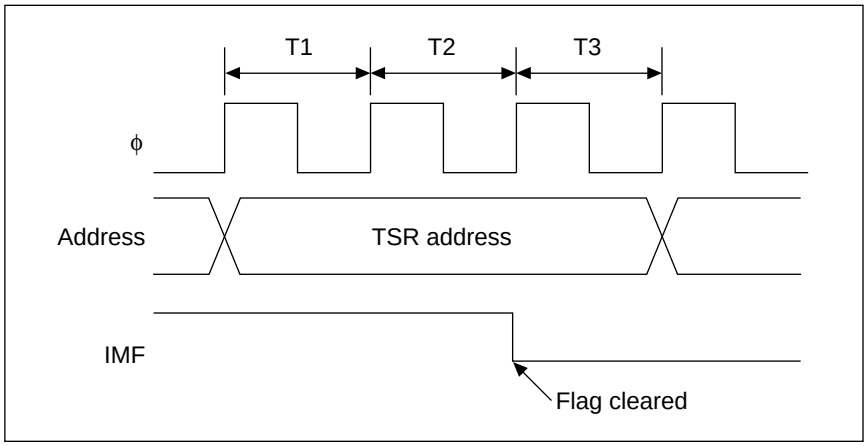


Figure 2.9 IMFB Flag

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

To clear the IMFB flag, use the BCLR instruction.

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-116
Topic	Clearing the Counters		

Question

How do I clear the ITU counter using software?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
0	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Clear the TCNT (timer counter) by writing H'0000 to it. The counter value is not cleared by rewriting the TSTR (timer start register).

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-117
Topic	Pulse Output From the ITU		

Question

How do I get a specific number of pulses output (say, 10) and then stop the pulse output?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
0	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

1. When 1 DMAC channel can be used: Pulses are output in the ITU's PWM mode. *In this case, the DMAC is started up by an ITU compare match.* Set DMA transfers for 10 and generate a transfer end interrupt to stop the ITU. This DMA transfer is aimed at starting up 10 times; set the data transfer so that it does not affect CPU operation (transfer data, transfer source address, transfer destination address).

2. When other timers can be used: Output pulses are input to the TCLK pin (clock input pin) and events counted by another timer (x). When the timer (x) compare register reaches a count of 10, a compare match interrupt is generated and the ITU stops. On the H8/300H, TIOCA0/TCLKC and TIOCB0/TCLKD are dual-function pins. For this reason, no extra wiring needs to be added on the board to output pulses from channel 0 and use TCLKC and TCLKD as input pins.

3. When using software: Generate compare match interrupts each time and count with the interrupt processing routine.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-118
Topic	ITU Cascade Connections		

Question

Can cascade connections be used with the ITU?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
0	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10.

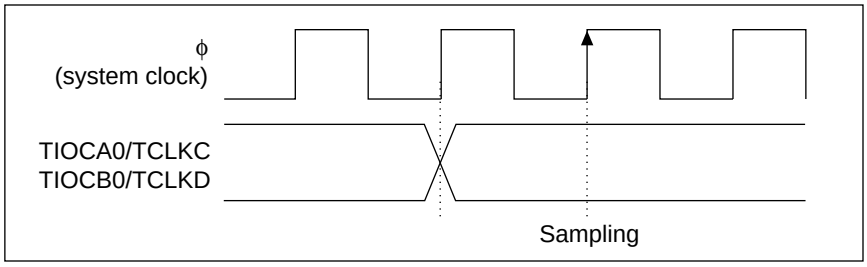


Figure 2.10 ITU Count Timing

When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next ϕ.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-119
Topic	Setting the ITU's PWM Output		

Question

When the ITU is used in PWM mode, how should the TIOR (timer I/O control register) be set?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
0	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

The TIOR setting does not affect PWM output. When the PWM mode is set with the PWM bit of the TMDRs (timer mode registers) located in each of the channels of the ITU, GRA/GRB are used as output compare registers for output setting, regardless of the contents of the TIOR.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-120-1
Topic	ITU Output and Port Output		

Question

When the ITU is set to toggle output on a GRB (output capture/input compare dual-function register B) compare match to get the output shown in figure 2.11, what kind of value is output when changing from port output to ITU output?

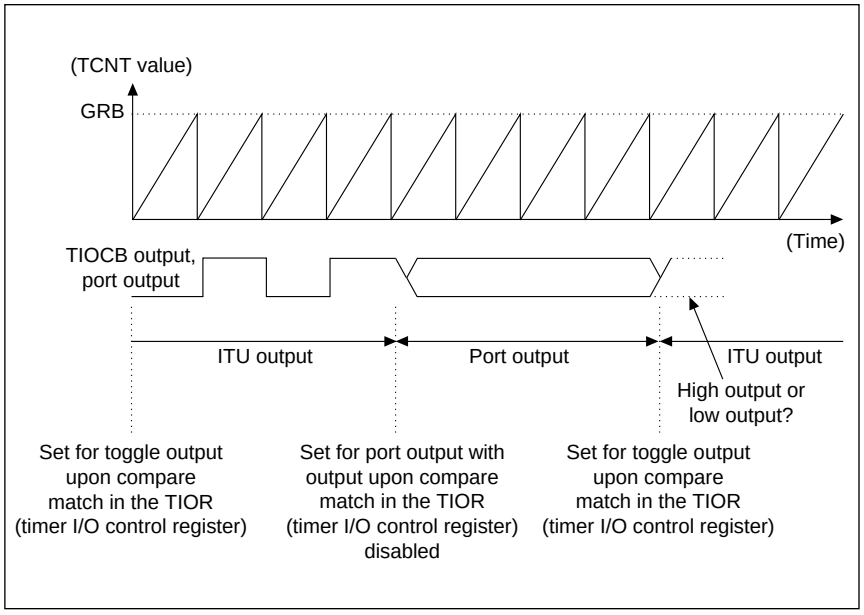


Figure 2.11 ITU Output and Port Output (Q)

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
0	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-120-2
Topic	ITU Output and Port Output		

Answer

1. When port output is changed to ITU output, the value from before the change is output.
2. When a compare match signal is generated at the point when the port output is to be changed to ITU output, the value changes. (See figure 2.12.)

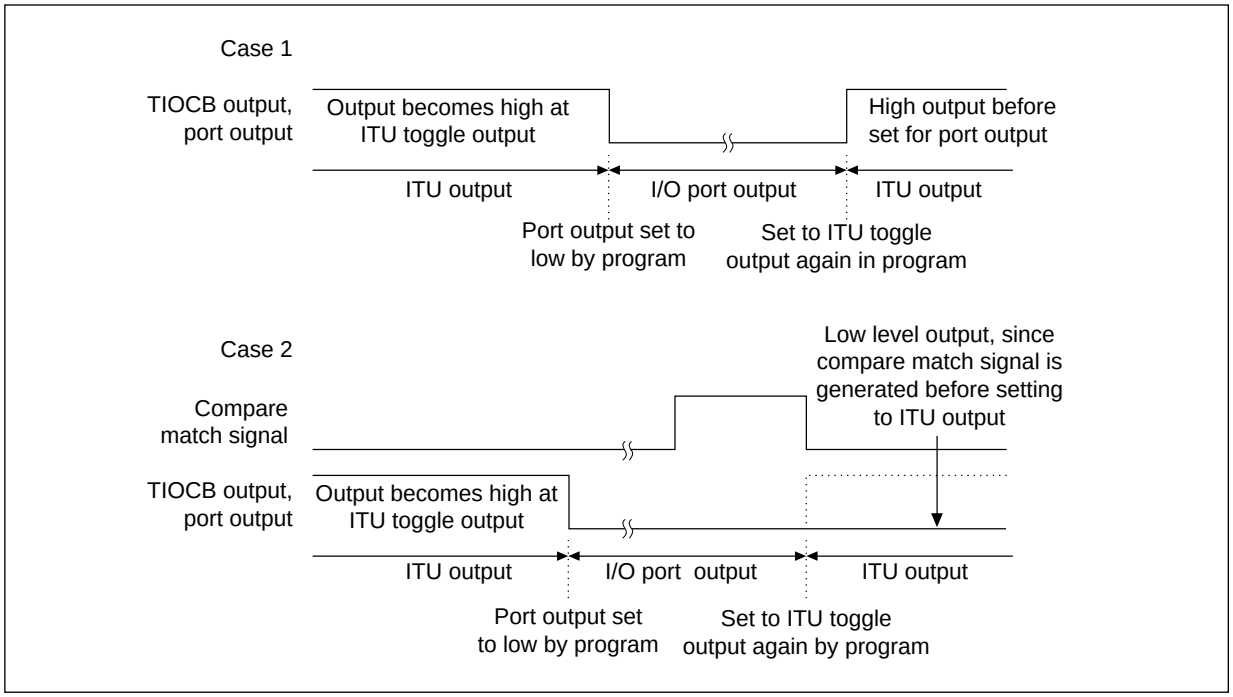


Figure 2.12 ITU Output and Port Output (A)

References

1. When the ITU was started after a reset, the TIOCn output is low until the first compare match occurs.
2. When set to input capture and output is disabled, the output level changes when an input capture occurs.

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-121-1
Topic	ITU Settings		

Question

Please explain in detail the pulse width, cycle settings and register settings for ITU pulse output as well as the relationship to the internal clock.

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
0	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

When outputting pulses in the PWM mode, the duty can be found from the following equation.

Duty = n + 1 / N + 1
where GRA = n (set the counter value corresponding to the Low width – 1), and
GRB = N (set the counter value corresponding to the cycle – 1)

Example: When the operating frequency is 10 MHz, the internal clock for the count is $\phi/2$ and GRB = 9, so to get a duty of 50% (with an N of 9):

(n + 1)/(9 + 1) = 0.5

GRA must be set to 4. The exact timing is shown in figures 2.13 to 2.16.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-121-2
Topic	ITU Settings		
Answer			

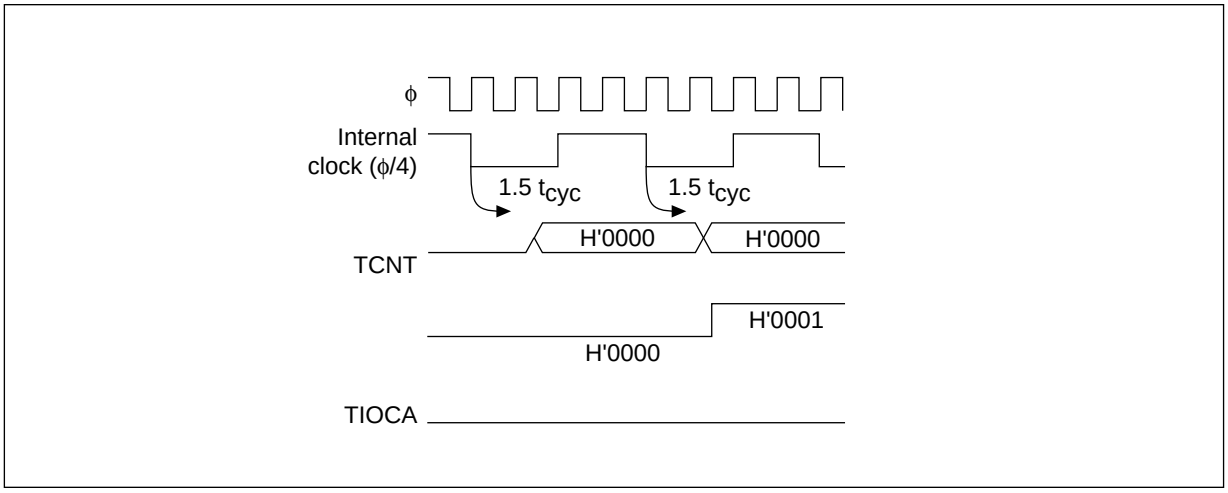


Figure 2.13 ITU Settings (1)

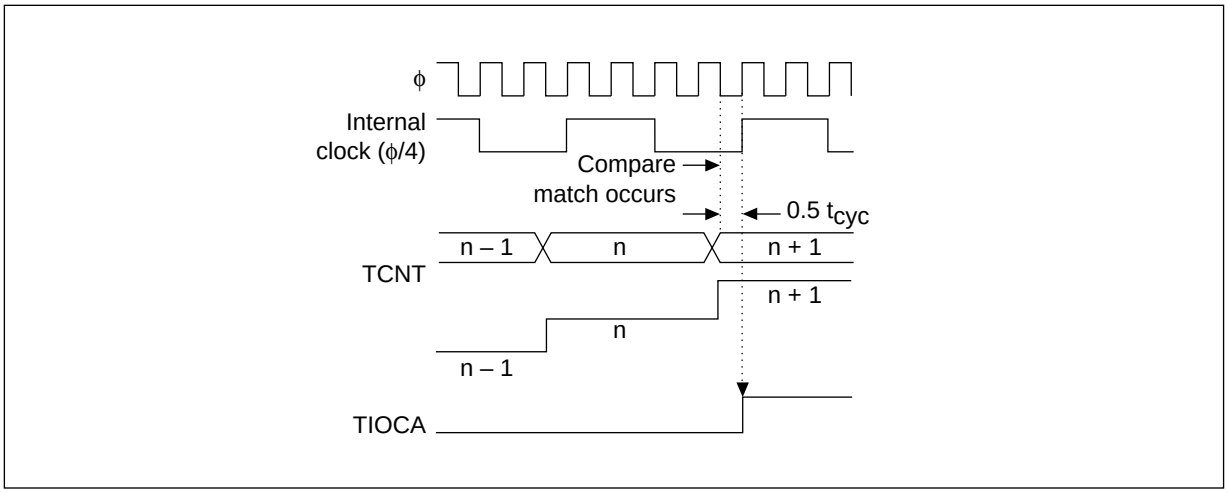


Figure 2.14 ITU Settings (2)

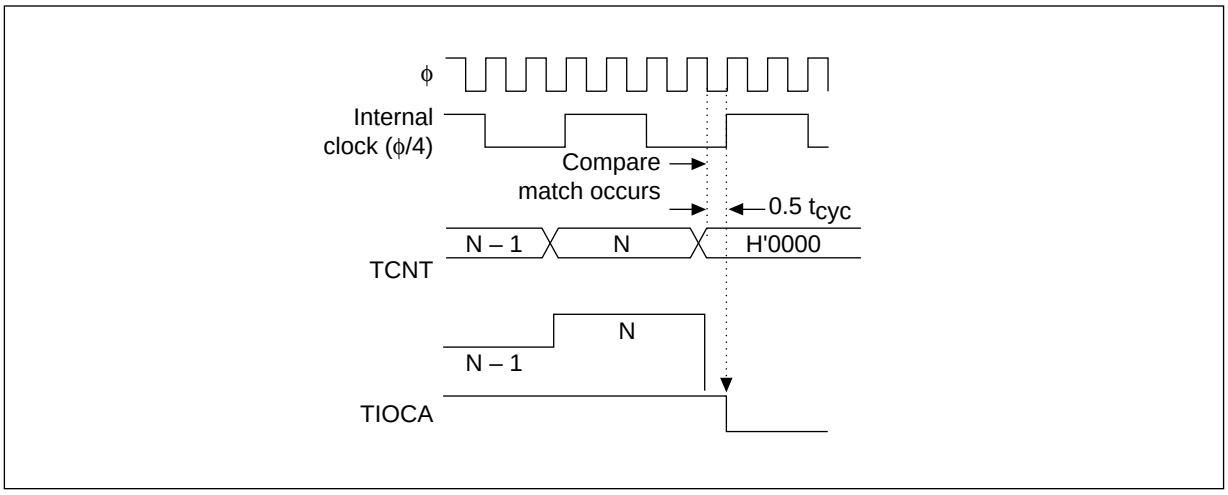


Figure 2.15 ITU Settings (3)

Product	Common	Q&A No.	QA300H-121-3
Topic	ITU Settings		
Answer			

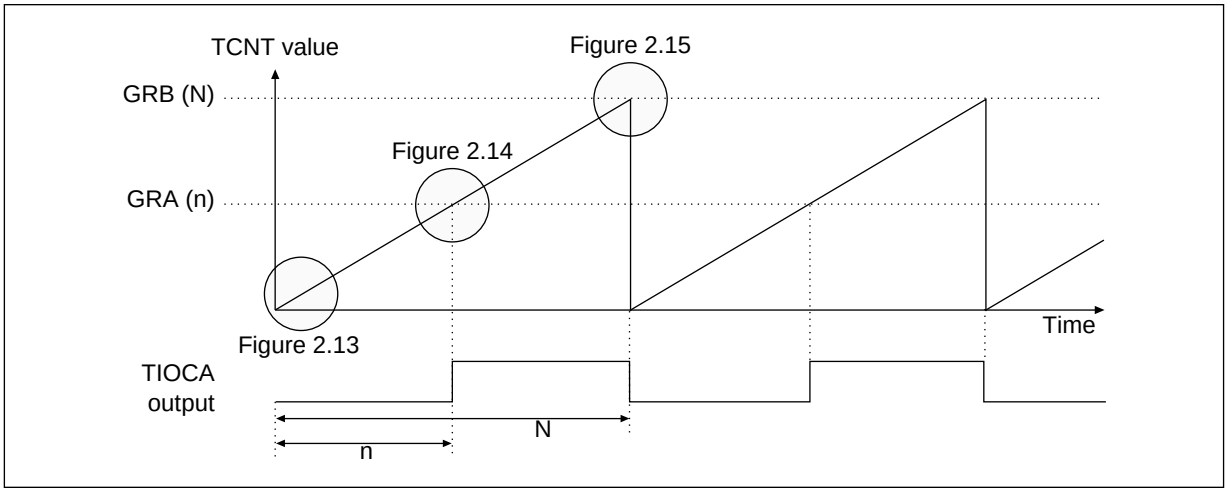


Figure 2.16 ITU Settings (4)

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-122
Topic	Independent Operation of TCNT4 Using Reset-Synchronized PWM Mode		

Question

The manual states that "TCNT4 runs independently" when reset-synchronized PWM mode is used. Do this mean it can be used for other purposes?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
0	ITU
	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

Reset-synchronized PWM mode uses channel 3 and 4 together, but the only counters and registers it uses are TCNT3, GRA3, GRA4, GRB3 and GRB4. This allows TCNT4 to be used independently. One way to use it might be to run it as an interval timer using counter overflows.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-123
Topic	Halting the WDT's System Clock		

Question

When the system clock is halted, does the WDT (watchdog timer) detect abnormalities?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
0	Watchdog timer
	SCI
	A/D converter
	I/O ports

Answer

When the system clock of the entire LSI is halted, the WDT count stops as well, so it cannot detect abnormalities.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-124
Topic	Using the RDR and TDR When the SCI Is Not Being Used		

Question

When the SCI is not being used:

1. Can the RDR (receive data register) be used as a data register?
2. Can the TDR (transmit data register)?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

Yes and No.

1. The RDR cannot be used as a data register because it is a read-only register.
2. The TDR can be used as a data register.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-125
Topic	I/O Settings of Clock Pins for the SCI		

Question

When the SCI is being used, does the DDR (data direction register) of the port for the SCK (serial clock) pin set the I/O specification for that pin?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

The I/O direction for the SCK pin when the SCI is being used is specified by the C/$\overline{A}$ bit (communications mode) of the SMR (serial mode register) and the CKE1 and CKE0 (clock enable) bits of the SCR (serial control register). Setting the DDR of the port is not necessary.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-126
Topic	Serial I/O Pin State		

Question

After using the dual-function pins that can be used as I/O ports (TXD, RXD and SCK) as SCI pins, I reset them as I/O ports with the SCR (serial control register) and SMR (serial mode register). What happens to the values of the DDR (data direction register) pins when this happens?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

SCI operation does not affect the contents of the DDR of the I/O port. This means that in the case described above the DDR holds the value it had before being set as an SCI pin.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-127
Topic	Simultaneous Transmission and Reception with the SCI		

Question

When the SCI is being used, can transmission using the internal clock occur simultaneous with reception on the external clock (or vice versa)?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

Only 1 clock source can be selected as the SCI transfer clock. This prevents simultaneous transmission and reception using 2 types of clocks. Simultaneous transmission/reception using the same clock is possible.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-128
Topic	RDRF		

Question

What happens if, when clearing the RDRF (receive data register full) flag of the SSR (serial status register) to 0 during SCI reception, it is cleared to 0 directly without first reading a 1?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

It will not be cleared. When the BCLR instruction is used, the SSR is first read in byte units, then the bit that corresponds to the RDRF flag is cleared to 0 and a write occurs, again in byte units. While the RDRF flag is set to 1 (RXI interrupt processing routine), the BCLR instruction thus cannot clear the RDRF flag.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-129-1
Topic	Setting for Asynchronous Transmission		

Question

Asynchronous transmission uses the SCI. How do I set it to do a transfer by software (i.e., using the data empty interrupt (TXI) but not the DMAC)?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

When the TDRE = 1, the data empty interrupt is always generated and the TIE is set to 1. There are thus 2 methods.

1. Setting the first byte with an interrupt processing routine:
   Rn ← 0 (transfer counter)
   TE = 1 (transfer enable)
   TIE = 1 (empty interrupt enable)

2. Setting the first byte with the initialization:
   Rn ← 1 (transfer counter)
   TE = 1 (transfer enable)
   First byte set to TDR
   TDRE cleared (transfer starts, TDRE = 1 after TDR → TSR
   TIE = 1 (empty interrupt enable)

In either case, the TXI interrupt processing routine is as shown in the figure 2.17.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-129-2
Topic	Setting for Asynchronous Transmission		
Answer			

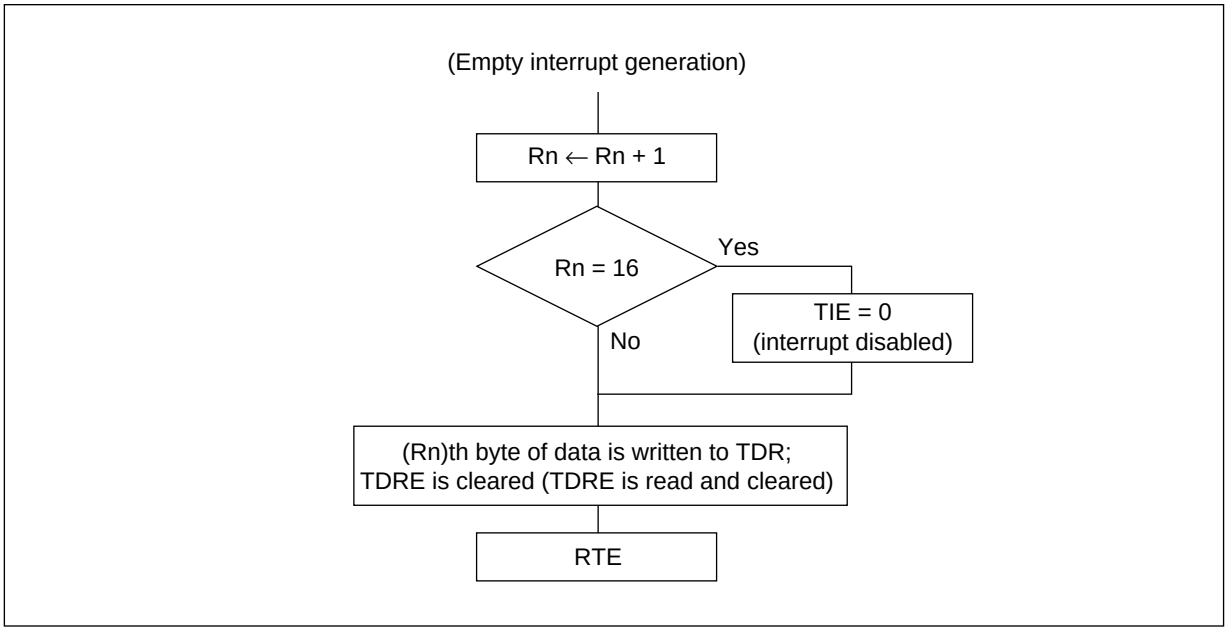


Figure 2.17 TXI Interrupt Processing Routine

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-130-1
Topic	How Data Is Transferred to the TDR		

Question

Are there ways, when transferring transfer data located in 16-bit bus space to the SCI's transmit data register (TDR, length 8 bits) as shown in figure 2.18, to:

1. Transfer using software?
2. Use the DMAC?

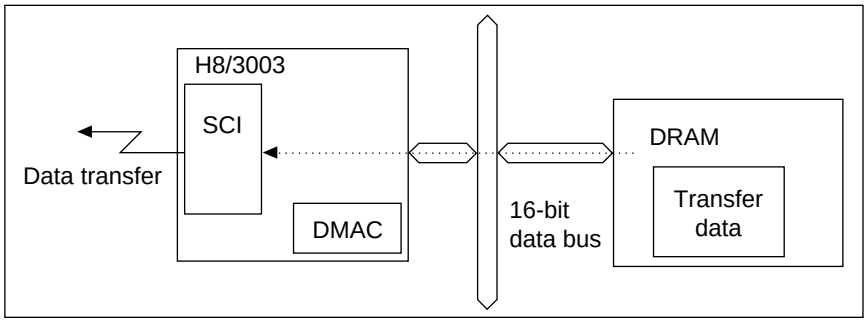
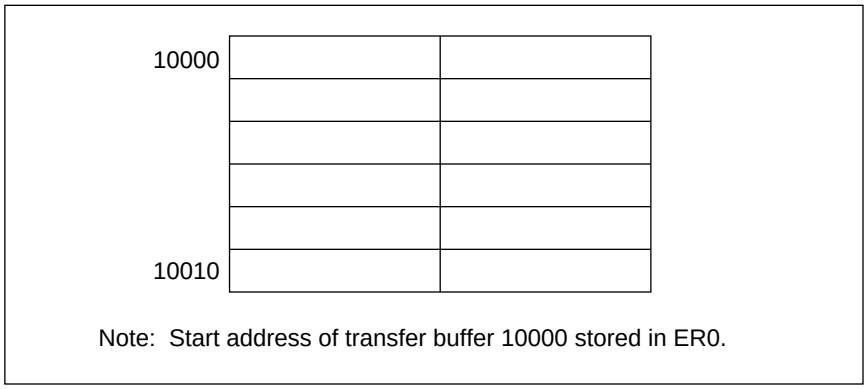


Figure 2.18 Transferring Data to the TDR

Answer

1. 16-bit bus spaces can be accessed in byte units. Read transfer data on the DRAM *1 byte at a time* and transfer it to the SCI's TDR. To transfer data stored in the transfer buffer, do as shown in figure 2.19.



Note: Start address of transfer buffer 10000 stored in ER0.

Figure 2.19 Transfer Buffer

References

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

Product	Common	Q&A No.	QA300H-130-2
Topic	How Data Is Transferred to the TDR		

Answer

```
LOOP:          MOV.B   #12,R2L      Set the number of transfer words
               Waiting for interrupt Can be placed in the sleep mode
               DEC.B   R2L          Copy the transfer data (1 byte) to
                                    R3L and increment the transfer
                                    buffer pointer (ER0) by 1

               BNE     LOOP         Continue until the transfer
                                    counter hits 0
TxI Interrupt: MOV.B   @ER0+,R3L    Transfer the transfer data to the
                                    SCI's TDR
               MOV.B   R3L,@TDR     Decrement transfer counter by 1
               BCLR    #7,@SSR      Clear TDRE to 0
               BNE     LOOP         Return to main routine
```

2. Using the DMAC: Start up the DMAC with the SCI's TXI interrupt and transfer the transfer data on DRAM 1 byte at a time to the SCI's TDR. Byte needs to be specified as the size in the DMAC. (Word size transfers are impossible, since they start up the DMAC at every transmission of a byte.)

References

The bus controller function can be used to enable word-sized transfers as shown in figure 2.20. For each read cycle (16-bit data), 2 consecutive write cycles of 8-bit data are necessary.

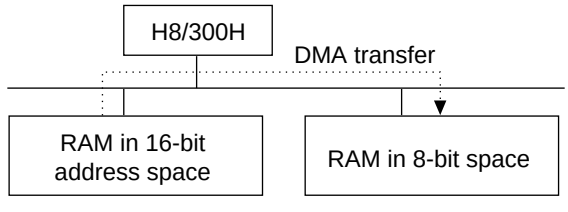


Figure 2.20 Using the Bus Controller Function to Enable Word-Sized Transfers

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-131A-1
Topic	Timing of Setting RDRF		

Question

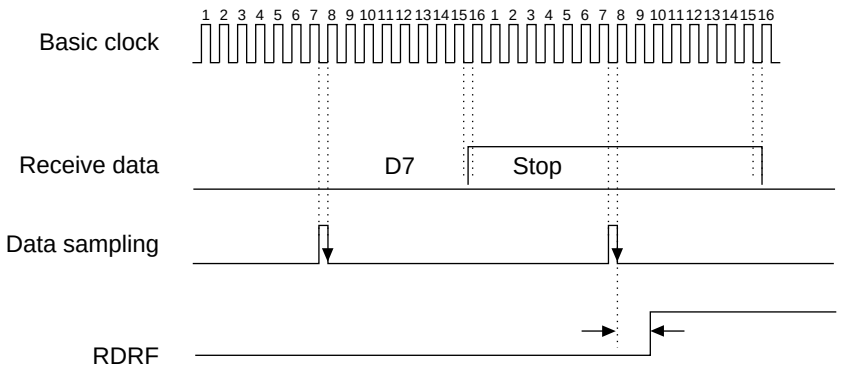
1. When data reception ends, the RDRF (receive data register full) flag of the SSR (serial status register) is set to 1. At what point in the asynchronous mode is the RDRF set?
2. When is it set in clock-synchronous mode?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

1. The RDRF flag is set after the MSB data is received and the data sampling clock falls. (See figure 2.21.)



Note: When SCK clock source is the internal clock, 0.5 basic clocks + 2 states. When SCK clock source is an external clock, 3-4 states.

Figure 2.21 8-Bit Data, 1 Stop Bit

Related Manuals

Manual Title

Other Technical Documentation

Document Name

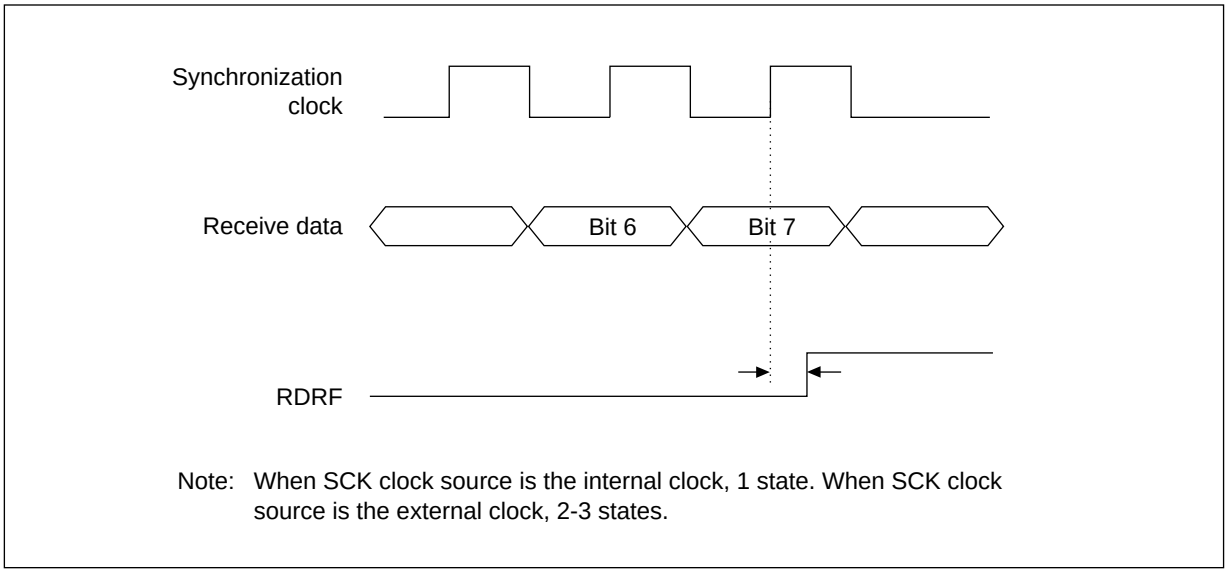
Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-131A-2
Topic	Timing of Setting RDRF		
Answer			

2. The RDRF flag is set after the MSB data is received and synchronization clock rises. (See figure 2.22.)



Note: When SCK clock source is the internal clock, 1 state. When SCK clock source is the external clock, 2-3 states.

Figure 2.22 8-Bit Data

Product	Common	Q&A No.	QA300H-132A-1
Topic	Timing of Setting TDRE		

Question

1. When 8-bit data transmission ends, the TDRE (transmit data register empty) flag of the SSR (serial status register) is set to 1. At what point in the asynchronous mode is the TDRE set?
2. When is it set in clock-synchronous mode?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

The TDRE flag is set at different times when there is transmission data in the TSR (transmit shift register) and when there is not.

1. Asynchronous mode. (See figure 2.23.)

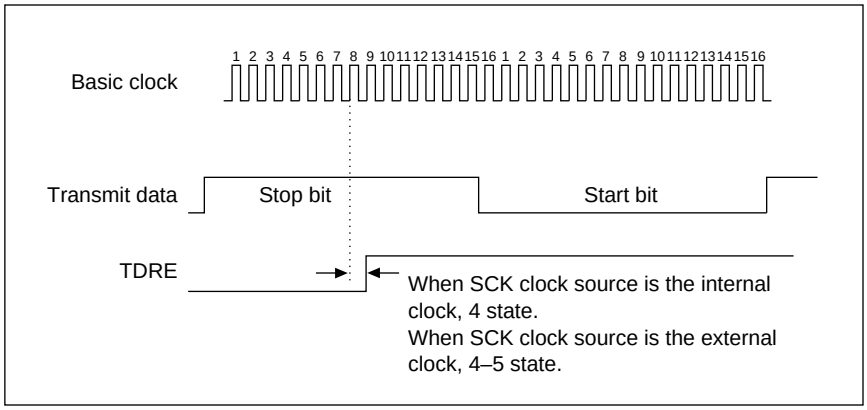


Figure 2.23 Transmit data in TSR (Asynchronous mode)

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Product	Common	Q&A No.	QA300H-132A-2
Topic	Timing of Setting TDRE		
Answer			

The start of transmission according to the setting of the TE (transmit enable) bit also follows this timing. (See figure 2.24.)

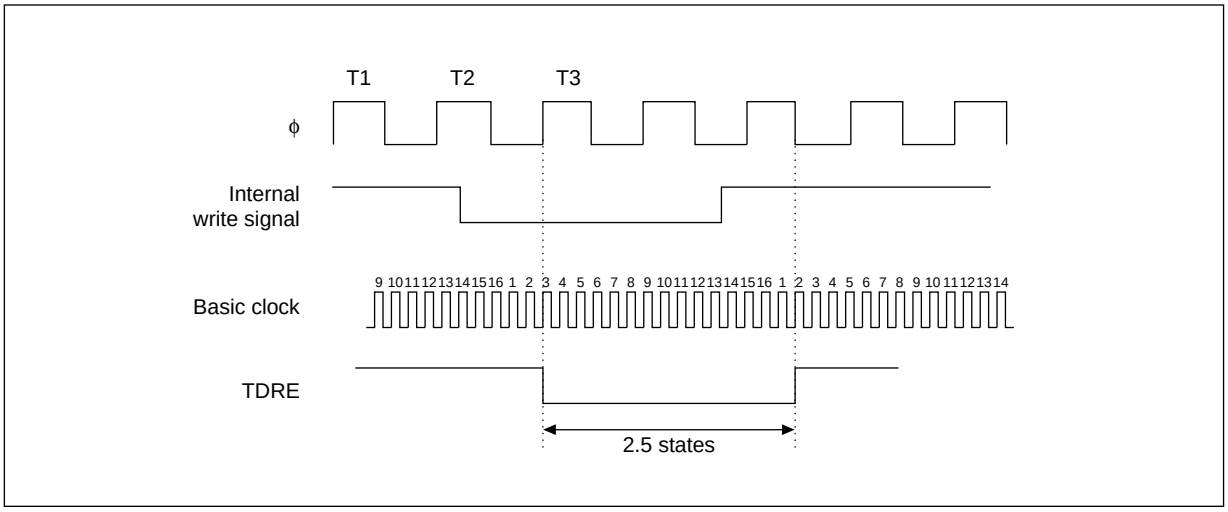


Figure 2.24 No transmit data in TSR (Asynchronous mode)

2. Clock-synchronous mode (See figures 2.25 and 2.26.)

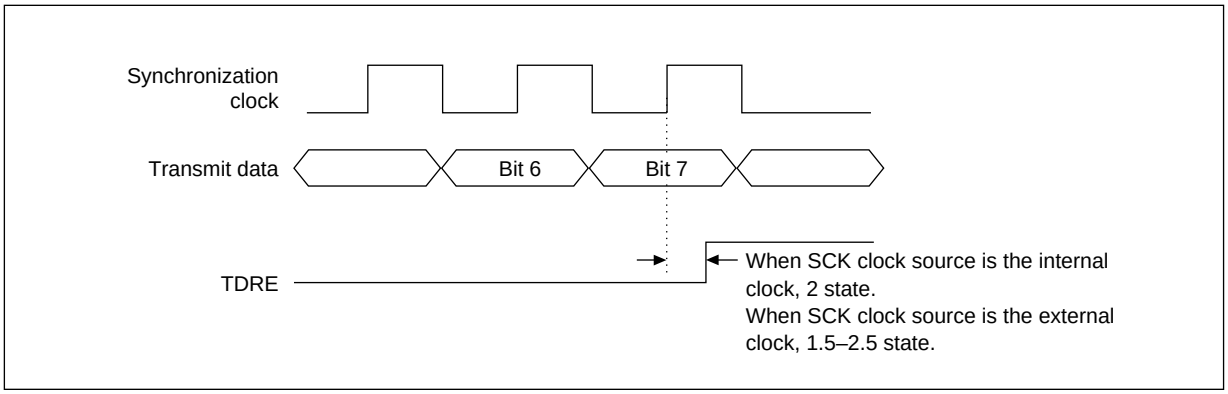


Figure 2.25 Transmit data in TSR (Clock-synchronous mode)

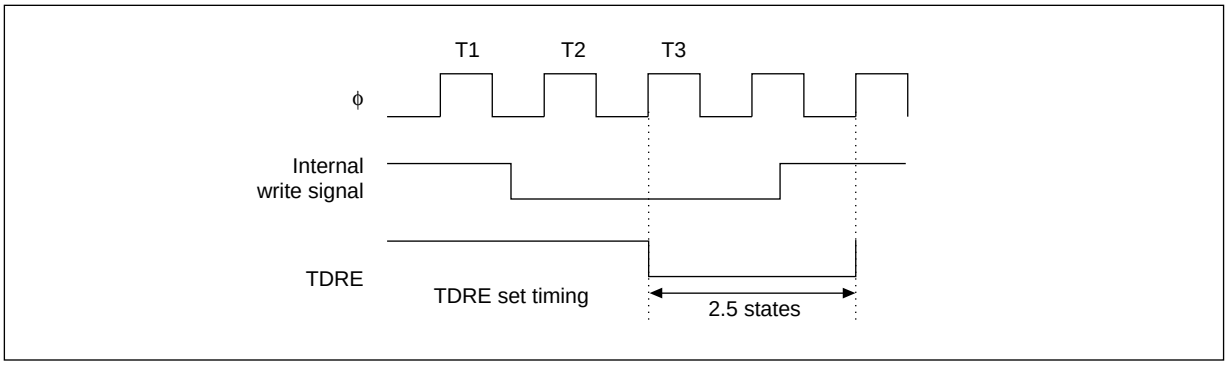


Figure 2.26 No transmit data in TSR (Clock-synchronous mode)

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-133
Topic	SCI Reception Errors		

Question

By returning to the main routine during a receive error interrupt routine without clearing the reception error flags of the SSR (serial status register), is a receive error interrupt generated again?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

The receive error flag is not automatically cleared. After returning to the main routine (after executing the RTE instruction), a receive error interrupt will be generated again.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-134
Topic	Operating the SCI in External Clock Mode		

Question

When the SCI is operated in clock-synchronous external clock mode:

1. Does the SCI start the next transmit operation if, after the completion of 1 byte of data transmission, the external clock is applied to the SCK pin before the H8/300H CPU writes to the TDR (transmit data register)?
2. What happens after reception?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

The results are as follows:

1. Transmission does not start. The next transmission will not start until the TDRE (transmit data register empty) of the SSR (serial status register) is cleared to 0.
2. Reception starts, however, an overrun error will occur unless the RDRF (receive data register full) of the SSR is cleared before the next data is completely received.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-135
Topic	System Clocks and SCK Phases		

Question

Is the SCK (serial transfer clock) output synchronous to system clock (ϕ) rise or fall?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
0	SCI
	A/D converter
	I/O ports

Answer

The SCK signal is output synchronous to system clock (ϕ) fall.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-136
Topic	Changing the A/D Mode and Channel During A/D Conversion		

Question

1. How do I switch the A/D conversion mode during A/D conversion?
2. How do I change the selected channel during A/D conversion?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
0	A/D converter
	I/O ports

Answer

1. Switching the A/D conversion mode during A/D conversion will decrease conversion accuracy. We advise against it.
2. Changing the selected channel during A/D conversion causes the same problem as switching the conversion mode. Again, we advise against it.

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

Before switching the A/D conversion mode or changing the selected channel, check the ADF (A/D end flag) in the ADCSR (A/D control/status register).

Product	Common	Q&A No.	QA300H-137
Topic	Using General-Purpose Ports		

Question

Can instructions that manipulate bits be used on I/O ports when a bit of the port is designated an output port?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
0	I/O ports

Answer

Yes. When a port set as an output port is read by the CPU, the contents of the port data register (DR) are read, regardless of the pin state. When an input port is read, the pin state is read. This means there are no problems in using instructions that manipulate bits. When there are pins in the port that have been designated input ports, however, the DR values of the input ports will become undefined (pin state). (See figure 2.27.)

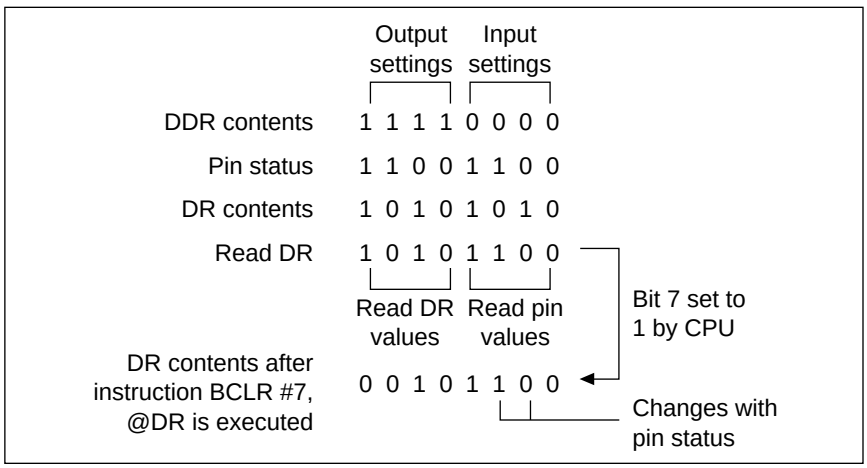


Figure 2.27 Using General-Purpose Ports

Related Manuals

Manual Title

Other Technical Documentation

Document Name

Related Microcomputer Technical Q&A

Title

References

The BSET, BCLR, BNOT, BST and BIST instructions manipulate bits.

Technical Questions and Answers

Product	Common	Q&A No.	QA300H-138
Topic	Processing Ports When Not in Use		

Question

How should I process ports that are not in use?

Classification—H8/300H

	Software
	Registers
	Bus controller
	Interrupts
	Resets
	Power-down mode
	Instructions
	Miscellaneous
	DMA controller
	ITU
	Watchdog timer
	SCI
	A/D converter
0	I/O ports

Answer

1. Clear the DDR (data direction register) of I/O ports to 0 to put them in input state and pull each pin up or down with a resistance of about 10 kΩ.
2. Handle input-only ports the same way.

Related Manuals

Manual Title

Other Technical Documentation

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Title

References