Hitachi America, Ltd.

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Application Engineering
TechNote

Cristian Tomescu

DRAM types and timing considerations for the H8/3003

The H8/3003, via its Refresh Controller, provides the necessary control signals for a direct and simple interface to word-size (x 16-bit) DRAMs. Please refer to chapter 7 (Refresh Controller) in the H8/3003 Hardware Manual as well as to the "External Memory Interface to the H8/3003" Application Note (AE-0043) for a detailed description of how to connect various DRAM types and sizes to the microcontroller.

Table 1 below lists all Hitachi x16 DRAM parts that can be interfaced to the H8/3003. Some features offered by each individual memory parts are not supported by the Refresh Controller. These are:

1. RAS-Only and Hidden-Refresh Modes.
2. Individual Byte-Write Capability (on the HM511664/L).
3. Fast-Page Mode (on all 4MBit parts).
4. Write-per-Bit (on the HM511665/L).

DEVICE	SIZE	ORGANIZATION row vs. column address size	BYTE CONTROL	ACCESS TIME	REFRESH TYPE	REFRESH INTERVAL
HM511664/L	64K x 16	8 x 8	2 WE	70/80/100 ns	CBR*/Self-Refresh	4 ms (32 ms L-version)
HM511665/L			No (1 WE)		CBR	
HM514260/L	256K x 16	9 x 9	2 CAS			8 ms (128 ms L-version)
HM514260A/AL					CBR/Self-Refresh	
HM51S4260A/AL					CBR/Self-Refresh	
HM514270/L			2 WE		CBR	
HM514270A/AL					CBR/Self-Refresh	
HM51S4270A/AL					CBR/Self-Refresh	
HM514170/L		10 x 8			CBR	16 ms (128 ms L-version)
HM514170A/AL					CBR/Self-Refresh	
HM51S4170A/AL					CBR/Self-Refresh	

***:** CBR stands for CAS-before-RAS.

Table 1. Hitachi DRAMs supported by the H8/3003

In addition, HM511666/L cannot be utilized since it operates in the static-column mode and not in the page mode.

Table 2 illustrates the critical DRAM control timing parameters guaranteed by the H8/3003 at 4 different operation frequencies, and compares them to the required values of the HM511664/L 1MBit DRAM at the 70, 80, and 100ns access speeds. Table 3 shows the same parameters for the HM514260/270/170 4Mbit DRAMs at the same access speeds.

PARAMETER	CYCLE	DRAM Required Timings (ns)			H8/3003 Guaranteed Timings			
		70ns	80ns	100ns	8MHz	10MHz	12MHz	16MHz
Trah (row address hold time)	Read/Write	min 10	min 10	min 10	min 25	min 20	min 15	min 10
Tasr* (row address setup time)		min 0	min 0	min 0	min 20	min 15	min 10	min 10
Trp (RAS precharge time)		min 45	min 45	min 60	min 85	min 70	min 55	min 35
Tcas (CAS pulse width)		min 25	min 30	min 40	min 110	min 40	min 40	min 40
Tcrp (CAS-RAS precharge time)		min 10	min 10	min 10	min 85	min 70	min 55	min 35
Tasc* (column address setup time)		min 0	min 0	min 0	min 20	min 15	min 10	min 10
Trac (RAS access time)	Read-Only	max 70	max 80	max 100	max 160	max 150	max 120	max 85
Tcac (CAS access time)		max 25	max 30	max 40	max 50	max 50	max 40	max 25
Taa (address access time)		max 40	max 45	max 55	max 105	max 55	max 55	max 55
Toff* (data hold time)		0 - 20	0 - 20	0 - 20	min 0	min 0	min 0	min 0
Tds* (data setup time)	Write-Only	min 0	min 0	min 0	min 75	min 40	min 40	min 40
Tcsr (CAS setup time)	Refresh	min 10	min 10	min 10	min 20	min 15	min 15	min 15

*: T_{asr}, T_{asc}, T_{off}, and T_{ds} are indicated as T_{as1}, T_{as1}, T_{rdh}, and T_{wds3} in the H8/3003 Hardware Manual Timing Diagrams.

Table 2. Timing Parameters for the HM511664/L 1Mbit DRAM

PARAMETER	CYCLE	DRAM Required Timings (ns)			H8/3003 Guaranteed Timings			
		70ns	80ns	100ns	8MHz	10MHz	12MHz	16MHz
Trah (row address hold time)	Read/Write	min 10	min 10	min 15	min 25	min 20	min 15	min 10
Tasr* (row address setup time)		min 0	min 0	min 0	min 20	min 15	min 10	min 10
Trp (RAS precharge time)		min 50	min 60	min 70	min 85	min 70	min 55	min 35
Tcas (CAS pulse width)		min 20	min 20	min 25	min 110	min 40	min 40	min 40
Tcrp (CAS-RAS precharge time)		min 15	min 15	min 15	min 85	min 70	min 55	min 35
Tasc* (column address setup time)		min 0	min 0	min 0	min 20	min 15	min 10	min 10
Trac (RAS access time)	Read-Only	max 70	max 80	max 100	max 160	max 150	max 120	max 85
Tcac (CAS access time)		max 20	max 20	max 25	max 50	max 50	max 40	max 25
Taa (address access time)		max 35	max 40	max 45	max 105	max 55	max 55	max 55
Toff* (data hold time)		0 - 15	0 - 15	0 - 15	min 0	min 0	min 0	min 0
Tds* (data setup time)	Write-Only	min 0	min 0	min 0	min 75	min 40	min 40	min 40
Tcsr (CAS setup time)	Refresh	min 10	min 10	min 10	min 20	min 15	min 15	min 15

*: T_{asr}, T_{asc}, T_{off}, and T_{ds} are indicated as T_{as1}, T_{as1}, T_{rdh}, and T_{wds3} in the H8/3003 Hardware Manual Timing Diagrams.

Table 3. Timing Parameters for the HM514260/270/170 4Mbit DRAMs.

In addition, T_{dh} (Write-Data Hold Time) is specified as minimum 15ns for all DRAM parts with respect to the falling edge of WE. The same parameter, as guaranteed by the H8/3003, is indicated as T_{wdh} in the H8/3003 Hardware Manual Timing Charts, and is specified as minimum 25ns at 8MHz, and minimum 20ns at frequencies greater than 8MHz **with respect to the rising edge of WE.** Therefore, this timing requirement is met by the H8/3003 with an ample margin.

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However, we see from Table 2 that the RAS Precharge (T_{rp}) and the CAS Access (T_{cac}) timing guaranteed by the H8/3003 violates the minimum requirements of the HM511664/L DRAM for the following operating conditions:

1. **T_{rp}** is violated if the H8/3003 is operating at 12-16MHz and a 100ns access time DRAM is utilized, and also if it is running at 16MHz with 70, 80, and 100ns access time DRAMs.
2. **T_{cac}** is violated if the H8/3003 is running at 16MHz and is interfaced to 80 and 100ns DRAMs.

Also, we see from Table 3 that the Row Address Hold (T_{rah}) and the RAS Precharge (T_{rp}) timings violate the minimum requirements of the HM514260/270/170 DRAMs for the following operating conditions:

1. **T_{rah}** is violated if the H8/3003 is operating at 16MHz and a 100ns DRAM is used.
2. **T_{rp}** is violated if the H8/3003 is operating at 12-16MHz with a 100ns DRAM, and also if it is running at 16MHz with 70, 80, or 100ns DRAMs.

In order to avoid any potential problems, general usage of 80ns or faster DRAMs is recommended, except when a HM511664/L 1Mbit DRAM is used and the microcontroller is operating at 16MHz. In this case, 70ns memory parts must be utilized in order to remove the CAS Access timing violation. In addition, when the CPU operates at the maximum frequency of 16MHz, insertion of one wait-state in the DRAM Refresh cycle will eliminate the RAS Precharge timing violation.

Note that the H8/3003 can also be connected to other types of DRAM than the word-wide (x16) types, such as x1, x4, x8, x9, and x18. Please consult the Hitachi DRAM Memory Data Book for more information on these devices, as well as technote TN-0154.

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