

H8/300H

Software standby mode recovery time for the H8/300H

TechNote

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Depending upon the type of its clock pulse generating circuitry, the H8/300H microcontrollers come in 2 versions: the clock-halving (2:1) version and the 1:1 version. In the clock-halving version, the system clock Φ is obtained by halving the incoming clock pulse by an internal frequency divider. In the 1:1 version, the external clock is not halved, but its pulse is adjusted to a 50% duty system clock by internal duty adjustment circuits. The H8/3003 is the only H8/300H microcontroller that comes in both versions; all other members (3002, 3042, 3048) are available only in the 1:1 configuration. With this in mind, the recovery time from the software standby mode depends upon 2 factors:

1. The type of system clock generating circuitry (as explained above).
2. The external clock source (crystal resonator versus oscillator).

If the external clock source is a crystal resonator, the minimum waiting time for internal clock stabilization upon exit from the software standby mode is 8ms. This minimum recovery time is set by appropriately setting bits STS 2-0 in the System Control Register (SYSCR). This condition is valid for both clock generating chip versions. If the external clock source is provided from an oscillator, the minimum recovery time is much shorter, and can be set by programming bits STS 2-0 of SYSCR as well. According to the hardware manuals, the minimum recovery time in this case is 8192 clock states for the 1:1 chip versions, and 4 clock states for the 2:1 chip versions. However, the recovery time for the 1:1 chip versions can be reduced to 4 states by setting all STS bits to 1, and by assuring that the external oscillator signal conforms to the timing restrictions shown in table 1 below. Figure 1 depicts graphically the external clock input timings specified in table 1.

Signal	Description	$2.7 < V_{CC} < 5.5$	$4.5 < V_{CC} < 5.5$
t_{EXL}	external clock pulse width low	min. 70 ns	min. 35ns
t_{EXH}	external clock pulse width high	min. 70 ns	min. 35 ns
t_{EXR}	external clock rise time	max. 10 ns	max. 5 ns
t_{EXF}	external clock fall time	max. 10 ns	max. 5 ns
f	operating frequency	$2\text{MHz} < f < 7\text{MHz}$	$2\text{MHz} < f < 14\text{MHz}$

Table 1

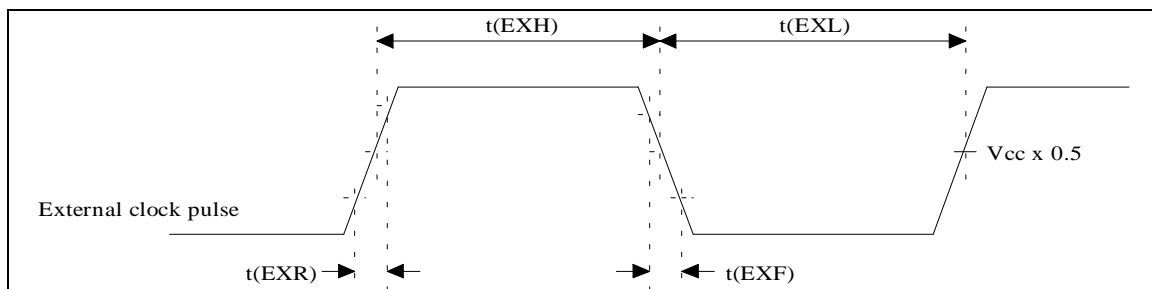


Figure 1

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