932723255 MH8333-p

H8/3332
Hardware Manual

HITACHI

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Section 1 Overview

The H8/3332 is a single-chip embedded controller with an H8/300 CPU core and a complement of on-chip supporting modules. They are particularly suited for keyboard control in notebook computers and similar applications.

The H8/300 CPU is a high-speed processor with a Hitachi-original architecture featuring powerful bit-manipulation instructions. It is ideally suited for realtime control applications. The on-chip supporting modules include a 16-bit free-running timer, two 8-bit timers, two pulse-width modulation (PWM) timers, a serial communication interface, an A/D converter, a keyboard controller, power management features, host CPU interface logic, and I/O ports.

The H8/3332 can operate in single-chip mode or in two expanded modes, depending on the memory requirements of the application. The operating mode is referred to in this manual as the embedded controller unit (MCU) mode.

The H8/3332 is available in a masked ROM version or in a one-time programmable (OTP) EPROM (or ZTAT™) version that can be programmed at the user site.

The embedded controller has a wide operating voltage range. It can operate at 3 V (2.7 V to 3.6 V) and at 5 V ±10%.

Features of the H8/3332 are listed in table 1-1.

Note: ZTAT is a trademark of Hitachi Ltd.

1.1 Block Diagram

Figure 1-1 is a block diagram of the H8/3332.

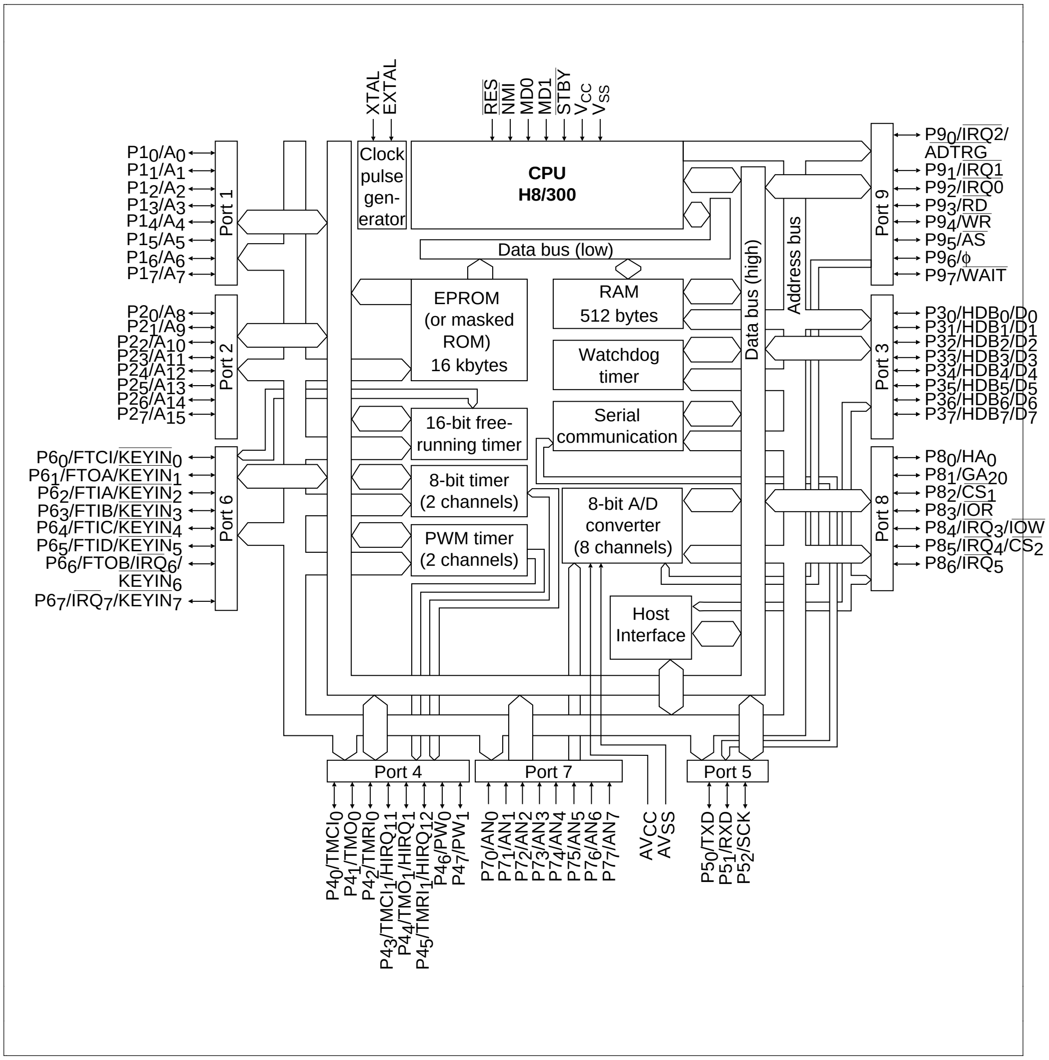


Figure 1-1 H8/3332 Block Diagram

1.2 Features

Table 1-1 Features

Item	Specification
CPU	Two-way general register configuration • Eight 16-bit registers, or • Sixteen 8-bit registers High-speed operation • Maximum clock rate: 10 MHz (at 5 V), 5 MHz (at 3 V) • Add/subtract: 0.2 µs • Multiply/divide: 1.4 µs Streamlined, concise instruction set • Instruction length: 2 or 4 bytes • Register-register arithmetic and logic operations • MOV instruction for data transfer between registers and memory Instruction set features • Multiply instruction (8 bits × 8 bits) • Divide instruction (16 bits ÷ 8 bits) • Bit-accumulator instructions • Register-indirect specification of bit positions
Memory	• 16-kbyte ROM or one-time programmable (OTP) EPROM; 512-byte RAM
16-bit free-running timer	• One 16-bit free-running counter (can also count external events) • Two output-compare lines • Four input capture lines (can be buffered)
8-bit timer (2 channels)	Each channel has • One 8-bit up-counter (can also count external events) • Two time constant registers
PWM timer (2 channels)	• Duty cycle can be set from 0 to 100% • Resolution: 1/250
Watchdog timer (1 channel)	• An overflow generates an NMI interrupt or reset • Can also be used as an interval timer

Table 1-1 Features (cont)

Item	Specification
Serial communication interface (SCI) (1 channel)	• Asynchronous or clocked synchronous mode (selectable) • Full duplex: can transmit and receive simultaneously • On-chip baud rate generator
A/D converter	• 8-bit resolution • Eight channels: single or scan mode (selectable) • Start of A/D conversion can be externally triggered • Sample-and-hold function
Host interface	• 8-bit host interface port • Supports industry-standard PC keyboard controller to host-CPU interface • Three host interrupt requests ($HIRQ_1$, $HIRQ_{11}$, $HIRQ_{12}$) • Regular and fast GATE A_{20} output • Two sets of registers, each with two data registers and one status register (selectable)
Keyboard controller	• Industry-standard serial enhanced AT and PS/2 keyboards • Keyboard scan and sense ports with wake-up interrupt for matrix keyboards
I/O ports	• 58 input/output lines (16 of which can drive LEDs) • 8 input-only lines
Interrupts	• Nine external interrupt lines: $\overline{NMI}$, $\overline{IRQ}_0$ to $\overline{IRQ}_7$ • 21 on-chip interrupt sources
Operating modes	• Expanded mode with on-chip ROM disabled (mode 1) • Expanded mode with on-chip ROM enabled (mode 2) • Single-chip mode (mode 3)
Power-down modes	• Sleep mode • Software standby mode • Hardware standby mode
Other features	• On-chip oscillator • 3 V or 5 V operation

1.3 Product Line-Up

The H8/3332 is available in 80- or 84-pin packages, for 3-V or 5-V operation (table 1-2). For the 3-V specification, the maximum operating frequency is 5 MHz. For other ordering information, see appendix F.

Table 1-2 Product Line-Up

Product Number (5V/10MHz version)	**Product Number (3V/5MHz version)**	**Package**	**ROM**
HD6473334CG10*		80 pin LCC (CG-84)	PROM version (with windows)
HD6473332F10		80 pin QFP (FP-80A)	ZTAT™ (PROM version)
HD6473332CP10		84 pin PLCC (CP-84)	
HD6433332F10		80 pin QFP (FP-80A)	Masked ROM
HD6433332F8			
HD6433332F6			
HD6433332VF5			
HD6433332CP10		84 pin PLCC (CP-84)	
HD6433332CP8			
HD6433332CP6			
HD6433332VCP5			

Note: * - under development

ZTAT™ (zero turn around time) is a trademark of Hitachi, Ltd.

1.4 Support Tools

H8/3332 hardware and software design is supported by the E3000 emulator, part number H33334EPS30H. The E3000 can emulate all functions of the H8/3332. It supports break and trace, and operates under a command line monitor or Windows interface. For more information, see the *E3000 H8/300 Series Emulator User's Manual* and the *E3000W H8/300 Series Emulator User's Manual*.

1.5 Pin Assignments and Functions

1.5.1 Pin Arrangement

Figure 1-2 shows the pin arrangement of the FP-80A package. Figure 1-3 shows the pin arrangement of the CP-84 package.

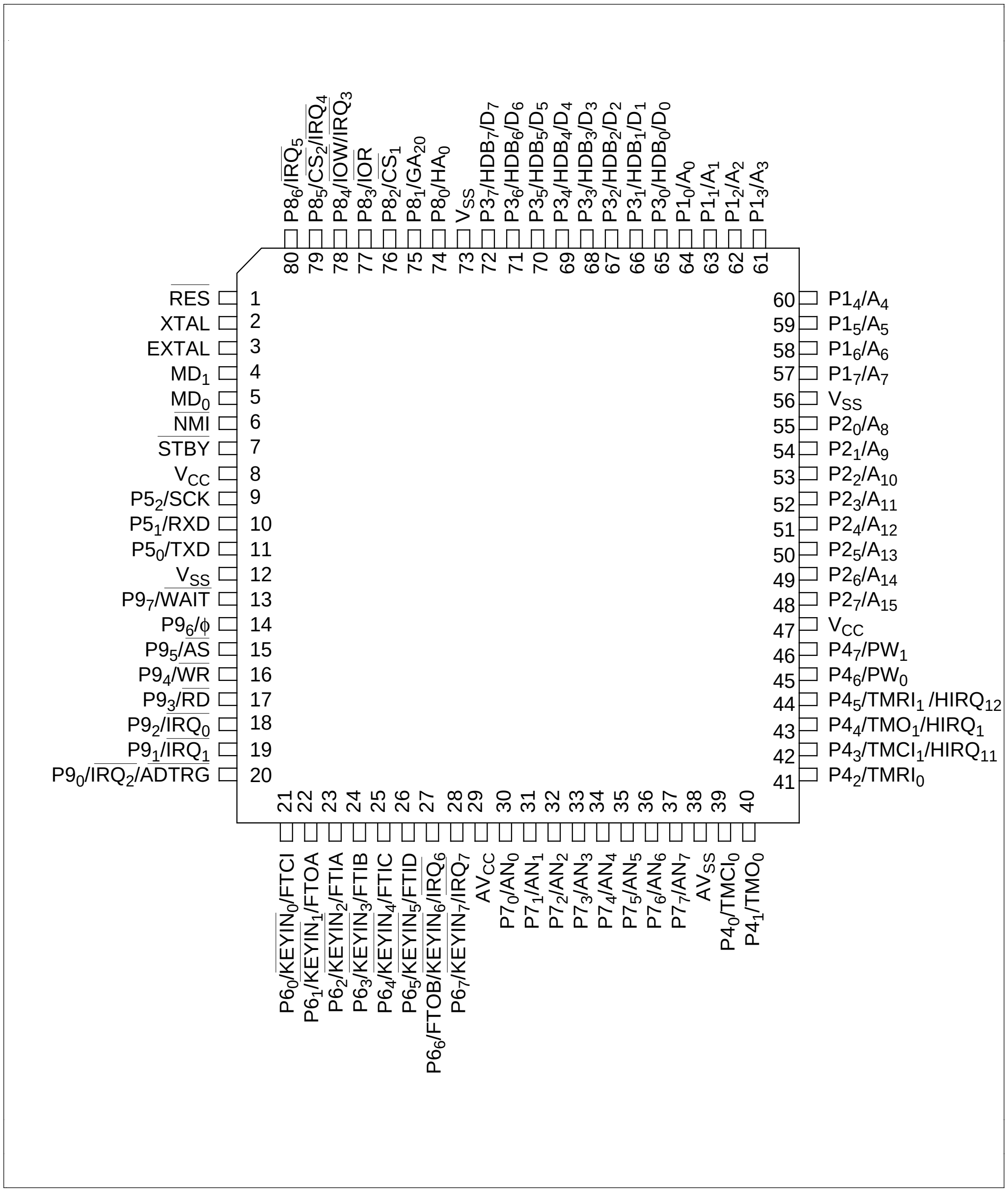


Figure 1-2 Pin Arrangement (FP-80A, Top View)

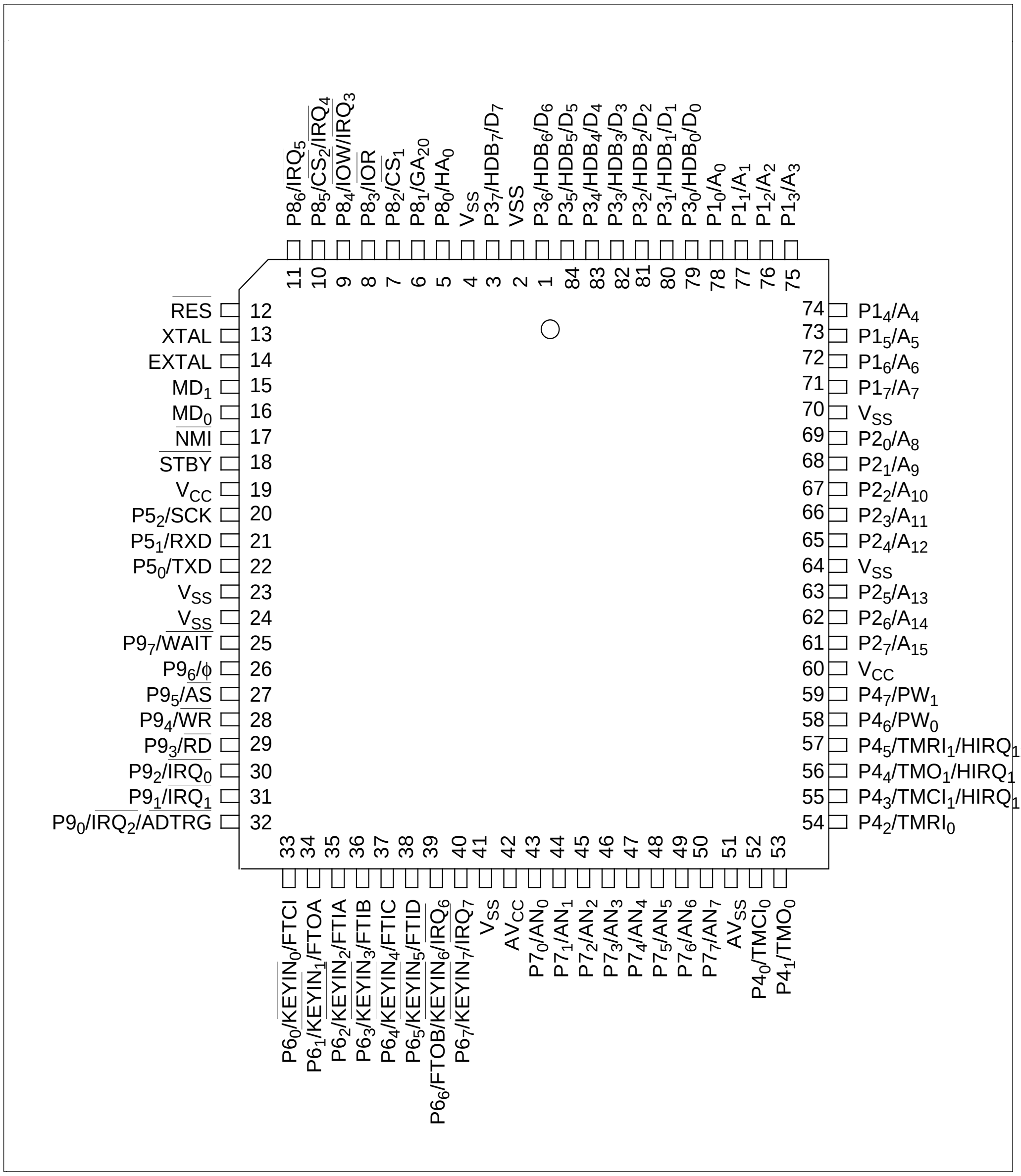


Figure 1-3 Pin Arrangement (CP-84, Top View)

1.5.2 Pin Functions

Pin Assignments in Each Operating Mode: Table 1-3 lists the assignments of the pins of the FP-80A, CP-84, and CG-84 packages in each operating mode.

Table 1-3 Pin Assignments in Each Operating Mode

Pin Number	Single-Chip Mode (Mode 3)	Expanded

CG-84				Modes	
CP-84	FP-80	HIF Disabled	HIF Enabled	(Modes 1, 2)	PROM Mode
1	71	P3$_6$	HDB$_6$	D$_6$	EO$_6$
2	—	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$
3	72	P3$_7$	HDB$_7$	D$_7$	EO$_7$
4	73	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$
5	74	P8$_0$	HA$_0$	P8$_0$	V$_{CC}$
6	75	P8$_1$	P8$_1$/GA$_{20}$	P8$_1$	V$_{CC}$
7	76	P8$_2$	$\overline{\text{CS}}_1$	P8$_2$	NC
8	77	P8$_3$	$\overline{\text{IOR}}$	P8$_3$	NC
9	78	P8$_4$/$\overline{\text{IRQ}}_3$	$\overline{\text{IOW}}$	P8$_4$/$\overline{\text{IRQ}}_3$	NC
10	79	P8$_5$/$\overline{\text{IRQ}}_4$	$\overline{\text{CS}}_2$	P8$_5$/$\overline{\text{IRQ}}_4$	NC
11	80	P8$_6$/$\overline{\text{IRQ}}_5$	P8$_6$/$\overline{\text{IRQ}}_5$	P8$_6$/$\overline{\text{IRQ}}_5$	NC
12	1	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	V$_{PP}$
13	2	XTAL	XTAL	XTAL	NC
14	3	EXTAL	EXTAL	EXTAL	NC
15	4	MD$_1$	MD$_1$	MD$_1$	V$_{SS}$
16	5	MD$_0$	MD$_0$	MD$_0$	V$_{SS}$
17	6	$\overline{\text{NMI}}$	$\overline{\text{NMI}}$	$\overline{\text{NMI}}$	EA$_9$
18	7	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	V$_{SS}$
19	8	V$_{CC}$	V$_{CC}$	V$_{CC}$	V$_{CC}$
20	9	P5$_2$/SCK	P5$_2$/SCK	P5$_2$/SCK	NC
21	10	P5$_1$/RXD	P5$_1$/RXD	P5$_1$/RXD	NC
22	11	P5$_0$/TXD	P5$_0$/TXD	P5$_0$/TXD	NC
23	12	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$
24	—	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$
25	13	P9$_7$	P9$_7$	$\overline{\text{WAIT}}$	NC
26	14	P9$_6$/ϕ	P9$_6$/ϕ	ϕ	NC

Table 1-3 Pin Assignments in Each Operating Mode (cont)

Pin Number		Single-Chip Mode (Mode 3)		Expanded	
CG-84				Modes	
CP-84	FP-80	HIF Disabled	HIF Enabled	(Modes 1, 2)	PROM Mode
27	15	$P9_5$	$P9_5$	$\overline{AS}$	NC
28	16	$P9_4$	$P9_4$	$\overline{WR}$	NC
29	17	$P9_3$	$P9_3$	$\overline{RD}$	NC
30	18	$P9_2/\overline{IRQ}_0$	$P9_2/\overline{IRQ}_0$	$P9_2/\overline{IRQ}_0$	NC
31	19	$P9_1/\overline{IRQ}_1$	$P9_1/\overline{IRQ}_1$	$P9_1/\overline{IRQ}_1$	NC
32	20	$P9_0/\overline{IRQ}_2/\overline{ADTRG}$	$P9_0/\overline{IRQ}_2/\overline{ADTRG}$	$P9_0/\overline{IRQ}_2/\overline{ADTRG}$	NC
33	21	$P6_0/FTCI/\overline{KEYIN}_0$	$P6_0/FTCI/\overline{KEYIN}_0$	$P6_0/FTCI/\overline{KEYIN}_0$	NC
34	22	$P6_1/FTOA/\overline{KEYIN}_1$	$P6_1/FTOA/\overline{KEYIN}_1$	$P6_1/FTOA/\overline{KEYIN}_1$	NC
35	23	$P6_2/FTIA/\overline{KEYIN}_2$	$P6_2/FTIA/\overline{KEYIN}_2$	$P6_2/FTIA/\overline{KEYIN}_2$	NC
36	24	$P6_3/FTIB/\overline{KEYIN}_3$	$P6_3/FTIB/\overline{KEYIN}_3$	$P6_3/FTIB/\overline{KEYIN}_3$	NC
37	25	$P6_4/FTIC/\overline{KEYIN}_4$	$P6_4/FTIC/\overline{KEYIN}_4$	$P6_4/FTIC/\overline{KEYIN}_4$	NC
38	26	$P6_5/FTID/\overline{KEYIN}_5$	$P6_5/FTID/\overline{KEYIN}_5$	$P6_5/FTID/\overline{KEYIN}_5$	NC
39	27	$P6_6/FTOB/\overline{IRQ}_6/\overline{KEYIN}_6$	$P6_6/FTOB/\overline{IRQ}_6/\overline{KEYIN}_6$	$P6_6/FTOB/\overline{IRQ}_6/\overline{KEYIN}_6$	NC
40	28	$P6_7/\overline{IRQ}_7/\overline{KEYIN}_7$	$P6_7/\overline{IRQ}_7/\overline{KEYIN}_7$	$P6_7/\overline{IRQ}_7/\overline{KEYIN}_7$	NC
41	—	V_{SS}	V_{SS}	V_{SS}	V_{SS}
42	29	AV_{CC}	AV_{CC}	AV_{CC}	V_{CC}
43	30	$P7_0/AN_0$	$P7_0/AN_0$	$P7_0/AN_0$	NC
44	31	$P7_1/AN_1$	$P7_1/AN_1$	$P7_1/AN_1$	NC
45	32	$P7_2/AN_2$	$P7_2/AN_2$	$P7_2/AN_2$	NC
46	33	$P7_3/AN_3$	$P7_3/AN_3$	$P7_3/AN_3$	NC
47	34	$P7_4/AN_4$	$P7_4/AN_4$	$P7_4/AN_4$	NC
48	35	$P7_5/AN_5$	$P7_5/AN_5$	$P7_5/AN_5$	NC
49	36	$P7_6/AN_6$	$P7_6/AN_6$	$P7_6/AN_6$	NC
50	37	$P7_7/AN_7$	$P7_7/AN_7$	$P7_7/AN_7$	NC
51	38	AV_{SS}	AV_{SS}	AV_{SS}	V_{SS}
52	39	$P4_0/TMCI_0$	$P4_0/TMCI_0$	$P4_0/TMCI_0$	NC
53	40	$P4_1/TMO_0$	$P4_1/TMO_0$	$P4_1/TMO_0$	NC

Table 1-3 Pin Assignments in Each Operating Mode (cont)

Pin Number		Single-Chip Mode (Mode 3)		Expanded Modes	
CG-84 CP-84	FP-80	HIF Disabled	HIF Enabled	(Modes 1, 2)	PROM Mode
54	41	P4$_2$/TMRI$_0$	P4$_2$/TMRI$_0$	P4$_2$/TMRI$_0$	NC
55	42	P4$_3$/TMCI$_1$	P4$_3$/TMCI$_1$/HIRQ$_{11}$	P4$_3$/TMCI$_1$	NC
56	43	P4$_4$/TMO$_1$	P4$_4$/TMO$_1$/HIRQ$_1$	P4$_4$/TMO$_1$	NC
57	44	P4$_5$/TMRI$_1$	P4$_5$/TMRI$_1$/HIRQ$_{12}$	P4$_5$/TMRI$_1$	NC
58	45	P4$_6$/PW$_0$	P4$_6$/PW$_0$	P4$_6$/PW$_0$	NC
59	46	P4$_7$/PW$_1$	P4$_7$/PW$_1$	P4$_7$/PW$_1$	NC
60	47	V$_{CC}$	V$_{CC}$	V$_{CC}$	V$_{CC}$
61	48	P2$_7$	P2$_7$	A$_{15}$	$\overline{CE}$
62	49	P2$_6$	P2$_6$	A$_{14}$	EA$_{14}$
63	50	P2$_5$	P2$_5$	A$_{13}$	EA$_{13}$
64	—	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$
65	51	P2$_4$	P2$_4$	A$_{12}$	EA$_{12}$
66	52	P2$_3$	P2$_3$	A$_{11}$	EA$_{11}$
67	53	P2$_2$	P2$_2$	A$_{10}$	EA$_{10}$
68	54	P2$_1$	P2$_1$	A$_9$	$\overline{OE}$
69	55	P2$_0$	P2$_0$	A$_8$	EA$_8$
70	56	V$_{SS}$	V$_{SS}$	V$_{SS}$	V$_{SS}$
71	57	P1$_7$	P1$_7$	A$_7$	EA$_7$
72	58	P1$_6$	P1$_6$	A$_6$	EA$_6$
73	59	P1$_5$	P1$_5$	A$_5$	EA$_5$
74	60	P1$_4$	P1$_4$	A$_4$	EA$_4$
75	61	P1$_3$	P1$_3$	A$_3$	EA$_3$
76	62	P1$_2$	P1$_2$	A$_2$	EA$_2$
77	63	P1$_1$	P1$_1$	A$_1$	EA$_1$
78	64	P1$_0$	P1$_0$	A$_0$	EA$_0$
79	65	P3$_0$	HDB$_0$	D$_0$	EO$_0$
80	66	P3$_1$	HDB$_1$	D$_1$	EO$_1$
81	67	P3$_2$	HDB$_2$	D$_2$	EO$_2$
82	68	P3$_3$	HDB$_3$	D$_3$	EO$_3$

Table 1-3 Pin Assignments in Each Operating Mode (cont)

Pin Number		Single-Chip Mode (Mode 3)		Expanded Modes (Modes 1, 2)	PROM Mode
CG-84 CP-84	FP-80	HIF Disabled	HIF Enabled		
83	69	$P3_4$	HDB_4	D_4	EO_4
84	70	$P3_5$	HDB_5	D_5	EO_5

Notes: 1. NC pins should not be connected to anything.

2. See Section 14.2, PROM mode, for details of PROM mode.

3. See Section 5, I/O Ports, for details of A_0 to A_{15} selection in mode 2.

Pin Description: Table 1-4 gives a concise description of the functions of each pin.

Table 1-4 Pin Description

Type	Symbol	Pin Number		I/O	Name and function
		CG-84 CP-84	FP-80A		
Power	V_{CC}	19, 60	8, 47	I	**Power:** Connected to the power supply (+5 V or +3 V). Connect V_{CC} pins to the system power supply (+5 V or +3 V).
	V_{SS}	2, 4, 23, 24, 41, 64, 70	12, 56, 73	I	**Ground:** Connected to ground (0 V). Connect V_{SS} pins to the system power supply (0 V).
Clock	XTAL	13	2	I	**Crystal:** Connected to a crystal oscillator. The crystal frequency should be double the desired system clock frequency.
	EXTAL	14	3	I	**External Crystal:** Connected to a crystal oscillator or external clock. The frequency of the external clock should be double the desired system clock frequency. See section 16.2, Oscillator Circuit, for examples of connections to a crystal and external clock.
	ϕ	26	14	O	**System Clock:** Supplies the system clock to peripheral devices.
System control	$\overline{\text{RES}}$	12	1	I	**Reset:** A low input causes the chip to reset.
	$\overline{\text{STBY}}$	18	7	I	**Standby:** A transition to the hardware standby mode (a power-down state) occurs when a low input is received at the $\overline{\text{STBY}}$ pin.
Address bus	A_{15} to A_0	61 to 63, 65 to 69, 71 to 78	48 to 55, 57 to 64	O	**Address Bus:** Address output pins.
Data bus	D_7 to D_0	3, 1, 84 to 79	72 to 65	I/O	**Data Bus:** 8-Bit bidirectional data bus.
Bus control	$\overline{\text{WAIT}}$	25	13	I	**Wait:** Requests the CPU to insert TW states into the bus cycle when an external address is accessed.
	$\overline{\text{RD}}$	29	17	O	**Read:** Goes low to indicate that the CPU is reading an external address.

Table 1-4 Pin Description (cont)

Type	Symbol	Pin Number	I/O	Name and function

		CG-84 CP-84	FP-80A		
Bus control	$\overline{WR}$	28	16	O	**Write:** Goes low to indicate that the CPU is writing to an external address.
	$\overline{AS}$	27	15	O	**Address Strobe:** Goes low to indicate that there is a valid address on the address bus.
Interrupt signals	$\overline{NMI}$	17	6	I	**Nonmaskable Interrupt:** Highest-priority interrupt request. The NMIEG bit in the system control register determines whether the interrupt is requested on the rising or falling edge of the $\overline{NMI}$ input.
	$\overline{IRQ_0}$ to $\overline{IRQ_7}$	30 to 32, 9 to 11, 39, 40	18 to 20, 78 to 80, 27, 28	I	**Interrupt Request 0 to 7:** Maskable interrupt request pins.
Operating mode control	MD1, MD0	15 16	4 5	I	**Mode:** Input pins for setting the MCU operating mode according to the table below. MD1 · MD0 · Mode · Description 0 · 1 · Mode 1 · Expanded mode with on-chip ROM disabled 1 · 0 · Mode 2 · Expanded mode with on-chip ROM enabled 1 · 1 · Mode 3 · Single-chip mode
Serial communication interface	TxD	22	11	O	**Transmit Data:** Data output pins for the serial communication interface.
	RxD	21	10	I	**Receive Data:** Data input pins for the serial communication interface.
	SCK	20	9	I/O	**Serial Clock:** Input/output pins for the serial clock.
16-bit free-	FTOA, FTOB	34, 39	22, 27	O	**FRT Output Compare A and B:** Output pins controlled by comparators A and B of the free-running timer.

Table 1-4 Pin Description (cont)

Type	Symbol	Pin Number		I/O	Name and function
		CG-84 CP-84	FP-80A		
running timer	FTCI	33	21	I	**FRT Counter Clock Input:** Input pin for an external clock signal for the free-running timer.
	FTIA to FTID	35, 36, 37, 38	23, 24, 25, 26	I	**FRT Input Capture A to D:** Input capture pins for the free-running timer.
8-bit timer	TMO_0, TMO_1	53, 56	40, 43	O	**8-Bit Timer Output (channels 0 and 1):** Compare-match output pins for the 8-bit timers.
	$TMCI_0$, $TMCI_1$	52, 55	39, 42	I	**8-Bit Timer Counter Clock Input (channels 0 and 1):** External clock input pins for the 8-bit timer counters.
	$TMRI_0$, $TMRI_1$	54, 57	41, 44	I	**8-Bit Timer Counter Reset Input (channels 0 and 1):** A high input at these pins resets the 8-bit timer counters.
PWM timer	PW_0, PW_1	58, 59	45, 46	O	**PWM Timer Output (channels 0 and 1):** Pulse-width modulation timer output pins.
A/D converter	AN_7 to AN_0	50 to 43	37 to 30	I	**Analog Input:** Analog signal input pins for the A/D converter.
	$\overline{ADTRG}$	32	20	I	**A/D Trigger:** External trigger input for starting the A/D converter.
	AV_{CC}	42	29	I	**Analog Reference Voltage:** Reference voltage pin for the A/D converter. If the A/D converter is not used, connect AV_{CC} to the system power supply (V_{CC}).
	AV_{SS}	51	38	I	**Analog Ground:** Ground pin for the A/D converter. Connect to system ground (0 V).
Host interface	HDB_7 to HDB_0	1, 3, 79 to 84	65 to 72	I/O	**Host Interface Data Bus**: Bidirectional 8-bit bus by which an external CPU can access the host interface.
	$\overline{CS}_1$, $\overline{CS}_2$	7, 10	76, 79	I	**Chip Select 1 and 2:** Input pins for selecting the first set ($\overline{CS}_1$) or second set ($\overline{CS}_2$) of registers.
	$\overline{IOR}$	8	77	I	**Read Enable:** Enables reading from the host interface.

Table 1-4 Pin Description (cont)

Type	Symbol	Pin Number		I/O	Name and function
		CG-84 CP-84	FP-80A		
Host interface	$\overline{\text{IOW}}$	9	78	I	**Write Enable:** Enables writing to the host interface.
	HA_0	5	74	I	**Command/Data:** Input to indicate whether the input byte to the host interface data bus is data or a command.
	GA_{20}	6	75	O	**GATE A_{20}:** Output for the GATE A_{20} signal.
	$HIRQ_1$, $HIRQ_{11}$, $HIRQ_{12}$	55 to 57	42 to 44	O	**Host Interrupts 1, 11, and 12:** Output for interrupting host CPU.
Keyboard control	$\overline{\text{KEYIN}}_0$ to $\overline{\text{KEYIN}}_7$	33 to 40	21 to 28	I	**Keyboard Input:** Input pins for matrix keyboard. (Generally, $P1_0$–$P1_7$ and $P2_0$–$P2_7$ are used as output lines for keyboard scan, but any available output port can also be used for this purpose.)
General-purpose I/O	$P1_7$ to $P1_0$	71 to 78	57 to 64	I/O	**Port 1:** An 8-bit input/output port with programmable input pull-up transistors and LED driving capability. The direction of each bit can be selected in the port 1 data direction register (P1DDR).
	$P2_7$ to $P2_0$	61 to 63, 65 to 69	48 to 55	I/O	**Port 2:** An 8-bit input/output port with programmable input pull-up transistors and LED driving capability. The direction of each bit can be selected in the port 2 data direction register (P2DDR).
	$P3_7$ to $P3_0$	3, 1, 84 to 79	72 to 65	I/O	**Port 3:** An 8-bit input/output port with programmable input pull-up MOS transistors. The direction of each bit can be selected in the port 3 data direction register (P3DDR).
	$P4_7$ to $P4_0$	59 to 52	46 to 39	I/O	**Port 4:** An 8-bit input/output port. The direction of each bit can be selected in the port 4 data direction register (P4DDR).
	$P5_2$ to $P5_0$	20 to 22	9 to 11	I/O	**Port 5:** A 3-bit input/output port. The direction of each bit can be selected in the port 5 data direction register (P5DDR).

Table 1-4 Pin Description (cont)

Type	Symbol	Pin Number		I/O	Name and function
		CG-84 CP-84	FP-80A		
General-purpose I/O	$P6_7$ to $P6_0$	40 to 33	28 to 21	I/O	**Port 6:** An 8-bit input/output port. The direction of each bit can be selected in the port 6 data direction register (P6DDR).
	$P7_7$ to $P7_0$	50 to 43	37 to 30	I	**Port 7:** An 8-bit input port.
	$P8_6$ to $P8_0$	11 to 5	80 to 74	I/O	**Port 8:** A 7-bit input/output port. The direction of each bit can be selected in the port 8 data direction register (P8DDR).
	$P9_7$ to $P9_0$	25 to 32	13 to 20	I/O	**Port 9:** An 8-bit input/output port. The direction of each bit (except for P96) can be selected in the port 9 data direction register (P9DDR).

Section 2 MCU Operating Modes and Address Space

2.1 Overview

2.1.1 Mode Selection

The H8/3332 operates in three modes numbered 1, 2, and 3. The mode is selected by the inputs at the mode pins (MD_1 and MD_0) when the chip comes out of a reset. See table 2-1.

Table 2-1 Operating Modes

MD_1	MD_0	Mode	Address Space	On-Chip ROM	On-Chip RAM
Low	Low	Mode 0	—	—	—
Low	High	Mode 1	Expanded: 64 kbytes	Disabled	Enabled (Note)
High	Low	Mode 2	Expanded: 64 kbytes	Enabled	Enabled (Note)
High	High	Mode 3	Single-chip	Enabled	Enabled

Note: In modes 1 and 2, external memory can be accessed instead of on-chip RAM by clearing the RAME bit in the system control register (SYSCR) to 0.

Modes 1 and 2 are expanded modes that permit access to off-chip memory and peripheral devices. The maximum address space supported by these externally expanded modes is 64 kbytes.

In mode 3 (single-chip mode), only on-chip ROM and RAM and the on-chip register field are used. All ports are available for general-purpose input and output.

Mode 0 is inoperative in the H8/3332. Avoid setting the mode pins to mode 0.

2.1.2 Mode and System Control Registers (MDCR and SYSCR)

Table 2-2 lists the registers related to the chip's operating mode: the system control register (SYSCR) and mode control register (MDCR). The mode control register indicates the inputs to the mode pins MD_1 and MD_0.

Table 2-2 Mode and System Control Registers

Name	Abbreviation	Read/Write	Address
System control register	SYSCR	R/W	H'FFC4
Mode control register	MDCR	R	H'FFC5

2.2 System Control Register (SYSCR): H'FFC4

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	XRST	NMIEG	HIE	RAME
Initial value	0	0	0	0	1	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

The system control register (SYSCR) is an eight-bit register that controls the operation of the chip.

Bit 7: Software Standby (SSBY): Enables transition to the software standby mode. For details, see section 15, “Power-Down State.”

On recovery from software standby mode by an external interrupt, the SSBY bit remains set to 1. It can be cleared by writing 0.

Bit 7 SSBY	Description	
0	The SLEEP instruction causes a transition to sleep mode.	(Initial state)
1	The SLEEP instruction causes a transition to software standby mode.	

Bits 6 to 4: Standby Timer Select 2 to 0 (STS2 to STS0): Select the clock settling time when the chip recovers from the software standby mode by an external interrupt. During the selected time the CPU and on-chip supporting modules continue to stand by. These bits should be set according to the clock frequency so that the settling time is at least 10 ms. For specific settings, see section 15.2, System Control Register: Power-Down Control Bits.

Bit 6, STS2	Bit 5, STS1	Bit 4, STS0	Description	
0	0	0	Settling time = 8192 states	(Initial state)
0	0	1	Settling time = 16384 states	
0	1	0	Settling time = 32768 states	
0	1	1	Settling time = 65536 states	
1	—	—	Settling time = 131072 states	

Bit 3: External Reset (XRST): The XRST bit indicates the reset source. Reset can be asserted either by external reset input or by watchdog timer overflow, if the watchdog timer is activated. The read-only XRST is set to 1 by external reset and reset to 0 by watchdog timer overflow.

Bit 3, XRST	Description	
0	Reset was generated by watchdog timer overflow	
1	Reset was generated by external reset input	(Initial state)

Bit 2: NMI Edge (NMIEG): Selects the valid edge of the $\overline{\text{NMI}}$ input.

Bit 2, NMIEG	Description	
0	An interrupt is requested on the falling edge of $\overline{\text{NMI}}$ input	(Initial state)
1	An interrupt is requested on the rising edge of $\overline{\text{NMI}}$ input	

Bit 1: Host Interface Enable (HIE): In the single-chip mode, HIE enables or disables the host interface. When enabled, the host interface can be accessed by both an external (master) CPU and the on-chip (slave) CPU. When disabled, the host interface can be accessed only by the on-chip CPU.

This bit affects the use of ports 3, 4, and 8.

Bit 1, HIE	Description	
0	The host interface is disabled	(Initial state)
1	Single-chip mode	The host interface is enabled (slave mode)
	Expanded modes	The host interface is disabled (but can be accessed by the on-chip CPU)

Bit 0: RAM Enable (RAME): Enables or disables the on-chip RAM. The RAME bit is initialized by a reset, but is not initialized in the software standby mode.

Bit 0, RAME	Description	
0	The on-chip RAM is disabled.	
1	The on-chip RAM is enabled.	(Initial state)

2.3 Mode Control Register (MDCR): H'FFC5

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MDS1	MDS0
Initial value	1	1	1	0	0	1	*	*
Read/Write	R	R	R	R	R	R	R	R

Note: * Initialized according to MD_1 and MD_0 inputs.

The mode control register (MDCR) is an eight-bit register that indicates the operating mode of the chip.

Bits 7 to 5: Reserved: These bits cannot be modified and are always read as 1.

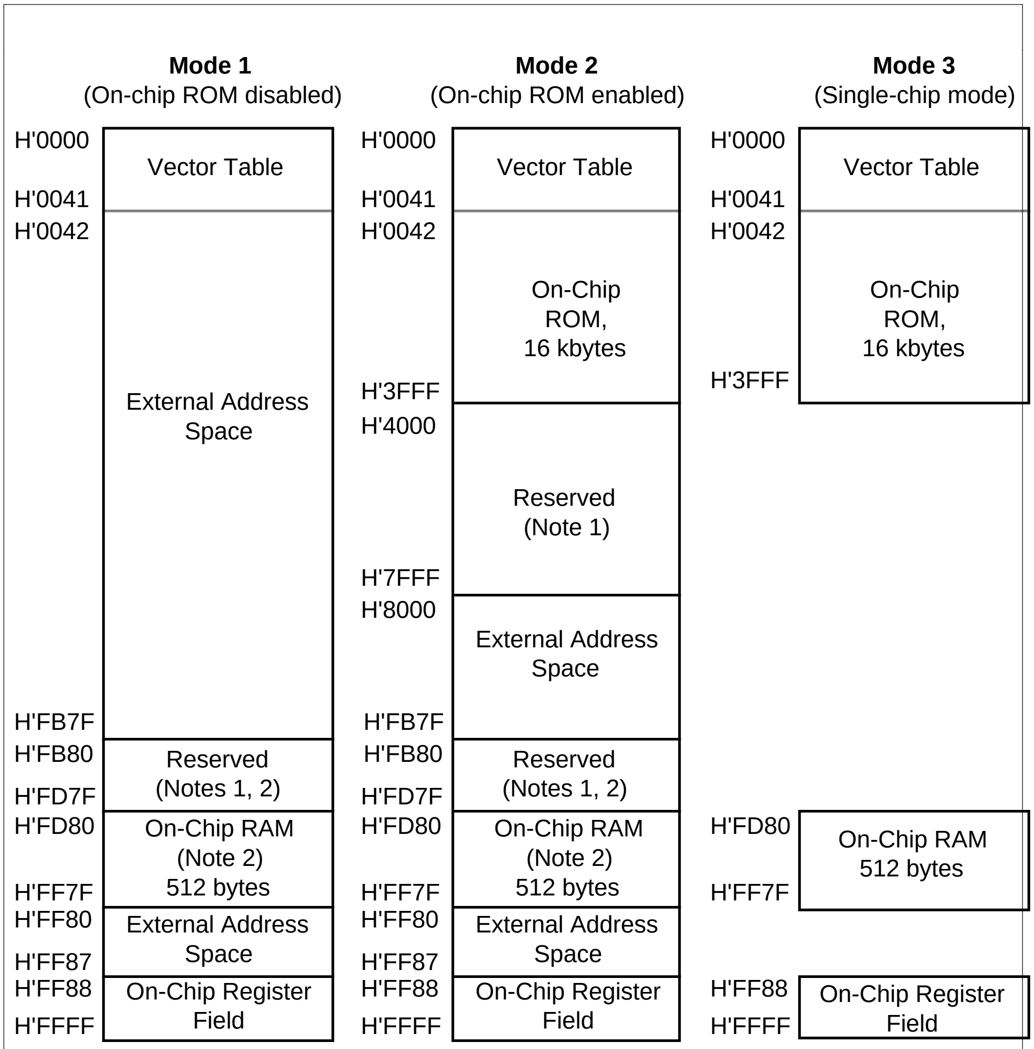
Bits 4 and 3: Reserved: These bits cannot be modified and are always read as 0.

Bit 2: Reserved: This bit cannot be modified and is always read as 1.

Bits 1 and 0: Mode Select 1 and 0 (MDS1 and MDS0): Indicate the values of the mode pins (MD_1 and MD_0), thereby indicating the current operating mode of the chip. MDS1 corresponds to MD_1 and MDS0 to MD_0 . These bits can be read but not written. When the mode control register is read, the levels at the mode pins (MD_1 and MD_0) are latched in these bits.

2.4 Address Space Map

Figures 2-1 shows a memory map in modes 1, 2, and 3.



Notes: 1. Do not access reserved areas.
2. External memory can be accessed at these addresses when the RAME bit, in the system control register (SYSCR), is cleared to 0.

Figure 2-1 H8/3332 Address Space Map

Section 3 CPU

3.1 Overview

The H8/3332 has the H8/300 CPU: a fast central processing unit with eight 16-bit general registers (also configurable as 16 eight-bit registers) and a concise instruction set designed for high-speed operation.

3.1.1 Features

The main features of the H8/300 CPU are:

- Two-way register configuration
  - Sixteen 8-bit general registers, or
  - Eight 16-bit general registers
- Instruction set with 57 basic instructions, including:
  - Multiply and divide instructions
  - Powerful bit-manipulation instructions
- Eight addressing modes
  - Register direct (Rn)
  - Register indirect (@Rn)
  - Register indirect with displacement (@(d:16, Rn))
  - Register indirect with post-increment or pre-decrement (@Rn+ or @–Rn)
  - Absolute address (@aa:8 or @aa:16)
  - Immediate (#xx:8 or #xx:16)
  - PC-relative (@(d:8, PC))
  - Memory indirect (@@aa:8)
- Maximum 64-kbyte address space
- High-speed operation
  - All frequently-used instructions are executed in two to four states
  - The maximum clock rate is 10MHz

— 8- or 16-bit register-register add or subtract:	0.2 µs
— 8 × 8-bit multiply:	1.4 µs
— 16 ÷ 8-bit divide:	1.4 µs

- Power-down mode
  - SLEEP instruction

3.1.2 Address Space

The H8/300 CPU has a maximum of 64 Kbyte of address space (tolerance for program code and data). The memory map differs according to the operating mode (modes 1, 2, and 3). (See Section 2.4, Address Space Map, for details.

3.2 Register Configuration

Figure 3-1 shows the register structure of the CPU. There are two groups of registers: the general registers and control registers.

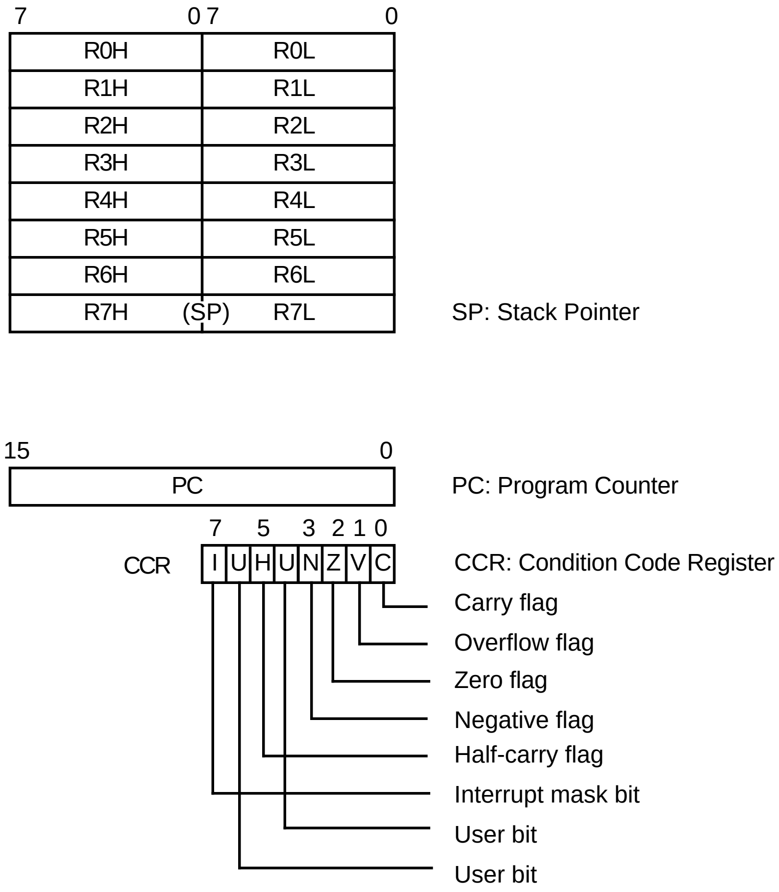


Figure 3-1 CPU Registers

3.2.1 General Registers

All the general registers can be used as both data registers and address registers. When used as address registers, the general registers are accessed as 16-bit registers (R0 to R7). When used as data registers, they can be accessed as 16-bit registers, or the high and low bytes can be accessed separately as 8-bit registers (R0H to R7H and R0L to R7L).

R7 also functions as the stack pointer, used implicitly by hardware in processing interrupts and subroutine calls. In assembly-language coding, R7 can also be denoted by the letters SP. As indicated in figure 3-2, R7 (SP) points to the top of the stack.

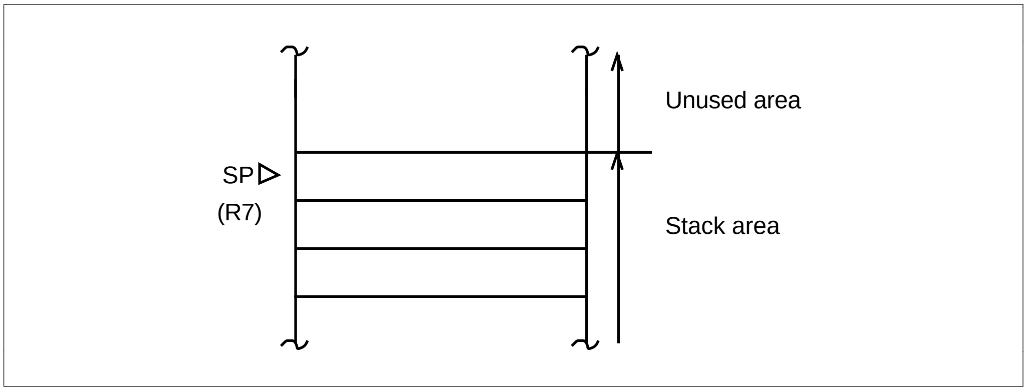


Figure 3-2 Stack Pointer

3.2.2 Control Registers

The CPU control registers include a 16-bit program counter (PC) and an 8-bit condition code register (CCR).

Program Counter (PC): This 16-bit register indicates the address of the next instruction the CPU will execute. Each instruction is accessed in 16 bits (1 word), so the least significant bit of the PC is ignored (always regarded as 0).

Condition Code Register (CCR): This 8-bit register contains internal status information, including carry (C), overflow (V), zero (Z), negative (N), and half-carry (H) flags and the interrupt mask bit (I).

Bit 7: Interrupt Mask Bit (I): When I is set to 1, all interrupts except NMI are masked. This bit is set to 1 automatically by a reset and at the start of interrupt handling.

Bit 6: User Bit (U): This U bit can be written and read by software (using the LDC, STC, ANDC, ORC, and XORC instructions).

Bit 5: Half-Carry (H): H is set to 1 when the ADD.B, ADDX.B, SUB.B, SUBX.B, NEG.B, or CMP.B instruction causes a carry or borrow out of bit 3, and is cleared to 0 otherwise. Similarly, it is set to 1 when the ADD.W, SUB.W, or CMP.W instruction causes a carry or borrow out of bit 11, and cleared to 0 otherwise. It is used implicitly in the DAA and DAS instructions.

Bit 4: User Bit (U): This U bit can be written and read by software (using the LDC, STC, ANDC, ORC, and XORC instructions).

Bit 3: Negative (N): N indicates the most significant bit (sign bit) of the result of an instruction.

Bit 2: Zero (Z): Z is set to 1 to indicate a zero result and cleared to 0 to indicate a non-zero result.

Bit 1: Overflow (V): V is set to 1 when an arithmetic overflow occurs, and cleared to 0 at other times.

Bit 0: Carry (C): C is used by:

- Add and subtract instructions, to indicate a carry or borrow at the most significant bit of the result
- Shift and rotate instructions, to store the value shifted out of the most significant or least significant bit
- Bit manipulation and bit load instructions, as a bit accumulator

The LDC, STC, ANDC, ORC, and XORC instructions enable the CPU to load and store the CCR, and to set or clear selected bits by logic operations. The N, Z, V, and C flags are used in conditional branching instructions (Bcc).

For the action of each instruction on the flag bits, see the *H8/300 Series Programming Manual*.

3.2.3 Initial Register Values

When the CPU is reset, the program counter (PC) is loaded from the vector table and the interrupt mask bit (I) in the CCR is set to 1. The other CCR bits and the general registers are not initialized.

In particular, the stack pointer (R7) is not initialized. To prevent program crashes the stack pointer should be initialized by software, by the first instruction executed after a reset.

3.3 Addressing Modes

The H8/300 CPU supports eight addressing modes. Each instruction uses a subset of these addressing modes.

Table 3-1 Addressing Modes

No.	Addressing mode	Symbol
1	Register direct	Rn
2	Register indirect	@Rn
3	Register indirect with displacement	@(d:16, Rn)
4	Register indirect with post-increment	@Rn+
	Register indirect with pre-decrement	@–Rn
5	Absolute address	@aa:8 or @aa:16
6	Immediate	#xx:8 or #xx:16
7	Program-counter-relative	@(d:8, PC)
8	Memory indirect	@@aa:8

1. Register Direct—Rn: The register field of the instruction specifies an 8- or 16-bit general register containing the operand. In most cases the general register is accessed as an 8-bit register. Only the MOV.W, ADD.W, SUB.W, CMP.W, ADDS, SUBS, MULXU (8 bits × 8 bits), and DIVXU (16 bits ÷ 8 bits) instructions have 16-bit operands.

2. Register indirect—@Rn: The register field of the instruction specifies a 16-bit general register containing the address of the operand.

3. Register Indirect with Displacement—@(d:16, Rn): This mode, which is used only in MOV instructions, is similar to register indirect but the instruction has a second word (bytes 3 and 4) which is added to the contents of the specified general register to obtain the operand address. For the MOV.W instruction, the resulting address must be even.

4. Register Indirect with Post-Increment or Pre-Decrement—@Rn+ or @–Rn:

   - Register indirect with Post-Increment—@Rn+

     The @Rn+ mode is used with MOV instructions that load registers from memory.

     It is similar to the register indirect mode, but the 16-bit general register specified in the register field of the instruction is incremented after the operand is accessed. The size of the increment is 1 or 2 depending on the size of the operand: 1 for MOV.B; 2 for MOV.W. For MOV.W, the original contents of the 16-bit general register must be even.

   - Register Indirect with Pre-Decrement—@–Rn

The @–Rn mode is used with MOV instructions that store register contents to memory.

It is similar to the register indirect mode, but the 16-bit general register specified in the register field of the instruction is decremented before the operand is accessed. The size of the decrement is 1 or 2 depending on the size of the operand: 1 for MOV.B; 2 for MOV.W. For MOV.W, the original contents of the 16-bit general register must be even.

5. Absolute Address—@aa:8 or @aa:16: The instruction specifies the absolute address of the operand in memory. The MOV.B instruction uses an 8-bit absolute address of the form H'FFxx. The upper 8 bits are assumed to be 1, so the possible address range is H'FF00 to H'FFFF (65280 to 65535). The MOV.B, MOV.W, JMP, and JSR instructions can use 16-bit absolute addresses.

6. Immediate—#xx:8 or #xx:16: The instruction contains an 8-bit operand in its second byte, or a 16-bit operand in its third and fourth bytes. Only MOV.W instructions can contain 16-bit immediate values.

   The ADDS and SUBS instructions implicitly contain the value 1 or 2 as immediate data. Some bit manipulation instructions contain 3-bit immediate data (#xx:3) in the second or fourth byte of the instruction, specifying a bit number.

7. Program-Counter-Relative—@(d:8, PC): This mode is used to generate branch addresses in the Bcc and BSR instructions. An 8-bit value in byte 2 of the instruction code is added as a sign-extended value to the program counter contents. The result must be an even number. The possible branching range is –126 to +128 bytes (–63 to +64 words) from the current address.

8. Memory Indirect—@@aa:8: This mode can be used by the JMP and JSR instructions. The second byte of the instruction code specifies an 8-bit absolute address from H'0000 to H'00FF (0 to 255). The word located at this address contains the branch address. The upper 8 bits of the absolute address are a 0 (H'00), thus the branch address is limited to values from 0 to 255 (H'0000 to H'00FF). Note that addresses H'0000 to H'0047 (0 to 71) are located in the vector table.With the H8/3332, addresses H’0000 to H’0041 (0 to 65) are located in the vector table.

   If an odd address is specified as a branch destination or as the operand address of a MOV.W instruction, the least significant bit is regarded as 0, causing word access to be performed at the address preceding the specified address. See section 3.4.2, Memory Data Formats, for further information.

3.3.1 How to Calculate Where the Execution Starts

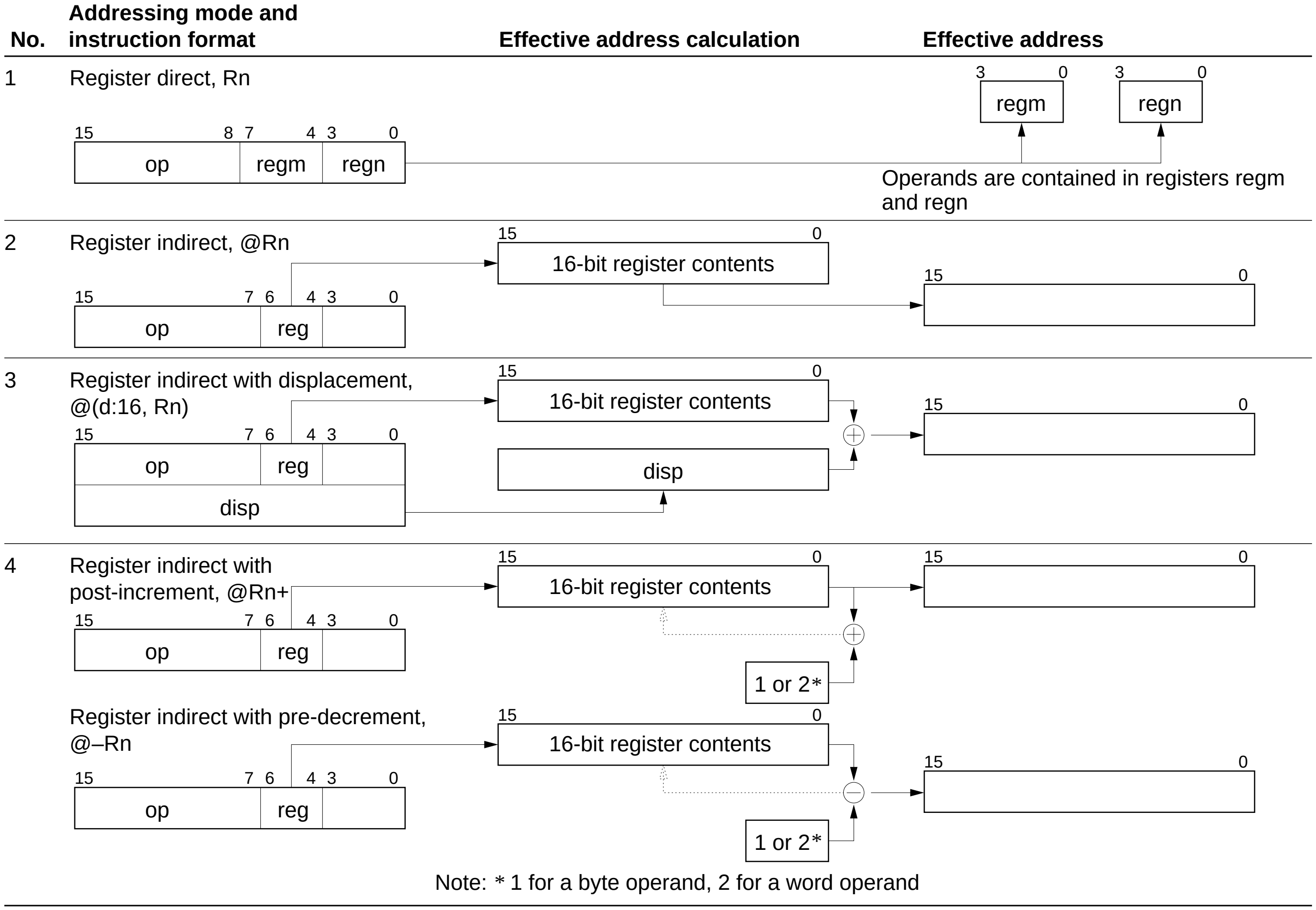
Table 3-2 shows how to calculate the Effective Address (EA:Effective Address) for each addressing mode.

In the operation instruction, 1) register direct, as well as 6) immediate (for each instruction, ADD.B, ADDX, SUBX, CMP.B, AND, OR, XOR) are used.

In the move instruction, 7) program counter relative and 8) all addressing mode to delete the memory indirect can be used.

In the bit manipulation instruction for the operand specifications, 1) register direct, 2) register indirect, as well as 5) absolute address (8 bit) can be used. Furthermore, to specify the bit number within the operand, 1) register direct (for each instruction, BSET, BCLR, BNOT, BTST) as well as 6) immediate (3 bit) can be used independently.

Table 3-2 Effective Address Calculation

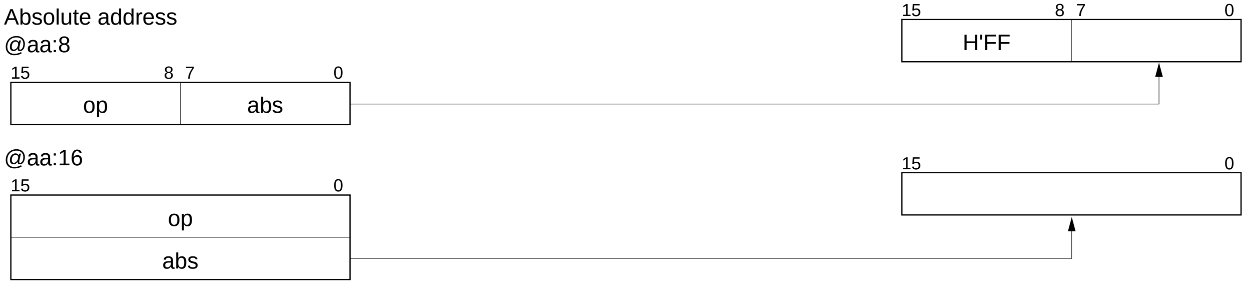


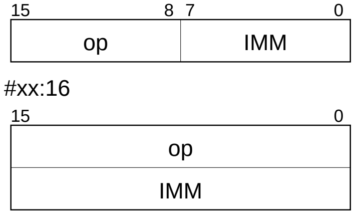
No.	Addressing mode and instruction format	Effective address calculation	Effective address
1	Register direct, Rn		Operands are contained in registers regm and regn
2	Register indirect, @Rn		
3	Register indirect with displacement, @(d:16, Rn)		
4	Register indirect with post-increment, @Rn+		
	Register indirect with pre-decrement, @–Rn		

Note: * 1 for a byte operand, 2 for a word operand

Table 3-2 Effective Address Calculation (cont)

No.	Addressing mode and instruction format	Effective address calculation	Effective address
5	Absolute address @aa:8 @aa:16		
6	Immediate #xx:8 #xx:16		Operand is 1- or 2-byte immediate data
7	PC-relative @(d:8, PC)		





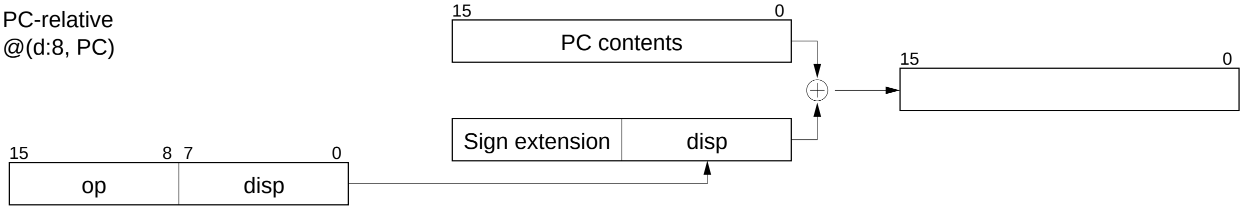
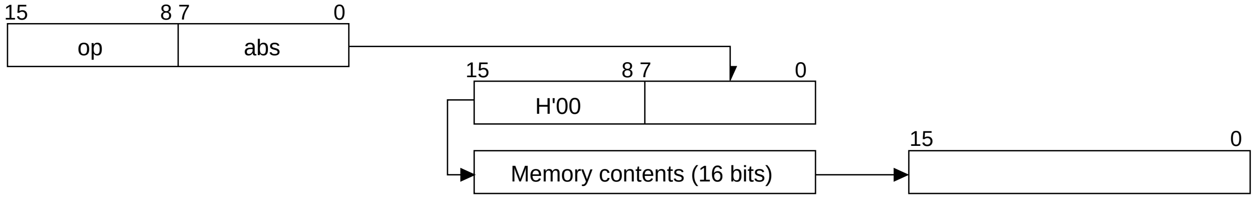


Table 3-2 Effective Address Calculation (cont)

No.	Addressing mode and instruction format	Effective address calculation	Effective address
8	Memory indirect, @@aa:8		

Notation

reg, regm, regn:	General register
op:	Operation field
disp:	Displacement
IMM:	Immediate data
abs:	Absolute address

3.4 Data Formats

The H8/300 CPU can process 1-bit data, 4-bit (BCD) data, 8-bit (byte) data, and 16-bit (word) data.

- Bit manipulation instructions operate on 1-bit data specified as bit n (n = 0, 1, 2,..., 7) in a byte operand.

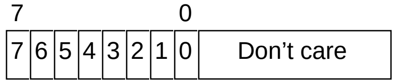
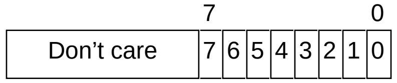
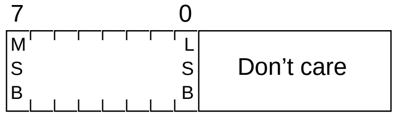
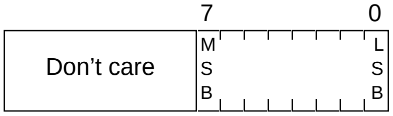
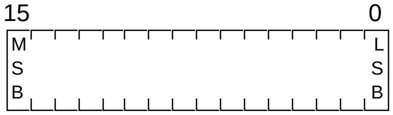
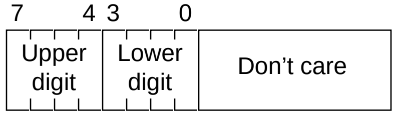
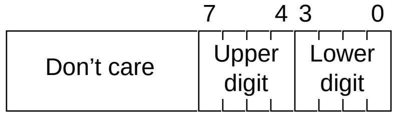
- All arithmetic and logic instructions except ADDS and SUBS can operate on byte data.

- The DAA and DAS instruction perform decimal arithmetic adjustments on byte data in packed BCD form. Each nibble of the byte is treated as a decimal digit.

- The MOV.W, ADD.W, SUB.W, CMP.W, ADDS, SUBS, MULXU (8 bits × 8 bits), and DIVXU (16 bits ÷ 8 bits) instructions operate on word data.

3.4.1 Data Formats in General Registers

Data of all the sizes above can be stored in general registers as shown in figure 3-3.

Data Type	Register Number	Data Format
1-bit data	RnH	
1-bit data	RnL	
Byte data	RnH	
Byte data	RnL	
Word data	Rn	
4-bit BCD data	RnH	
4-bit BCD data	RnL	

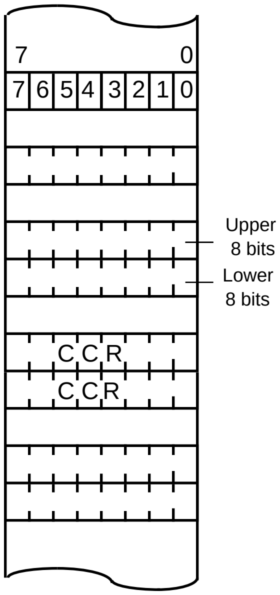
Note: RnH: Upper byte of general register
RnL: Lower byte of general register
MSB: Most significant bit
LSB: Least significant bit

Figure 3-3 Register Data Formats

3.4.2 Memory Data Formats

Figure 3-4 indicates the data formats in memory.

Word data stored in memory must always begin at an even address. In word access the least significant bit of the address is regarded as 0. If an odd address is specified, no address error occurs but the access is performed at the preceding even address. This rule affects MOV.W instructions and branching instructions, and implies that only even addresses should be stored in the vector table.

Data Type	Address	Data Format
1-bit data	Address n	
Byte data	Address n	
Word data	Even address	
	Odd address	
Byte data (CCR) on stack	Even address	
	Odd address	
Word data on stack	Even address	
	Odd address	

CCR: Condition Code Register

Figure 3-4 Memory Data Formats

When the stack is addressed by register R7, it must always be accessed a word at a time. When the CCR is pushed on the stack, two identical copies of the CCR are pushed to make a complete word. When they are returned, the lower byte is ignored.

3.5 Instruction Set

Table 3-3 lists the H8/300 instruction set.

Table 3-3 Instruction Classification

Function	Instructions	Types
Data transfer	MOV, MOVTPE [Note 3], MOVFPE [Note 3], PUSH [Note 1], POP [Note 1]	3
Arithmetic operations	ADD, SUB, ADDX, SUBX, INC, DEC, ADDS, SUBS, DAA, DAS, MULXU, DIVXU, CMP, NEG	14
Logic operations	AND, OR, XOR, NOT	4
Shift	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR	8
Bit manipulation	BSET, BCLR, BNOT, BTST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR, BLD, BILD, BST, BIST	14
Branch	Bcc [Note 2], JMP, BSR, JSR, RTS	5
System control	RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP	8
Block data transfer	EEPMOV	1
		Total: 57

Notes: 1. PUSH Rn is equivalent to MOV.W Rn, @–SP.
POP Rn is equivalent to MOV.W @SP+, Rn.
2 Bcc is a conditional branch instruction in which cc represents a condition code.
3. Not supported by the H8/3332.

The following sections give a concise summary of the instructions in each category, and indicate the bit patterns of their object code. The notation used is defined in table 3-4.

Table 3-4 Operation Notation

Notation	Meaning	Notation	Meaning
Rd	General register (destination)	#xx:3	3-bit immediate data
Rs	General register (source)	#xx:8	8-bit immediate data
Rn	General register	#xx:16	16-bit immediate data
(EAd)	Destination operand	disp	Displacement
(EAs)	Source operand	+	Addition
SP	Stack pointer	–	Subtraction
PC	Program counter	×	Multiplication
CCR	Condition code register	÷	Division
N	N (negative) bit of CCR	∧	AND logical
Z	Z (zero) bit of CCR	∨	OR logical
V	V (overflow) bit of CCR	⊕	Exclusive OR logical
C	C (carry) bit of CCR	→	Move
#imm	Immediate data	¬	Not

Note: :3/:8/:16 represents 3, 8, or 16 bit length.

3.5.1 Data Transfer Instructions

Table 3-5 describes the data transfer instructions. Figure 3-5 shows their object code formats.

Table 3-5 Data Transfer Instructions

Instruction	**Size** [Note]	**Function**
MOV	B/W	(EAs) → Rd, Rs → (EAd) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register. The Rn, @Rn, @(d:16, Rn), @aa:16, #xx:8 or #xx:16, @–Rn, and @Rn+ addressing modes are available for byte or word data. The @aa:8 addressing mode is available for byte data only. The @–R7 and @R7+ modes require word operands. Do not specify byte size for these two modes.
MOVTPE	B	Not supported.
MOVFPE	B	Not supported.
PUSH	W	Rn → @–SP Pushes a 16-bit general register onto the stack. Equivalent to MOV.W Rn, @–SP.
POP	W	@SP+ → Rn Pops a 16-bit general register from the stack. Equivalent to MOV.W @SP+, Rn.

Note: Size: operand size
B: Byte
W: Word

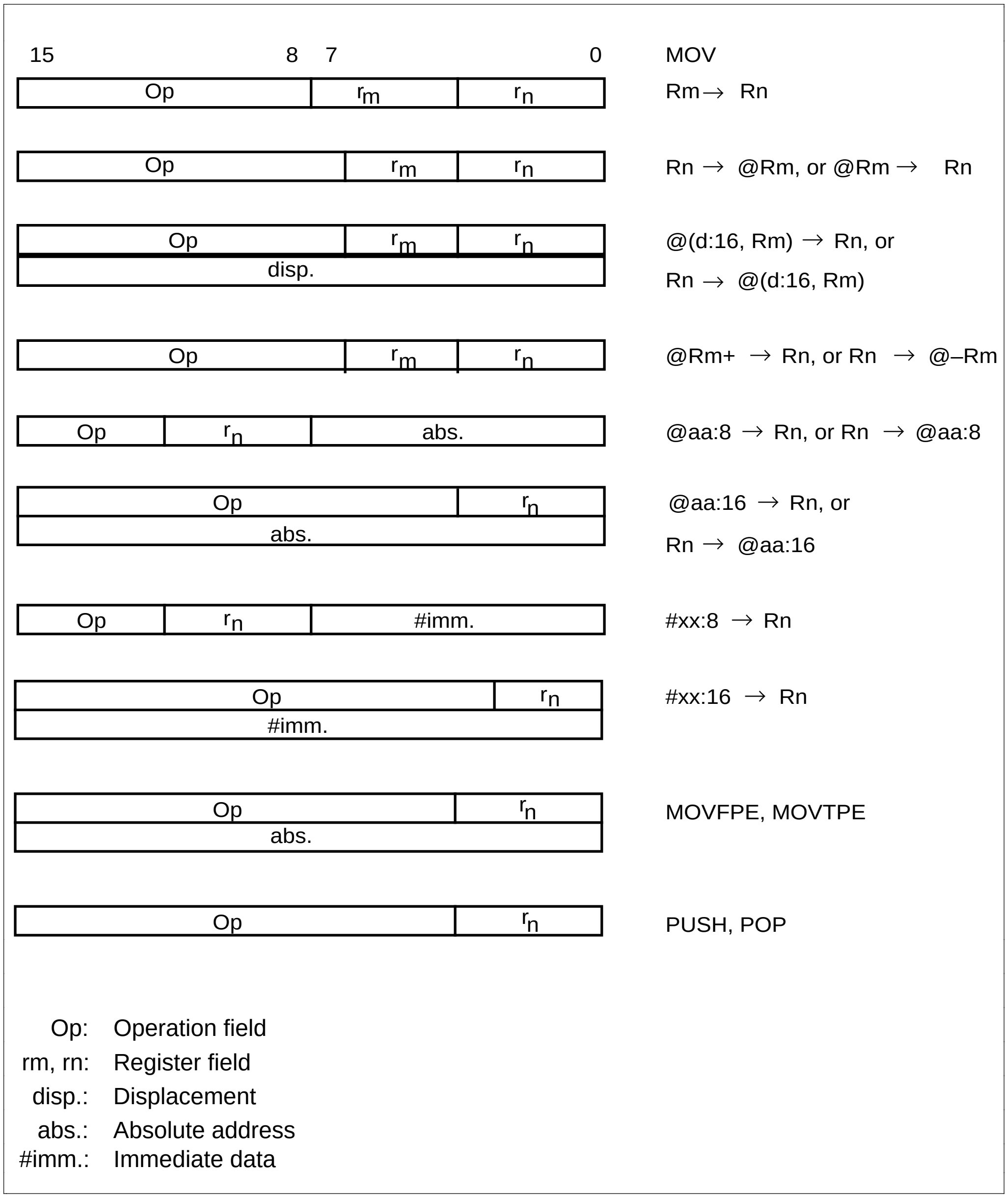


Figure 3-5 Data Transfer Instruction Codes

3.5.2 Arithmetic Operations

Table 3-6 describes the arithmetic instructions. See figure 3-6 in section 3.5.4, “Shift Operations” for their object codes.

Table 3-6 Arithmetic Instructions

Instruction	Size Note	Function
ADD SUB	B/W	Rd ± Rs → Rd, Rd + #imm → Rd Adds or subtracts data in two general registers, or adds immediate data and data in a general register. Immediate data cannot be subtracted from data in a general register. Word data can be added or subtracted only when both words are in general registers.
ADDX SUBX	B	Rd ± Rs ± C → Rd, Rd ± #imm ± C → Rd Adds or subtracts with carry or borrow on byte data in two general registers, or adds or subtracts immediate data and data in a general register.
INC DEC	B	Rd ± #1 → Rd Increments or decrements a general register.
ADDS SUBS	W	Rd ± #imm → Rd Adds or subtracts immediate data to or from data in a general register. The immediate data must be 1 or 2.
DAA DAS	B	Rd decimal adjust → Rd Decimal-adjusts (adjusts to packed BCD) an addition or subtraction result in a general register by referring to the CCR.
MULXU	B	Rd × Rs → Rd Performs 8-bit × 8-bit unsigned multiplication on data in two general registers, providing a 16-bit result.
DIVXU	B	Rd ÷ Rs → Rd Performs 16-bit ÷ 8-bit unsigned division on data in two general registers, providing an 8-bit quotient and 8-bit remainder.
CMP	B/W	Rd – Rs, Rd – #imm Compares data in a general register with data in another general register or with immediate data. Word data can be compared only between two general registers.
NEG	B	0 – Rd → Rd Obtains the two's complement (arithmetic complement) of data in a general register.

Notes: Size: operand size
B: Byte
W: Word

3.5.3 Logic Operations

Table 3-7 describes the four instructions that perform logic operations. See figure 3-6 in section 3.5.4, Shift Operations, for their object codes.

Table 3-7 Logic Operation Instructions

Instruction	Size Note	Function
AND	B	Rd ∧ Rs → Rd, Rd ∧ #imm → Rd Performs a logical AND operation on a general register and another general register or immediate data.
OR	B	Rd ∨ Rs → Rd, Rd ∨ #imm → Rd Performs a logical OR operation on a general register and another general register or immediate data.
XOR	B	Rd ⊕ Rs → Rd, Rd ⊕ #imm → Rd Performs a logical exclusive OR operation on a general register and another general register or immediate data.
NOT	B	¬ (Rd) → (Rd) Obtains the one’s complement (logical complement) of general register contents.

Note: Size: operand size
B: Byte

3.5.4 Shift Operations

Table 3-8 describes the eight shift instructions. Figure 3-6 shows the object code formats of the arithmetic, logic, and shift instructions.

Table 3-8 Shift Instructions

Instruction	Size Note	Function
SHAL SHAR	B	Rd shift → Rd Performs an arithmetic shift operation on general register contents.
SHLL SHLR	B	Rd shift → Rd Performs a logical shift operation on general register contents.
ROTL ROTR	B	Rd rotate → Rd Rotates general register contents.
ROTXL ROTXR	B	Rd rotate through carry → Rd Rotates general register contents through the C (carry) bit.

Note: Size: operand size
B: Byte

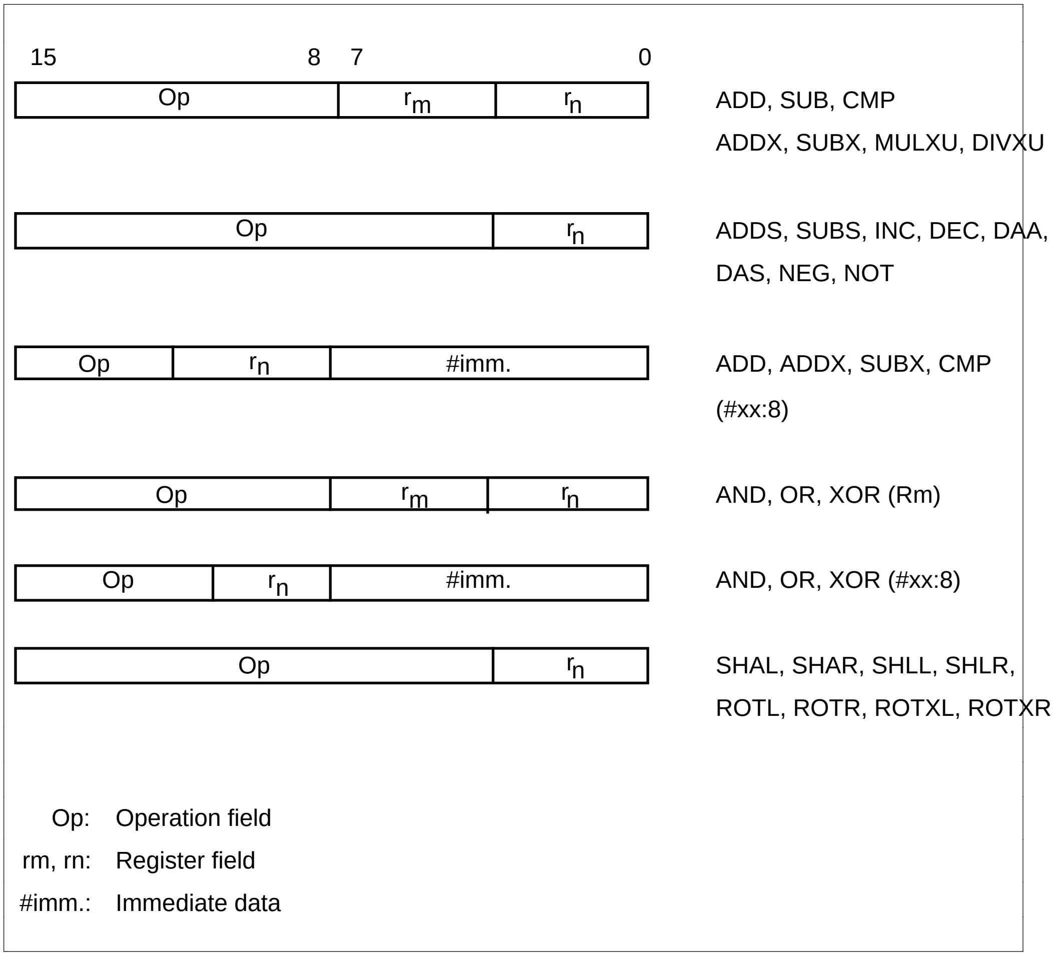


Figure 3-6 Arithmetic, Logic, and Shift Instruction Codes

3.5.5 Bit Manipulations

Table 3-9 describes the bit-manipulation instructions. Figure 3-7 shows their object code formats.

Table 3-9 Bit-Manipulation Instructions (1)

Instruction	Size Note	Function
BSET	B	1 → (<bit-No.> of <EAd>) Sets a specified bit in a general register or memory to 1. The bit is specified by a bit number, given in 3-bit immediate data or the lower three bits of a general register.
BCLR	B	0 → (<bit-No.> of <EAd>) Clears a specified bit in a general register or memory to 0. The bit is specified by a bit number, given in 3-bit immediate data or the lower three bits of a general register.
BNOT	B	¬(<bit-No.> of <EAd>) → (<bit-No.> of <EAd>) Inverts a specified bit in a general register or memory. The bit is specified by a bit number, given in 3-bit immediate data or the lower three bits of a general register
BTST	B	¬ (<bit-No.> of <EAd>) → Z Tests a specified bit in a general register or memory and sets or clears the Z flag accordingly. The bit is specified by a bit number, given in 3-bit immediate data or the lower three bits of a general register.
BAND	B	C ∧ (<bit-No.> of <EAd>) → C ANDs the C flag with a specified bit in a general register or memory.
BIAND		C ∧ [¬ (<bit-No.> of <EAd>)] → C ANDs the C flag with the inverse of a specified bit in a general register or memory. The bit number is specified by 3-bit immediate data.
BOR	B	C ∨ (<bit-No.> of <EAd>) → C ORs the C flag with a specified bit in a general register or memory.
BIOR		C ∨ [¬ (<bit-No.> of <EAd>)] → C ORs the C flag with the inverse of a specified bit in a general register or memory. The bit number is specified by 3-bit immediate data.

Table 3-9 Bit-Manipulation Instructions (cont)

Instruction	Size Note	Function
BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C XORs the C flag with a specified bit in a general register or memory.
BIXOR		C ⊕ ¬ [(<bit-No.> of <EAd>)] → C XORs the C flag with the inverse of a specified bit in a general register or memory. The bit number is specified by 3-bit immediate data.
BLD	B	(<bit-No.> of <EAd>) → C Copies a specified bit in a general register or memory to the C flag.
BILD		¬ (<bit-No.> of <EAd>) → C Copies the inverse of a specified bit in a general register or memory to the C flag. The bit number is specified by 3-bit immediate data.
BST	B	C → (<bit-No.> of <EAd>) Copies the C flag to a specified bit in a general register or memory.
BIST		¬ C → (<bit-No.> of <EAd>) Copies the inverse of the C flag to a specified bit in a general register or memory. The bit number is specified by 3-bit immediate data.

Note: Size: operand size
B: Byte

Notes on Bit Manipulation Instructions: BSET, BCLR, BNOT, BST, and BIST are read-modify-write instructions. They read a byte of data, modify one bit in the byte, then write the byte back. Care is required when these instructions are applied to registers with write-only bits and to the I/O port registers.

Step		Description
1	Read	Read one byte at the specified address
2	Modify	Modify one bit in the byte data
3	Write	Write the modified data byte back to the specified address

Example 1: BCLR is executed to clear bit 0 in the port 4 data direction register (P4DDR) under the following conditions.

- $P4_7$: Input pin, low
- $P4_6$: Input pin, high
- $P4_5$–$P4_0$: Output pins, low

The intended purpose of this BCLR instruction is to switch $P4_0$ from output to input.

Before Execution of BCLR Instruction:

	$P4_7$	$P4_6$	$P4_5$	$P4_4$	$P4_3$	$P4_2$	$P4_1$	$P4_0$
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low	High	Low	Low	Low	Low	Low	Low
DDR	0	0	1	1	1	1	1	1
DR	1	0	0	0	0	0	0	0

Execution of BCLR Instruction:

```
BCLR  #0, @P4DDR ;clear bit 0 in data direction register
```

After Execution of BCLR Instruction:

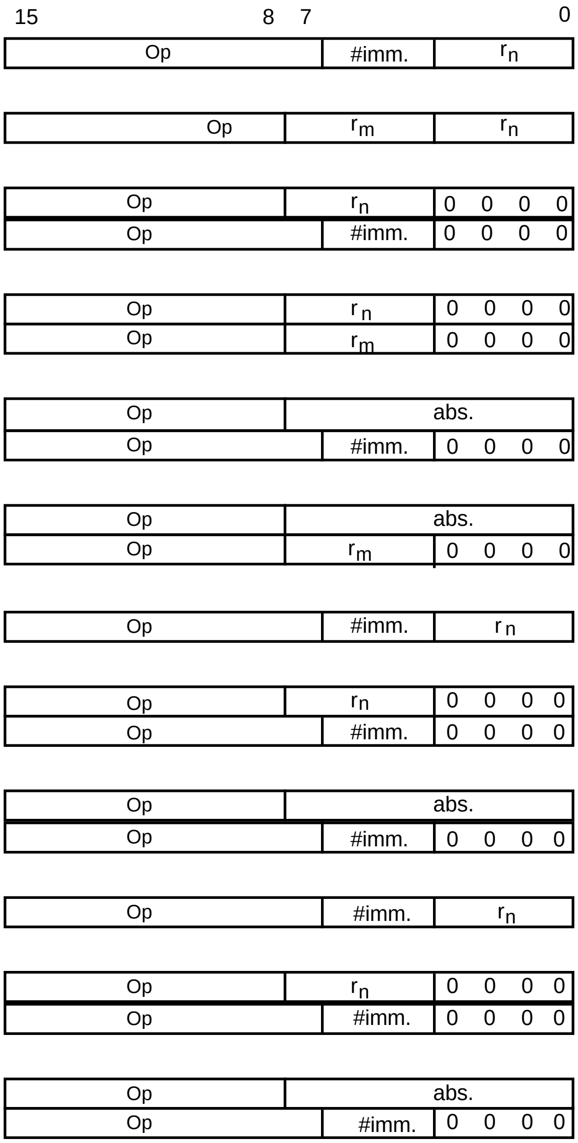
	P47	P46	P45	P44	P43	P42	P41	P40
Input/output	Output	Output	Output	Output	Output	Output	Output	Input
Pin state	Low	High	Low	Low	Low	Low	Low	High
DDR	1	1	1	1	1	1	1	0
DR	1	0	0	0	0	0	0	0

Explanation: To execute the BCLR instruction, the CPU begins by reading P4DDR. Since P4DDR is a write-only register, it is read as H'FF, even though its true value is H'3F.

Next the CPU clears bit 0 of the read data, changing the value to H'FE.

Finally, the CPU writes this value (H'FE) back to P4DDR to complete the BCLR instruction.

As a result, P40DDR is cleared to 0, making $P4_0$ an input pin. In addition, P47DDR and P46DDR are set to 1, making $P4_7$ and $P4_6$ output pins.



BSET, BCLR, BNOT, BTST
Operand: register direct (Rn)
Bit No.: immediate (#xx:3)

Operand: register direct (Rn)
Bit No.: register direct (Rm)

Operand: register indirect (@Rn)
Bit No.: immediate (#xx:3)

Operand: register indirect (@Rn)
Bit No.: register direct (Rm)

Operand: absolute (@aa:8)
Bit No.: immediate (#xx:3)

Operand: absolute (@aa:8)
Bit No.: register direct (Rm)

BAND, BOR, BXOR, BLD, BST
Operand: register direct (Rn)
Bit No.: immediate (#xx:3)

Operand: register indirect (@Rn)
Bit No.: immediate (#xx:3)

Operand: absolute (@aa:8)
Bit No.: immediate (#xx:3)

BIAND, BIOR, BIXOR, BILD, BIST
Operand: register direct (Rn)
Bit No.: immediate (#xx:3)

Operand: register indirect (@Rn)
Bit No.: immediate (#xx:3)

Operand: absolute (@aa:8)
Bit No.: immediate (#xx:3)

Op: Operation field
rm, rn: Register field
abs.: Absolute address
#imm.: Immediate data

Figure 3-7 Bit Manipulation Instruction Codes

3.5.6 Branching Instructions

Table 3-10 describes the branching instructions. Figure 3-8 shows their object code formats.

Table 3-10 Branching Instructions

Instruction	Size	Function
Bcc	—	Branches if condition cc is true.

Mnemonic	cc field	Description	Condition
BRA (BT)	0 0 0 0	Always (True)	Always
BRN (BF)	0 0 0 1	Never (False)	Never
BHI	0 0 1 0	High	$C \vee Z = 0$
BLS	0 0 1 1	Low or Same	$C \vee Z = 1$
BCC (BHS)	0 1 0 0	Carry Clear (High or Same)	$C = 0$
BCS (BLO)	0 1 0 1	Carry Set (Low)	$C = 1$
BNE	0 1 1 0	Not Equal	$Z = 0$
BEQ	0 1 1 1	Equal	$Z = 1$
BVC	1 0 0 0	Overflow Clear	$V = 0$
BVS	1 0 0 1	Overflow Set	$V = 1$
BPL	1 0 1 0	Plus	$N = 0$
BMI	1 0 1 1	Minus	$N = 1$
BGE	1 1 0 0	Greater or Equal	$N \oplus V = 0$
BLT	1 1 0 1	Less Than	$N \oplus V = 1$
BGT	1 1 1 0	Greater Than	$Z \vee (N \oplus V) = 0$
BLE	1 1 1 1	Less or Equal	$Z \vee (N \oplus V) = 1$

JMP	—	Branches unconditionally to a specified address.
JSR	—	Branches to a subroutine at a specified address.
BSR	—	Branches to a subroutine at a specified displacement from the current address.
RTS	—	Returns from a subroutine

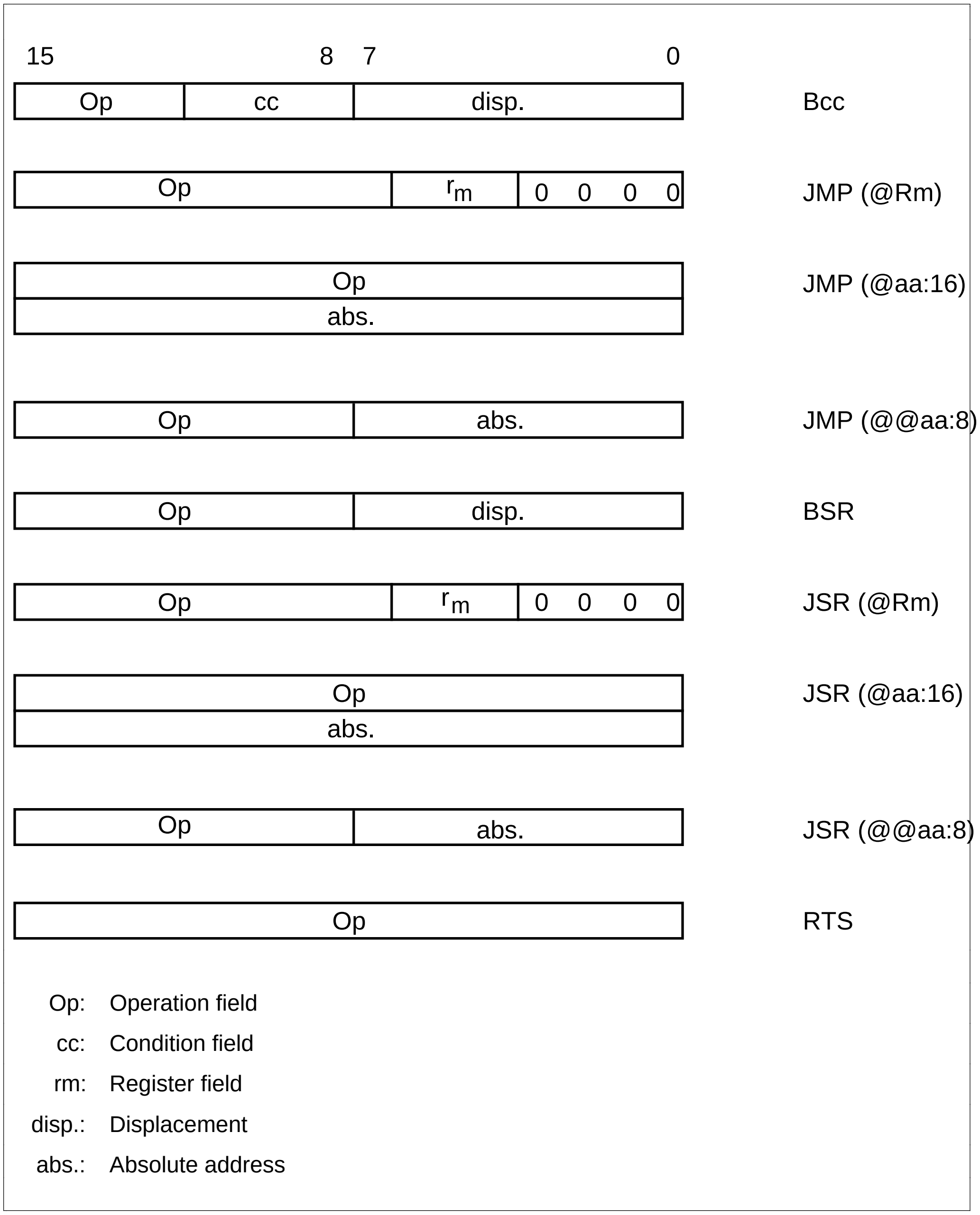


Figure 3-8 Branching Instruction Codes

3.5.7 System Control Instructions

Table 3-11 describes the system control instructions. Figure 3-9 shows their object code formats.

Table 3-11 System Control Instructions

Instruction	Size Note	Function
RTE	—	Returns from an exception-handling routine.
SLEEP	—	Causes a transition to the power-down state.
LDC	B	Rs → CCR, #imm → CCR Moves immediate data or general register contents to the condition code register.
STC	B	CCR → Rd Copies the condition code register to a specified general register.
ANDC	B	CCR ∧ #imm → CCR Logically ANDs the condition code register with immediate data.
ORC	B	CCR ∨ #imm → CCR Logically ORs the condition code register with immediate data.
XORC	B	CCR ⊕ #imm → CCR Logically exclusive-ORs the condition code register with immediate data.
NOP	—	PC + 2 → PC Only increments the program counter.

Note: Size: operand size

B: Byte

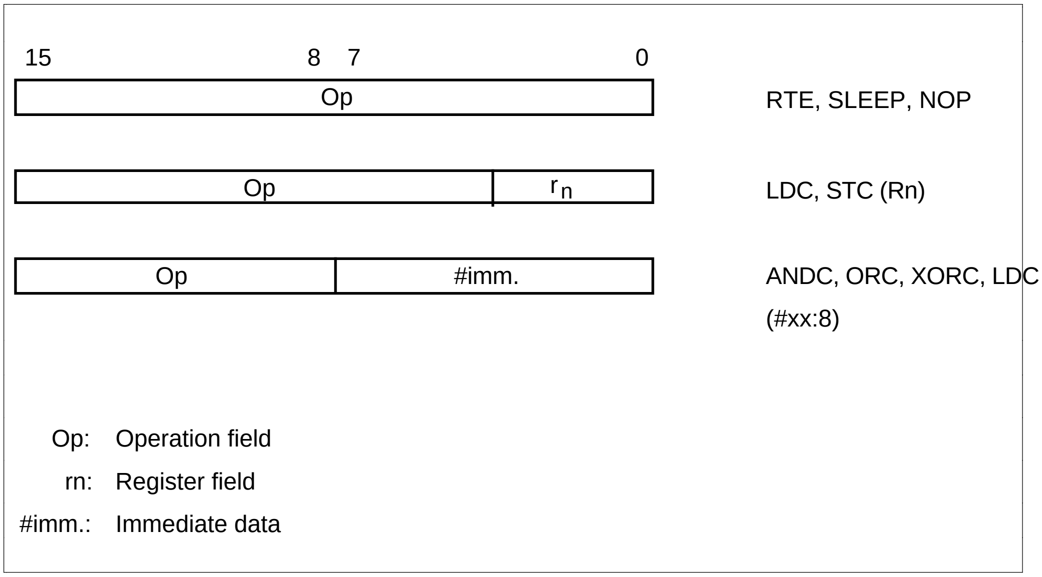


Figure 3-9 System Control Instruction Codes

3.5.8 Block Data Transfer Instruction

Table 3-12 describes the EEPMOV instruction. Figure 3-10 shows its object code format.

Table 3-12 Block Data Transfer Instruction/EEPROM Write Operation

Instruction	Size	Function
EEPMOV	—	if R4L ≠ 0 then repeat @R5+ → @R6+ R4L − 1 → R4L until R4L = 0 else next; Moves a data block according to parameters set in general registers R4L, R5, and R6. R4L: size of block (bytes) R5: starting source address R6: starting destination address Execution of the next instruction starts as soon as the block transfer is completed.

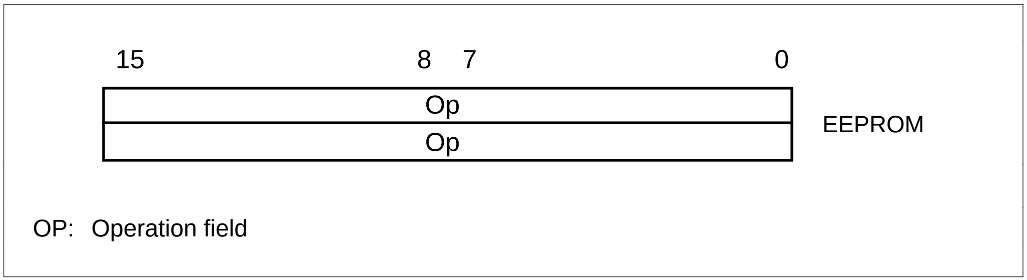


Figure 3-10 Block Data Transfer Instruction/EEPROM Write Operation Code

Notes on EEPMOV Instruction:

1. The EEPMOV instruction is a block data transfer instruction. It moves the number of bytes specified by R4L from the address specified by R5 to the address specified by R6. (See figure 3-11a.)

2. When setting R4L and R6, make sure that the final destination address (R6 + R4L) does not exceed H'FFFF. The value in R6 must not change from H'FFFF to H'0000 during execution of the instruction. (See figure 3-11b.)

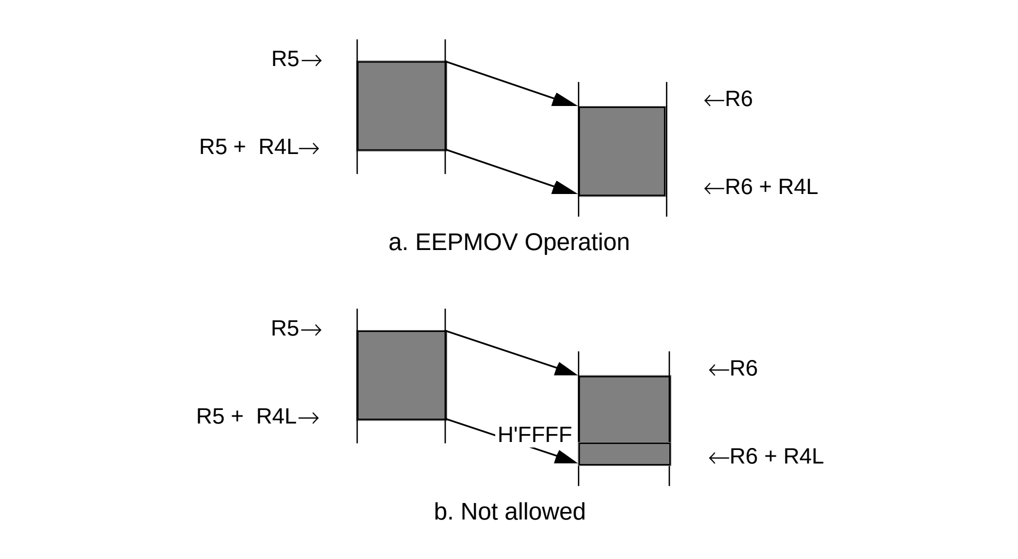


Figure 3-11 EEPMOV Instruction

3.6 CPU States

The CPU has three states: the program execution state, exception-handling state, and power-down state. The power-down state is further divided into three modes: the sleep mode, software standby mode, and hardware standby mode. Figure 3-12 summarizes these states, and figure 3-13 shows a map of the state transitions.

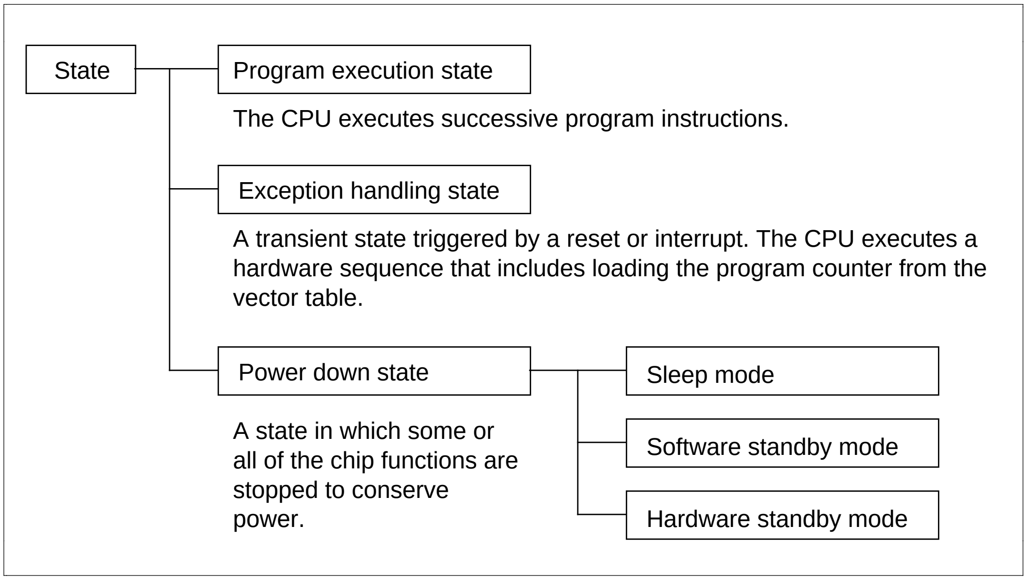
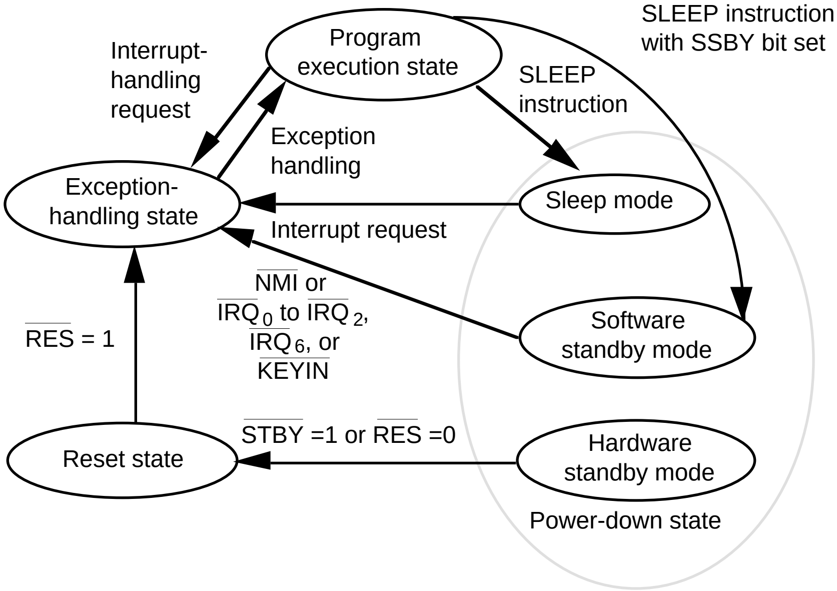

State
Program execution state
The CPU executes successive program instructions.
Exception handling state
A transient state triggered by a reset or interrupt. The CPU executes a hardware sequence that includes loading the program counter from the vector table.
Power down state
A state in which some or all of the chip functions are stopped to conserve power.
Sleep mode
Software standby mode
Hardware standby mode

Figure 3-12 Operating States



Notes: 1. A transition to the reset state occurs when $\overline{\text{RES}}$ goes low or by watchdog timer overflow (with reset option selected), except when the chip is in the hardware standby mode.

2. A transition from any state to the hardware standby mode occurs when $\overline{\text{STBY}}$ goes low.

Figure 3-13 State Transitions

3.6.1 Program Execution State

In program execution state the CPU executes program instructions.

3.6.2 Exception-Handling State

The exception-handling state is a transient state that occurs when the CPU is reset or accepts an interrupt. In this state the CPU carries out a hardware-controlled sequence that prepares it to execute a user-coded exception-handling routine.

In the hardware exception-handling sequence the CPU does the following:

1. Saves the program counter and condition code register to the stack (except in the case of a reset).

2. Sets the interrupt mask (I) bit in the condition code register to 1.

3. Fetches the start address of the exception-handling routine from the vector table.

4. Branches to that address, returning to the program execution state.

See section 4, Exception Handling, for further information on the exception-handling state.

3.6.3 Power-Down State

The power-down state includes three modes: the sleep mode, the software standby mode, and the hardware standby mode.

Sleep Mode: The sleep mode is entered when a SLEEP instruction is executed. The CPU halts, but CPU register contents remain unchanged and the on-chip supporting modules continue to function.

Software Standby Mode: The software standby mode is entered if the SLEEP instruction is executed while the SSBY (Software Standby) bit in the system control register (SYSCR) is set. The CPU and all on-chip supporting modules halt. The on-chip supporting modules are initialized, but the contents of the on-chip RAM and CPU registers remain unchanged. I/O port outputs also remain unchanged.

Hardware Standby Mode: The hardware standby mode is entered when the input at the $\overline{\text{STBY}}$ pin goes low. All chip functions halt, including I/O port output. The on-chip supporting modules are initialized, but on-chip RAM contents are held.

See section 15, Power-Down State, for further information.

3.7 Access Timing and Bus Cycle

The CPU is driven by the system clock (ϕ). The period from one rising edge of the system clock to the next is referred to as a "state."

Memory access is performed in a two- or three-state bus cycle. On-chip memory, on-chip supporting modules, and external devices are accessed in different bus cycles as described below.

3.7.1 Access to On-Chip Memory (RAM and ROM)

On-chip ROM and RAM are accessed in a cycle of two states designated T1 and T2. Either byte or word data can be accessed, via a 16-bit data bus. Figure 3-14 shows the on-chip memory access cycle. Figure 3-15 shows the associated pin states.

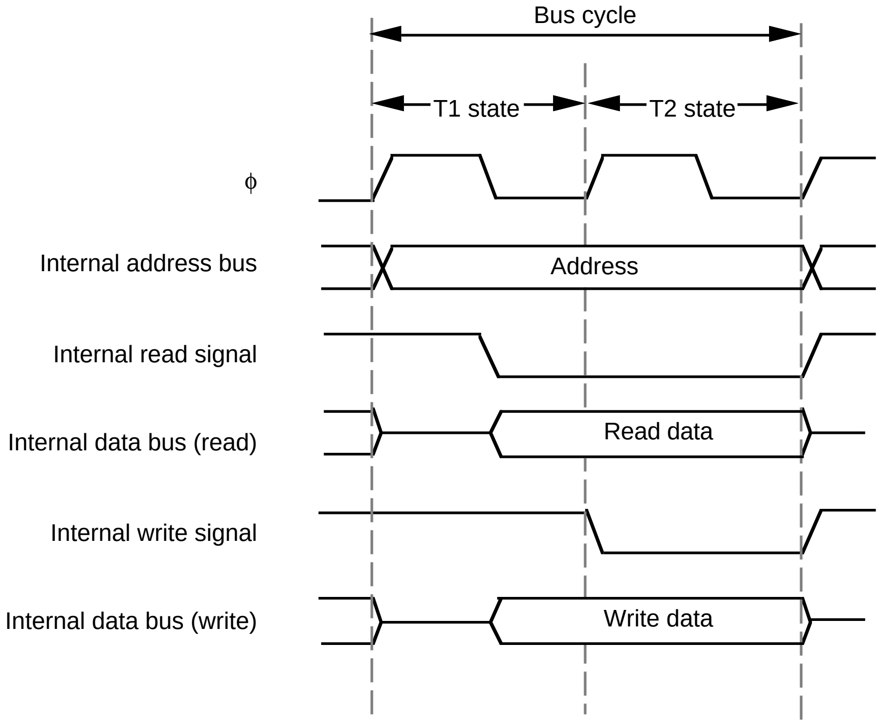


Figure 3-14 On-Chip Memory Access Cycle

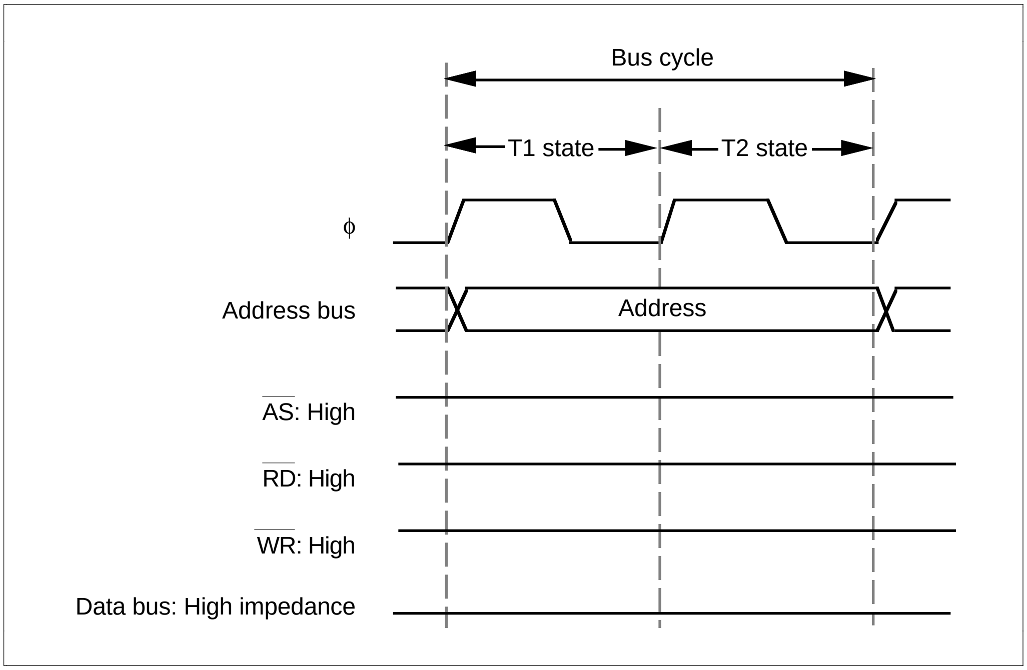


Figure 3-15 Pin States during On-Chip Memory Access Cycle

3.7.2 Access to On-Chip Register Field and External Devices

The on-chip register field (I/O ports, on-chip supporting module registers, etc.) and external devices are accessed in a cycle consisting of three states: T1, T2, and T3. Only one byte of data can be accessed per cycle, via an 8-bit data bus. Access to word data or instruction codes requires two consecutive cycles (six states).

Figure 3-16 shows the access cycle for the on-chip register field. Figure 3-17 shows the associated pin states. Figures 3-18 and 3-19 show the read and write access timing for external devices.

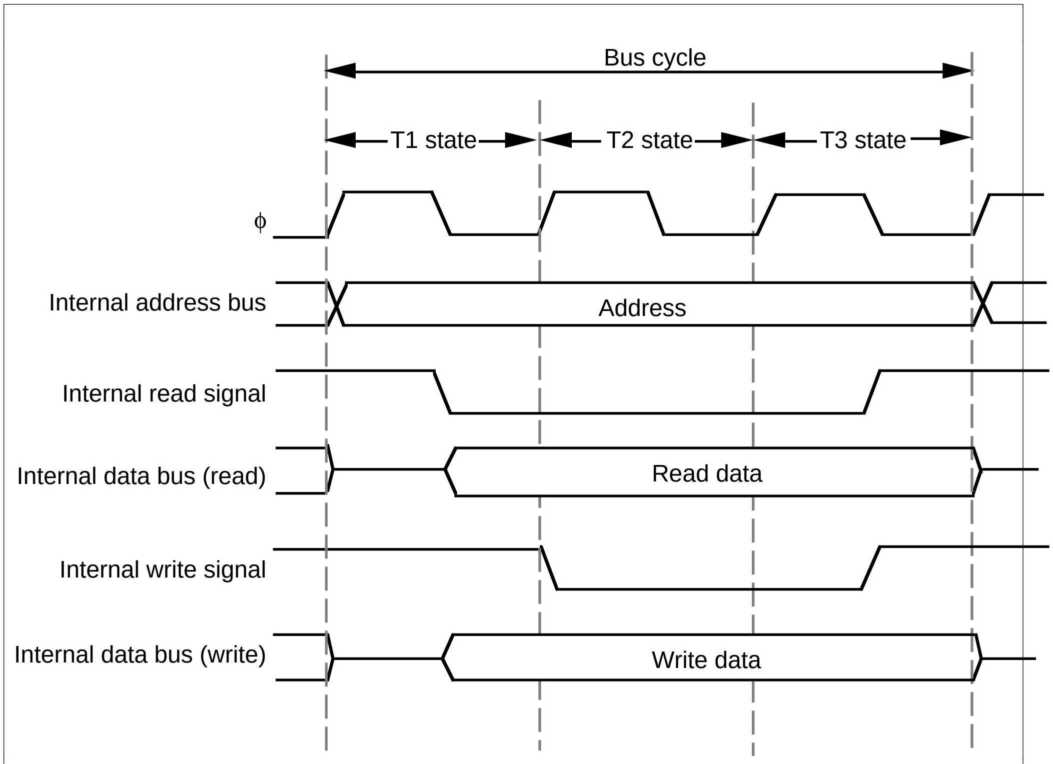


Figure 3-16 On-Chip Register Field Access Cycle

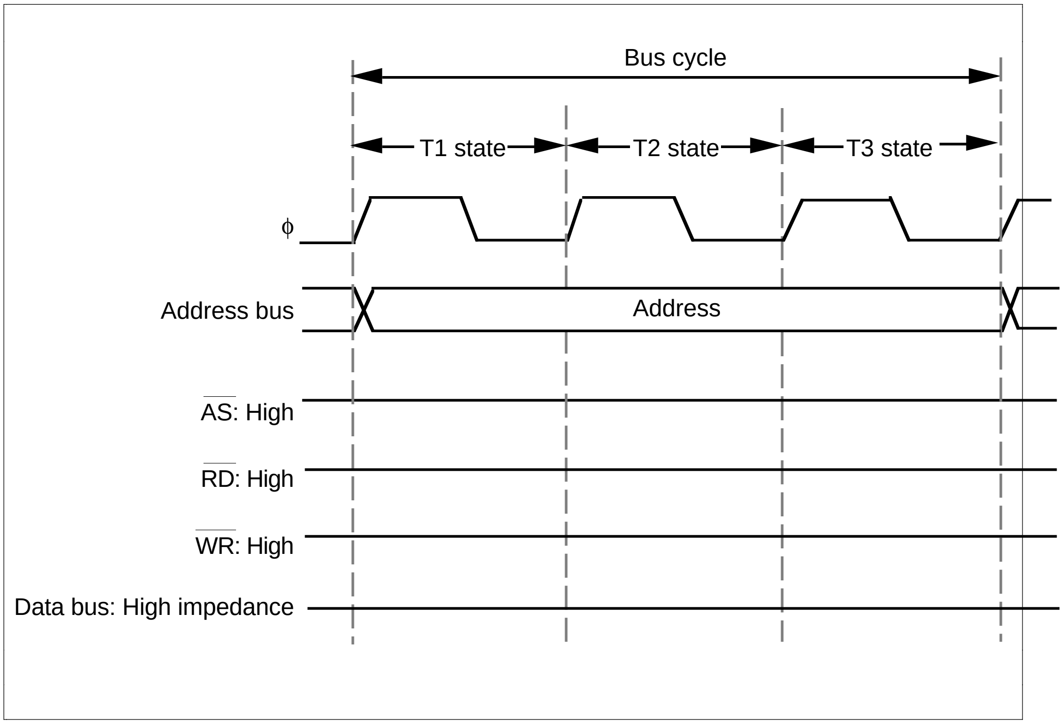


Figure 3-17 Pin States during On-Chip Register Field Access Cycle

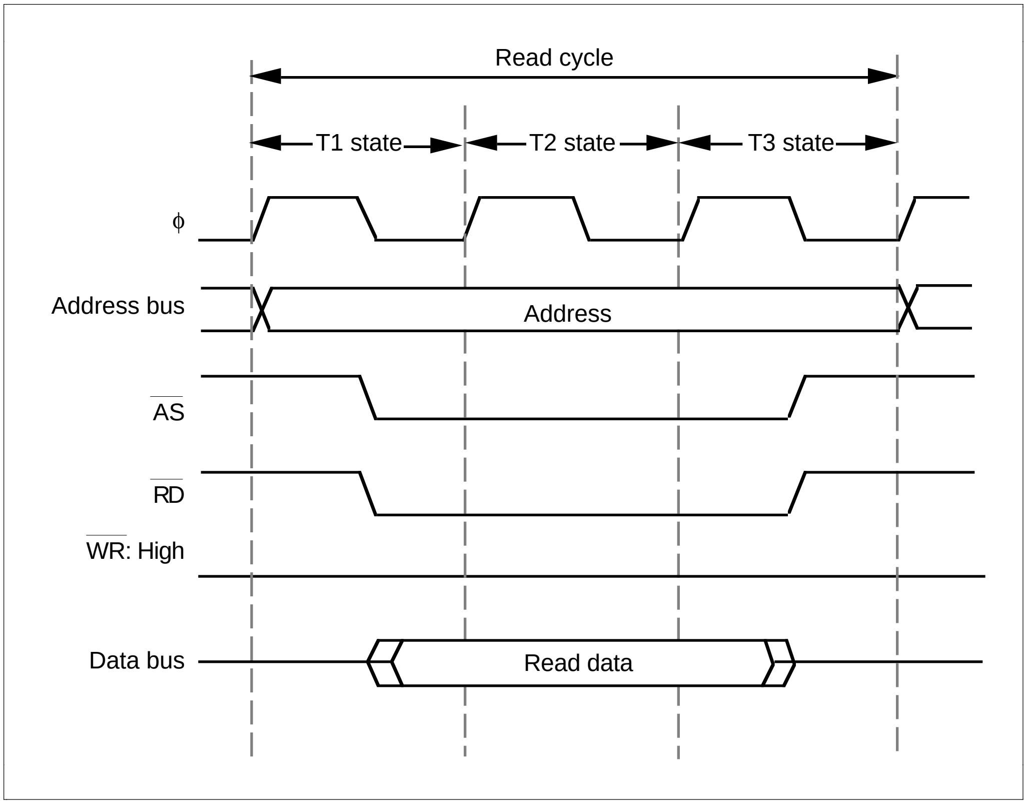


Figure 3-18 External Device Read Access Timing

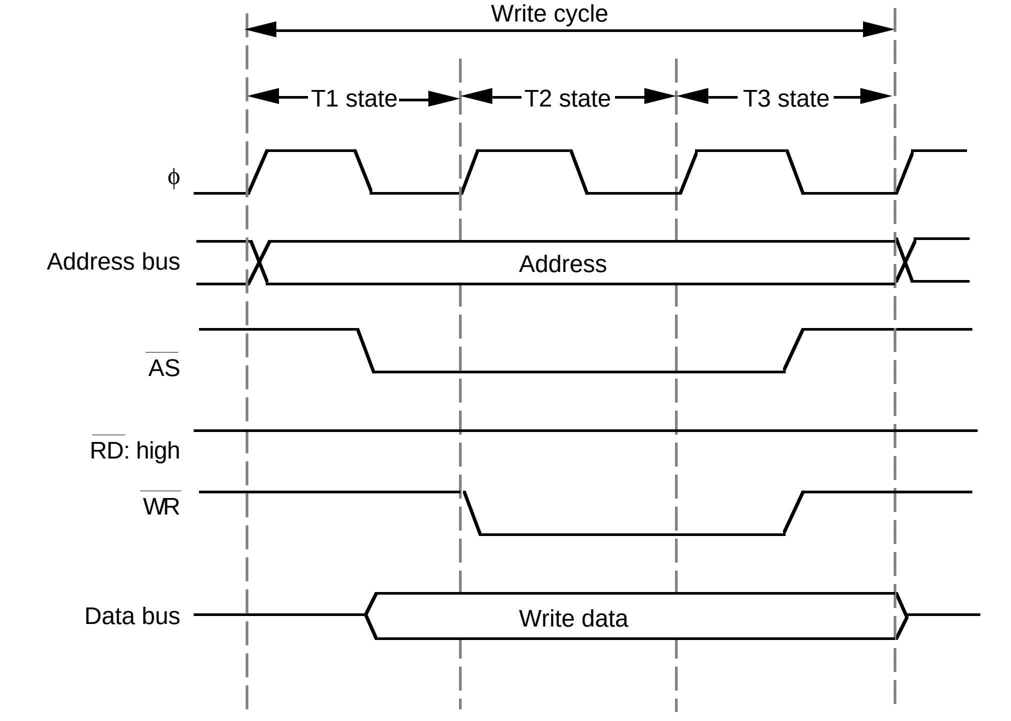


Figure 3-19 External Device Write Access Timing

Section 4 Exception Handling

4.1 Overview

The H8/3332 recognizes only two kinds of exceptions: interrupts and the reset. Table 4-1 indicates their priority and the timing of their hardware exception-handling sequence.

Table 4-1 Hardware Exception-Handling Sequences and Priority

Priority	Type of exception	Timing of exception-handling sequence
High ↑	Reset	The hardware exception-handling sequence begins as soon as$\overline{\text{RES}}$ changes from low to high.
	Interrupt	When an interrupt is requested, the hardware exception-handling sequence begins at the end of the current instruction, or at the end of the current hardware exception-handling sequence.
Low		

4.2 Reset

4.2.1 Overview

A reset has the highest exception-handling priority. When the $\overline{\text{RES}}$ pin goes low or watchdog timer overflow (with reset option selected) starts, all current processing stops and the chip enters the reset state. The internal state of the CPU and the registers of the on-chip supporting modules are initialized. When reset becomes inactive ($\overline{\text{RES}}$ returns from low to high, or at the end of watchdog reset pulse), the reset exception-handling sequence starts.

4.2.2 Reset Sequence

The reset state begins when either the $\overline{\text{RES}}$ pin goes low or watchdog timer overflows (with reset option selected). To ensure correct resetting, at power-on the $\overline{\text{RES}}$ pin should be held low for at least 20 ms. In a reset during operation, the $\overline{\text{RES}}$ pin should be held low for at least 10 system clock cycles. The watchdog reset pulse width is always 12 system clock periods. For the pin states during a reset, see appendix C, Pin States.

When reset becomes inactive, hardware carries out the following reset exception-handling sequence.

1. The registers of the CPU and on-chip supporting modules are initialized, and the I bit in the condition code register (CCR) is set to 1

2. The CPU loads the program counter with the first word in the vector table (stored at addresses H'0000 and H'0001) and starts program execution.

The $\overline{\text{RES}}$ pin should be held low when power is switched off, as well as when power is switched on.

Figure 4-1 indicates the timing of the reset sequence in modes 2 and 3. Figure 4-2 indicates the timing in mode 1.

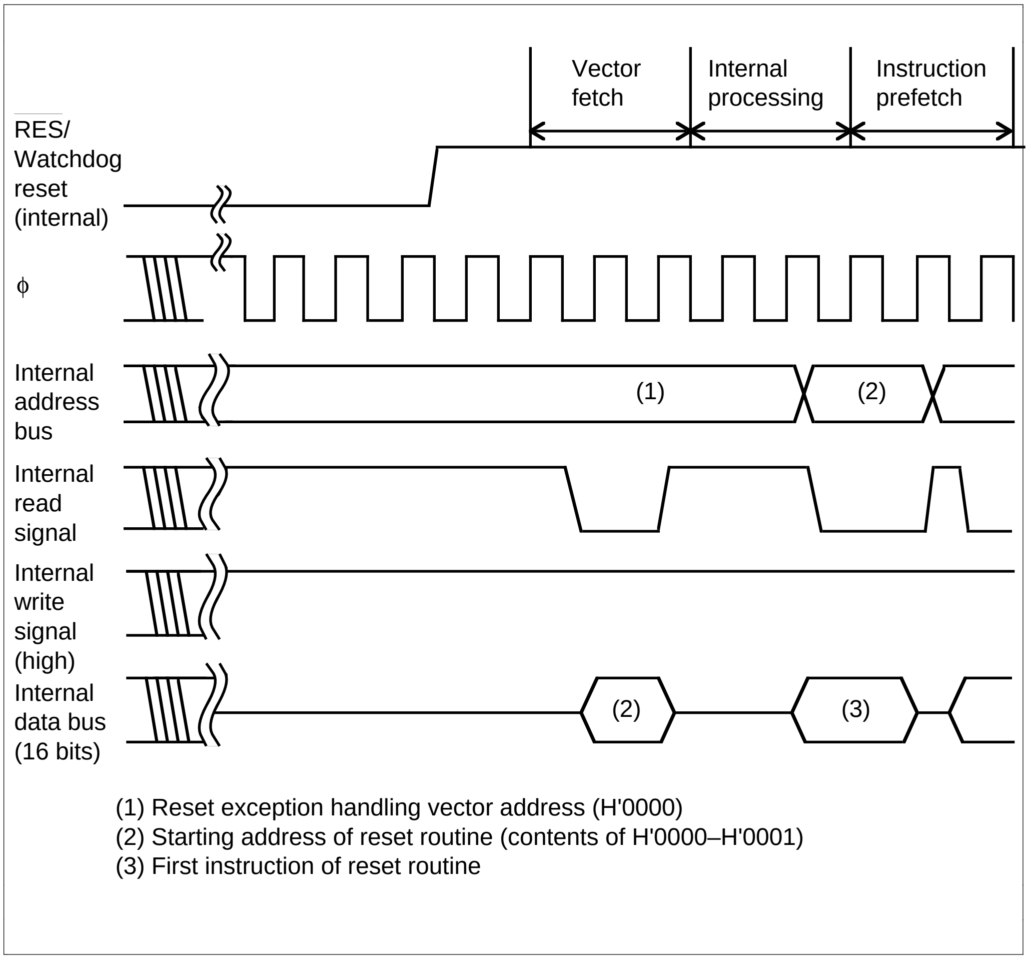
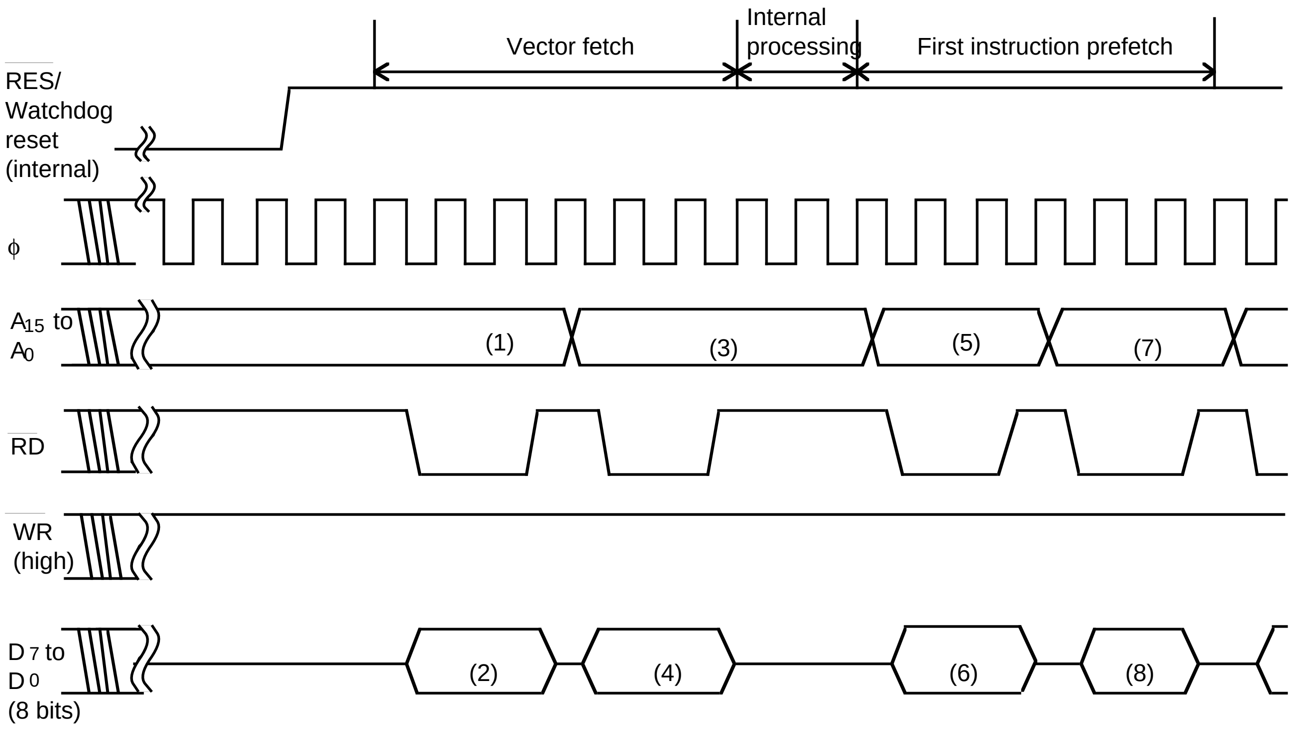

Vector fetch
Internal processing
Instruction prefetch
RES/ Watchdog reset (internal)
φ
Internal address bus
(1)
(2)
Internal read signal
Internal write signal (high)
Internal data bus (16 bits)
(2)
(3)
(1) Reset exception handling vector address (H'0000)
(2) Starting address of reset routine (contents of H'0000–H'0001)
(3) First instruction of reset routine

Figure 4-1 Reset Sequence (Mode 2 or 3, Reset Routine in On-Chip ROM)



(1), (3) Reset vector address: (1) = H'0000, (3) = H'0001

(2), (4) Starting address of reset routine (contents of reset vector): (2) = upper byte, (4) = lower byte

(5), (7) Starting address of reset routine: (5) = (2)(4), (7) = (2)(4) + 1

(6), (8) First instruction of reset routine: (6) = first byte, (8) = second byte

Figure 4-2 Reset Sequence (Mode 1)

4.2.3 Disabling Interrupts after Reset

After a reset, if an interrupt were to be accepted before initialization of the stack pointer (SP: R7), the program counter and condition code register might not be saved correctly, leading to a program crash. To prevent this, all interrupts, including NMI, are disabled immediately after a reset. The first program instruction is therefore always executed. This instruction should initialize the stack pointer (example: MOV.W #xx:16, SP).

4.3 Interrupts

4.3.1 Overview

The interrupt sources include 15 input pins for external interrupts (NMI, IRQ_0 to IRQ_7, $KEYIN_0$ to $KEYIN_7$) and 21 internal sources in the on-chip supporting modules. Table 4-2 lists the interrupt sources in priority order and gives their vector addresses. When two or more interrupts are requested, the interrupt with highest priority is served first.

The features of these interrupts are:

- NMI has the highest priority and is always accepted. All internal and external interrupts except NMI can be masked by the I bit in the CCR. When the I bit is set to 1, interrupts other than NMI are not accepted.

- IRQ_0 to IRQ_7 can be sensed on the falling edge of the input signal, or level-sensed. The type of sensing can be selected for each interrupt individually. NMI is edge-sensed, and either the rising or falling edge can be selected.

- All interrupts are individually vectored. The software interrupt-handling routine does not have to determine what type of interrupt has occurred.

- IRQ_6 (vector 10) is shared by 8 external sources ($KEYIN_0$ to $KEYIN_7$). Each one can be masked by user software.

- The watchdog timer either generates an NMI or OVF interrupt, depending on the application. See section 11, Watchdog Timer, for details.

Table 4-2 Interrupts

Source	Interrupt	Vector No.	Address of Entry in Vector Table	Priority
External Interrupts	NMI	3	H'0006–H'0007	High
	IRQ$_0$	4	H'0008–H'0009	↑
	IRQ$_1$	5	H'000A–H'000B	
	IRQ$_2$	6	H'000C–H'000D	
	IRQ$_3$	7	H'000E–H'000F	
	IRQ$_4$	8	H'0010–H'0011	
	IRQ$_5$	9	H'0012–H'0013	
	IRQ$_6$ (Multiplexed with keyboard matrix interrupt)	10	H'0014–H'0015	
	IRQ$_7$	11	H'0016–H'0017	
Free-Running Timer	ICIA (Input capture A)	12	H'0018–H'0019	
	ICIB (Input capture B)	13	H'001A–H'001B	
	ICIC (Input capture C)	14	H'001C–H'001D	
	ICID (Input capture D)	15	H'001E–H'001F	
	OCIA (Output compare A)	16	H'0020–H'0021	
	OCIB (Output compare B)	17	H'0022–H'0023	
	FOVI (Overflow)	18	H'0024–H'0025	
8-Bit Timer 0	CMI0A (Compare-match A)	19	H'0026–H'0027	
	CMI0B (Compare-match B)	20	H'0028–H'0029	
	OVI0 (Overflow)	21	H'002A–H'002B	
8-Bit Timer 1	CMI1A (Compare-match A)	22	H'002C–H'002D	
	CMI1B (Compare-match B)	23	H'002E–H'002F	
	OVI1 (Overflow)	24	H'0030–H'0031	
Host Interface	IBF1 (IDR1 full)	25	H'0032–H'0033	
	IBF2 (IDR2 full)	26	H'0034–H'0035	
Serial Communication Interface	ERI (Receive error)	27	H'0036–H'0037	
	RXI (Receive end)	28	H'0038–H'0039	
	TXI (TDR empty)	29	H'003A–H'003B	
	TEI (TSR empty)	30	H'003C–H'003D	
A/D Converter	ADI (Conversion end)	31	H'003E–H'003F	↓
Watchdog timer	OVF (Watchdog overflow)	32	H'0040–H'0041	Low

Notes: 1. H'0000 and H'0001 contain the reset vector.

2. H'0002 and H'0005 are reserved by the H8/3332 and are not available to the user.

4.3.2 Interrupt-Related Registers

The interrupt-related registers are the system control register (SYSCR), IRQ sense control register (ISCR), IRQ enable register (IER), and keyboard matrix interrupt mask register (KMIMR).

Table 4-3 Registers Read by Interrupt Controller

Name	Abbreviation	Read/write	Address
System control register	SYSCR	R/W	H'FFC4
IRQ sense control register	ISCR	R/W	H'FFC6
IRQ enable register	IER	R/W	H'FFC7
Keyboard matrix interrupt mask register	KMIMR	R/W	H'FFF1

System Control Register (SYSCR)—H'FFC4: The first four bits of the system control register concern the software standby mode, and the last two bits enable the on-chip RAM and host interface. Bit 2 is the only bit read by the interrupt controller. (See section 2.4.2 for a description of the other bits.)

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	XRST	NMIEG	HIE	RAME
Initial value	0	0	0	0	1	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

- Bit 2: Nonmaskable Interrupt Edge (NMIEG): Controls the valid edge on the $\overline{\text{NMI}}$ line. Determines whether a nonmaskable interrupt is generated on the falling or rising edge of the $\overline{\text{NMI}}$ input signal.

NMIEG	Description	
0	An interrupt request is generated on the falling edge of $\overline{\text{NMI}}$	(Initial state)
1	An interrupt request is generated on the rising edge of $\overline{\text{NMI}}$	

See section 2.2, System Control Register, for information on the other SYSCR bits.

IRQ Sense Control Register (ISCR)—H'FFC6:

Bit	7	6	5	4	3	2	1	0
	IRQ$_7$SC	IRQ$_6$SC	IRQ$_5$SC	IRQ$_4$SC	IRQ$_3$SC	IRQ$_2$SC	IRQ$_1$SC	IRQ$_0$SC
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 0 to 7: $\overline{\mathrm{IRQ}}_0$ to $\overline{\mathrm{IRQ}}_7$ Sense Control ($\mathrm{IRQ}_0\mathrm{SC}$ to $\mathrm{IRQ}_7\mathrm{SC}$): Determine whether the $\overline{\mathrm{IRQ}}_0$ to $\overline{\mathrm{IRQ}}_7$ inputs are level-sensed or sensed on the falling edge.

ISCR Bit

Bits 0–7, **$\mathrm{IRQ}_0\mathrm{SC}$–$\mathrm{IRQ}_7\mathrm{SC}$**	**Description**
0	An interrupt request is generated when $\overline{\mathrm{IRQ}}_0$ to $\overline{\mathrm{IRQ}}_7$ inputs are low (Initial state)
1	An interrupt request is generated by the falling edge of the $\overline{\mathrm{IRQ}}_0$ to $\overline{\mathrm{IRQ}}_7$ inputs

IRQ Enable Register (IER)—H'FFC7:

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	$\mathrm{IRQ}_7\mathrm{E}$	$\mathrm{IRQ}_6\mathrm{E}$	$\mathrm{IRQ}_5\mathrm{E}$	$\mathrm{IRQ}_4\mathrm{E}$	$\mathrm{IRQ}_3\mathrm{E}$	$\mathrm{IRQ}_2\mathrm{E}$	$\mathrm{IRQ}_1\mathrm{E}$	$\mathrm{IRQ}_0\mathrm{E}$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 0 to 7: $\overline{\mathrm{IRQ}}_0$ to $\overline{\mathrm{IRQ}}_7$ Enable ($\mathrm{IRQ}_0\mathrm{E}$ to $\mathrm{IRQ}_7\mathrm{E}$): Enable or disable the $\overline{\mathrm{IRQ}}_i$ signals individually.

Bits 7–0, **$\mathrm{RQ}_0\mathrm{E}$–$\mathrm{IRQ}_7\mathrm{E}$**	**Description**
0	$\overline{\mathrm{IRQ}}_0$ to $\overline{\mathrm{IRQ}}_7$ interrupt requests are disabled (Initial state)
1	$\overline{\mathrm{IRQ}}_0$ to $\overline{\mathrm{IRQ}}_7$ interrupt requests are enabled

Edge-sensed interrupt signals (those for which bits $\mathrm{IRQ}_0\mathrm{SC}$ to $\mathrm{IRQ}_7\mathrm{SC}$ are set to 1) are latched if the corresponding bit $\mathrm{IRQ}_0\mathrm{E}$ to $\mathrm{IRQ}_7\mathrm{E}$ is set to 1 (enabling the interrupt) and held until the interrupt is served. They are latched regardless of the value of the interrupt mask bit (I) in the CCR, and are held even if bits $\mathrm{IRQ}_0\mathrm{E}$ to $\mathrm{IRQ}_7\mathrm{E}$ are cleared to 0. When the interrupt mask bit (I) is cleared to 0, the latched interrupt source will cause an interrupt service.

When anomalies occur in execution of this type of interrupt handling, the interrupt source can be cleared by the following procedure:

1. Set the I bit of the CCR to 1 to disable the interrupt.
2. Clear the bits corresponding to $\mathrm{IRQ}_0\mathrm{E}$ - $\mathrm{IRQ}_7\mathrm{E}$ to 0. This disables a new interrupt source.
3. Clear the bits corresponding to $\mathrm{IRQ}_0\mathrm{SC}$ - $\mathrm{IRQ}_7\mathrm{SC}$ to 0, and then reset to 1. Interrupt sources are cleared when the CCR’s I bit = 1, IRQnSC = 0 and IRQnE = 0.

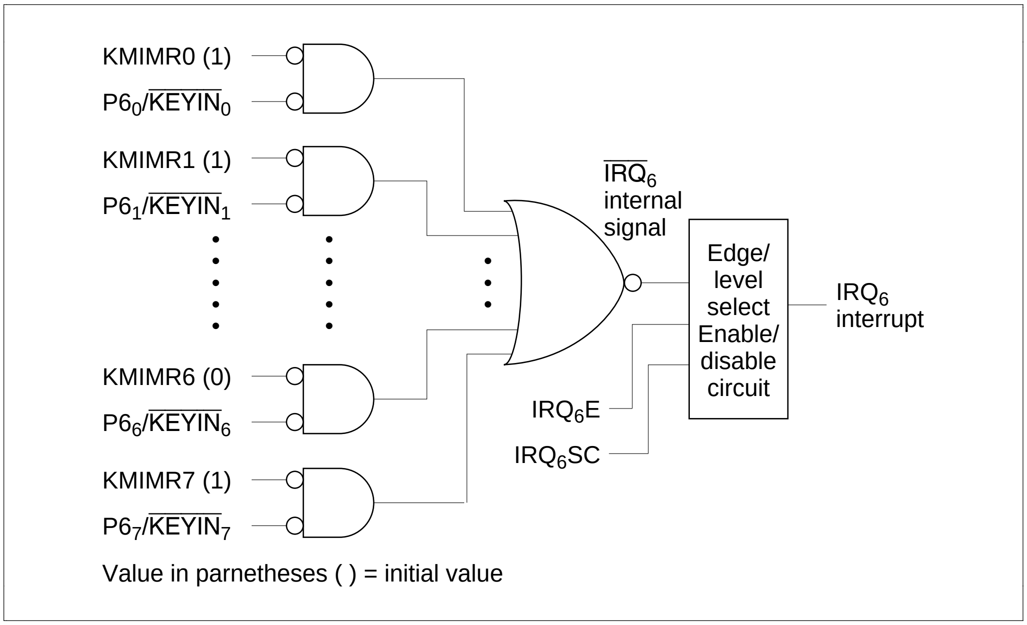
Keyboard Matrix Interrupt Mask Register (KMIMR)—H'FFF1: The KMIMR is an 8-bit register that is dedicated to the keyboard matrix scan/sense application. This register is initialized in normal operating mode where only input from $\overline{\text{IRQ}_6}$ is enabled. If keyboard interrupt is enabled for the keyboard scan/sense application, the user has to set up corresponding mask bits based on the keyboard structure in order to detect keystrokes properly.

Figure 4-3 shows how the $\overline{\text{IRQ}_6}$ interrupt is related to the KMIMR register

Bit	7	6	5	4	3	2	1	0
	KMIMR7	KMIMR6	KMIMR5	KMIMR4	KMIMR3	KMIMR2	KMIMR1	KMIMR0
Initial value	1	0	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

KMIMR0–KMIMR7	Description
0	Keyboard input interrupt is not masked
1	Keyboard input interrupt is masked

Note: Initial value of KMIMR6 is “0”.



KMIMR0 (1)
P6$_0$/$\overline{\text{KEYIN}_0}$
KMIMR1 (1)
P6$_1$/$\overline{\text{KEYIN}_1}$
KMIMR6 (0)
P6$_6$/$\overline{\text{KEYIN}_6}$
KMIMR7 (1)
P6$_7$/$\overline{\text{KEYIN}_7}$
$\overline{\text{IRQ}_6}$ internal signal
Edge/ level select Enable/ disable circuit
IRQ$_6$ interrupt
IRQ$_6$E
IRQ$_6$SC
Value in parnetheses ( ) = initial value

Figure 4-3 KMIMR Register and IRQ$_6$ Interrupt

4.3.3 External Interrupts

The external interrupts are NMI and IRQ$_0$ to IRQ$_7$. NMI, IRQ$_0$, IRQ$_1$, IRQ$_2$, and IRQ$_6$ (including KEYIN$_0$–KEYIN$_7$) can be used to recover from software standby mode.

NMI: A nonmaskable interrupt is generated on the rising or falling edge of the $\overline{\text{NMI}}$ input signal regardless of whether the I (interrupt mask) bit is set in the CCR. The valid edge is selected by the NMIEG bit in the system control register. The NMI vector number is 3. In the NMI hardware exception-handling sequence the I bit in the CCR is set to 1. NMI has the highest priority.

IRQ_0 to IRQ_7: These interrupt signals are level-sensed or sensed on the falling edge of the input, as selected by ISCR bits IRQ_0SC to IRQ_7SC. These interrupts can be masked collectively by the I bit in the CCR, and can be enabled and disabled individually by setting and clearing bits IRQ_0E to IRQ_7E in the IRQ enable register.

When one of these interrupts is accepted, the I bit is set to 1. IRQ_0 to IRQ_7 have interrupt vector numbers 4 to 11. They are prioritized in order from IRQ_7 (low) to IRQ_0 (high). For details, see table 4-2.

IRQ_6 is also used as the keyboard input interrupt. When any of $\overline{\text{KEYIN}}_0$–$\overline{\text{KEYIN}}_7$ (P6_0–P6_7) pins are used for matrix keyboard sense inputs, the corresponding KMIMR mask bits can be cleared to enable that key input line's interrupt. The remaining unused key inputs' KMIMR bits should be set to disable their interrupts. These eight lines then become a single IRQ_6 interrupt.

When P6_0–P6_7 are not used as key inputs and $\overline{\text{IRQ}}_6$ (P6_6) is desired, clear KMIMR_6 to 0 while and set all other KMIMR bits to 1, and also enable IRQ_6E bit in the IRQ enable register.

Interrupts IRQ_0 to IRQ_7 do not depend on whether pins $\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_7$ are input or output pins. When using external interrupts IRQ_0 to IRQ_7, clear the corresponding DDR bits to 0 to set these pins to the input state, and do not use these pins as input or output pins for the timers, serial communication interface, or A/D converter.

4.3.4 Internal Interrupts

Twenty-one internal interrupts can be requested by the on-chip supporting modules. Each interrupt source has its own vector number, so the interrupt-handling routine does not have to determine which interrupt has occurred. All internal interrupts are masked when the I bit in the CCR is set to 1. When one of these interrupts is accepted, the I bit is set to 1 to mask further interrupts (except NMI). The vector numbers are 12 to 32. For the priority order, see table 4-2.

4.3.5 Interrupt Handling

Interrupts are controlled by an interrupt controller that arbitrates between simultaneous interrupt requests, commands the CPU to start the hardware interrupt exception-handling sequence, and furnishes the necessary vector number. Figure 4-4 shows a block diagram of the interrupt controller.

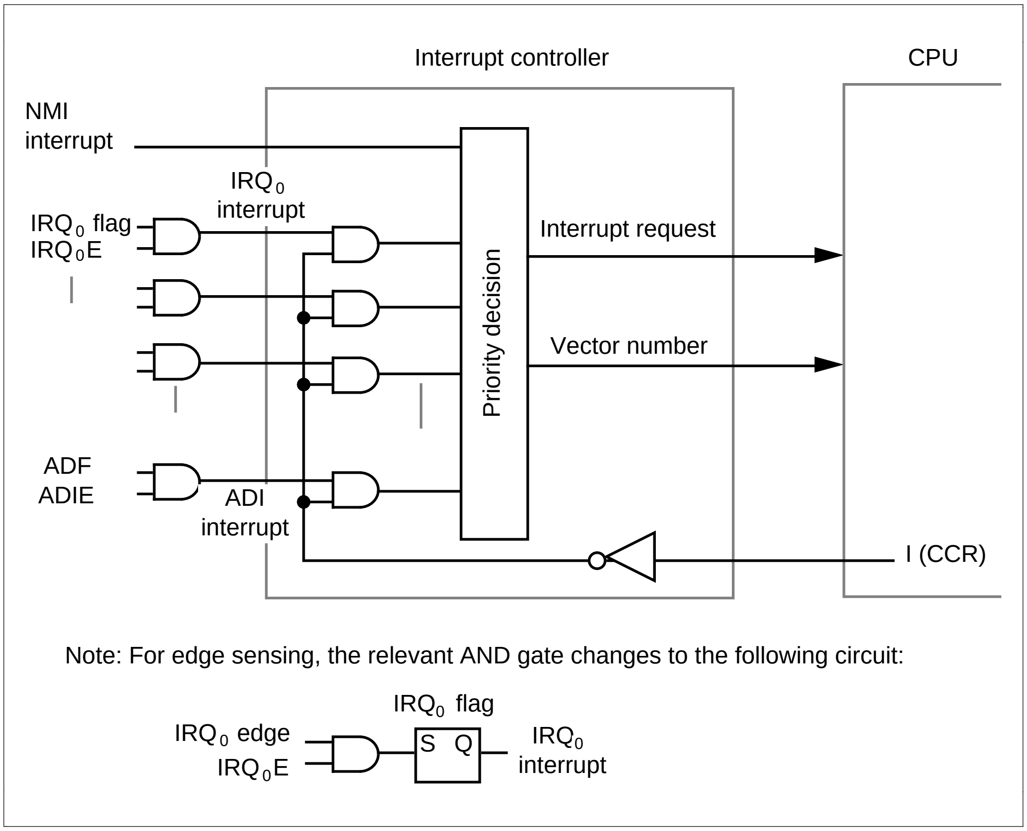


Figure 4-4 Block Diagram of Interrupt Controller

The IRQ interrupts and interrupts from the on-chip supporting modules (except the watchdog timer) all have corresponding enable bits. When the enable bit is cleared to 0, the interrupt signal is not sent to the interrupt controller, so the interrupt is ignored. These interrupts can also all be masked by setting the CPU's interrupt mask bit (I) to 1. Accordingly, these interrupts are accepted only when their enable bit is set to 1 and the I bit is cleared to 0.

The nonmaskable interrupt (NMI) is always accepted, except in the reset state and hardware standby mode.

When an NMI or another enabled interrupt is requested, the interrupt controller transfers the interrupt request to the CPU and indicates the corresponding vector number. (When two or more interrupts are requested, the interrupt controller selects the vector number of the interrupt with the highest priority.) When notified of an interrupt request, at the end of the current instruction or current hardware exception-handling sequence, the CPU starts the hardware exception-handling sequence for the interrupt and latches the vector number.

Figure 4-5 is a flowchart of the interrupt (and reset) operations. Figure 4-7 shows the interrupt timing sequence for the case in which the software interrupt-handling routine is in on-chip ROM and the stack is in on-chip RAM.

1. An interrupt request is sent to the interrupt controller when an NMI interrupt occurs, and when an interrupt occurs on an IRQ input line or in an on-chip supporting module provided the enable bit of that interrupt is set to 1.

2. The interrupt controller checks the I bit in the CCR and accepts the interrupt request if the I bit is cleared to 0. If the I bit is set to 1 only NMI requests are accepted; other interrupt requests remain pending.

3. Among all accepted interrupt requests, the interrupt controller selects the request with the highest priority and passes it to the CPU. Other interrupt requests remain pending.

4. When it receives the interrupt request, the CPU waits until completion of the current instruction or hardware exception-handling sequence, then starts the hardware exception-handling sequence for the interrupt and latches the interrupt vector number.

5. In the hardware exception-handling sequence, the CPU first pushes the PC and CCR onto the stack. See figure 4-6. The stacked PC indicates the address of the first instruction that will be executed on return from the software interrupt-handling routine.

6. Next the I bit in the CCR is set to 1, masking all further interrupts except NMI.

7. The vector address corresponding to the vector number is generated, the vector table entry at this vector address is loaded into the program counter, and execution branches to the software interrupt-handling routine at the address indicated by that entry.

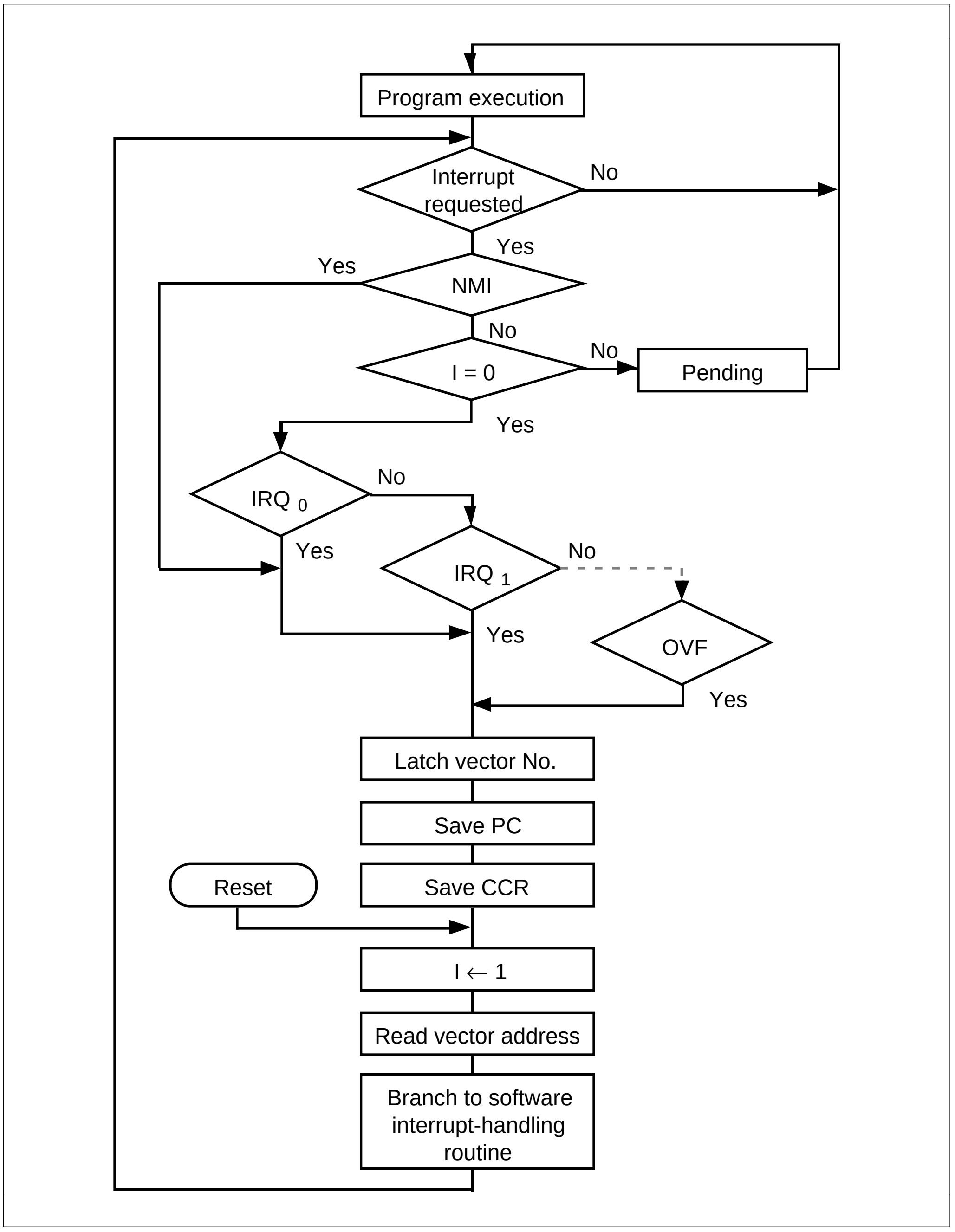
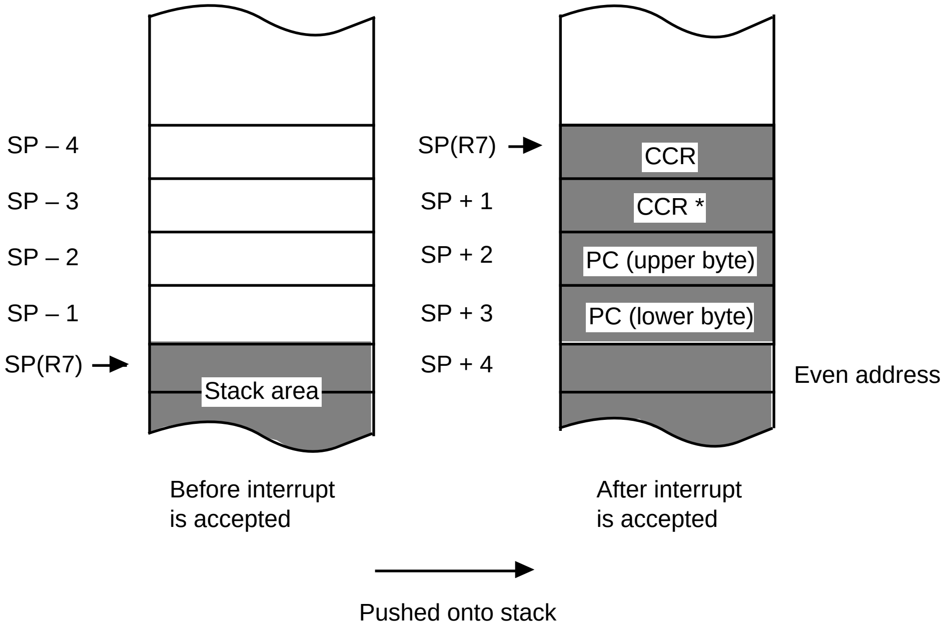


Figure 4-5 Hardware Interrupt-Handling Sequence

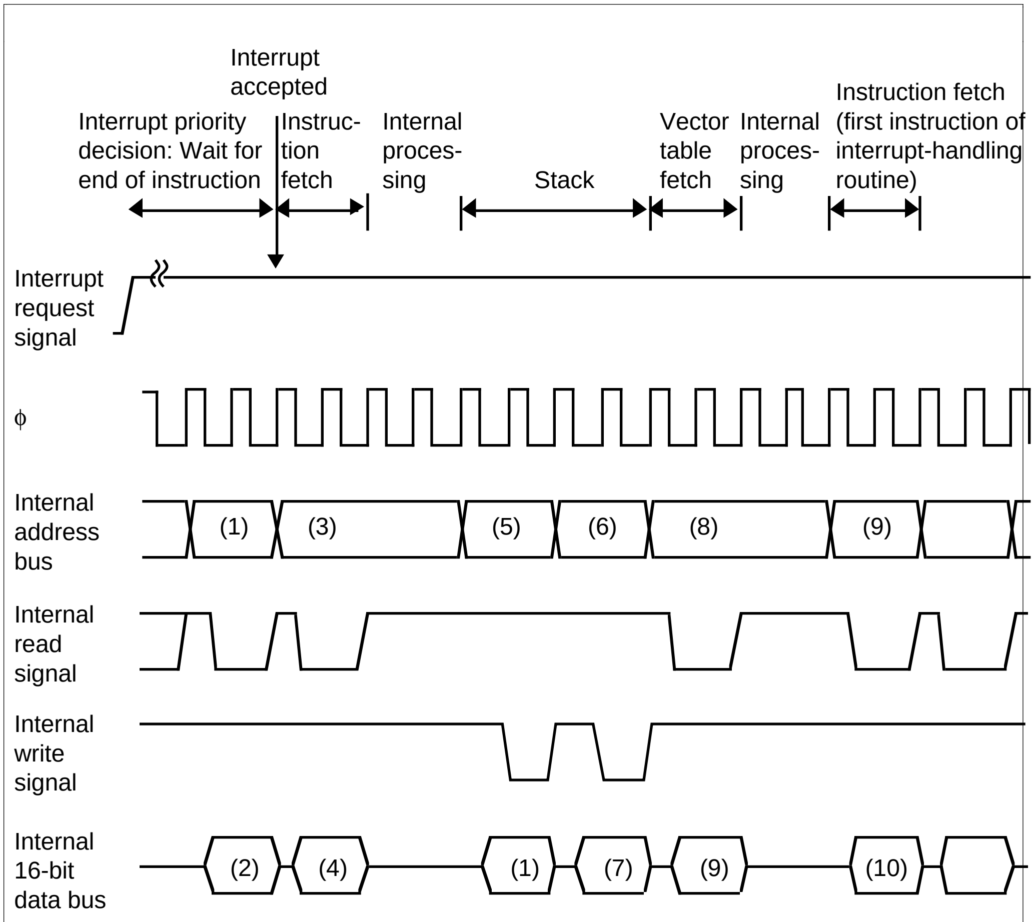


PC:	Program counter	*: Ignored on return
CCR:	Condition code register	
SP:	Stack pointer	

Notes: 1. The PC contains the address of the first instruction executed after return.

2. Registers must be saved and restored by word access at an even address.

Figure 4-6 Use of Stack in Interrupt Handling



(1) Instruction prefetch address (Pushed on stack. Instruction is executed on return from interrupt-handling routine.)
(2), (4) Instruction code (Not executed)
(3) Instruction prefetch address (Not executed)
(5) SP–2
(6) SP–4
(7) CCR
(8) Address of vector table entry
(9) Vector table entry (address of first instruction interrupt-handling routine)
(10) First instruction of interrupt-handling routine

Figure 4-7 Timing of Interrupt Sequence

4.3.6 Interrupt Response Time

Table 4-4 indicates the number of states that elapse from an interrupt request signal until the first instruction of the software interrupt-handling routine is executed. Since on-chip memory is accessed 16 bits at a time, very fast interrupt service can be obtained by placing interrupt-handling routines in on-chip ROM and the stack in on-chip RAM.

Table 4-4 Number of States before Interrupt Service

		Number of states	
No.	**Reason for wait**	**On-chip memory**	**External memory**
1	Interrupt priority decision	2[Note 3]	2[Note 3]
2	Wait for completion of current instruction[Note 1]	1 to 13	5 to 17[Note 2]
3	Save PC and CCR	4	12[Note 2]
4	Fetch vector	2	6[Note 2]
5	Fetch instruction	4	12[Note 2]
6	Internal processing	4	4
	Total	17 to 29	41 to 53[Note 2]

Notes: 1. These values do not apply if the current instruction is EEPMOV.

2. If wait states are inserted in external memory access, add the number of wait states.

3. 1 for internal interrupts.

4.3.7 Precaution

Note that the following type of contention can occur in interrupt handling:

Contention between Interrupt Request and Disable: When software clears the enable bit of an interrupt to 0 to disable the interrupt, the interrupt becomes disabled after execution of the clearing instruction. If an enable bit is cleared by a BCLR or MOV instruction, for example, and the interrupt is requested during execution of that instruction, at the instant when the instruction ends the interrupt is still enabled, so after execution of the instruction, the hardware exception-handling sequence is executed for the interrupt. If a higher-priority interrupt is requested at the same time, however, the hardware exception-handling sequence is executed for the higher-priority interrupt and the interrupt that was disabled is ignored.

Similar considerations apply when an interrupt request flag is cleared to 0.

Figure 4-8 shows an example in which the OCIAE bit is cleared to 0.

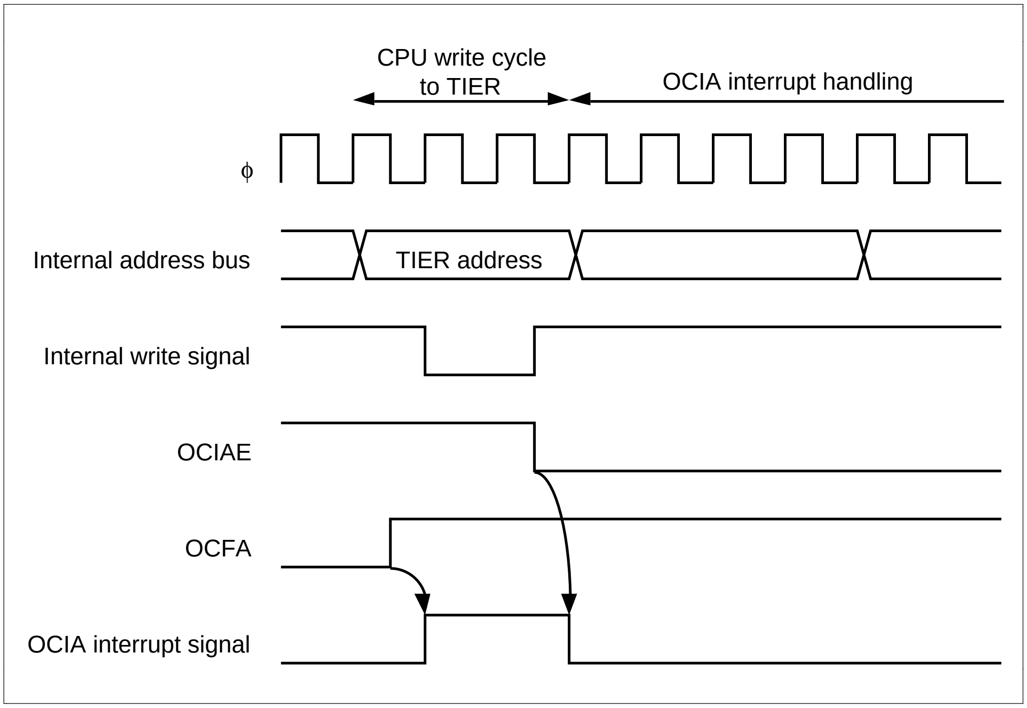


Figure 4-8 Contention between Interrupt and Disabling Instruction

The above contention does not occur if the enable bit or flag is cleared to 0 while the interrupt mask bit (I) is set to 1.

4.4 Note on Stack Handling

In word access, the least significant bit of the address is always assumed to be 0. The stack is always accessed by word access. Care should be taken to keep an even value in the stack pointer (general register R7). Use the PUSH and POP (or MOV.W Rn, @–SP and MOV.W @SP+, Rn) instructions to push and pop registers on the stack.

Setting the stack pointer to an odd value can cause programs to crash. Figure 4-9 shows an example of damage caused when the stack pointer contains an odd address.

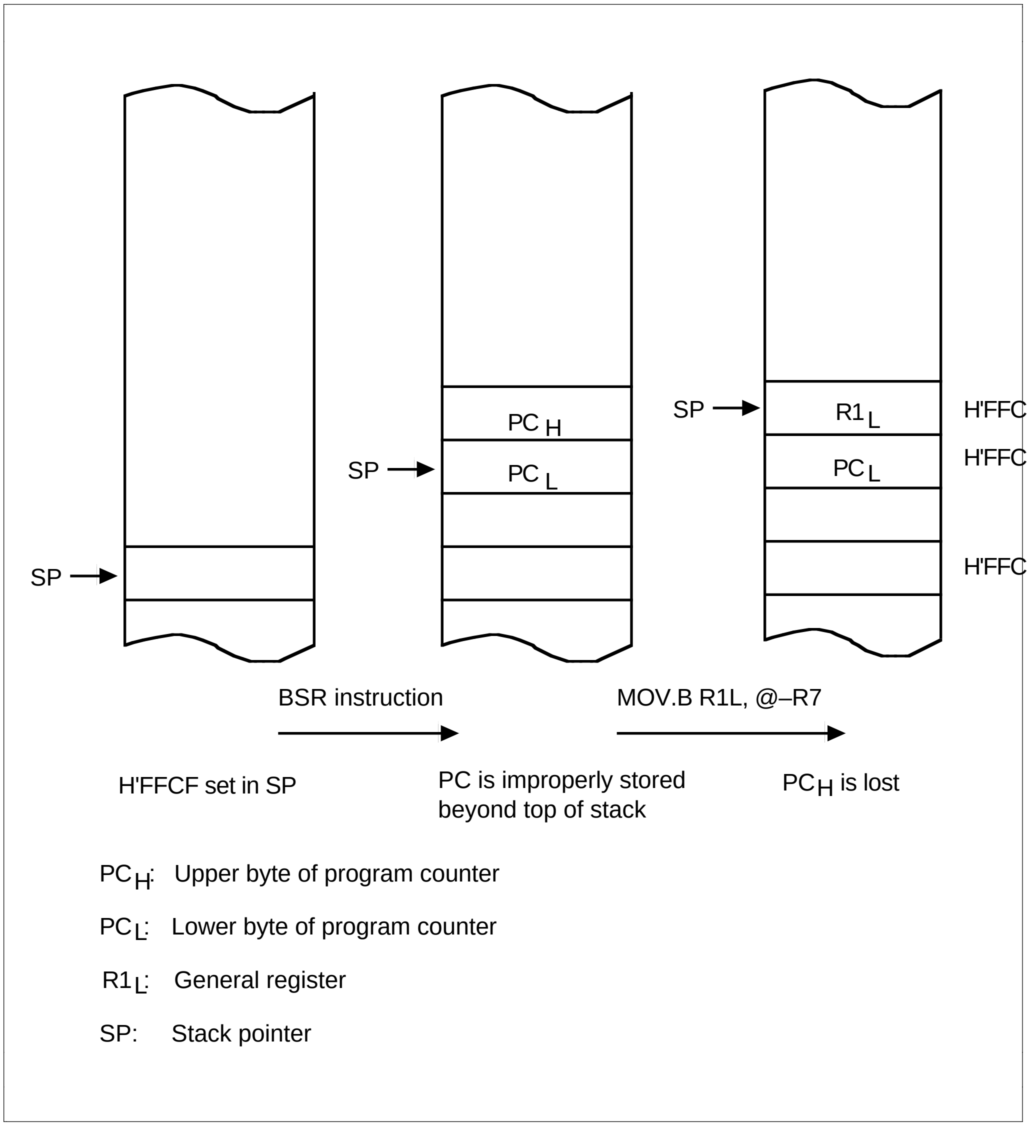


Figure 4-9 Example of Damage Caused by Setting an Odd Address in R7

Section 5 I/O Ports

5.1 Overview

The H8/3332 has nine parallel I/O ports, including:

- Six 8-bit input/output ports: ports 1, 2, 3, 4, 6, and 9
- One 8-bit input port: port 7
- One 7-bit input/output port: port 8
- One 3-bit input/output port: port 5

Ports 1, 2, and 3 have programmable input pull-up transistors. Ports 1 to 6, 8, and 9 can drive a Darlington pair. Ports 1 to 4, 6, and 9 can drive one TTL load and a 90-pF capacitive load. Ports 5 and 8 can drive one TTL load and a 30-pF capacitive load. Ports 1 and 2 can drive LEDs (10-mA current sink).

Input and output are memory-mapped. The CPU views each port as a data register (DR) located in the register field at the high end of the address space. Each port (except port 7) also has a data direction register (DDR) which determines which pins are used for input and which for output.

5.1.1 Output

To send data to an output port, the CPU selects output in the data direction register and writes the desired data in the data register, causing the data to be held in a latch. The latch output drives the pin through a buffer amplifier. If the CPU reads the data register of an output port, it obtains the data held in the latch rather than the actual level of the pin.

5.1.2 Input

To read data from an I/O port, the CPU selects input in the data direction register and reads the data register. This causes the input logic level at the pin to be placed directly on the internal data bus. There is no intervening input latch.

The data direction registers are write-only registers; their contents are invisible to the CPU. If the CPU reads a data direction register, all bits are read as 1, regardless of their true values. Care is required if bit manipulation instructions are used to set and clear the data direction bits. See the note on bit manipulation instructions in section 3.5.5, Bit Manipulation.

5.1.3 Auxiliary Functions

In addition to their general-purpose input/output functions, all of the I/O ports have auxiliary functions. Most of the auxiliary functions are software-selectable and must be enabled by setting bits in control registers. When selected, an auxiliary function usually replaces the general-purpose input/output function, but in some cases both functions can operate simultaneously. Table 5-1 summarizes the auxiliary functions of the ports.

Table 5-1 Port Functions

			Expanded Modes		Single-Chip Mode 3	
Port	**Description**	**Pins**	**Mode 1**	**Mode 2**	**Master Mode**	**Slave Mode**
Port 1	• 8-bit input-output port • Can drive LEDs • Input pull-ups	$P1_7$ to $P1_0$/ A_7 to A_0	Address output (low)	General input when DDR = 0 (initial state) Address output (low) when DDR = 1	General input/output	I/O port or output port for key scan
Port 2	• 8-bit input-output port • Can drive LEDs • Input pull-ups	$P2_7$ to $P2_0$/ A_{15} to A_8	Address output (high)	General input when DDR = 0 (initial state) Address output (high) when DDR = 1	General input/output	I/O port or output port for key scan
Port 3	• 8-bit input-output port • Input pull-ups	$P3_7$ to $P3_0$/ D_7 to D_0	Data bus	Data bus	General input/output	Host interface data bus (HDB_7 to HDB_0)
Port 4	• 8-bit input-	$P4_7$ to $P4_6$	General input/output, 8-bit timer 0/1			I/O or PWM0/1 output
	output port	$P4_5$	input/output ($TMCI_0$, TMO_0, $TMRI_0$, $TMCI_1$,			$HIRQ_{12}$
		$P4_4$	TMO_1, $TMRI_1$), or PWM timer 0/1 output			$HIRQ_1$
		$P4_3$	(PW_0, PW_1)			$HIRQ_{11}$
		$P4_2$ to $P4_{0-}$				I/O or timer 0 output
Port 5	• 3-bit input-output port	$P5_2$ to $P5_0$	General input/output or serial communication interface input/output (TxD, RxD, SCK)			
Port 6	• 8-bit input-output port	$P6_7$ to $P6_0$	General input/output, 16-bit free-running timer input/output (FTCI, FTOA, FTOB, FTIA, FTIB, FTIC, FTID), or external interrupt input ($\overline{\text{IRQ}}_6^{\text{Note}}$, $\overline{\text{IRQ}}_7$)			Key sense inputs for key scan
Port 7	• 8-bit input port	$P7_7$ to $P7_0$	General input, analog input to A/D converter (AN_7 to AN_0)			

Note: Each port 6 pin can be used as an $\overline{\text{IRQ}}_6$ interrupt input source according to the contents of the KMIMR register (section 4.3.2).

Table 5-1 Port Functions (cont)

			Expanded Modes		Single-Chip Mode 3	
Port	**Description**	**Pins**	**Mode 1**	**Mode 2**	**Master Mode**	**Slave Mode**
Port 8	• 7-bit input-output port	$P8_6/\overline{\text{IRQ}}_5$	General input/output, or external interrupt input ($\overline{\text{IRQ}}_3$, $\overline{\text{IRQ}}_4$, $\overline{\text{IRQ}}_5$)			General I/O or external interrupt ($\overline{\text{IRQ}}_5$)
		$P8_5/\overline{\text{IRQ}}_4$				$\overline{\text{CS}}_2$ input
		$P8_4/\overline{\text{IRQ}}_3$				$\overline{\text{IOW}}$ input
		$P8_3$	General input/output			$\overline{\text{IOR}}$ input
		$P8_2$				$\overline{\text{CS}}_1$ input
		$P8_1$				GA_{20} output
		$P8_0$				HA_0 input
Port 9	• 8-bit input-output port	$P9_7/\overline{\text{WAIT}}$	$\overline{\text{WAIT}}$ input		General input/output	
		$P9_6/\phi$	System clock output		General input when DDR = 0 (initial state) System clock output when DDR = 1	
		$P9_5/\overline{\text{AS}}$	$\overline{\text{AS}}$ output		General input/output	
		$P9_4/\overline{\text{WR}}$	$\overline{\text{WR}}$ output			
		$P9_3/\overline{\text{RD}}$	$\overline{\text{RD}}$ output			
		$P9_2/\overline{\text{IRQ}}_0$ $P9_1/\overline{\text{IRQ}}_1$	General input/output or external interrupt input ($\overline{\text{IRQ}}_0$, $\overline{\text{IRQ}}_1$)			
		$P9_0/\overline{\text{ADTRG}}/\overline{\text{IRQ}}_2$	General input/output, A/D converter trigger input ($\overline{\text{ADTRG}}$), or external interrupt input ($\overline{\text{IRQ}}_2$)			

5.2 Port 1

Port 1 is an 8-bit input/output port that also provides the low bits of the address bus. The function of port 1 depends on the MCU mode as indicated in table 5-2.

Table 5-2 Port 1 Functions

Mode	Function
1	Address bus (low) (A_7 to A_0)
2	Input port or address bus (low) (A_7 to A_0) depending on data direction register setting: 0 = Input pin 1 = Address pin
3	Input/output port

Pins of port 1 can drive a single TTL load and a 90-pF capacitive load when they are used as output pins. They can also drive light-emitting diodes and a Darlington pair. When they are used as input pins, they have programmable input pull-up transistors.

Table 5-3 details the port 1 registers.

Table 5-3 Port 1 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 1 data direction register	P1DDR	W	H'FF (mode 1) H'00 (modes 2 and 3)	H'FFB0
Port 1 data register	P1DR	R/W	H'00	H'FFB2
Port 1 pull-up control register	P1PCR	R/W	H'00	H'FFAC

5.2.1 Port 1 Data Direction Register (P1DDR)—H'FFB0

Bit	7	6	5	4	3	2	1	0
	P1$_7$DDR	P1$_6$DDR	P1$_5$DDR	P1$_4$DDR	P1$_3$DDR	P1$_2$DDR	P1$_1$DDR	P1$_0$DDR
Mode 1								
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—
Modes 2 and 3								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P1DDR is an 8-bit register that selects the direction of each pin in port 1. A pin functions as an output pin if the corresponding bit in P1DDR is set to 1, and as an input pin if the bit is cleared to 0.

5.2.2 Port 1 Data Register (P1DR)—H'FFB2

Bit	7	6	5	4	3	2	1	0
	$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P1DR is an 8-bit register containing the data for pins $P1_7$ to $P1_0$. When the CPU reads P1DR for output pins, it reads the value in the P1DR latch. However, for input pins, it obtains the logic level directly from the pin, bypassing the P1DR latch.

5.2.3 Port 1 Pull-Up Control Register (P1PCR)—H'FFAC

Bit	7	6	5	4	3	2	1	0
	$P1_7$PCR	$P1_6$PCR	$P1_5$PCR	$P1_4$PCR	$P1_3$PCR	$P1_2$PCR	$P1_1$PCR	$P1_0$PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: 1 = Pull-up on
0 = Pull-up off

The P1PCR is an 8-bit read/write register that controls the input pull-ups in port 1. If a bit in P1DDR is cleared to 0 (designating input), and the corresponding bit in P1PCR is set to 1, the input pull-up for that bit is turned on.

5.2.4 Modes

Mode 1: In mode 1 (expanded mode without on-chip ROM), port 1 is automatically used for address output. The port 1 data direction register cannot be written to. All bits in P1DDR are automatically set to 1 and cannot be cleared to 0.

Mode 2: In mode 2 (expanded mode with on-chip ROM), the use of port 1 can be selected on a pin-by-pin basis. A pin is used for general-purpose input if its data direction bit is cleared to 0, or for address output if its data direction bit is set to 1.

Mode 3: In the single-chip mode port 1 is a general-purpose input/output port.

Reset: A reset clears P1DDR, P1DR, and P1PCR to all 0, placing all pins in the input state with the input pull-ups off. In mode 1, when the chip comes out of reset, P1DDR is set to all 1.

Hardware Standby Mode: All pins are placed in the high-impedance state with the input pull-ups off. In modes 2 and 3, P1DDR is initialized to H'00.

Software Standby Mode: In the software standby mode, P1DDR, P1DR, and P1PCR remain in their previous state. Address output pins are low. General-purpose output pins continue to output the data in P1DR.

Input Pull-Up Transistors: Port 1 has built-in programmable input pull-up transistors that are available in modes 2 and 3. The input pull-up for each bit can be turned on and off individually. To turn on an input pull-up in mode 2 or 3, set the corresponding P1PCR bit to 1 and clear the corresponding P1DDR bit to 0. P1PCR is cleared to H'00 by a reset and in the hardware standby mode. Clearing P1PCR to H'00 turns all input pull-ups off. In software standby mode, the previous state is maintained.

Table 5-4 indicates the states of the input pull-ups in each operating mode.

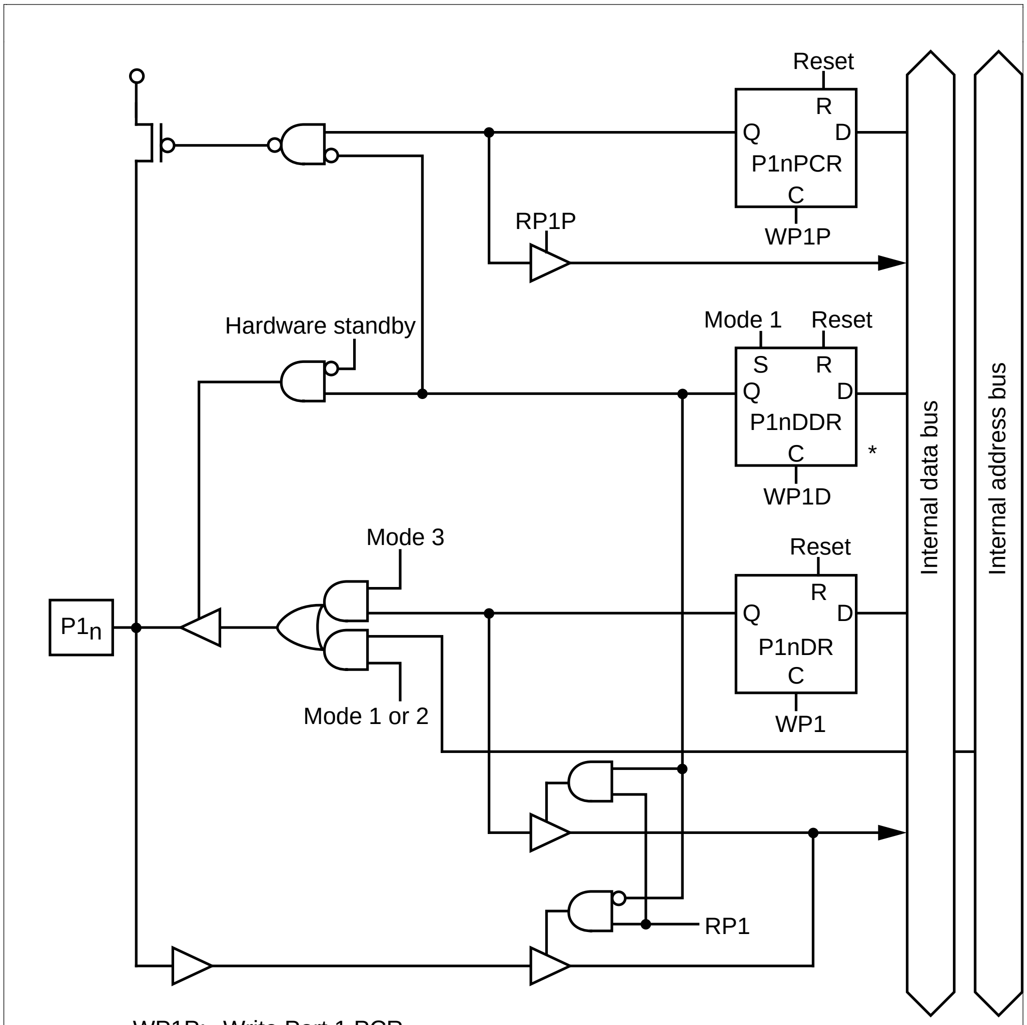
Table 5-4 Input Pull-Up States (Port 1)

Mode	Reset	Hardware Standby	Software Standby	Other Operating Modes
1	Off	Off	Off	Off
2	Off	Off	On/off	On/off
3	Off	Off	On/off	On/off

Notes: Off: The input pull-up is always off.

On/off: The input pull-up is on if P1PCR = 1 and P1DDR = 0, but off otherwise.

Figure 5-1 shows a schematic diagram of port 1.



WP1P: Write Port 1 PCR
WP1D: Write Port 1 DDR
WP1: Write Port 2
RP1P: Read Port 2 PCR
RP1: Read Port 2
n = 0 to 7
* Set-priority

Figure 5-1 Port 1 Schematic Diagram

5.3 Port 2

Port 2 is an 8-bit input/output port that also provides the high bits of the address bus. The function of port 2 depends on the MCU mode as indicated in Table 5-5.

Table 5-5 Port 2 Functions

Mode	Function
1	Address bus (high) (A_{15} to A_8)
2	Input port or address bus (high) (A_{15} to A_8) depending on data direction register setting: 0 = Input pin 1 = Address pin
3	Input/output port

Pins of port 2 can drive a single TTL load and a 90-pF capacitive load when they are used as output pins. They can also drive light-emitting diodes and a Darlington pair. When they are used as input pins, they have programmable input pull-ups.

Table 5-6 details the port 2 registers.

Table 5-6 Port 2 Registers

Name	Abbreviation	Read/Write	Initial value	Address
Port 2 data direction register	P2DDR	W	H'FF (mode 1) H'00 (modes 2 and 3)	H'FFB1
Port 2 data register	P2DR	R/W	H'00	H'FFB3
Port 2 pull-up control register	P2PCR	R/W	H'00	H'FFAD

5.3.1 Port 2 Data Direction Register (P2DDR)—H'FFB1

Bit	7	6	5	4	3	2	1	0
	P2$_7$DDR	P2$_6$DDR	P2$_5$DDR	P2$_4$DDR	P2$_3$DDR	P2$_2$DDR	P2$_1$DDR	P2$_0$DDR
Mode 1								
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—
Modes 2 and 3								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P2DDR is an 8-bit register that selects the direction of each pin in port 2. A pin functions as an output pin if the corresponding bit in P2DDR is set to 1, and as an input pin if the bit is cleared to 0.

5.3.2 Port 2 Data Register (P2DR)—H'FFB3

Bit	7	6	5	4	3	2	1	0
	$P2_7$	$P2_6$	$P2_5$	$P2_4$	$P2_3$	$P2_2$	$P2_1$	$P2_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P2DR is an 8-bit register containing the data for pins $P2_7$ to $P2_0$. When the CPU reads P2DR for output pins, it reads the value in the P2DR latch. However, for input pins, it obtains the logic level directly from the pin, bypassing the P2DR latch.

5.3.3 Port 2 Pull-Up Control Register (P2PCR)—H'FFAD

Bit	7	6	5	4	3	2	1	0
	$P2_7$PCR	$P2_6$PCR	$P2_5$PCR	$P2_4$PCR	$P2_3$PCR	$P2_2$PCR	$P2_1$PCR	$P2_0$PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: 1 = Pull-up on
0 = Pull-up off

The P2PCR is an 8-bit read/write register that controls the input pull-ups in port 2. If a bit in P2DDR is cleared to 0 (designating input, and the corresponding bit in P1PCR is set to 1, the input pull-up for that bit is turned on.

5.3.4 Modes

Mode 1: In mode 1 (expanded mode without on-chip ROM), port 2 is automatically used for address output. The port 2 data direction register is can’t be written. All bits in P2DDR are automatically set to 1 and cannot be cleared to 0.

Mode 2: In mode 2 (expanded mode with on-chip ROM), the usage of port 2 can be selected on a pin-by-pin basis. A pin is used for general-purpose input if its data direction bit is cleared to 0, or for address output if its data direction bit is set to 1.

Mode 3: In the single-chip mode port 2 is a general-purpose input/output port.

Reset: A reset clears P2DDR, P2DR, and P2PCR to all 0, placing all pins in the input state with the input pull-ups off. In mode 1, when the chip comes out of reset, P2DDR is set to all 1.

Hardware Standby Mode: All pins are placed in the high-impedance state with the input pull-ups off. In modes 2 and 3, P2DDR is initialized to H’00.

Software Standby Mode: In the software standby mode, P2DDR, P2DR, and P2PCR remain in their previous state. Address output pins are low. General-purpose output pins continue to output the data in P2DR.

Input Pull-Ups: Port 2 has built-in programmable input pull-ups that are available in modes 2 and 3. The input pull-up for each bit can be turned on and off individually. To turn on an input pull-up in mode 2 or 3, set the corresponding P2PCR bit to 1 and clear the corresponding P2DDR bit to 0. P2PCR is cleared to H'00 by a reset and in the hardware standby mode. Clearing P2PCR to H'00 turns all input pull-ups off. In software standby mode, the previous state is maintained.

Table 5-7 indicates the states of the input pull-ups in each operating mode.

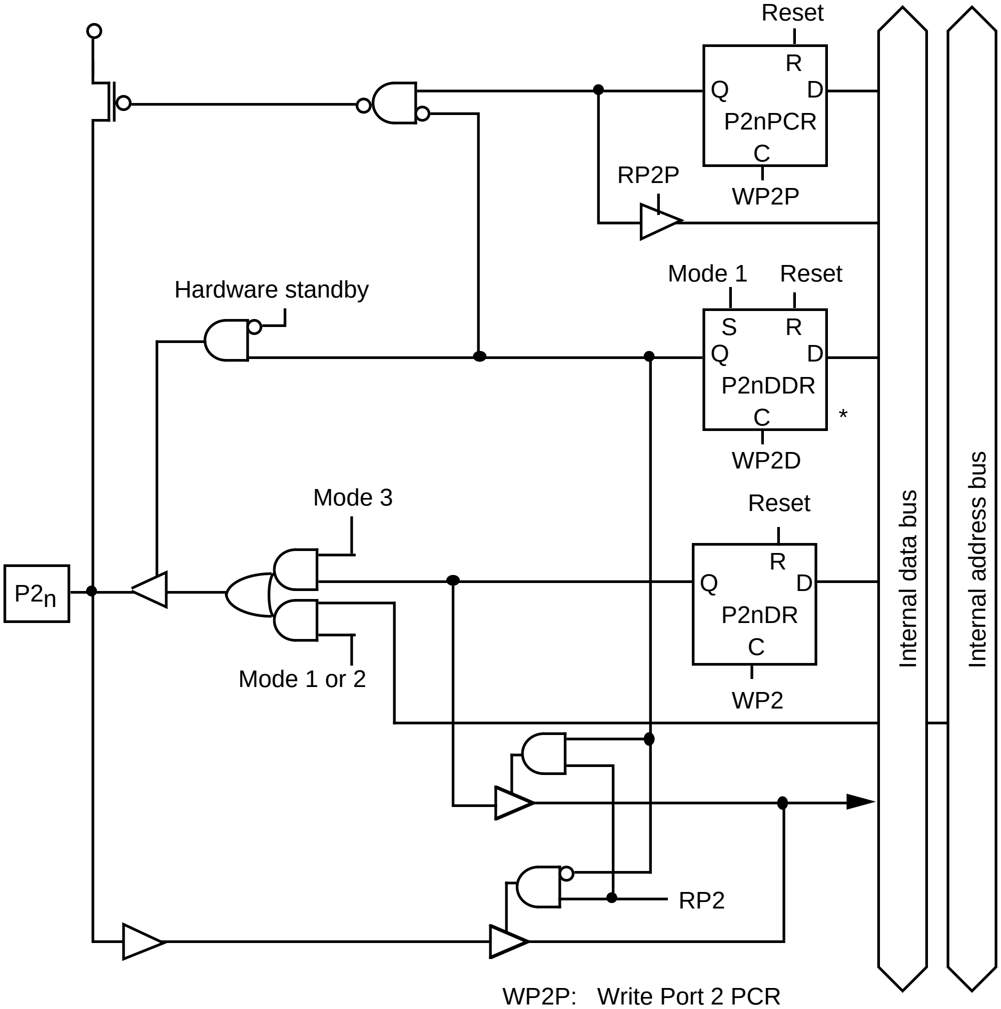
Table 5-7 Input Pull-Up States (Port 2)

Mode	Reset	Hardware Standby	Software Standby	Other Operating Modes
1	Off	Off	Off	Off
2	Off	Off	On/off	On/off
3	Off	Off	On/off	On/off

Notes: Off: The input pull-up is always off.

On/off: The input pull-up is on if P2PCR = 1 and P2DDR = 0, but off otherwise.

Figure 5-2 shows a schematic diagram of port 2.



WP2P: Write Port 2 PCR
WP2D: Write Port 2 DDR
WP2: Write Port 2
RP2: Read Port 2
RP2P: Read Port 2 PCR
n = 0 to 7
* Set-priority

Figure 5-2 Port 2 Schematic Diagram

5.4 Port 3

Port 3 is an 8-bit input/output port that also provides the external data bus and host interface (master-slave) data bus. The function of port 3 depends on the MCU mode as indicated in table 5-8.

Table 5-8 Functions of Port 3

Mode	Function
1	Data bus
2	Data bus
3	Input/output port or host interface data bus

Pins of port 3 can drive a single TTL load and a 90-pF capacitive load when they are used as output pins. They can also drive a Darlington pair. When they are used as input pins, they have programmable input pull-ups.

Table 5-9 details the port 3 registers.

Table 5-9 Port 3 Registers

Name	Abbreviation	Read/Write	Initial value	Address
Port 3 data direction register	P3DDR	W	H'00	H'FFB4
Port 3 data register	P3DR	R/W	H'00	H'FFB6
Port 3 pull-up control register	P3PCR	R/W	H'00	H'FFAE

5.4.1 Port 3 Data Direction Register (P3DDR)—H'FFB4

Bit	7	6	5	4	3	2	1	0
	P3$_7$DDR	P3$_6$DDR	P3$_5$DDR	P3$_4$DDR	P3$_3$DDR	P3$_2$DDR	P3$_1$DDR	P3$_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P3DDR is an 8-bit register that selects the direction of each pin in port 3. A pin functions as an output pin if the corresponding bit in P3DDR is set to 1, and as an input pin if the bit is cleared to 0.

5.4.2 Port 3 Data Register (P3DR)—H'FFB6

Bit	7	6	5	4	3	2	1	0
	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P3DR is an 8-bit register containing the data for pins $P3_7$ to $P3_0$. When the CPU reads P3DR, for output pins it reads the value in the P3DR latch, but for input pins, it obtains the logic level directly from the pin, bypassing the P3DR latch.

5.4.3 Port 3 Pull-Up Control Register (P3PCR)—H'FFAE

Bit	7	6	5	4	3	2	1	0
	$P3_7$PCR	$P3_6$PCR	$P3_5$PCR	$P3_4$PCR	$P3_3$PCR	$P3_2$PCR	$P3_1$PCR	$P3_0$PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: 1 = Pull-up on
0 = Pull-up off

The P3PCR is an 8-bit read/write register that controls the input pull-ups in port 3. If a bit in P3DDR is cleared to 0 (designating input), and the corresponding bit in P1PCR is set to 1, the input pull-up for that bit is turned on.

The input pull-ups should not be used in slave mode (when the host interface is enabled). P3DR should be cleared to H'00 (its initial value) in slave mode.

5.4.4 Modes

Modes 1 and 2: In the expanded modes, port 3 is automatically used as the data bus. The values in P3DDR and P3DR are ignored.

Mode 3: In the single-chip mode, when the host interface enable (HIE) bit in the system control register is cleared to 0, port 3 can be used as a general-purpose input/output port.

When HIE is set to 1, entering the slave mode, port 3 is used as the host interface data bus (HDB7 to HDB0). P3DR and P3DDR should also be cleared to H'00 in slave mode.

See section 12, “Host interface” for further information.

Reset and Hardware Standby Mode: A reset or entry to the hardware standby mode clears P3DDR, P3DR, and P3PCR to all 0, and clears the HIE bit to 0. In modes 1 and 2, all pins are placed in the data input (high-impedance) state. In mode 3 (single-chip mode), all pins are in the input state with the input pull-ups off.

Software Standby Mode: In the software standby mode, P3DDR, P3DR, P3PCR, and the HIE bit remain in their previous state. In modes 1 and 2 and slave mode, all pins are placed in the data input (high-impedance) state. In mode 3 with the host interface disabled, all pins remain in their previous input or output state. However, in mode 3 with the host interface enabled, all pins go into the high-impedance state if the corresponding DDR bit is set to 0. They will output 1 if the corresponding DDR bit is set to 1.

Input Pull-Ups: Port 3 has built-in programmable input pull-ups that are available in mode 3. The input pull-up for each bit can be turned on and off individually. To turn on an input pull-up in mode 3, set the corresponding P3PCR bit to 1 and clear the corresponding P3DDR bit to 0. P3PCR is cleared to H'00 by a reset and in the hardware standby mode, turning all input pull-ups off. In software standby mode, the previous state is maintained.

Table 5-10 indicates the states of the input pull-up transistors in each operating mode.

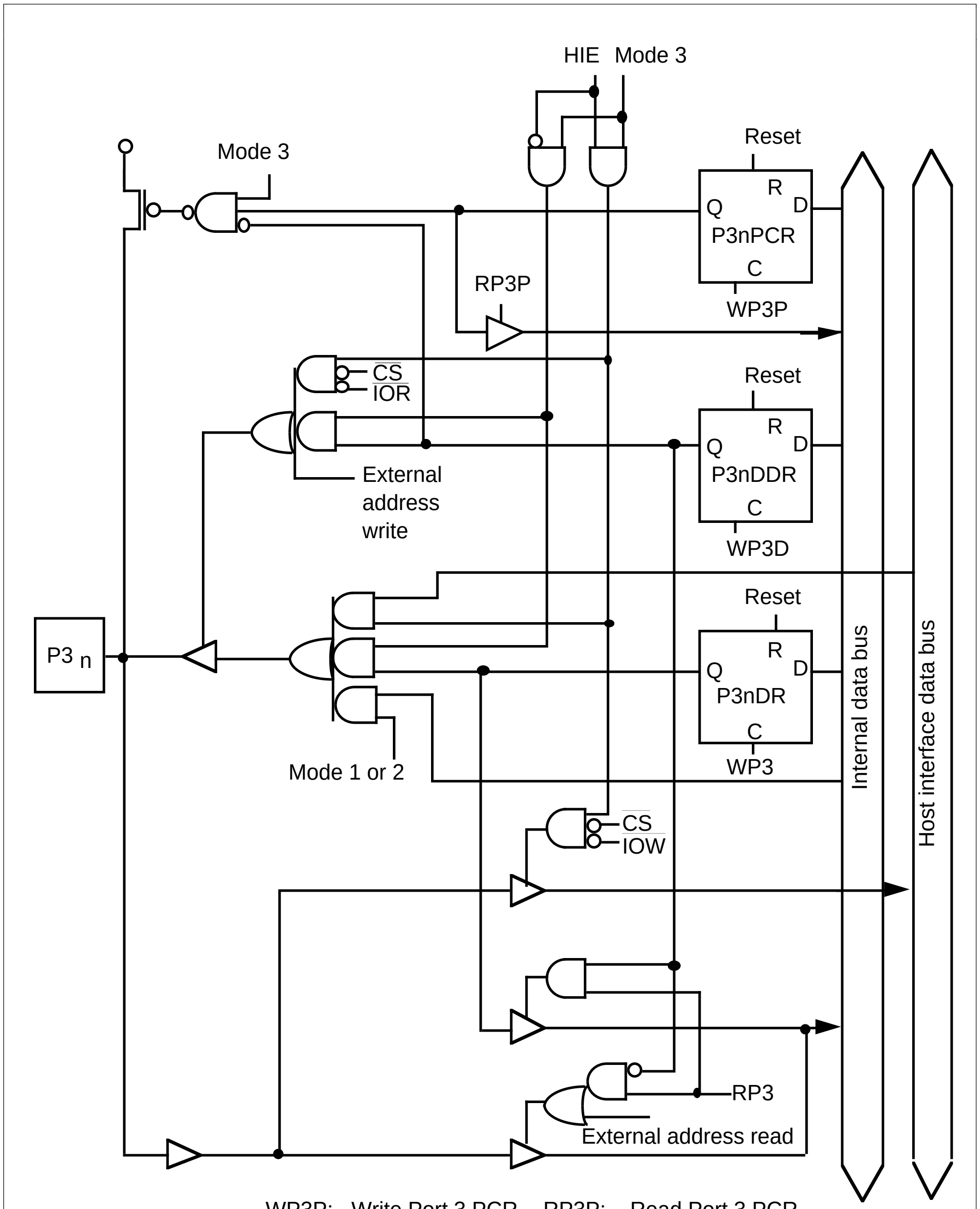
Table 5-10 Input Pull-Up States (Port 3)

Mode	Reset	Hardware Standby	Software Standby	Other Operating Modes
1	Off	Off	Off	Off
2	Off	Off	Off	Off
3	Off	Off	On/off	On/off

Notes: Off: The input pull-up is always off.

On/off: The input pull-up is on if P3PCR = 1 and P3DDR = 0, but off otherwise.

Figure 5-3 shows a schematic diagram of port 3.



WP3P:	Write Port 3 PCR	RP3P:	Read Port 3 PCR
WP3D:	Write Port 3 DDR	RP3:	Read Port 3
WP3:	Write Port 3	n = 0 to 7	

Figure 5-3 Port 3 Schematic Diagram

5.5 Port 4

Port 4 is an 8-bit input/output port that also provides the input and output pins for the 8-bit timers and the output pins for the PWM timers. In slave mode operation, P4$_3$–P4$_5$ are used as host interrupt request outputs. The pin functions depend on control bits in the control registers of the timers and HIE bit. Pins not used by the timers and host interrupt request are available for general-purpose input/output. Table 5-11 lists the pin functions, which are the same in both the expanded and single-chip modes.

Table 5-11 Port 4 Pin Functions (Modes 1 to 3)

Use	Pin Functions							
I/O port	P4$_0$	P4$_1$	P4$_2$	P4$_3$	P4$_4$	P4$_5$	P4$_6$	P4$_7$
Timer	TMCI$_0$	TMO$_0$	TMRI$_0$	TMCI$_1$	TMO$_1$	TMRI$_1$	PW$_0$	PW$_1$
Host Interface	P4$_0$	P4$_1$	P4$_2$	HIRQ$_{11}$	HIRQ$_1$	HIRQ$_{12}$	P4$_6$	P4$_7$

See section 7, 8-Bit Timers, and section 8, PWM Timers, for details of the timer control bits.

Pins of port 4 can drive a single TTL load and a 90-pF capacitive load when they are used as output pins. They can also drive a Darlington pair.

Table 5-12 details the port 4 registers.

Table 5-12 Port 4 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 4 data direction register	P4DDR	W	H'00	H'FFB5
Port 4 data register	P4DR	R/W	H'00	H'FFB7

5.5.1 Port 4 Data Direction Register (P4DDR)—H'FFB5

Bit	7	6	5	4	3	2	1	0
	P4$_7$DDR	P4$_6$DDR	P4$_5$DDR	P4$_4$DDR	P4$_3$DDR	P4$_2$DDR	P4$_1$DDR	P4$_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P4DDR is an 8-bit register that selects the direction of each pin in port 4. A pin functions as an output pin if the corresponding bit in P4DDR is set to 1, and as an input pin if the bit is cleared to 0.

5.5.2 Port 4 Data Register (P4DR)—H'FFB7

Bit	7	6	5	4	3	2	1	0
	$P4_7$	$P4_6$	$P4_5$	$P4_4$	$P4_3$	$P4_2$	$P4_1$	$P4_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PP4DR is an 8-bit register containing the data for pins $P4_7$ to $P4_0$. When the CPU reads P4DR, for output pins (P4DDR = 1), it reads the value in the P4DR latch, but for input pins (P4DDR = 0), it obtains the logic level directly from the pin, bypassing the P4DR latch. This also applies to pins used for timer input or output.

5.5.3 Port 4 Functions

Pins $P4_0$, $P4_2$, $P4_3$, and $P4_5$: As indicated in table 5-8, pins $P4_0$, $P4_2$, $P4_3$, and $P4_5$ can be used for general-purpose input or output, or input of 8-bit timer clock and reset signals. When a pin is used for timer signal input, its P4DDR bit should normally be cleared to 0; otherwise the timer will receive the value in P4DR. In slave mode, $P4_3$ and $P4_5$ are used as $HIRQ_{11}$ and $HIRQ_{12}$ interrupt outputs.

Pins $P4_1$, $P4_4$, $P4_6$, and $P4_7$: As indicated in table 5-8, pins $P4_1$, $P4_4$, $P4_6$, and $P4_7$ can be used for general-purpose input or output, or for 8-bit timer output ($P4_1$ and $P4_4$) or PWM timer output ($P4_6$ and $P4_7$). Pins used for timer output are unaffected by the values in P4DDR and P4DR. In slave mode, $P4_4$ is used as $HIRQ_1$ interrupt output.

Reset and Hardware Standby Mode: A reset or entry to the hardware standby mode clears P4DDR and P4DR to all 0 and makes all pins into input port pins.

Software Standby Mode: In the software standby mode, the control registers of the 8-bit and PWM timers are initialized but P4DDR and P4DR remain in their previous states. All pins become input or output port pins depending on the setting of P4DDR. Output pins output the values in P4DR.

Figures 5-4 to 5-7 show schematic diagrams of port 4.

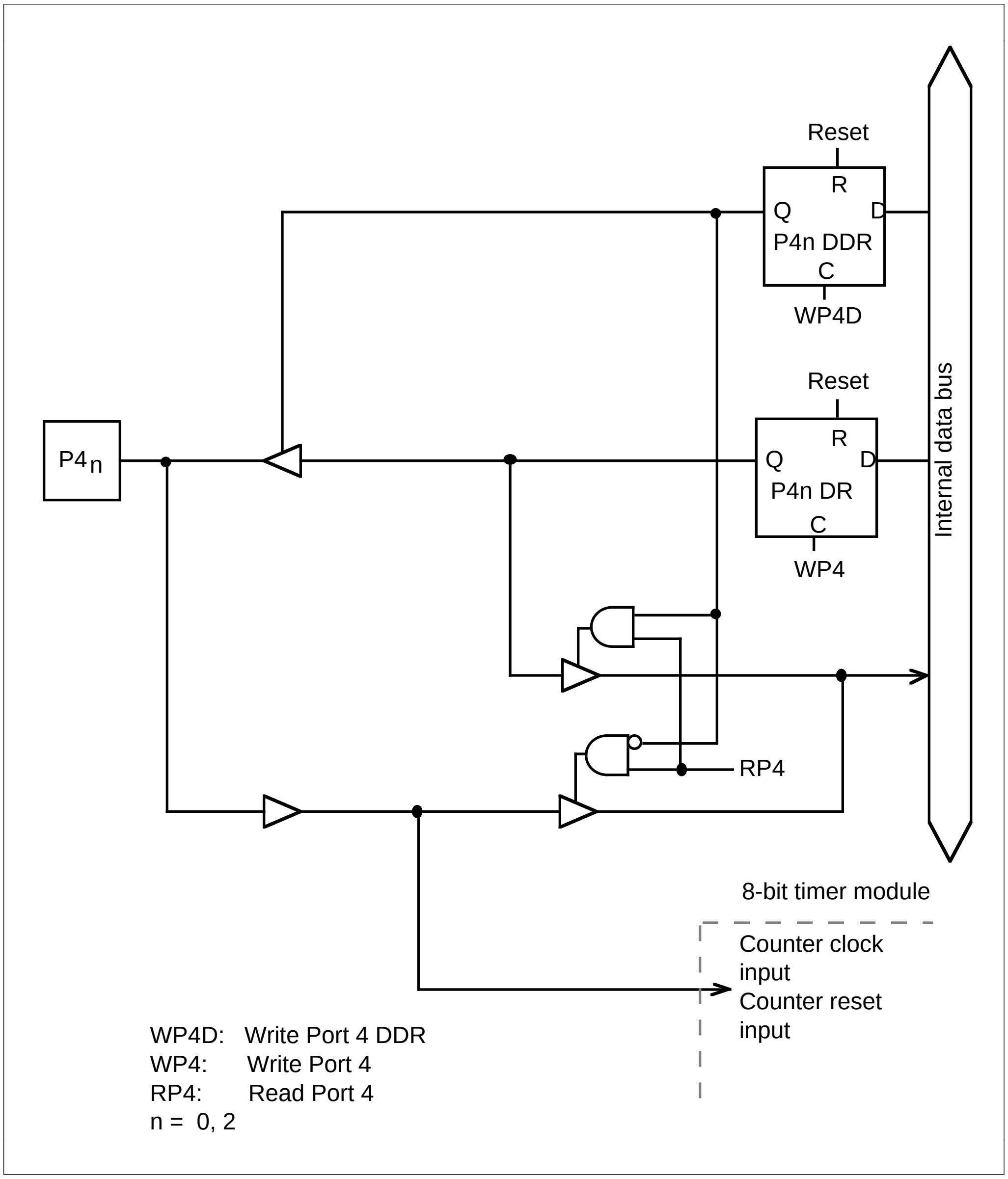


Figure 5-4 Port 4 Schematic Diagram (Pins $P4_0$ and $P4_2$)

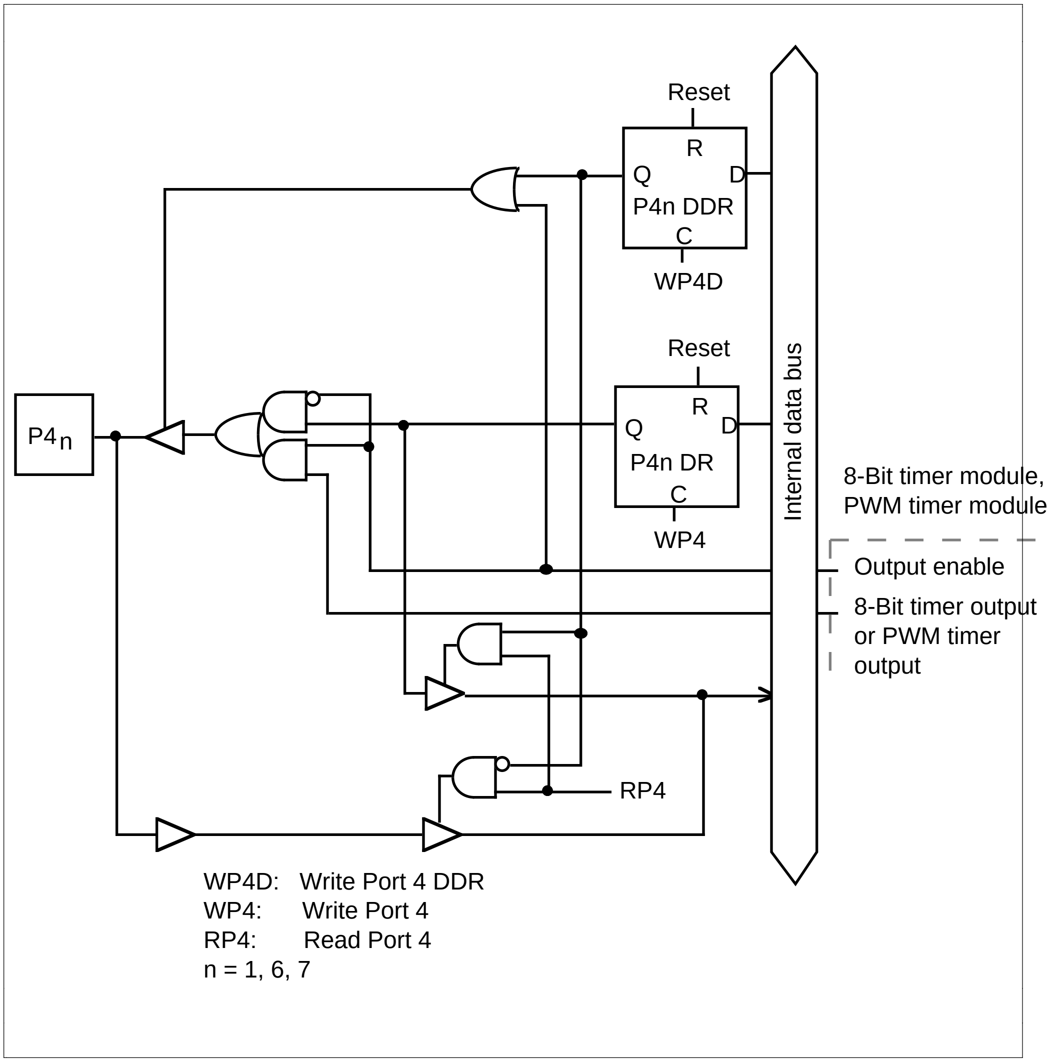


Figure 5-5 Port 4 Schematic Diagram (Pins 4$_1$, P4$_6$, and P4$_7$)

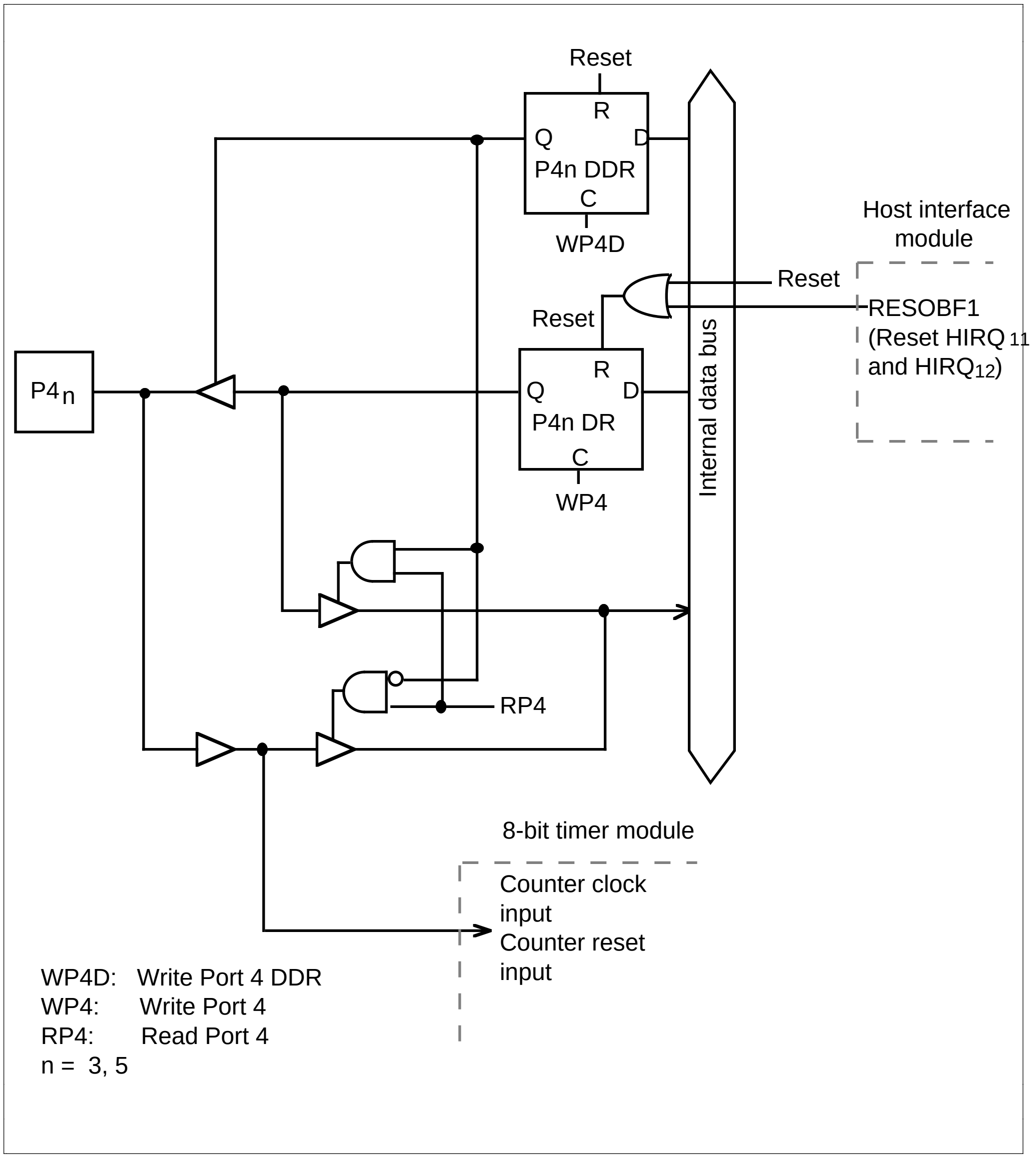


Figure 5-6 Port 4 Schematic Diagram (Pins P4$_3$ and P4$_5$)

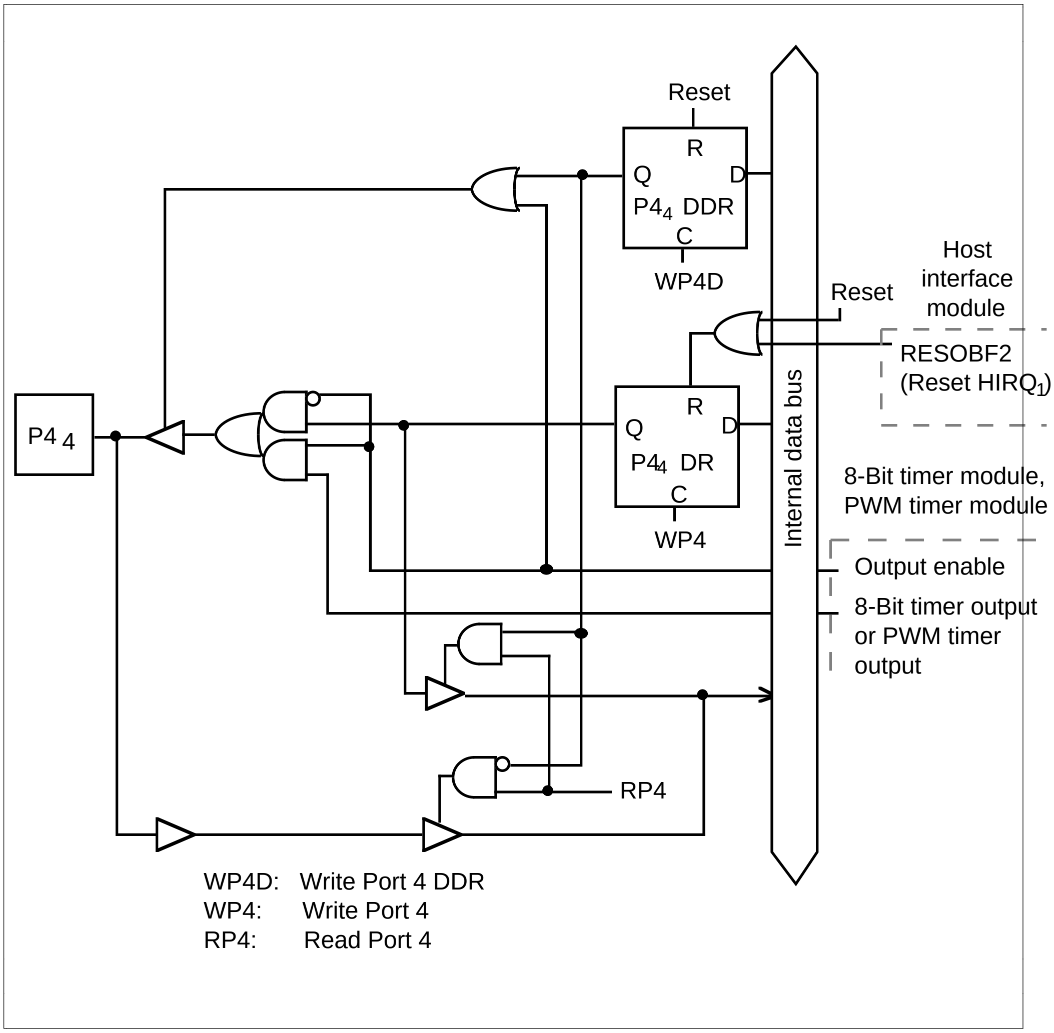


Figure 5-7 Port 4 Schematic Diagram (Pin P4$_4$)

5.6 Port 5

Port 5 is a 3-bit input/output port that also provides the input and output pins for asynchronous serial communication. The pin functions depend on control bits in the serial control register (SCR). Pins not used for serial communication are available for general-purpose input/output. Table 5-13 lists the pin functions, which are the same in both the expanded and single-chip modes.

Table 5-13 Port 5 Pin Functions (Modes 1 to 3)

Use	Pin Functions		
I/O port	P5$_0$	P5$_1$	P5$_2$
Timer	TxD	RxD	SCK

See section 9, Serial Communication Interface, for details of the serial control bits. Pins used by the serial communication interface are switched between input and output without regard to the values in the data direction register.

Pins of port 5 can drive a single TTL load and a 30-pF capacitive load when they are used as output pins. They can also drive a Darlington pair.

Table 5-14 details the port 5 registers.

Table 5-14 Port 5 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 5 data direction register	P5DDR	W	H'F8	H'FFB8
Port 5 data register	P5DR	R/W	H'F8	H'FFBA

5.6.1 Port 5 Data Direction Register (P5DDR)—H'FFB8

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	P5$_2$DDR	P5$_1$DDR	P5$_0$DDR
Initial value	1	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	W	W	W

P5DDR is an 8-bit register that selects the direction of each pin in port 5. A pin functions as an output pin if the corresponding bit in P5DDR is set to 1, and as an input pin if the bit is cleared to 0.

5.6.2 Port 5 Data Register (P5DR)—H'FFBA

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	P5$_2$	P5$_1$	P5$_0$
Initial value	1	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	R/W	R/W	R/W

P5DR is an 8-bit register containing the data for pins P5$_2$ to P5$_0$. When the CPU reads P5DR, for output pins (P5DDR = 1), it reads the value in the P5DR latch. However, for input pins

(P5DDR = 0), it obtains the logic level directly from the pin, bypassing the P5DR latch. This also applies to pins used for serial communication.

5.6.3 Port 5 Functions

Pin P5$_0$: Can be used for general-purpose input or output, or for output of serial transmit data (TxD). When used for TxD output, pin P5$_0$ is unaffected by the values in P5DDR and P5DR.

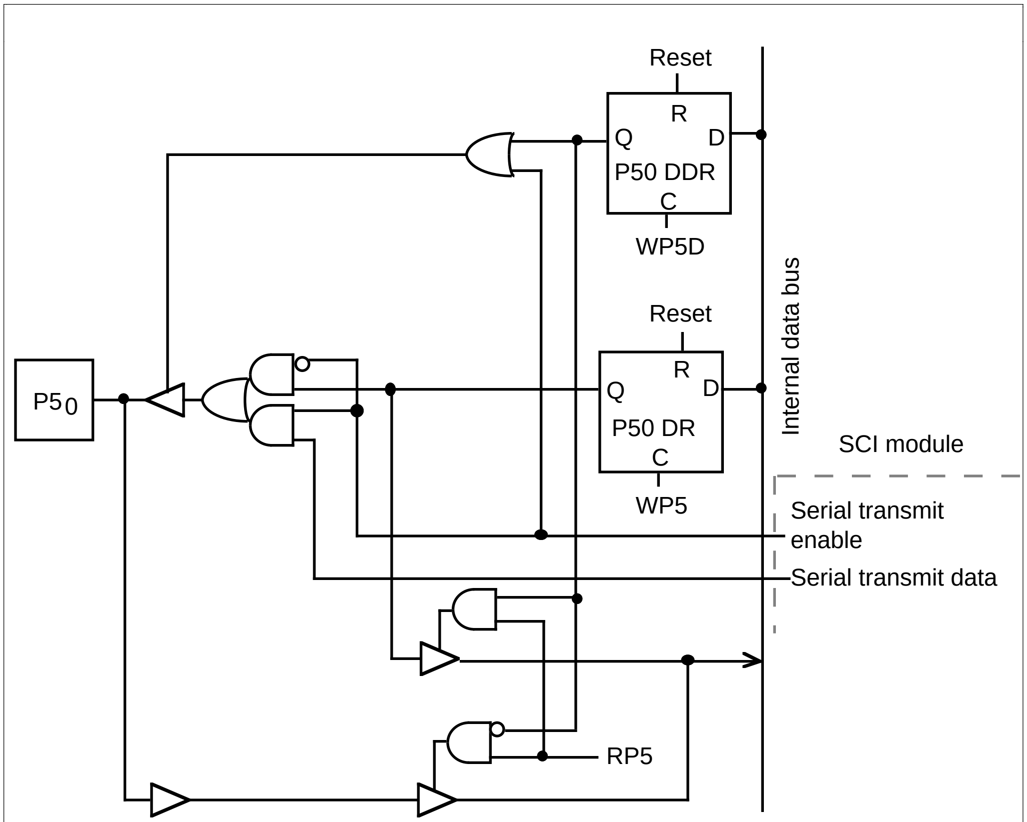
Pin P5$_1$: Can be used for general-purpose input or output, or for input of serial receive data (RxD). When used for RxD input, pin P5$_1$ is unaffected by P5DDR and P5DR.

Pin P5$_2$: Can be used for general-purpose input or output, or for serial clock input or output (SCK). When used for SCK input or output, pin P5$_2$ is unaffected by P5DDR and P5DR.

Reset and Hardware Standby Mode: A reset or entry to the hardware standby mode makes all pins of port 5 into input port pins.

Software Standby Mode: In the software standby mode, the serial control register is initialized but P5DDR and P5DR remain in their previous states. All pins become input or output port pins depending on the setting of P5DDR. Output pins output the values in P5DR.

Figures 5-8 to 5-10 show schematic diagrams of port 5.



WP5D: Write Port 5 DDR
WP5: Write Port 5
RP5: Read Port 5

Figure 5-8 Port 5 Schematic Diagram (Pin P5$_0$)

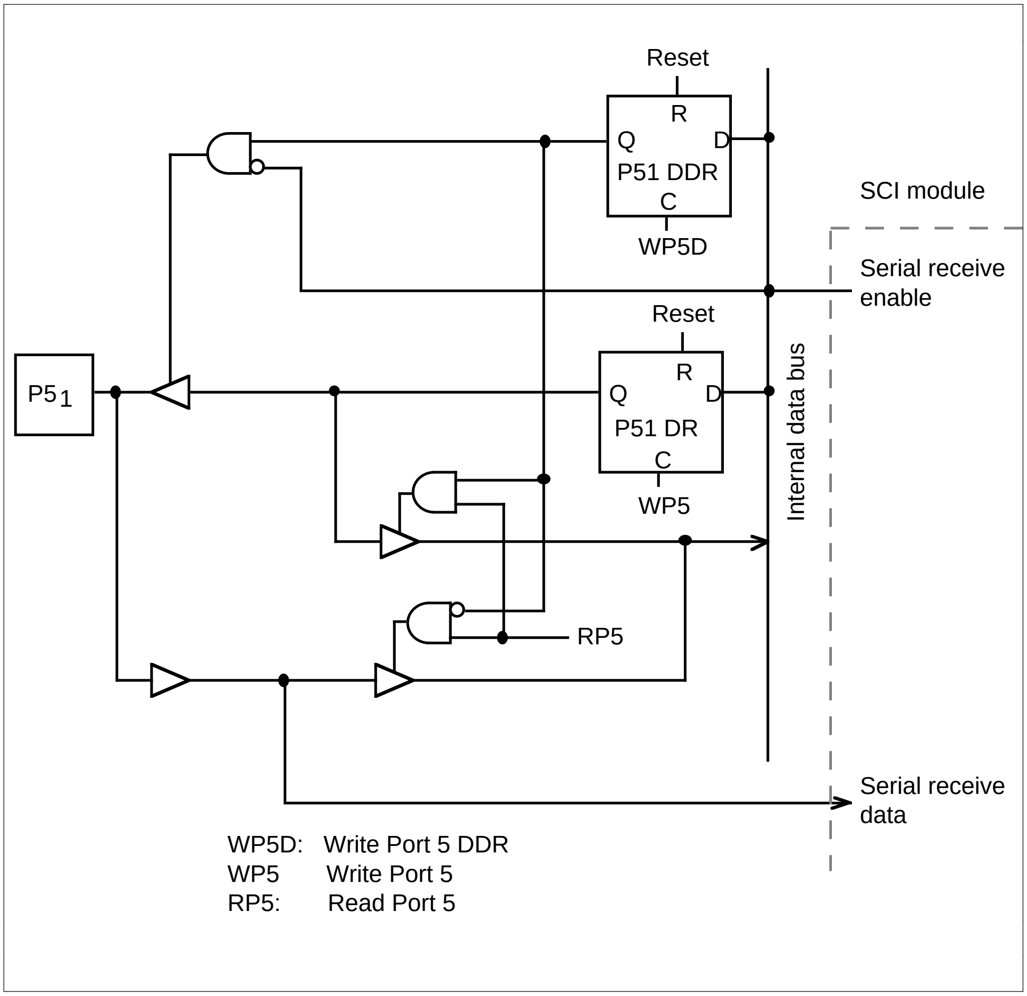


Figure 5-9 Port 5 Schematic Diagram (Pin P5$_1$)

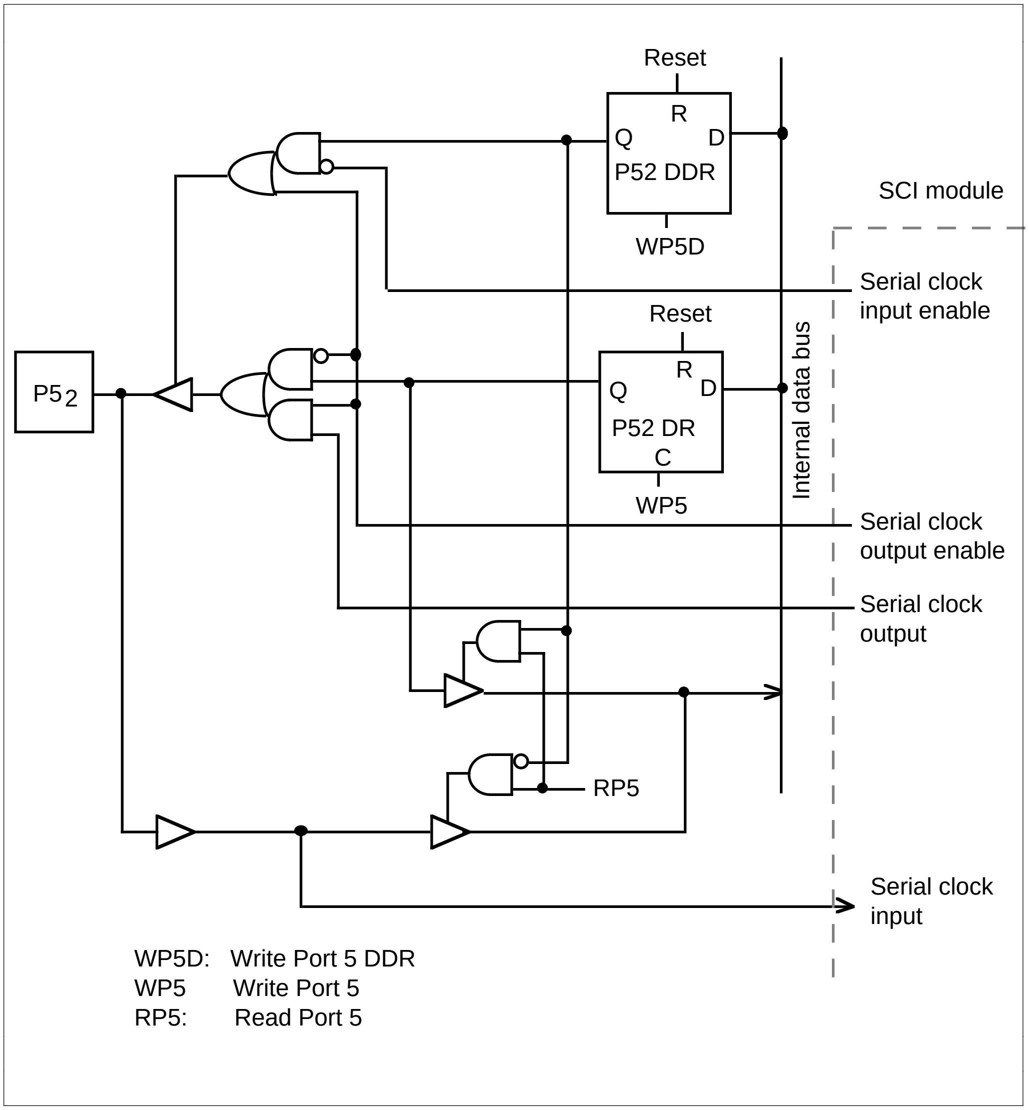


Figure 5-10 Port 5 Schematic Diagram (Pin P5$_2$)

5.7 Port 6

Port 6 is an 8-bit input/output port that also provides the input and output pins for the free-running timer, keyboard input sense lines, and the $\overline{IRQ}_6$ and $\overline{IRQ}_7$ input/output pins. The pin functions depend on control bits in the free-running timer control registers, and on bit 6 or 7 of the interrupt enable register. Pins not used for timer or interrupt functions are available for general-purpose input/output. Table 5-15 lists the pin functions, which are the same in both the expanded and single-chip modes.

Table 5-15 Port 6 Pin Functions

Use	Pin Functions (Modes 1 to 3)							
I/O port	$P6_0$	$P6_1$	$P6_2$	$P6_3$	$P6_4$	$P6_5$	$P6_6$	$P6_7$
Timer/ interrupt	FTCI	FTOA	FTIA	FTIB	FTIC	FTID	FTOB/$\overline{\text{IRQ}}_6$	$\overline{\text{IRQ}}_7$
Keyboard scan	$\overline{\text{KEYIN}}_0$	$\overline{\text{KEYIN}}_1$	$\overline{\text{KEYIN}}_2$	$\overline{\text{KEYIN}}_3$	$\overline{\text{KEYIN}}_4$	$\overline{\text{KEYIN}}_5$	$\overline{\text{KEYIN}}_6$	$\overline{\text{KEYIN}}_7$

See section 4, Exception Handling, and section 6, 16-Bit Free-Running Timer, for details of the free-running timer and interrupts.

Pins of port 6 can drive a single TTL load and a 90-pF capacitive load when they are used as output pins. They can also drive a Darlington pair.

Table 5-16 details the port 6 registers.

Table 5-16 Port 6 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 6 data direction register	P6DDR	W	H'00	H'FFB9
Port 6 data register	P6DR	R/W	H'00	H'FFBB

5.7.1 Port 6 Data Direction Register (P6DDR)—H'FFB9

Bit	7	6	5	4	3	2	1	0
	$P6_7$DDR	$P6_6$DDR	$P6_5$DDR	$P6_4$DDR	$P6_3$DDR	$P6_2$DDR	$P6_1$DDR	$P6_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P6DDR is an 8-bit register that selects the direction of each pin in port 6. A pin functions as an output pin if the corresponding bit in P6DDR is set to 1, and as an input pin if the bit is cleared to 0.

5.7.2 Port 6 Data Register (P6DR)—H'FFBB

Bit	7	6	5	4	3	2	1	0
	$P6_7$	$P6_6$	$P6_5$	$P6_4$	$P6_3$	$P6_2$	$P6_1$	$P6_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P6DR is an 8-bit register containing the data for pins $P6_7$ to $P6_0$. When the CPU reads P6DR, for output pins (P6DDR = 1) it reads the value in the P6DR latch, but for input pins (P6DDR = 0), it obtains the logic level directly from the pin, bypassing the P6DR latch. This also applies to pins used for input and output of timer and interrupt signals.

5.7.3 Port 6 Functions

Pins $P6_0$, $P6_2$, $P6_3$, $P6_4$, and $P6_5$: As indicated in table 5-16, pins $P6_0$, $P6_2$, $P6_3$, $P6_4$, and $P6_5$ can be used for general-purpose input or output, for input of free-running timer clock and input capture signals, or for keyboard input scan. When a pin is used for free-running timer or keyboard scan input, its P6DDR bit should be cleared to 0; otherwise the free-running timer or keyboard scan will receive the value in P6DR.

Pin $P6_1$: Pin $P6_1$ can be used for general-purpose input or output, for the output compare A signal (FTOA) of the free-running timer, or for keyboard input scan. When used for FTOA output, this pin is unaffected by the values in P6DDR and P6DR.

Pin $P6_6$: Pin $P6_6$ can be used for general-purpose input or output, for the output compare B signal (FTOB) of the free-running timer, for $\overline{IRQ_6}$ input, or for keyboard input scan. When used for FTOB output, this pin is unaffected by the values in P6DDR and P6DR. When this pin is used for $\overline{IRQ_6}$ or keyboard scan input, $P6_6$DDR should normally be cleared to 0, so that the value in P6DR will not generate interrupts.

Pin $P6_7$: Pin $P6_7$ can be used for general-purpose input or output, $\overline{IRQ_7}$ input, or for keyboard input scan. When it is used for $\overline{IRQ_7}$ or keyboard scan input, $P6_7$DDR should normally be cleared to 0, so that the value in P6DR will not generate interrupts.

Reset and Hardware Standby Mode: A reset or entry to the hardware standby mode clears P6DDR and P6DR to all 0 and makes all pins into input port pins.

Software Standby Mode: In the software standby mode, the free-running timer control registers are initialized but P6DDR and P6DR remain in their previous states. All pins become input or output port pins depending on the setting of P6DDR. Output pins output the values in P6DR.

Figures 5-11 to 5-14 shows schematic diagrams of port 6.

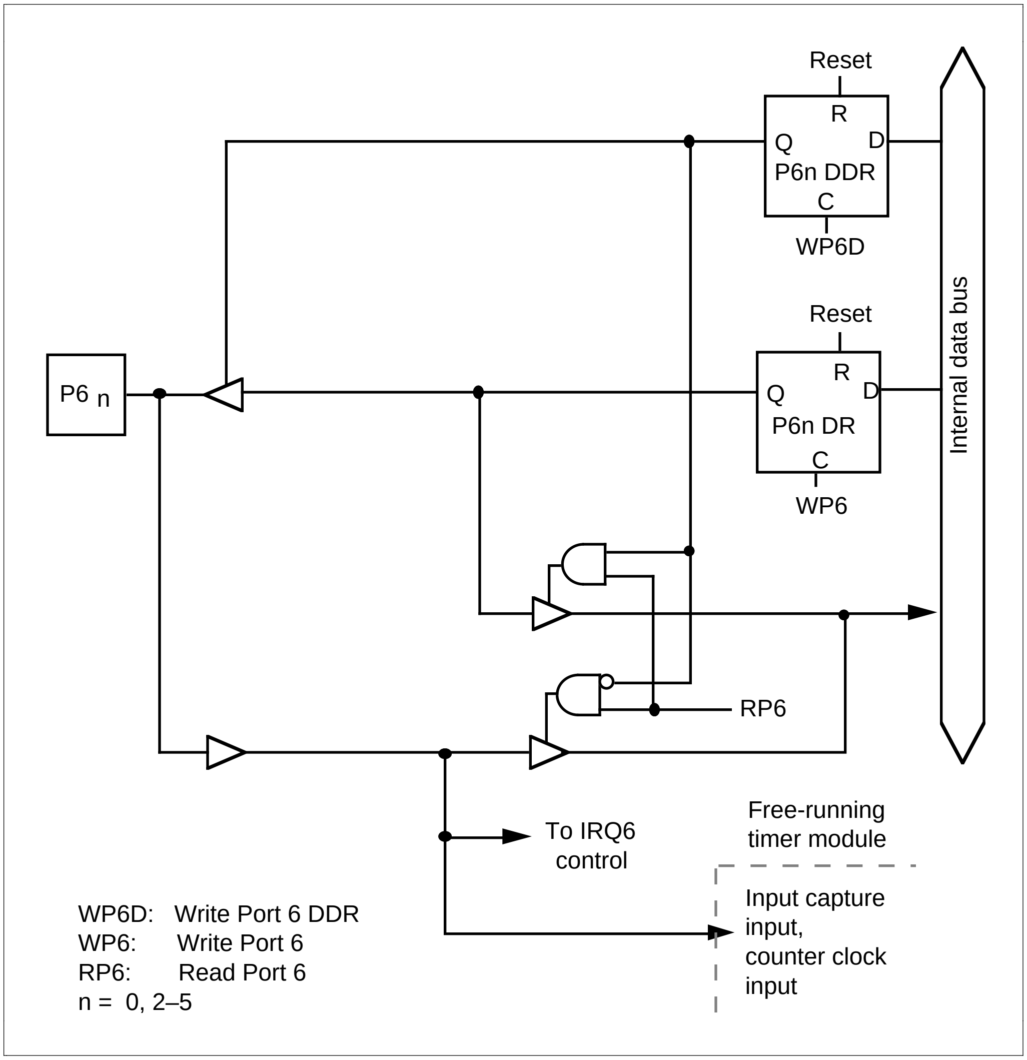


Figure 5-11 Port 6 Schematic Diagram (Pins $P6_0$, $P6_2$, $P6_3$, $P6_4$, and $P6_5$)

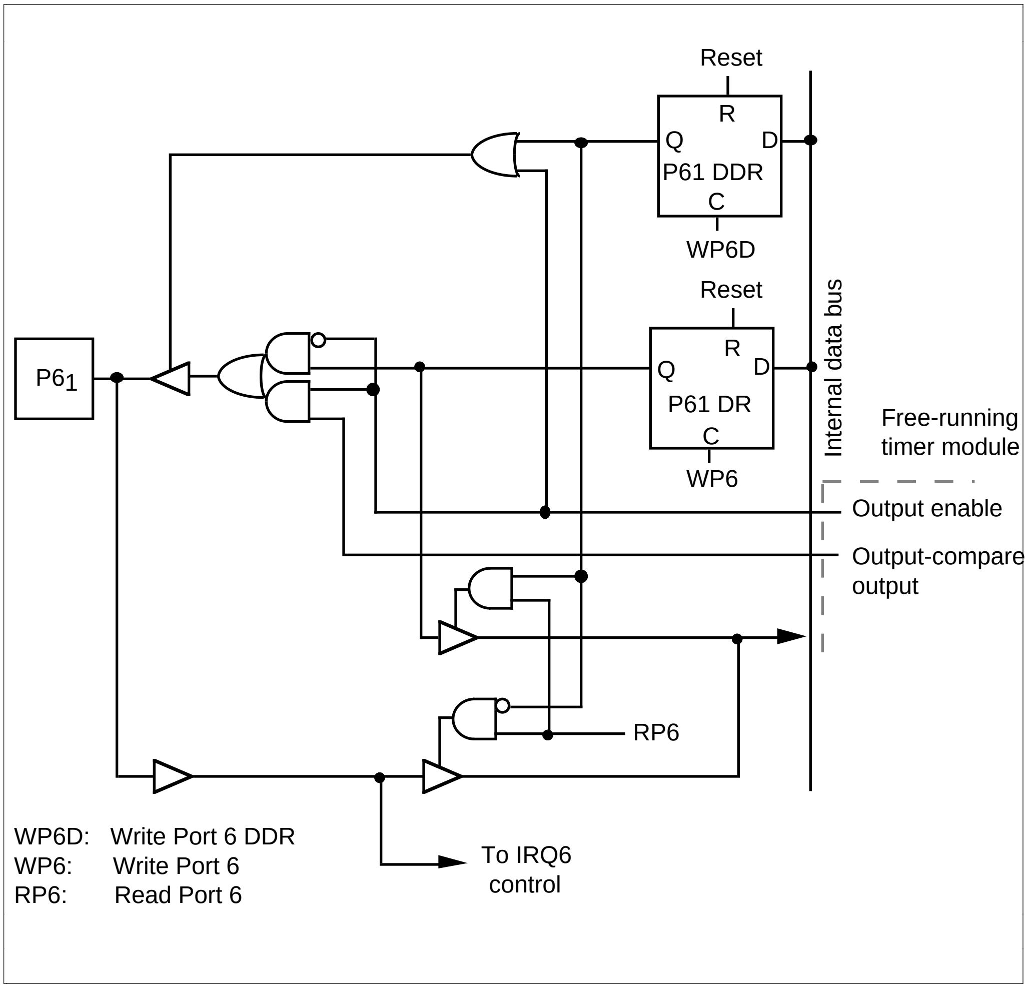


Figure 5-12 Port 6 Schematic Diagram (Pin $P6_1$)

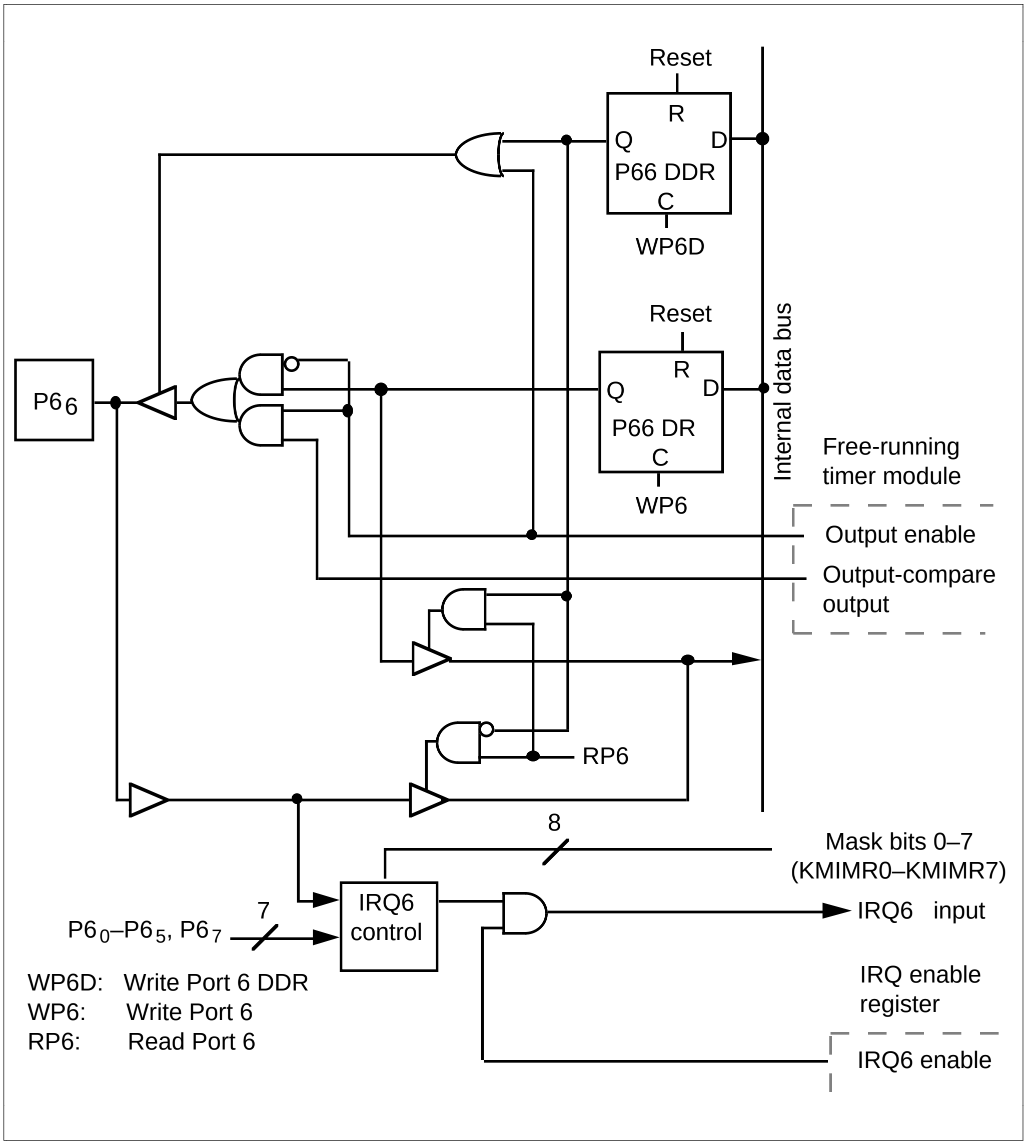


Figure 5-13 Port 6 Schematic Diagram (Pin $P6_6$)

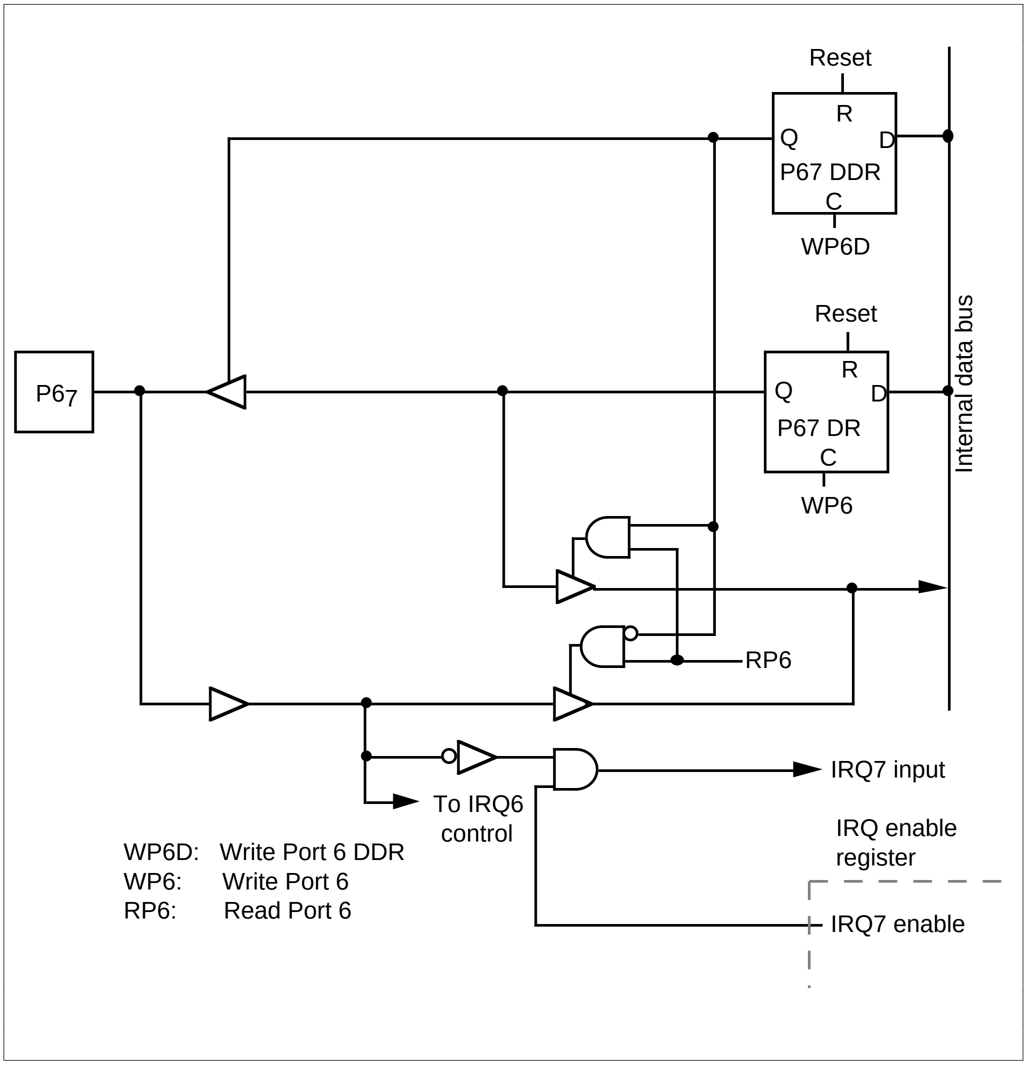


Figure 5-14 Port 6 Schematic Diagram (Pin P6$_7$)

5.8 Port 7

Port 7 is an 8-bit input port that also provides the analog input pins for the A/D converter module. The pin functions are the same in both the expanded and single-chip modes.

Table 5-17 lists the pin functions. Table 5-18 describes the port 7 data register, which simply consists of connections of the port 7 pins to the internal data bus. Figure 5-15 shows a schematic diagram of port 7.

Table 5-17 Port 7 Pin Functions (Modes 1 to 3)

Use	Pin Functions							
I/O port	$P7_0$	$P7_1$	$P7_2$	$P7_3$	$P7_4$	$P7_5$	$P7_6$	$P7_7$
Analog input	AN_0	AN_1	AN_2	AN_3	AN_4	AN_5	AN_6	AN_7

Table 5-18 Port 7 Register

Name	Abbreviation	Read/Write	Initial Value	Address
Port 7 data register	P7DR	R	Undetermined	H'FFBE

5.8.1 Port 7 Data Register (P7DR)—H'FFBE

Bit	7	6	5	4	3	2	1	0
	$P7_7$	$P7_6$	$P7_5$	$P7_4$	$P7_3$	$P7_2$	$P7_1$	$P7_0$
Initial value	*	*	*	*	*	*	*	*
Read/Write	R	R	R	R	R	R	R	R

Note: *: Depends on the levels of pins $P7_7$ to $P7_0$.

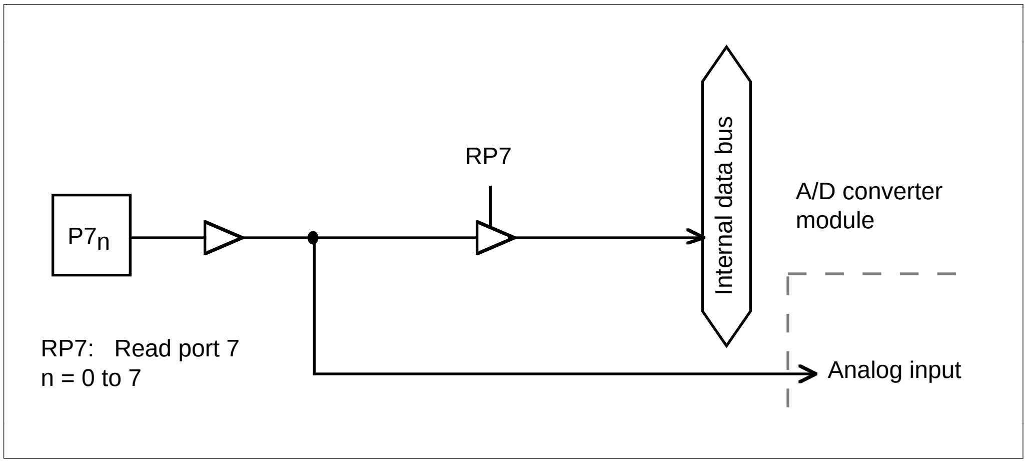


Figure 5-15 Port 7 Schematic Diagram

5.9 Port 8

Port 8 is a 7-bit input/output port that also provides pins for host interface inputs (single-chip mode) and interrupt input. Table 5-19 lists the pin functions.

Table 5-19 Port 8 Pin Functions

I/O Port	Interrupt Input	Slave Mode
P80 input/output	—	HA$_0$ input
P81 input/output	—	GA$_{20}$ output
P82 input/output	—	$\overline{\text{CS}}_1$ input
P83 input/output	—	$\overline{\text{IOR}}$ input
P84 input/output	$\overline{\text{IRQ}}_3$ input	$\overline{\text{IOW}}$ input
P85 input/output	$\overline{\text{IRQ}}_4$ input	$\overline{\text{CS}}_2$ input
P86 input/output	$\overline{\text{IRQ}}_5$ input	—

Pins of port 8 can drive a single TTL load and a 30-pF capacitive load when they are used as output pins. They can also drive a Darlington pair.

Table 5-20 details the port 8 registers.

Table 5-20 Port 8 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 8 data direction register	P8DDR	W	H'80	H'FFBD
Port 8 data register	P8DR	R/W	H'80	H'FFBF

5.9.1 Port 8 Data Direction Register (P8DDR)—H'FFBD

Bit	7	6	5	4	3	2	1	0
	—	P8$_6$DDR	P8$_5$DDR	P8$_4$DDR	P8$_3$DDR	P8$_2$DDR	P8$_1$DDR	P8$_0$DDR
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	W	W	W	W	W	W	W

P8DDR is an 8-bit register that selects the direction of each pin in port 8. A pin functions as an output pin if the corresponding bit in P8DDR is set to 1, and as in input pin if the bit is cleared to 0.

Bit 7 is reserved. It cannot be modified, and is always read as 1.

5.9.2 Port 8 Data Register (P8DR)—H'FFBF

Bit	7	6	5	4	3	2	1	0
	—	$P8_6$	$P8_5$	$P8_4$	$P8_3$	$P8_2$	$P8_1$	$P8_0$
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P8DR is an 8-bit register containing the data for pins $P8_6$ to $P8_0$. When the CPU reads P8DR, for output pins (P8DDR = 1) it reads the value in the P8DR latch. However, for input pins (P8DDR = 0), it obtains the logic level directly from the pin, bypassing the P8DR latch.

Bit 7 is reserved. It cannot be modified, and is always read as 1.

5.9.3 Port 8 Functions

Pin $P8_0$: When the host interface is disabled (HIE = 0), pin $P8_0$ can be used for general-purpose input or output. In the slave mode (HIE = 1), this pin is used for register select input (HA_0). In slave mode, this pin is unaffected by the values in P8DDR and P8DR.

Pin $P8_1$: When the host interface is disabled (HIE = 0), pin $P8_1$ can be used for general-purpose input or output. In the slave mode (HIE = 1), this pin is used for GATE A_{20} output (GA_{20}). Enable the output function for GA_{20} application by writing a 1 to the DDR bit.

Pins $P8_2$ and $P8_3$: Pins $P8_2$ and $P8_3$ are available for general-purpose input or output if the host interface is disabled (HIE = 0).

In the slave mode (mode 3 with HIE = 1), pins $P8_2$ and $P8_3$ are used for chip select input ($\overline{CS_1}$) and I/O read input ($\overline{IOR}$), respectively. They are unaffected by the bits in P8DDR and P8DR.

Pin $P8_4$: Pin $P8_4$ can be used for general-purpose input or output, for input of $\overline{IOW}$ in slave mode, or for $\overline{IRQ_3}$ input. When this pin is used for $\overline{IRQ_3}$ input, $P8_4$DDR should normally be cleared to 0, so that the value in P8DR will not generate interrupts.

Pin $P8_5$: Pin $P8_5$ can be used for general-purpose input or output, for input of $\overline{CS_2}$ in slave mode, or for $\overline{IRQ_4}$ input. When this pin is used for $\overline{IRQ_4}$ input, $P8_5$DDR should normally be cleared to 0, so that the value in P8DR will not generate interrupts.

Pin $P8_6$: Pin $P8_6$ has the same functions in all modes. It can be used for general-purpose input or output, or for $\overline{IRQ_5}$ input. When this pin is used for $\overline{IRQ_5}$ input, $P8_6$DDR should normally be cleared to 0, so that the value in P8DR will not generate interrupts.

Reset: A reset clears bits $P8_6$DDR to $P8_0$DDR to 0 and clears the HIE bit, and interrupt enable bits to 0, making $P8_6$ to $P8_0$ into input port pins.

Hardware Standby Mode: All pins are placed in the high-impedance state.

Software Standby Mode: In the software standby mode, the HIE bit, the interrupt enable register, P8DDR, and P8DR remain in their previous states. All pins remain in their previous state.

Figures 5-16 to 5-21 show schematic diagrams of port 8.

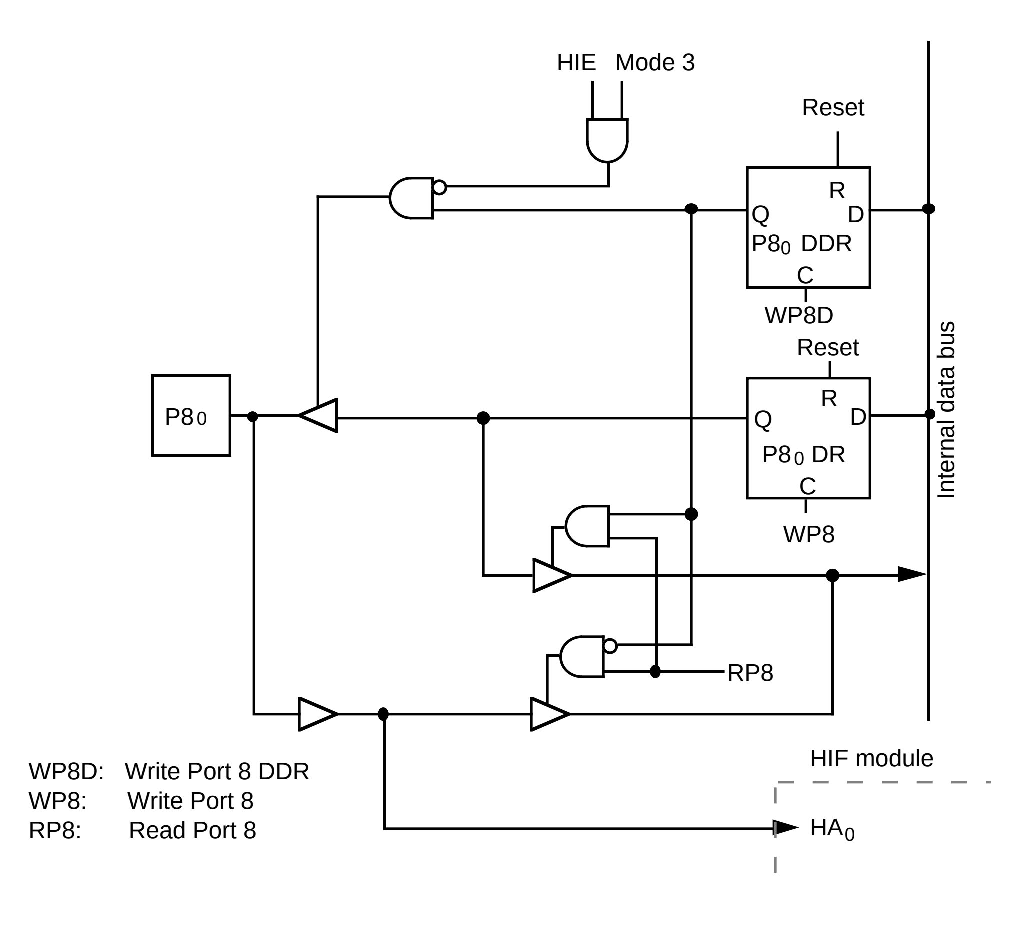
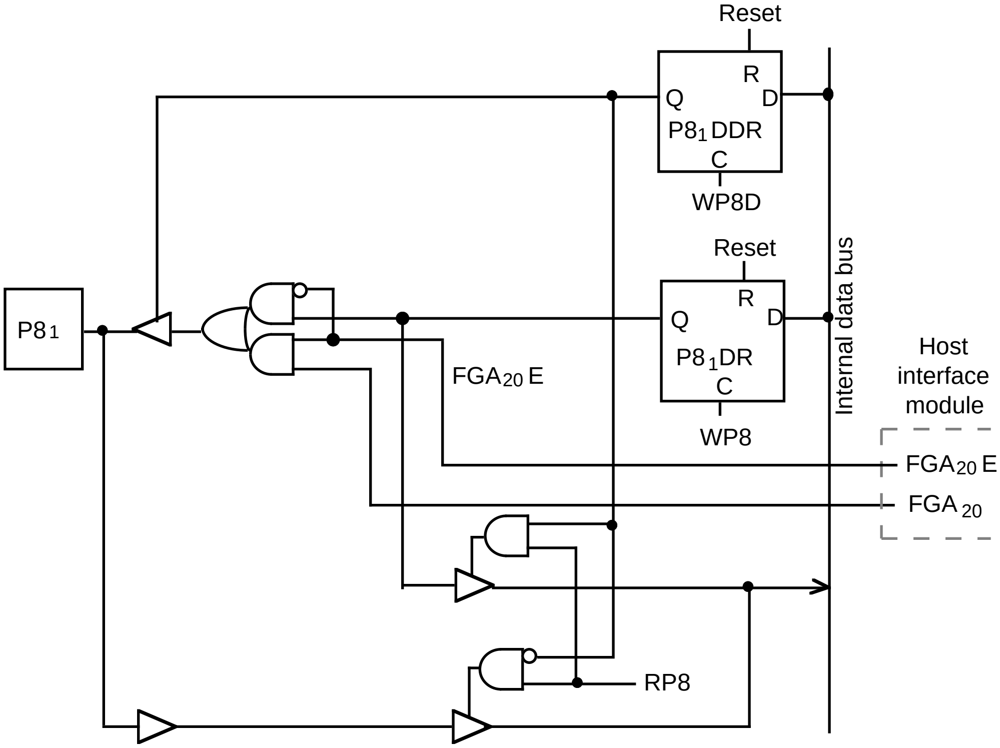


Figure 5-16 Port 8 Schematic Diagram (Pin P80)



WP8D: Write Port 8 DDR
WP8: Write Port 8
RP8: Read Port 8

Figure 5-17 Port 8 Schematic Diagram (Pin $P8_1$)

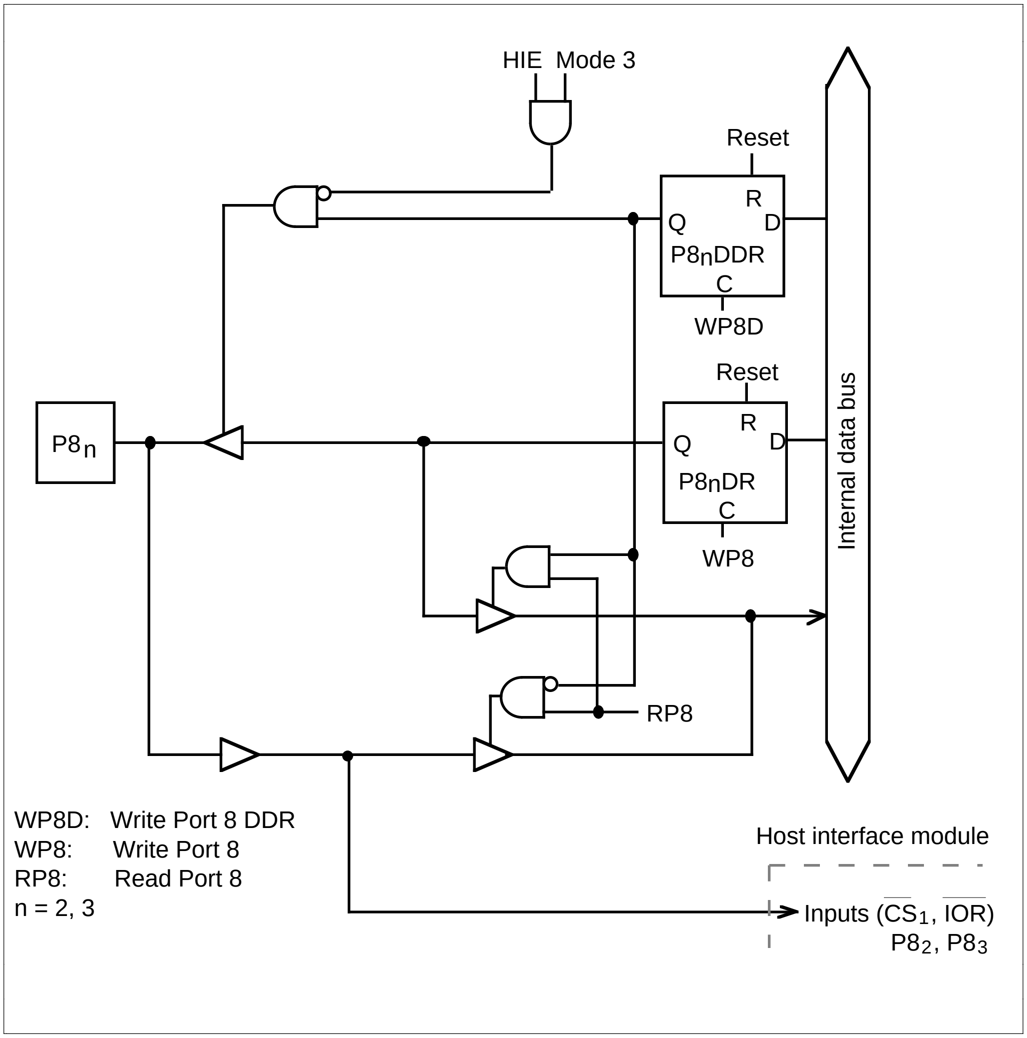


Figure 5-18 Port 8 Schematic Diagram (Pins $P8_2$ and $P8_3$)

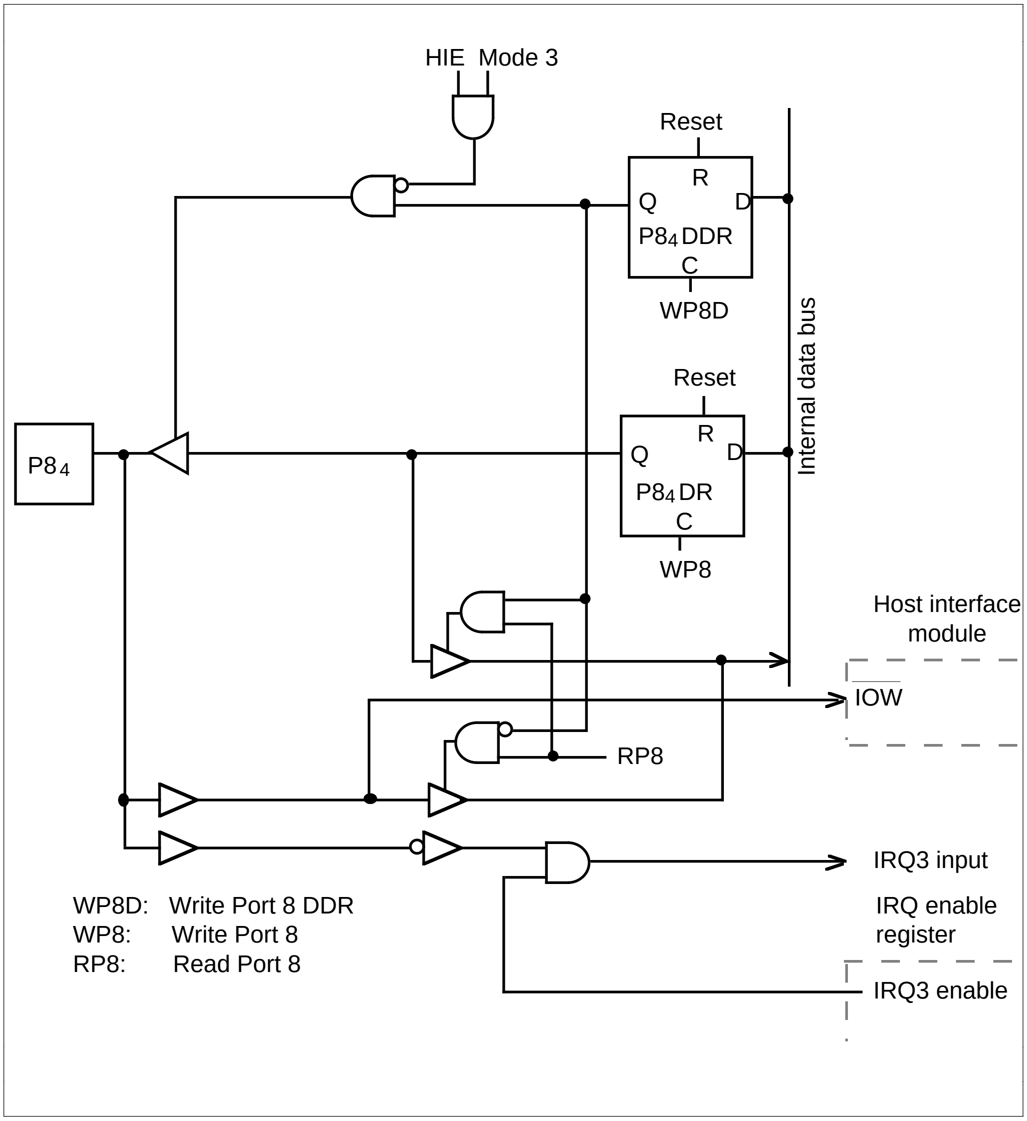


Figure 5-19 Port 8 Schematic Diagram (Pin $P8_4$)

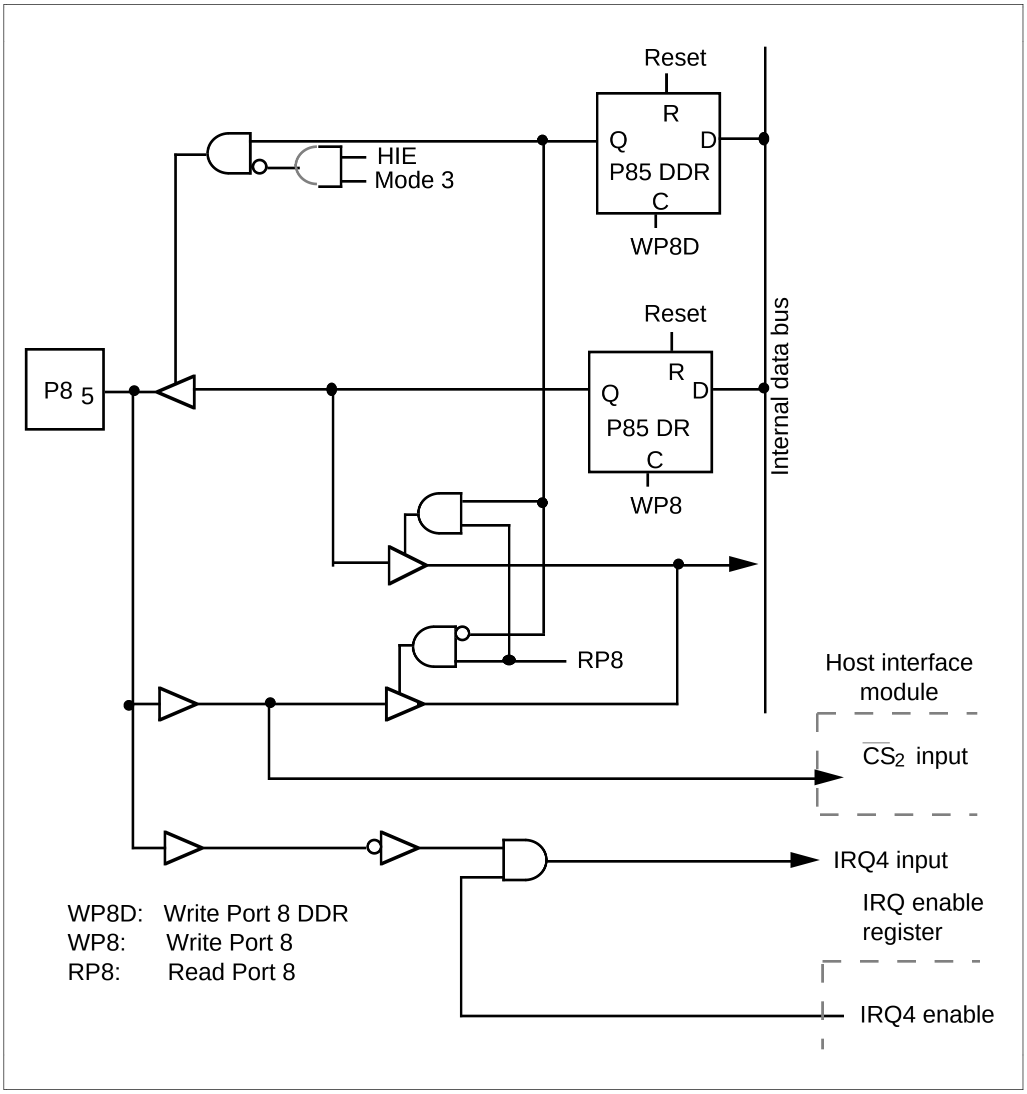


Figure 5-20 Port 8 Schematic Diagram (Pin $P8_5$)

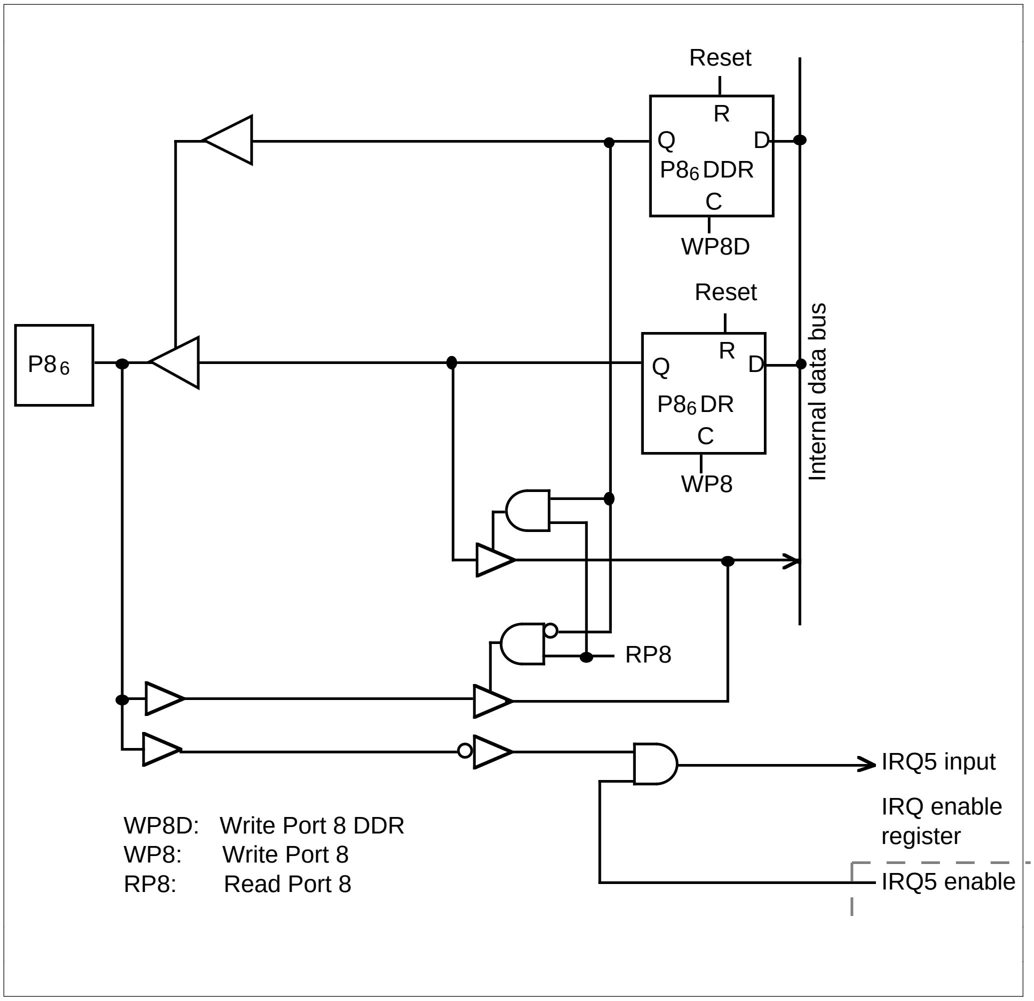


Figure 5-21 Port 8 Schematic Diagram (Pin $P8_6$)

5.10 Port 9

Port 9 is an 8-bit input/output port that also provides pins for interrupt input ($\overline{IRQ_0}$ to $\overline{IRQ_2}$), A/D trigger input, system clock (ϕ) output, bus control signals (in the expanded modes).

Pins $P9_7$ to $P9_3$ have different functions in different modes. Pins $P9_2$ to $P9_0$ have the same functions in all modes. Table 5-21 lists the pin functions.

Table 5-21 Port 9 Pin Functions

Pin	Expanded Modes	Single-Chip Mode
$P9_0$	P90 input/output , $\overline{\text{IRQ}}_2$ input, and $\overline{\text{ADTRG}}$ input (simultaneously)	
$P9_1$	P91 input/output and $\overline{\text{IRQ}}_1$ input (simultaneously)	
$P9_2$	P92 input/output and $\overline{\text{IRQ}}_0$ input (simultaneously)	
$P9_3$	$\overline{\text{RD}}$ output	$P9_3$ input/output
$P9_4$	$\overline{\text{WR}}$ output	$P9_4$ input/output
$P9_5$	$\overline{\text{AS}}$ output	P95 input/output
$P9_6$	ϕ output	$P9_6$ input or ϕ output
$P9_7$	$\overline{\text{WAIT}}$ input	$P9_7$ input/output

Pins of port 9 can drive a single TTL load and a 90-pF capacitive load when they are used as output pins.

Table 5-22 details the port 9 registers.

Table 5-22 Port 9 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 9 data direction register	P9DDR	W	H'40 (modes 1 and 2) H'00 (mode 3)	H'FFC0
Port 9 data register	P9DR	R/W Note 1	Undetermined Note 2	H'FFC1

Notes: 1. Bit 6 is read-only.

2. Bit 6 is undetermined. Other bits are initially 0.

5.10.1 Port 9 Data Direction Register (P9DDR)—H'FFC0

Bit	7	6	5	4	3	2	1	0
	$P9_7$DDR	$P9_6$DDR	$P9_5$DDR	$P9_4$DDR	$P9_3$DDR	$P9_2$DDR	$P9_1$DDR	$P9_0$DDR
Modes 1 and 2								
Initial value	0	1	0	0	0	0	0	0
Read/Write	W	—	W	W	W	W	W	W
Mode 3								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P9DDR is an 8-bit register that selects the direction of each pin in port 9. A pin functions as an output pin if the corresponding bit in P9DDR is set to 1, and as in input pin if the bit is cleared to 0.

5.10.1 Port 9 Data Register (P9DR)—H'FFC1

Bit	7	6	5	4	3	2	1	0
	$P9_7$	$P9_6$	$P9_5$	$P9_4$	$P9_3$	$P9_2$	$P9_1$	$P9_0$
Initial value	0	*	0	0	0	0	0	0
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Determined by the level at pin $P9_6$.

P9DR is an 8-bit register containing the data for pins $P9_7$ to $P9_0$. When the CPU reads P9DR, for output pins (P9DDR = 1) it reads the value in the P9DR latch, but for input pins (P9DDR = 0), it obtains the logic level directly from the pin, bypassing the P9DR latch. This also applies to pins used for interrupt input, A/D trigger input, clock output, and control signal input or output.

5.10.3 Port 9 Functions

Pins $P9_0$, $P9_1$, and $P9_2$: Pins $P9_0$, $P9_1$, and $P9_2$ can be used for general-purpose input or output, interrupt request input, or A/D trigger input. See table 5-18. If a pin is used for interrupt or A/D trigger input, its data direction bit should be cleared to 0, so that the output from P9DR will not generate an interrupt request or A/D trigger signal.

Pins $P9_3$ and $P9_4$: In modes 1 and 2 (the expanded modes), pins $P9_3$ and $P9_4$ are used for output of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ bus control signals. They are unaffected by the values in P9DDR and P9DR.

In mode 3, these pins can be used for general-purpose input or output.

Pin $P9_5$: In modes 1 and 2, pin $P9_5$ is used for output of the $\overline{\text{AS}}$ bus control signal. It is unaffected by the values in P9DDR and P9DR.

In mode 3, this pin can be used for general-purpose input or output.

Pin $P9_6$: In modes 1 and 2, pin $P9_6$ is used for system clock (ϕ) output.

In mode 3, this pin is used for general-purpose input if $P9_6$DDR is cleared to 0, or system clock output if $P9_6$DDR is set to 1.

Pin $P9_7$: In modes 1 and 2, pin $P9_7$ is used for input of the $\overline{\text{WAIT}}$ bus control signal. It is unaffected by the values in P9DDR and P9DR.

In mode 3 (single-chip mode), this pin can be used for general-purpose input or output.

Reset: In the single-chip mode (mode 3), a reset initializes all pins of port 9 to the general-purpose input function. In the expanded modes (modes 1 and 2), $P9_0$ to $P9_2$ are initialized as input port pins, and $P9_3$ to $P9_7$ are initialized to their bus control and system clock output functions.

Hardware Standby Mode: All pins are placed in the high-impedance state.

Software Standby Mode: All pins remain in their previous state. For $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{AS}}$, and ϕ this means the high output state.

Figures 5-22 to 5-26 show schematic diagrams of port 9.

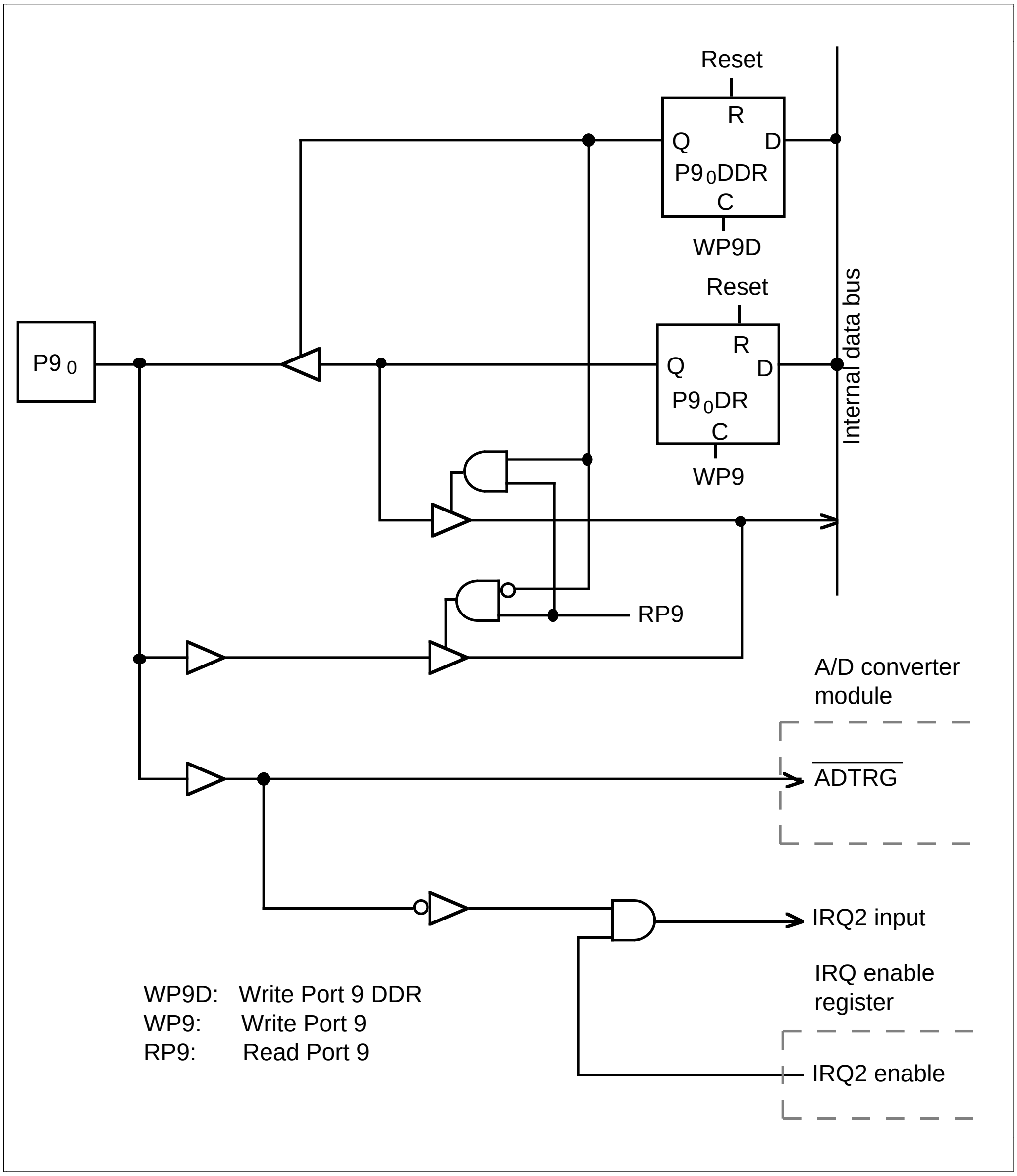


Figure 5-22 Port 9 Schematic Diagram (Pin P9$_0$)

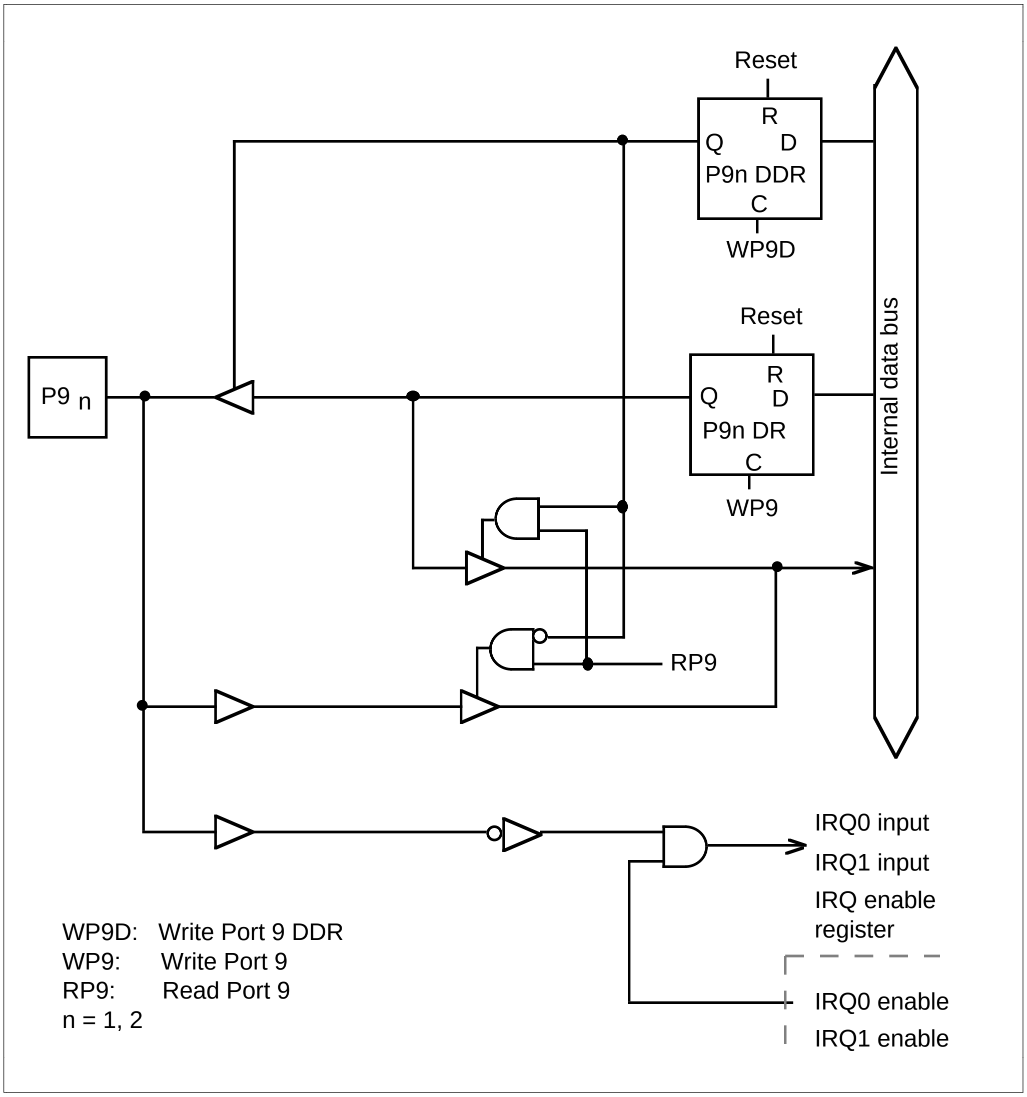


Figure 5-23 Port 9 Schematic Diagram (Pins $P9_1$ to $P9_2$)

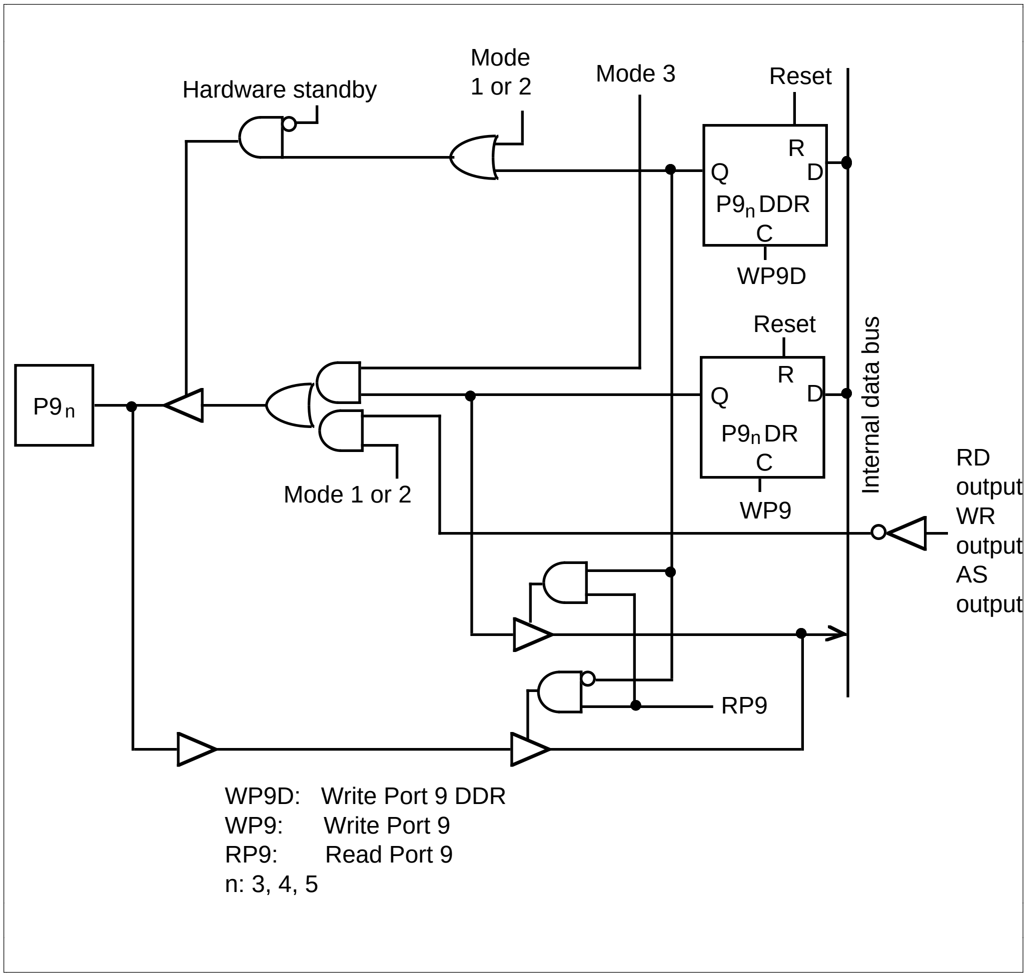


Figure 5-24 Port 9 Schematic Diagram (Pin P9$_3$, P9$_4$, P9$_5$)

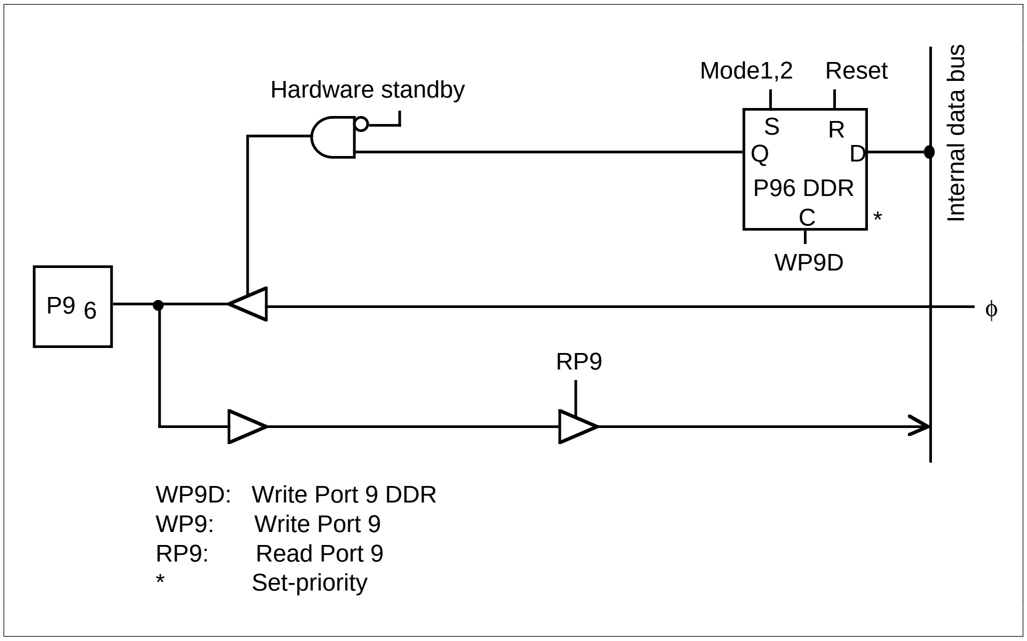


Figure 5-25 Port 9 Schematic Diagram (Pin $P9_6$)

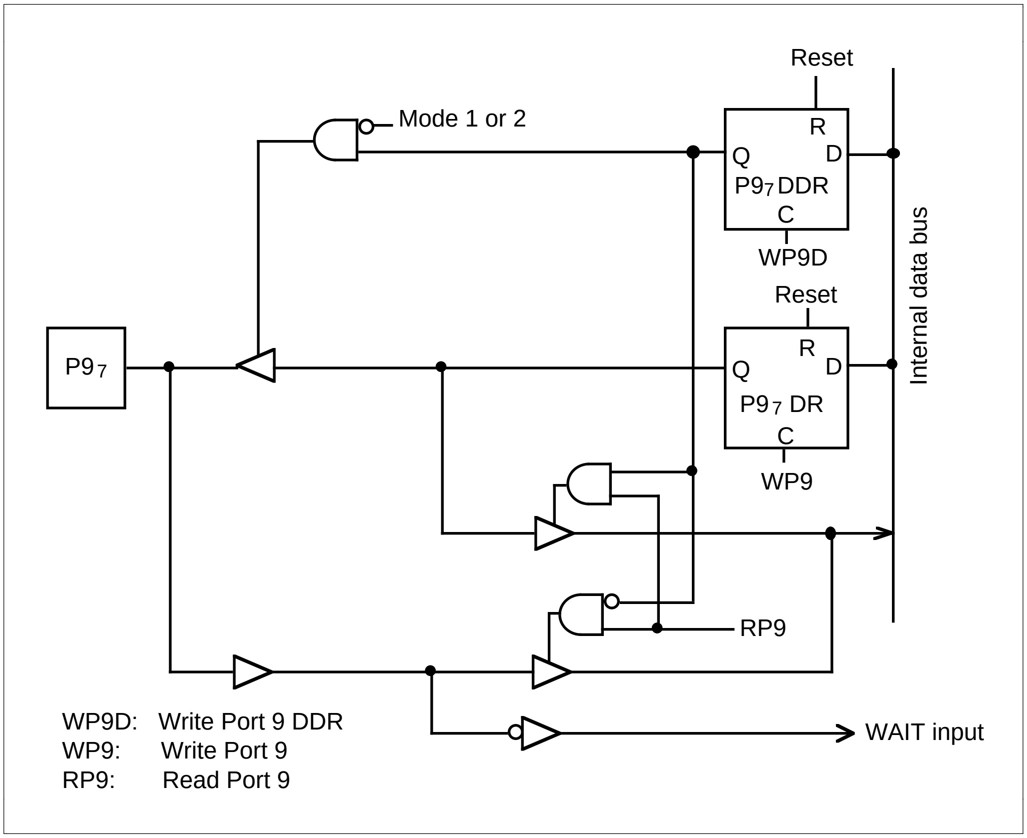


Figure 5-26 Port 9 Schematic Diagram (Pin $P9_7$)

Section 6 16-Bit Free-Running Timer

6.1 Overview

The H8/3332 has an on-chip 16-bit free-running timer (FRT) module that uses a 16-bit free-running counter as a time base. Applications of the FRT module include rectangular-wave output (up to two independent waveforms), input pulse width measurement, and measurement of external clock periods.

6.1.1 Features

- Four selectable clock sources
  The free-running counter can be driven by an internal clock source (ϕ/2, ϕ/8, or ϕ/32), or an external clock input (enabling use as an external event counter)

- Two independent comparators
  Each comparator can generate an independent waveform

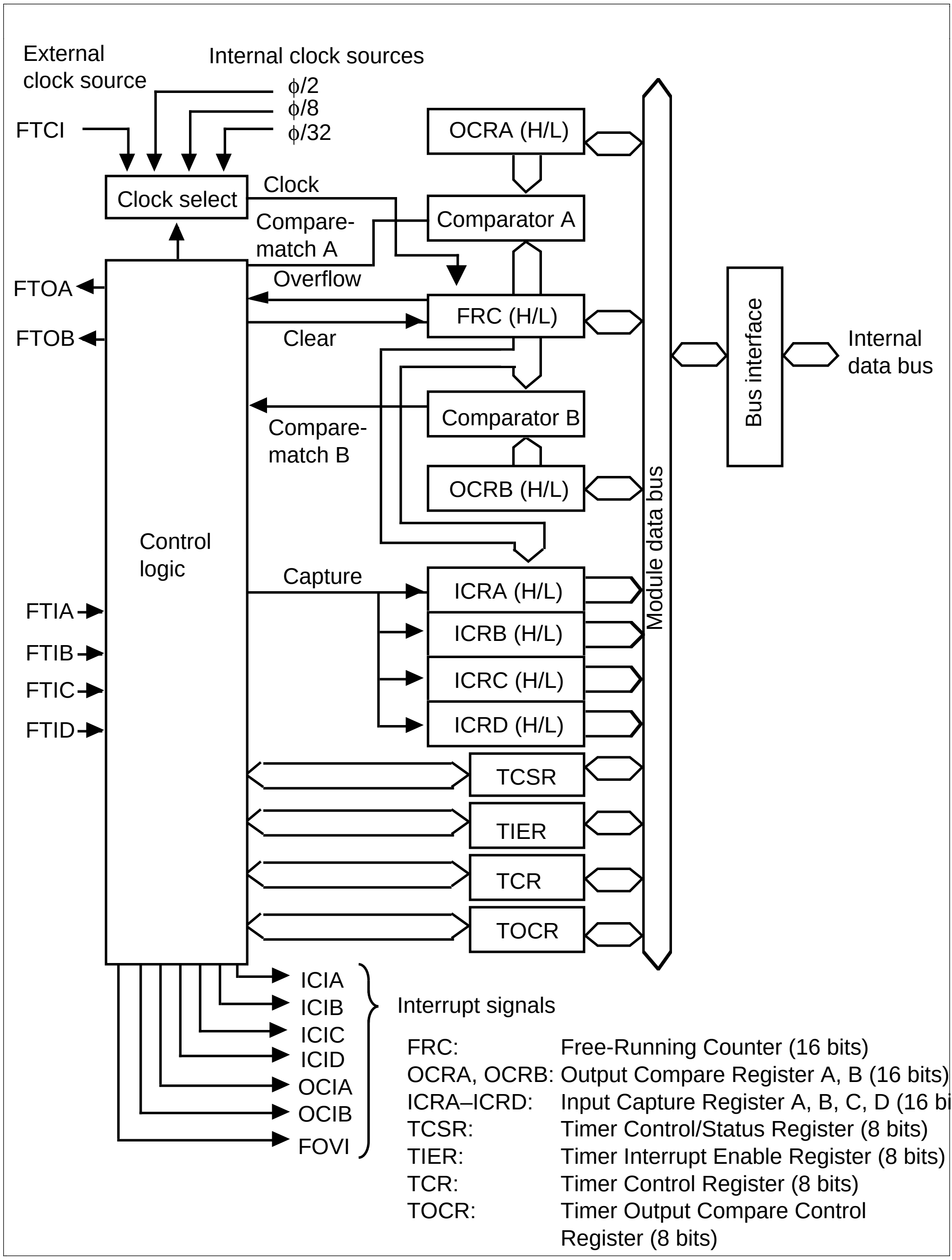
- Four input capture channels
  — The current count can be captured on the rising or falling edge (selectable) of an input signal
  — The four input capture registers can be used separately, or in a buffer mode

- Counter can be cleared under program control
  The free-running counters can be cleared on compare-match A

- Seven independent interrupts
  Compare-match A and B, input capture A to D, and overflow interrupts are requested independently

6.1.2 Block Diagram

Figure 6-1 shows a block diagram of the free-running timer.



FRC:	Free-Running Counter (16 bits)
OCRA, OCRB:	Output Compare Register A, B (16 bits)
ICRA–ICRD:	Input Capture Register A, B, C, D (16 bits)
TCSR:	Timer Control/Status Register (8 bits)
TIER:	Timer Interrupt Enable Register (8 bits)
TCR:	Timer Control Register (8 bits)
TOCR:	Timer Output Compare Control Register (8 bits)

Figure 6-1 Block Diagram of 16-Bit Free-Running Timer

6.1.3 Input and Output Pins

Table 6-1 lists the input and output pins of the free-running timer module.

Table 6-1 Input and Output Pins of Free-Running Timer Module

Name	Abbreviation	I/O	Function
Counter clock input	FTCI	Input	Input of external free-running counter clock signal
Output compare A	FTOA	Output	Output controlled by comparator A
Output compare B	FTOB	Output	Output controlled by comparator B
Input capture A	FTIA	Input	Trigger for capturing current count into input capture register A
Input capture B	FTIB	Input	Trigger for capturing current count into input capture register B
Input capture C	FTIC	Input	Trigger for capturing current count into input capture register C
Input capture D	FTID	Input	Trigger for capturing current count into input capture register D

6.1.4 Register Configuration

Table 6-2 lists the registers of the free-running timer module.

Table 6-2 Register Configuration

Name	Abbreviation	R/W	Initial Value	Address
Timer interrupt enable register	TIER	R/W	H'01	H'FF90
Timer control/status register	TCSR	R/(W) Note 1	H'00	H'FF91
Free-running counter (high)	FRC (H)	R/W	H'00	H'FF92
Free-running counter (low)	FRC (L)	R/W	H'00	H'FF93
Output compare register A/B (high) Note 2	OCRA/B (H)	R/W	H'FF	H'FF94
Output compare register A/B (low) Note 2	OCRA/B (L)	R/W	H'FF	H'FF95
Timer control register	TCR	R/W	H'00	H'FF96
Timer output compare control register	TOCR	R/W	H'E0	H'FF97
Input capture register A (high)	ICRA (H)	R	H'00	H'FF98
Input capture register A (low)	ICRA (L)	R	H'00	H'FF99
Input capture register B (high)	ICRB (H)	R	H'00	H'FF9A
Input capture register B (low)	ICRB (L)	R	H'00	H'FF9B
Input capture register C (high)	ICRC (H)	R	H'00	H'FF9C
Input capture register C (low)	ICRC (L)	R	H'00	H'FF9D
Input capture register D (high)	ICRD (H)	R	H'00	H'FF9E
Input capture register D (low)	ICRD (L)	R	H'00	H'FF9F

Notes: 1. Software can write a 0 to clear bits 7 to 1, but cannot write a 1 in these bits.

2. OCRA and OCRB share the same addresses. Access is controlled by the OCRS bit in TOCR.

6.2 Register Descriptions

6.2.1 Free-Running Counter (FRC)—H'FF92

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The FRC is a 16-bit read/write incrementing register that increments on an internal pulse generated from a clock source. The clock source is selected by the clock select 1 and 0 bits (CKS1 and CKS0) of the timer control register (TCR).

When the FRC overflows from H'FFFF to H'0000, the overflow flag (OVF) in the timer control/status register (TCSR) is set to 1.

Because the FRC is a 16-bit register, a temporary register (TEMP) is used when the FRC is written or read. See section 6.3, CPU Interface, for details.

The FRC is initialized to H'0000 at a reset and in the standby modes. It can also be cleared by compare-match A.

6.2.2 Output Compare Registers A and B (OCRA and OCRB)—H'FF94

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OCRA and OCRB are 16-bit read/write registers. Their contents are continually compared with the value in the FRC. When a match is detected, the corresponding output compare flag (OCFA or OCFB) is set in the timer control/status register (TCSR).

In addition, if the output enable bit (OEA or OEB) in the timer output compare control register (TOCR) is set to 1, when the output compare register and FRC values match, the logic level selected by the output level bit (OLVLA or OLVLB) in the TOCR is output at the output compare pin (FTOA or FTOB).

OCRA and OCRB share the same address. They are differentiated by the OCRS bit in the TOCR. A temporary register (TEMP) is used for write access, as explained in section 6.3, CPU Interface.

OCRA and OCRB are initialized to H'FFFF at a reset and in the standby modes.

6.2.3 Input Capture Registers A to D (ICRA to ICRD)

—H'FF98, H'FF9A, H'FF9C, H'FF9E

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/ Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Each input capture register is a 16-bit read-only register.

When the rising or falling edge of the signal at an input capture pin (FTIA to FTID) is detected, the current value of the FRC is copied to the corresponding input capture register (ICRA to ICRD). (The FRC contents are transferred to the input capture register regardless of the value of the input capture flag (ICFA to ICFD).) At the same time, the corresponding input capture flag (ICFA to ICFD) in the timer control/status register (TCSR) is set to 1. The input capture edge is selected by the input edge select bits (IEDGA to IEDGD) in the timer control register (TCR).

Input capture can be buffered by using the input capture registers in pairs. When the BUFEA bit in the timer control register (TCR) is set to 1, ICRC is used as a buffer register for ICRA as shown in figure 6-2. When an FTIA input is received, the old ICRA contents are moved into ICRC, and the new FRC count is copied into ICRA.

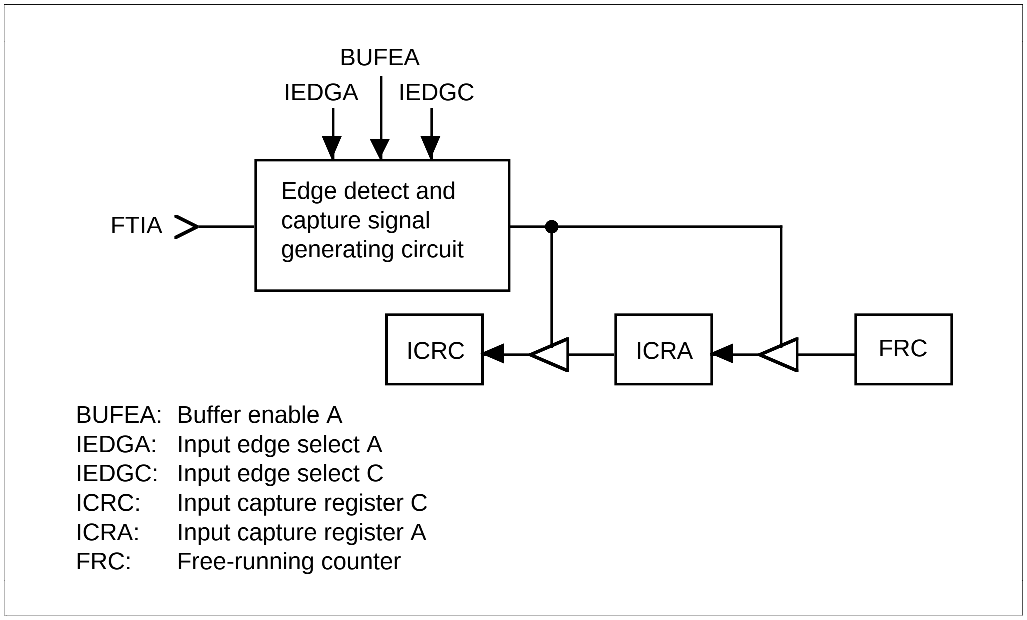

BUFEA
IEDGA
IEDGC
FTIA
Edge detect and capture signal generating circuit
ICRC
ICRA
FRC
BUFEA: Buffer enable A
IEDGA: Input edge select A
IEDGC: Input edge select C
ICRC: Input capture register C
ICRA: Input capture register A
FRC: Free-running counter

Figure 6-2 Input Capture Buffering

Similarly, when the BUFEB bit in TIER is set to 1, ICRD is used as a buffer register for ICRB.

When input capture is buffered, if the two input edge bits are set to different values (IEDGA ≠ IEDGC or IEDGB ≠ IEDGD), then input capture is triggered on both the rising and falling edges of the FTIA or FTIB input signal. If the two input edge bits are set to the same value (IEDGA = IEDGC or IEDGB = IEDGD), then input capture is triggered on only one edge (table 6-3).

Table 6-3 Buffered Input Capture Edge Selection (Example)

IEDGA	IEDGC	Input Capture Edge
0	0	Captured on falling edge of input capture A (FTIA) (Initial value)
0	1	Captured on both rising and falling edges of input capture A (FTIA)
1	0	
1	1	Captured on rising edge of input capture A (FTIA)

Because the input capture registers are 16-bit registers, a temporary register (TEMP) is used when they are read. See section 6.3, CPU Interface, for details.

To ensure input capture, the width of the input capture pulse (FTIA, FTIB, FTIC, FTID) should be at least 1.5 system clock periods (1.5ϕ). When triggering is enabled on both edges, the input capture pulse width should be at least 2.5 system clock periods (figure 6-3).

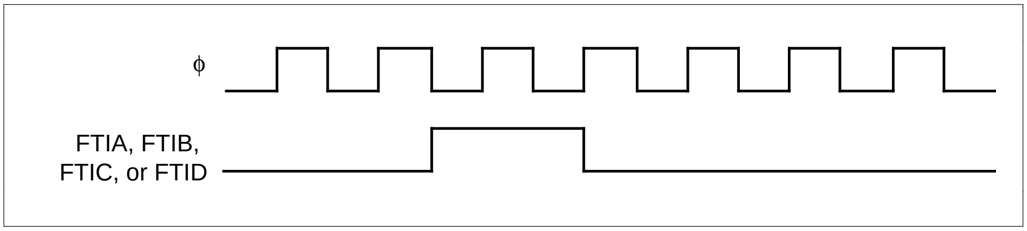


Figure 6-3 Minimum Input Capture Pulse Width

The input capture registers are initialized to H'0000 at a reset and in the standby modes.

Note: When input capture is detected, the FRC value is transferred to the input capture register even if the input capture flag is already set.

6.2.4 Timer Interrupt Enable Register (TIER)—H'FF90

Bit	7	6	5	4	3	2	1	0
	ICIAE	ICIBE	ICICE	ICIDE	OCIAE	OCIBE	OVIE	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

The TIER is an 8-bit read/write register that enables and disables interrupts.

The TIER is initialized to H'01 (all interrupts disabled) at a reset and in the standby modes.

Bit 7: Input Capture Interrupt A Enable (ICIAE): Selects whether to request input capture interrupt A (ICIA) when input capture flag A (ICFA) in the timer status/control register (TCSR) is set to 1.

Bit 7: ICIAE	Description	
0	Input capture interrupt request A (ICIA) is disabled	(Initial value)
1	Input capture interrupt request A (ICIA) is enabled	

Bit 6: Input Capture Interrupt B Enable (ICIBE): Selects whether to request input capture interrupt B (ICIB) when input capture flag B (ICFB) in the timer status/control register (TCSR) is set to 1.

Bit 6: ICIBE	Description	
0	Input capture interrupt request B (ICIB) is disabled	(Initial value)
1	Input capture interrupt request B (ICIB) is enabled	

Bit 5: Input Capture Interrupt C Enable (ICICE): Selects whether to request input capture interrupt C (ICIC) when input capture flag C (ICFC) in the timer status/control register (TCSR) is set to 1.

Bit 5: ICICE	Description	
0	Input capture interrupt request C (ICIC) is disabled	(Initial value)
1	Input capture interrupt request C (ICIC) is enabled	

Bit 4: Input Capture Interrupt D Enable (ICIDE): Selects whether to request input capture interrupt D (ICID) when input capture flag D (ICFD) in the timer status/control register (TCSR) is set to 1.

Bit 4: ICIDE	Description	
0	Input capture interrupt request D (ICID) is disabled	(Initial value)
1	Input capture interrupt request D (ICID) is enabled	

Bit 3: Output Compare Interrupt A Enable (OCIAE): Selects whether to request output compare interrupt A (OCIA) when output compare flag A (OCFA) in the timer status/control register (TCSR) is set to 1.

Bit 3: OCIAE	Description	
0	Output compare interrupt request A (OCIA) is disabled	(Initial value)
1	Output compare interrupt request A (OCIA) is enabled	

Bit 2: Output Compare Interrupt B Enable (OCIBE): Selects whether to request output compare interrupt B (OCIB) when output compare flag B (OCFB) in the timer status/control register (TCSR) is set to 1.

Bit 2: OCIBE	Description
0	Output compare interrupt request B (OCIB) is disabled (Initial value)
1	Output compare interrupt request B (OCIB) is enabled

Bit 1: Timer overflow Interrupt Enable (OVIE): Selects whether to request a free-running timer overflow interrupt (FOVI) when the timer overflow flag (OVF) in the timer status/control register (TCSR) is set to 1.

Bit 1: OVIE	Description
0	Timer overflow interrupt request (FOVI) is disabled (Initial value)
1	Timer overflow interrupt request (FOVI) is enabled

Bit 0: Reserved: This bit cannot be modified and is always read as 1.

6.2.5 Timer Control/Status Register (TCSR)—H'FF91

Bit	7	6	5	4	3	2	1	0
	ICFA	ICFB	ICFC	ICFD	OCFA	OCFB	OVF	CCLRA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/W

Note: *: Software can write a 0 in bits 7 to 1 to clear the flags, but cannot write a 1 in these bits.

The TCSR is an 8-bit readable and partially writeable register. It contains seven interrupt flags and specifies whether to clear the counter on compare-match A (when the FRC and OCRA values match).

The TCSR is initialized to H'00 at a reset and in the standby modes.

Bit 7: Input Capture Flag A (ICFA): The ICFA status bit is set to 1 to flag an input capture A event. If BUFEA = 0, ICFA indicates that the FRC value has been copied to ICRA. If BUFEA = 1, ICFA indicates that the old ICRA value has been moved into ICRC and the new FRC value has been copied to ICRA.

ICFA must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 7: ICFA	Description
0	To clear ICFA, the CPU must read ICFA after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when an FTIA input signal causes the FRC value to be copied to ICRA

Bit 6: Input Capture Flag B (ICFB): The ICFB status bit is set to 1 to flag an input capture B event. If BUFEB = 0, ICFB indicates that the FRC value has been copied to ICRB. If BUFEB = 1, ICFB indicates that the old ICRB value has been moved into ICRD and the new FRC value has been copied to ICRB.

ICFB must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 6: ICFB	Description
0	To clear ICFB, the CPU must read ICFB after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when an FTIB input signal causes the FRC value to be copied to ICRB

Bit 5: Input Capture Flag C (ICFC): The ICFC status bit is set to 1 to flag input of a rising or falling edge of FTIC as selected by the IEDGC bit. When BUFEA = 0, this indicates capture of the FRC count in ICRC. When BUFEA = 1, however, the FRC count is not captured, so ICFC becomes simply an external interrupt flag. In other words, the buffer mode frees FTIC for use as a general-purpose interrupt signal (which can be enabled or disabled by the ICICE bit).

ICFC must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 5: ICFC	Description
0	To clear ICFC, the CPU must read ICFC after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when an FTIC input signal is received

Bit 4: Input Capture Flag D (ICFD): The ICFD status bit is set to 1 to flag the input of a rising or falling edge of FTID as selected by the IEDGD bit. When BUFEB = 0, this indicates capture of the FRC count in ICRD. When BUFEB = 1, however, the FRC count is not captured, so ICFD becomes simply an external interrupt flag. In other words, the buffer mode frees FTID for use as a general-purpose interrupt signal (that can be enabled or disabled by the ICIDE bit).

ICFD must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 4: ICFD	Description
0	To clear ICFD, the CPU must read ICFD after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when an FTID input signal is received

Bit 3: Output Compare Flag A (OCFA): Set to 1 when the FRC value matches the OCRA value. The OCFA flag must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 3: OCFA	Description
0	To clear OCFA, the CPU must read OCFA after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when FRC = OCRA

Bit 2: Output Compare Flag B (OCFB): Set to 1 when the FRC value matches the OCRB value. The OCFB flag must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 2: OCFB	Description
0	To clear OCFB, the CPU must read OCFB after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when FRC = OCRB

Bit 1: Timer Overflow Flag (OVF): Set to 1 when the FRC overflows (changes from H'FFFF to H'0000). The OVF flag must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 1: OVF	Description
0	To clear OVF, the CPU must read OVF after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when FRC changes from H'FFFF to H'0000

Bit 0: Counter Clear A (CCLRA): Selects whether to clear the FRC at compare-match A (when the FRC and OCRA values match).

Bit 0: CCLRA	Description
0	FRC not cleared (Initial value)
1	FRC cleared at compare-match A

6.2.6 Timer Control Register (TCR)—H'FF96

Bit	7	6	5	4	3	2	1	0
	IEDGA	IEDGB	IEDGC	IEDGD	BUFEA	BUFEB	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The TCR is an 8-bit read/write register that selects the rising or falling edge of the input capture signals, enables the input capture buffer mode, and selects the FRC clock source.

The TCR is initialized to H'00 at a reset and in the standby modes.

Bit 7: Input Edge Select A (IEDGA): Causes input capture A events to be recognized on the selected edge of the input capture A signal (FTIA).

Bit 7: IEDGA	Description
0	Input capture A events are recognized on the falling edge of FTIA (Initial value)
1	Input capture A events are recognized on the rising edge of FTIA

Bit 6: Input Edge Select B (IEDGB): Causes input capture B events to be recognized on the selected edge of the input capture B signal (FTIB).

Bit 6: IEDGB	Description
0	Input capture B events are recognized on the falling edge of FTIB (Initial value)
1	Input capture B events are recognized on the rising edge of FTIB

Bit 5: Input Edge Select C (IEDGC): Causes input capture C events to be recognized on the selected edge of the input capture C signal (FTIC). In buffer mode (when BUFEA = 1), it also causes input capture A events to be recognized on the selected edge of FTIA.

Bit 5: IEDGC	Description
0	Input capture C events are recognized on the falling edge of FTIC (Initial value)
1	Input capture C events are recognized on the rising edge of FTIC

Bit 4: Input Edge Select D (IEDGD): Causes input capture D events to be recognized on the selected edge of the input capture D signal (FTID). In the buffer mode (when BUFEB = 1), it also causes input capture B events to be recognized on the selected edge of FTIB.

Bit 4: IEDGD	Description
0	Input capture D events are recognized on the falling edge of FTID (Initial value)
1	Input capture D events are recognized on the rising edge of FTID

Bit 3: Buffer Enable A (BUFEA): Selects whether to use ICRC as a buffer register for ICRA.

Bit 3: BUFEA	Description	
0	ICRC is used for input capture C	(Initial value)
1	ICRC is used as a buffer register for input capture A and input C is not captured	

Bit 2: Buffer Enable B (BUFEB): Selects whether to use ICRD as a buffer register for ICRB.

Bit 2: BUFEB	Description	
0	ICRD is used for input capture D	(Initial value)
1	ICRD is used as a buffer register for input capture B and input D is not captured	

Bits 1 and 0: Clock Select (CKS1 and CKS0): Select external clock input or one of three internal clock sources for the FRC. External clock pulses are counted on the rising edge.

Bit 1: CKS1	Bit 0: CKS0	Description	
0	0	ϕ/2 Internal clock source	(Initial value)
0	1	ϕ/8 Internal clock source	
1	0	ϕ/32 Internal clock source	
1	1	External clock source (rising edge)	

6.2.7 Timer Output Compare Control Register (TOCR)—H'FF97

Bit	7	6	5	4	3	2	1	0
	—	—	—	OCRS	OEA	OEB	OLVLA	OLVLB
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

The TOCR is an 8-bit read/write register that controls the output compare function. Selects the output compare output level, enables output compare output, and controls the switching of access to output compare registers A and B.

The TOCR is initialized to H'E0 at a reset and in the standby modes.

Bits 7 to 5: Reserved: Cannot be modified and are always read as 1.

Bit 4: Output Compare Register Select (OCRS): When the CPU accesses addresses H'FF94 and H'FF95, OCRS directs the access to either OCRA or OCRB. These two registers share the same addresses as follows:

- Upper byte of OCRA and upper byte of OCRB: H'FF94
- Lower byte of OCRA and lower byte of OCRB: H'FF95

Bit 4: OCRS	Description
0	The CPU can access OCRA (Initial value)
1	The CPU can access OCRB

Bit 3: Output Enable A (OEA): Enables or disables output of the output compare A signal (FTOA). When output compare A is disabled, the corresponding pin is used as a general-purpose input/output port.

Bit 3: OEA	Description
0	Output compare A output is disabled (Initial value)
1	Output compare A output is enabled

Bit 2: Output Enable B (OEB): Enables or disables output of the output compare B signal (FTOB). When output compare B is disabled, the corresponding pin is used as a general-purpose input/output or interrupt port.

Bit 2: OEB	Description
0	Output compare B output is disabled (Initial value)
1	Output compare B output is enabled

Bit 1: Output Level A (OLVLA): Selects the logic level to be output at the FTOA pin when the FRC and OCRA values match.

Bit 1: OLVLA	Description
0	Logic level 0 (low) is output for compare-match A (Initial value)
1	Logic level 1 (high) is output for compare-match A

Bit 0: Output Level B (OLVLB): Selects the logic level to be output at the FTOB pin when the FRC and OCRB values match.

Bit 0: OLVLB	Description
0	Logic level 0 (low) is output for compare-match B (Initial value)
1	Logic level 1 (high) is output for compare-match B

6.3 CPU Interface

The free-running counter (FRC), output compare registers (OCRA and OCRB), and input capture registers (ICRA to ICRD) are 16-bit registers, but they are connected to an 8-bit data bus. When the CPU accesses these registers, to ensure that both bytes are written or read simultaneously, the access is performed using an 8-bit temporary register (TEMP).

These registers are written and read as follows:

- Register write

  When the CPU writes to the upper byte, the byte of write data is placed in TEMP. Next, when the CPU writes to the lower byte, this byte of data is combined with the byte in TEMP and all 16 bits are written in the register simultaneously.

- Register read

  When the CPU reads the upper byte, the upper byte of data is sent to the CPU and the lower byte is placed in TEMP. When the CPU reads the lower byte, it receives the value in TEMP.

  (As an exception, when the CPU reads OCRA or OCRB, it reads both the upper and lower bytes directly, without using TEMP.)

Programs that access these registers should normally use word access. Equivalently, they may access first the upper byte, then the lower byte by two consecutive byte accesses. Data will not be transferred correctly if the bytes are accessed in reverse order, if only one byte is accessed, or if the upper and lower bytes are accessed separately and another register is accessed in between, altering the value in TEMP.

6.3.1 Coding Examples

- To write the contents of general register R0 to OCRA: `MOV.W R0, @OCRA`

- To transfer the contents of ICRA to general register R0: `MOV.W @ICRA, R0`

Figures 6-4 and 6-5 show the data flow when the FRC is accessed. The other registers are accessed in the same way.

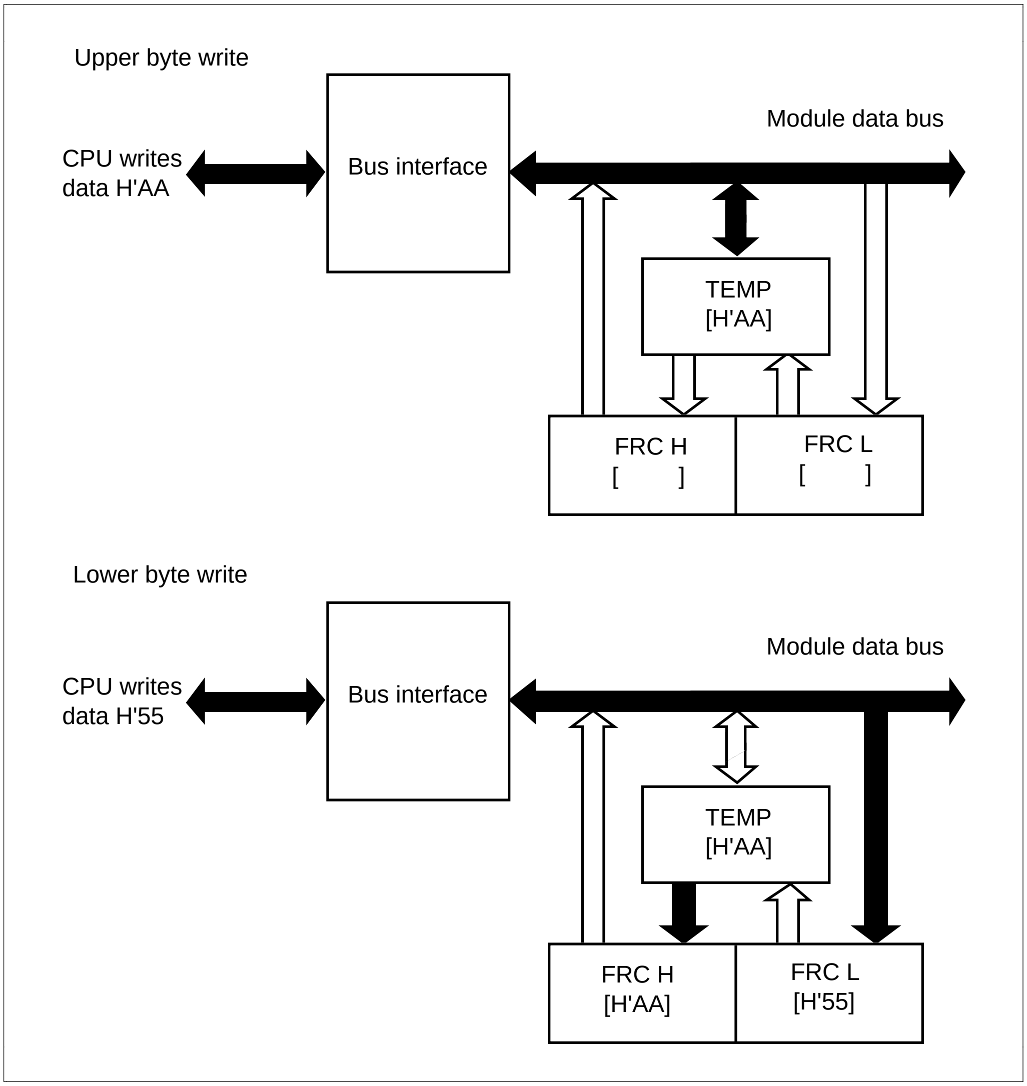


Figure 6-4 Write Access to FRC (When CPU Writes H'AA55)

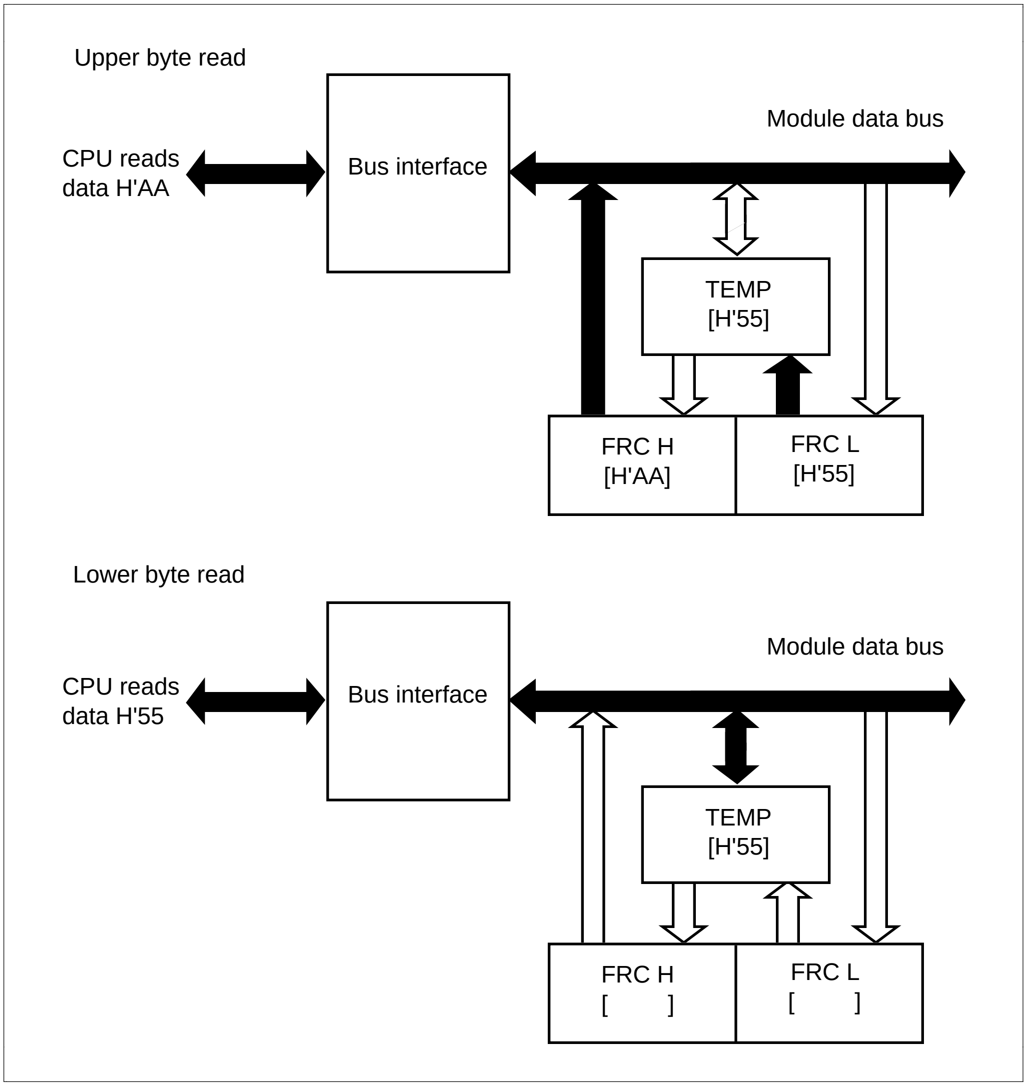


Figure 6-5 Read Access to FRC (When FRC Contains H'AA55)

6.4 Operation

6.4.1 FRC Increment Timing

The FRC increments on a pulse generated once for each period of the selected (internal or external) clock source. The clock source is selected by bits CKS0 and CKS1 in TCR.

Internal Clock: The internal clock sources (ϕ/2, ϕ/8, ϕ/32) are created from the system clock (ϕ) by a prescaler. The FRC increments on a pulse generated from the falling edge of the prescaler output. See figure 6-6.

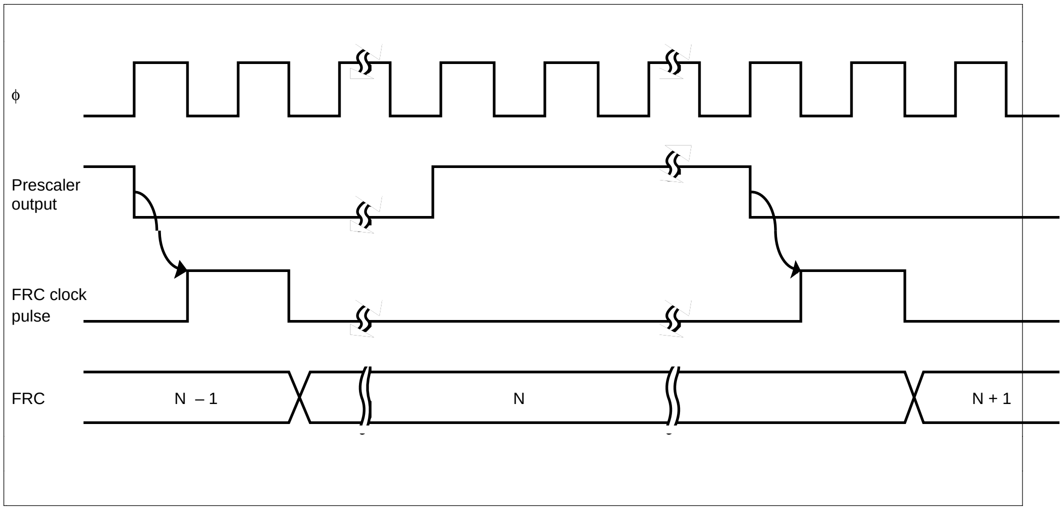


Figure 6-6 Increment Timing for Internal Clock Source

External Clock: If external clock input is selected, the FRC increments on the rising edge of the FTCI clock signal. Figure 6-7 shows the increment timing.

The pulse width of the external clock signal must be at least 1.5 system clock (φ) periods (figure 6-8). The counter will not increment correctly if the pulse width is shorter than 1.5 system clock periods.

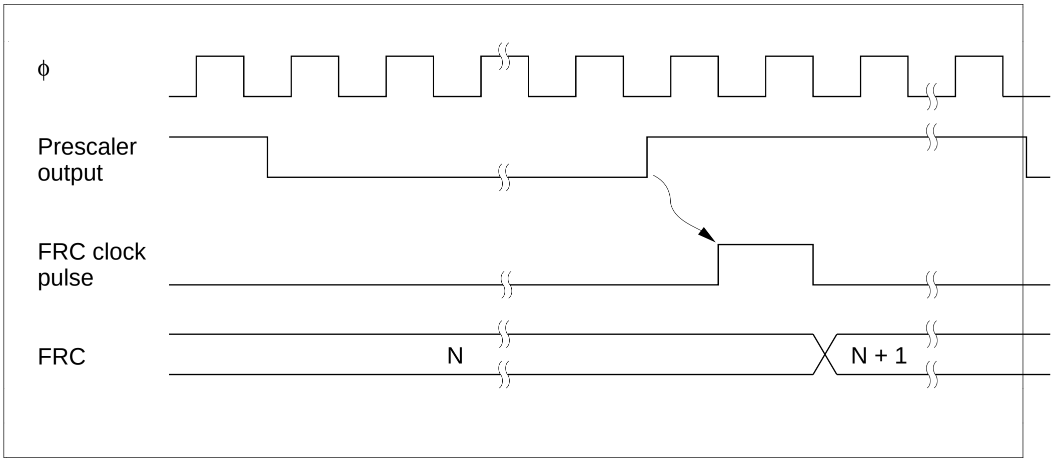


Figure 6-7 Increment Timing for External Clock Source

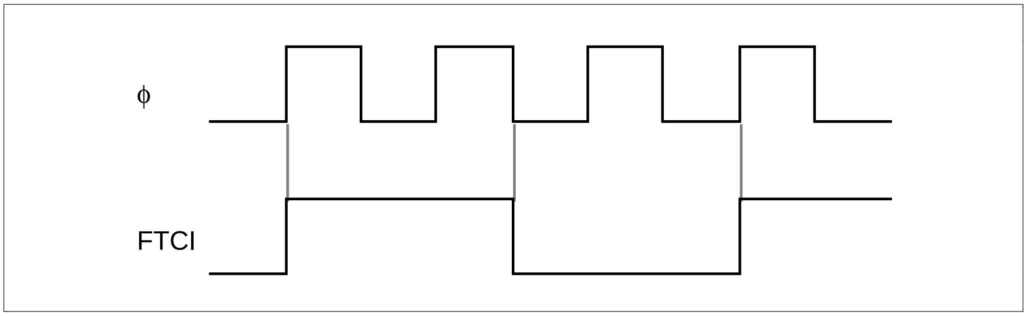


Figure 6-8 Minimum External Clock Pulse Width

6.4.2 Output Compare Timing

Setting the Output Compare Flags A and B (OCFA and OCFB): The output compare flags are set to 1 by an internal compare-match signal generated when the FRC value matches the OCRA or OCRB value. This compare-match signal is generated at the last state in which the two values match, just before the FRC increments to a new value.

Accordingly, when the FRC and OCR values match, the compare-match signal is not generated until the next period of the clock source. Figure 6-9 shows the timing of the setting of the output compare flags.

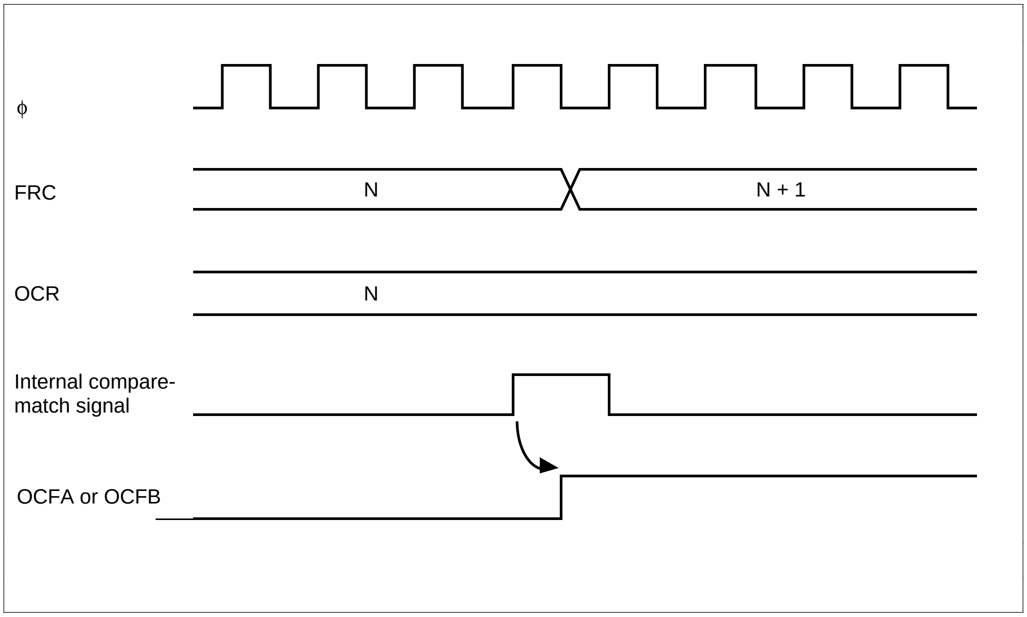


Figure 6-9 Setting the Output Compare Flags

Output Timing: When a compare-match occurs, the logic level selected by the output level bit (OLVLA or OLVLB) in TOCR is output at the output compare pin (FTOA or FTOB). Figure 6-10 shows the timing of this operation for compare-match A.

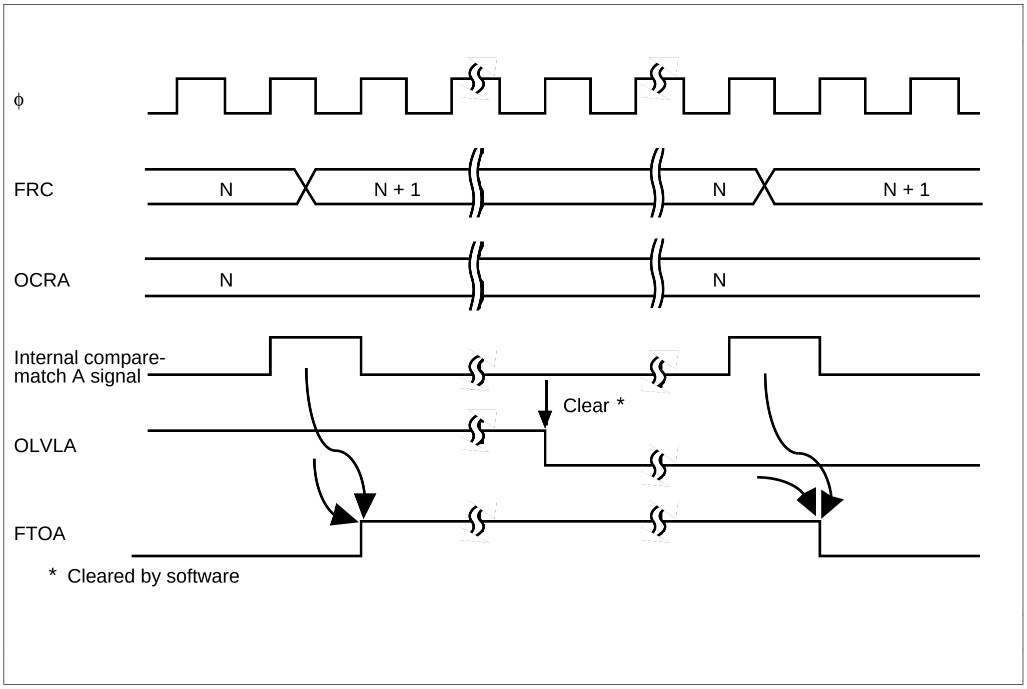


Figure 6-10 Timing of Output Compare A

FRC Clear Timing: If the CCLRA bit in the TCSR is set to 1, the FRC is cleared when compare-match A occurs. Figure 6-11 shows the timing of this operation.

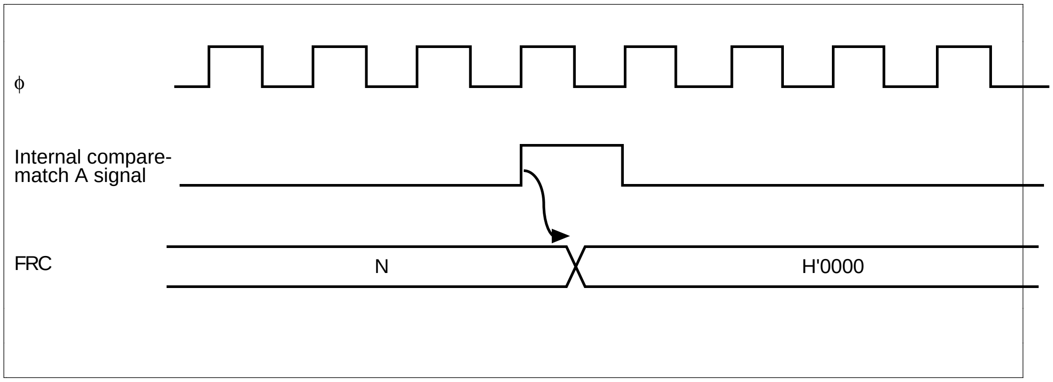


Figure 6-11 Compare-Match A Clears FRC

6.4.3 Input Capture Timing

Input Capture Timing: An internal input capture signal is generated from the rising or falling edge of the signal at the input capture pin FTIx (x = A, B, C, D), as selected by the corresponding IEDGx bit in TCR. Figure 6-12 shows the usual input capture timing when the rising edge is selected (IEDGx = 1).

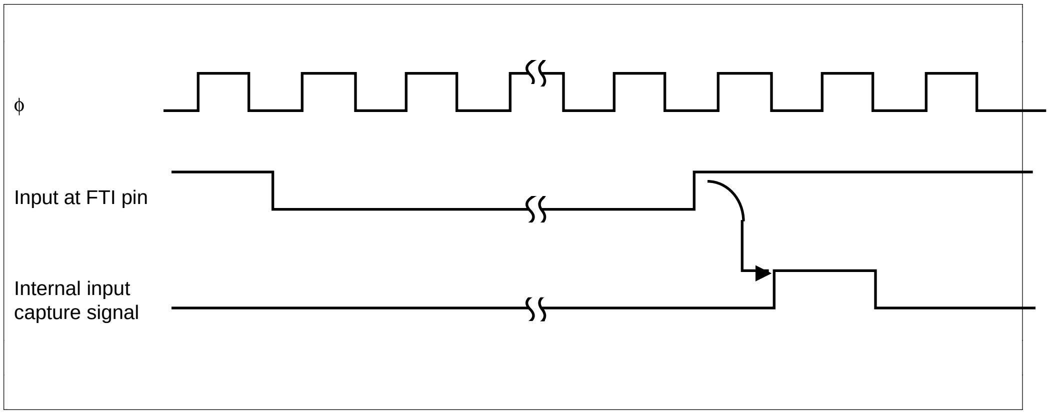


Figure 6-12 Input Capture Timing (Normal Case)

If the upper byte of ICRA/B/C/D is being read when the corresponding input capture signal arrives, the internal input capture signal is delayed by one state. Figure 6-13 shows the timing for this case.

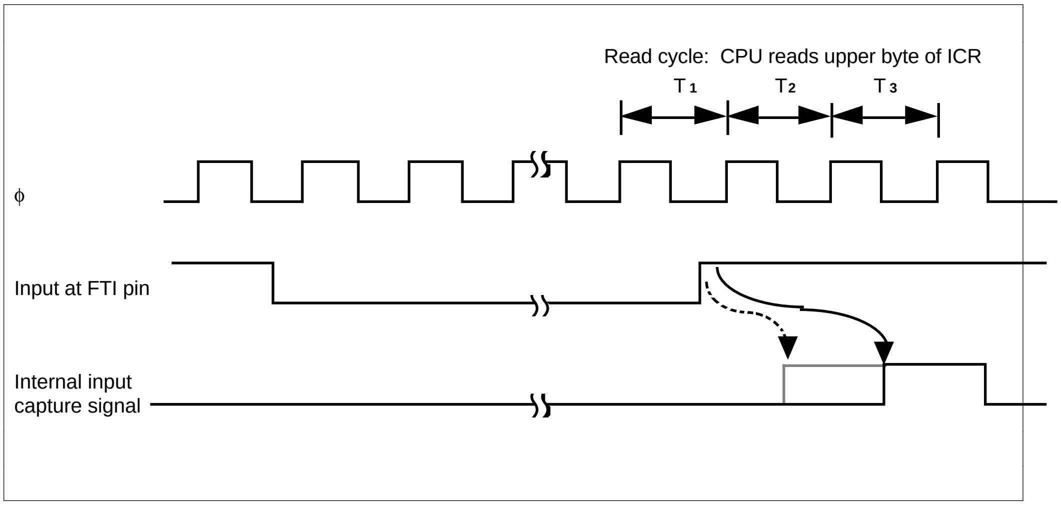

Read cycle: CPU reads upper byte of ICR
T1
T2
T3
φ
Input at FTI pin
Internal input capture signal

Figure 6-13 Input Capture Timing (1-State Delay)

In buffer mode, this delay occurs if the CPU is reading either of the two registers concerned. When ICRA and ICRC are used in buffer mode, for example, if the upper byte of either ICRA or ICRC is being read when the FTIA input arrives, the internal input capture signal is delayed by one state. Figure 6-14 shows the timing for this case. The case of ICRB and ICRD is similar.

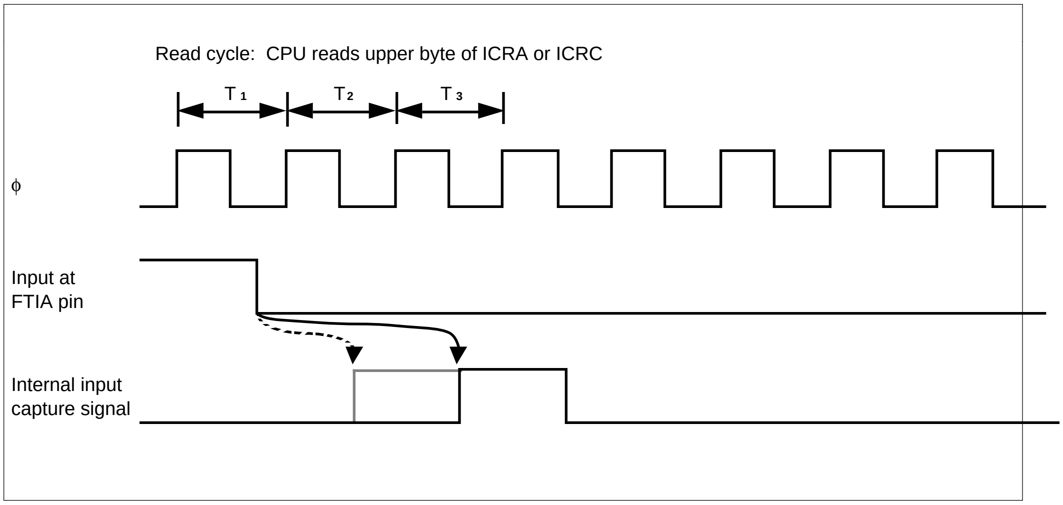

Read cycle: CPU reads upper byte of ICRA or ICRC
T1
T2
T3
ϕ
Input at FTIA pin
Internal input capture signal

Figure 6-14 Input Capture Timing (1-State Delay, Buffer Mode)

Figure 6-15 shows how input capture operates when ICRA and ICRC are used in buffer mode and IEDGA and IEDGC are set to different values (IEDGA = 0 and IEDGC = 1, or IEDGA = 1 and IEDGC = 0), so that input capture is performed on both the rising and falling edges of FTIA.

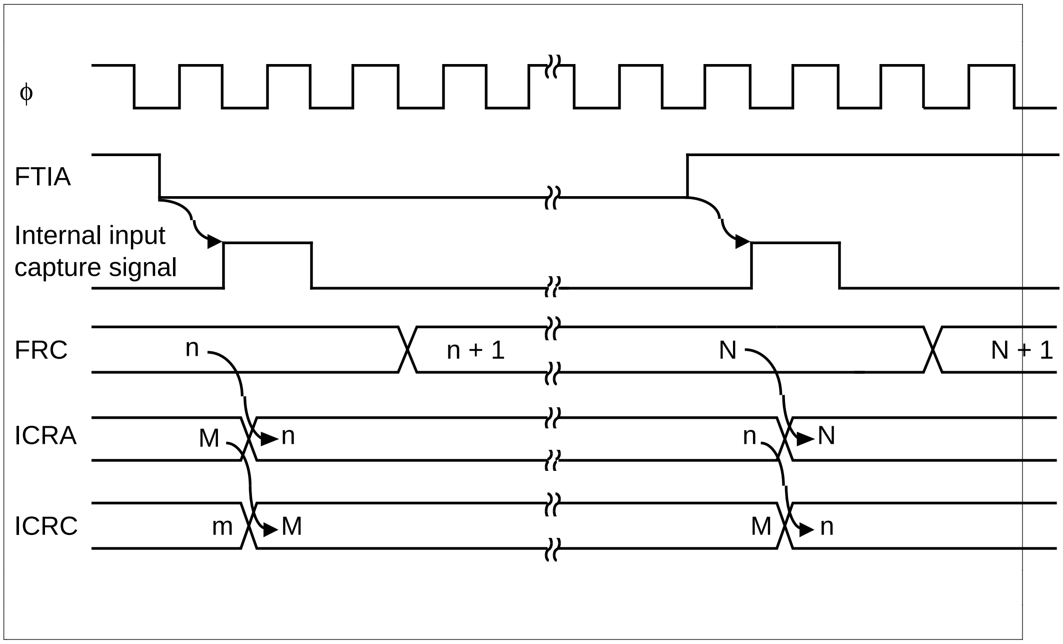


Figure 6-15 Buffered Input Capture with Both Edges Selected

In this mode, FTIC does not cause the FRC contents to be copied to ICRC. However, input capture flag C still sets on the edge of FTIC selected by IEDGC, and if the interrupt enable bit (ICICE) is set, a CPU interrupt is requested.

The situation when ICRB and ICRD are used in buffer mode is similar.

Timing of Input Capture Flag (ICF) Setting: The input capture flag ICFx (x = A, B, C, D) is set to 1 by the internal input capture signal. Figure 6-16 shows the timing of this operation.

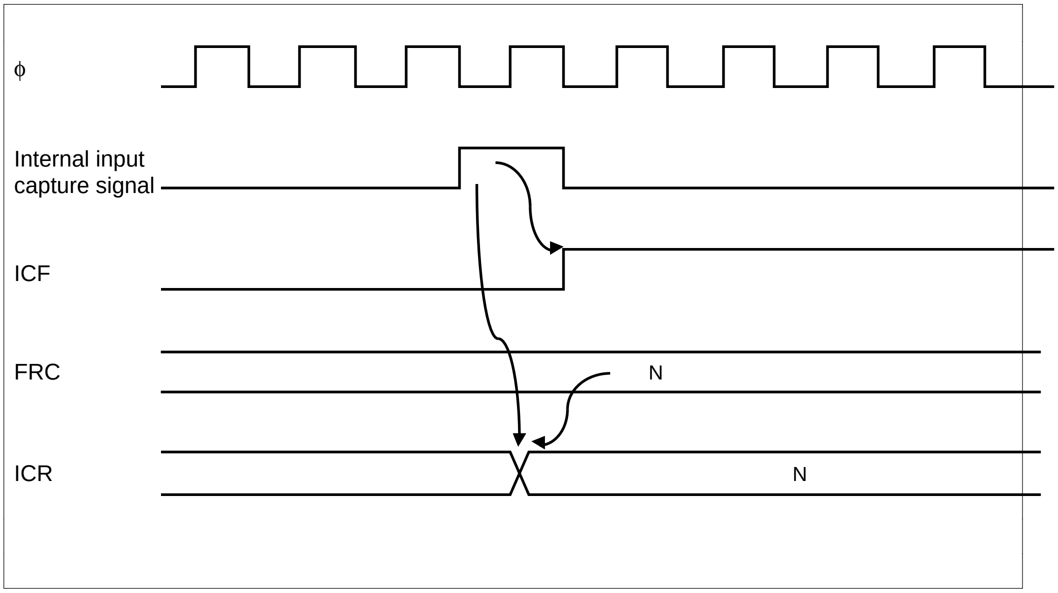


Figure 6-16 Setting the Input Capture Flag

6.4.4 Setting the FRC Overflow Flag (OVF)

The FRC overflow flag (OVF) is set to 1 when the FRC overflows (changes from H'FFFF to H'0000). Figure 6-17 shows the timing of this operation.

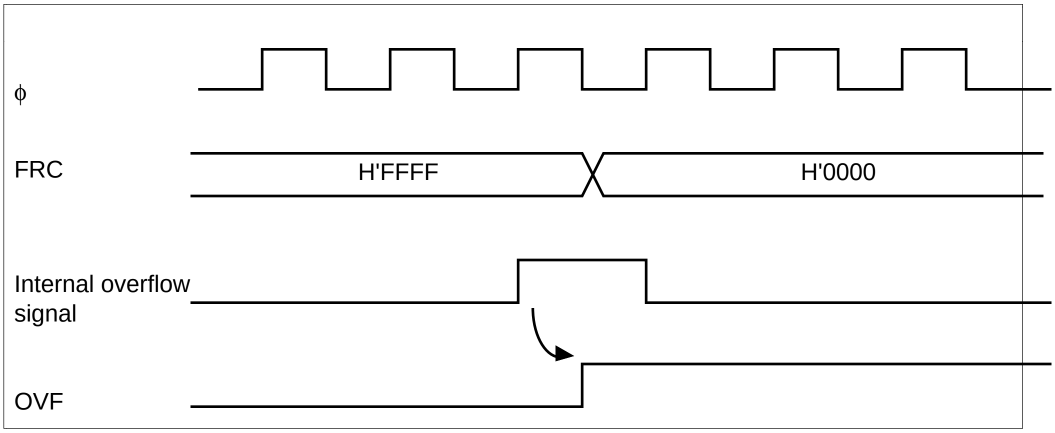


Figure 6-17 Setting the Overflow Flag (OVF)

6.5 Interrupts

The free-running timer channel can request seven types of interrupts: input capture A to D (ICIA, ICIB, ICIC, ICID), output compare A and B (OCIA and OCIB), and overflow (FOVI). Each interrupt is requested when the corresponding enable and flag bits are set. Independent signals are sent to the interrupt controller for each type of interrupt. Table 6-4 lists information about these interrupts.

Table 6-4 Free-Running Timer Interrupts

Interrupt	Description	Priority
ICIA	Requested when ICFA and ICIAE are set	High
ICIB	Requested when ICFB and ICIBE are set	↑
ICIC	Requested when ICFC and ICICE are set	
ICID	Requested when ICFD and ICIDE are set	
OCIA	Requested when OCFA and OCIAE are set	
OCIB	Requested when OCFB and OCIBE are set	↓
FOVI	Requested when OVF and OVIE are set	Low

6.6 Sample Application

In the example below, the free-running timer channel generates two square-wave outputs with a 50% duty factor and arbitrary phase relationship (figure 6-18). The programming is as follows:

1. The CCLRA bit in the TCSR is set to 1.

2. Each time a compare-match interrupt occurs, software inverts the corresponding output level bit in TOCR (OLVLA or OLVLB).

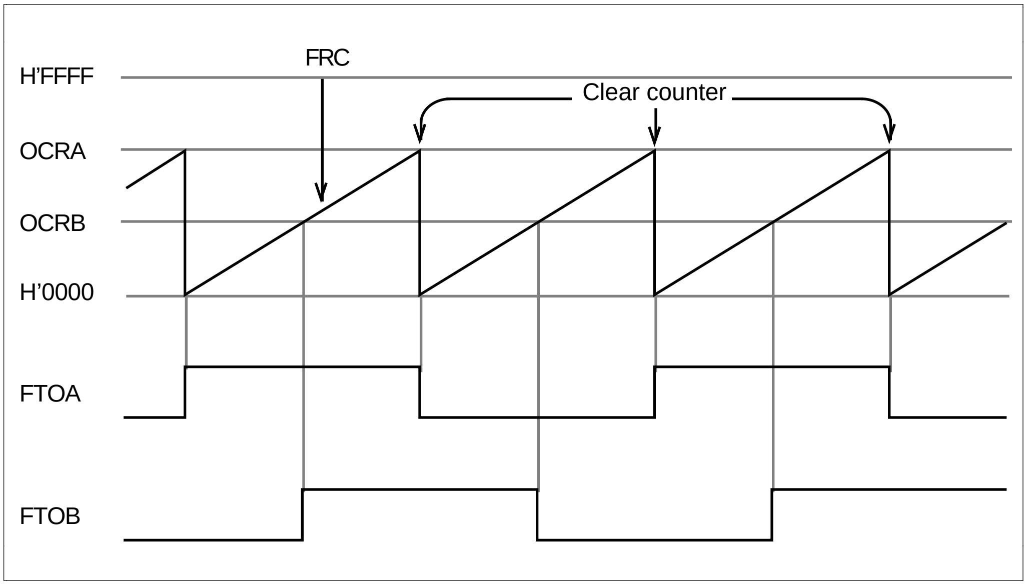


Figure 6-18 Square-Wave Output (Example)

6.7 Application Notes

Application programmers should note that the following types of contention can occur in the free-running timers.

6.7.1 Contention between FRC Write and Clear

If an internal counter clear signal is generated during the T3 state of a write cycle to the lower byte of the free-running counter, the clear signal takes priority and the write is not performed.

Figure 6-19 shows this type of contention.

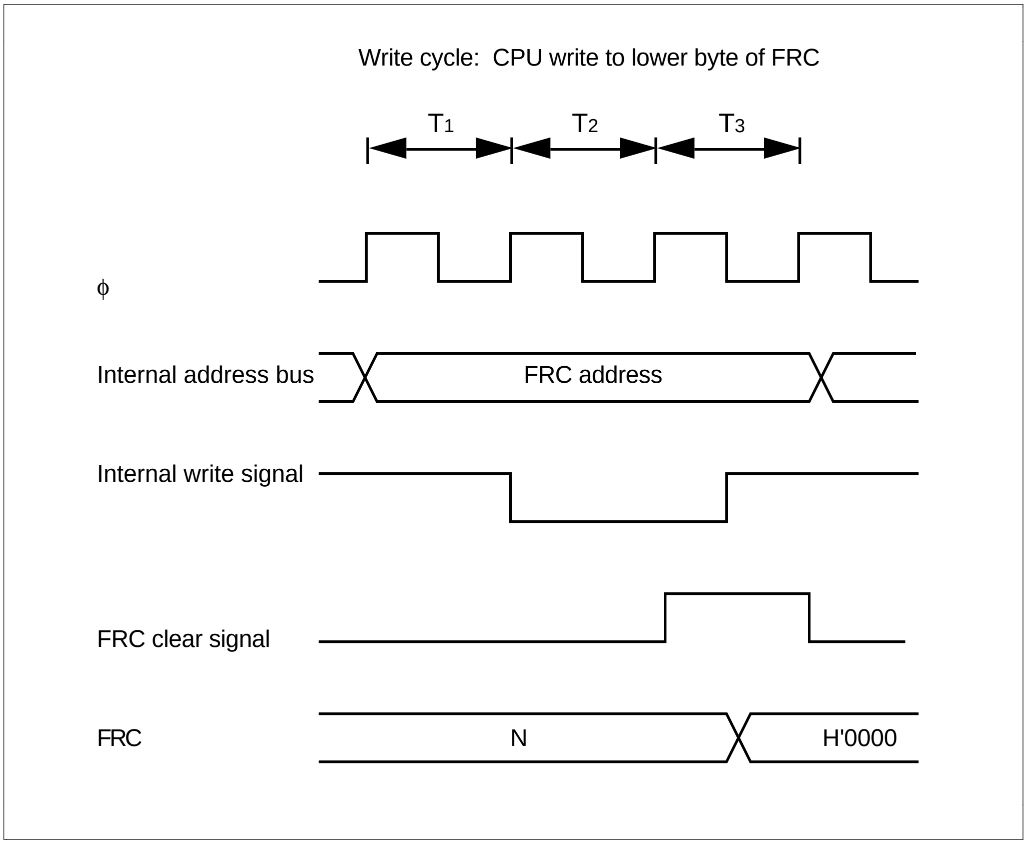


Figure 6-19   FRC Write-Clear Contention

6.7.2 Contention between FRC Write and Increment

If an FRC increment pulse is generated during the T3 state of a write cycle to the lower byte of the free-running counter, the write takes priority and the FRC is not incremented.

Figure 6-20 shows this type of contention.

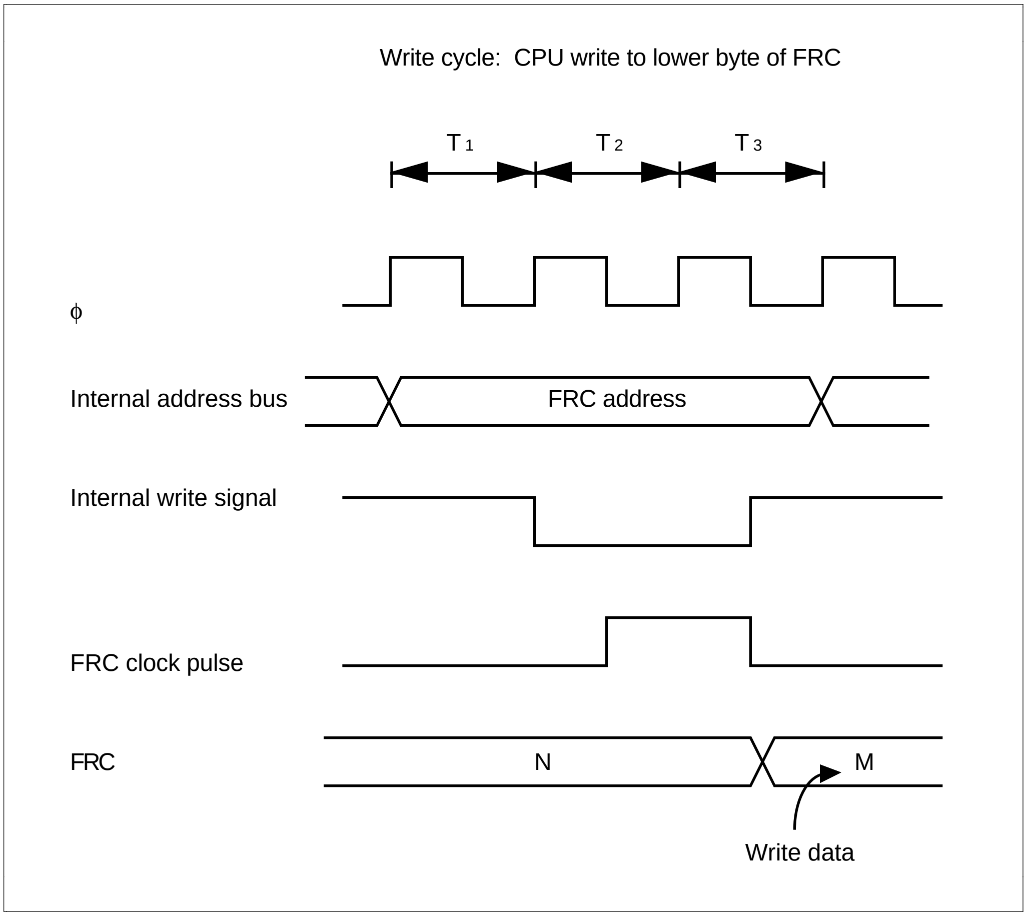


Figure 6-20 FRC Write-Increment Contention

6.7.3 Contention between OCR Write and Compare-Match

If a compare-match occurs during the T3 state of a write cycle to the lower byte of OCRA or OCRB, the write takes precedence and the compare-match signal is inhibited.

Figure 6-21 shows this type of contention.

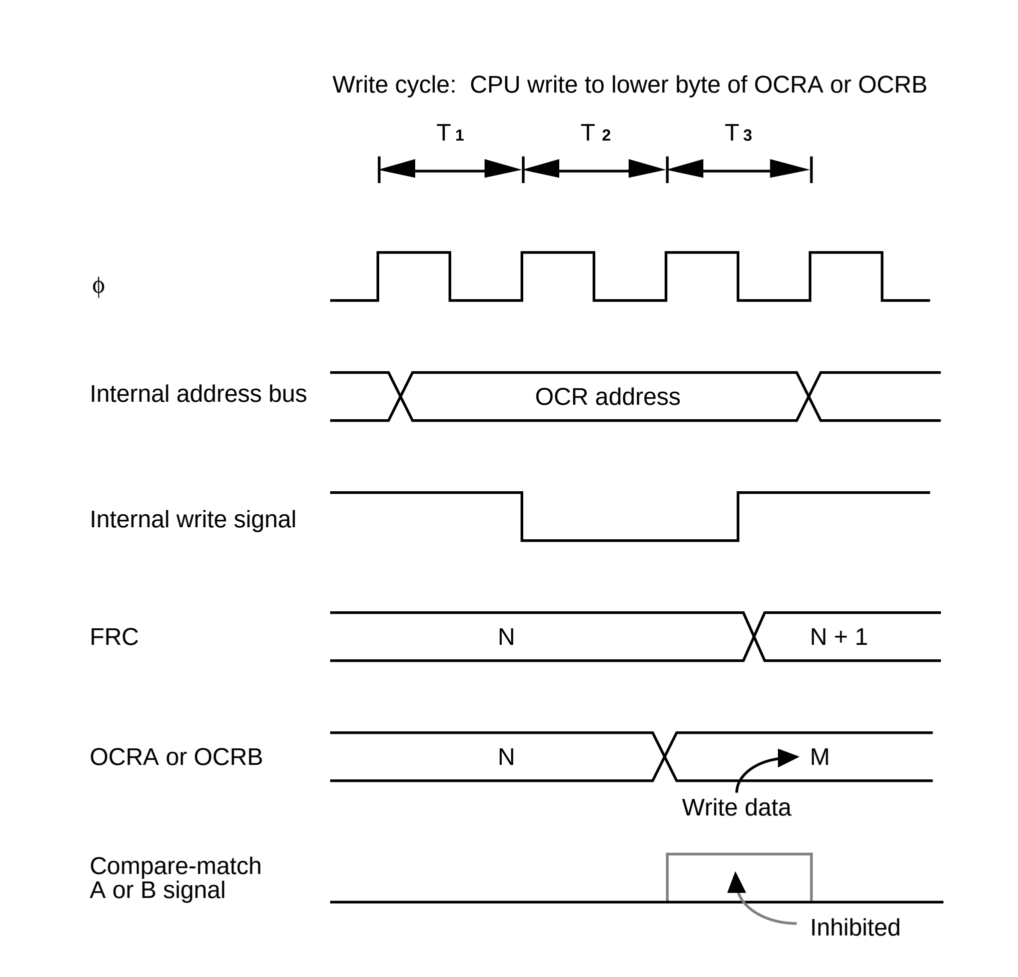


Figure 6-21 Contention between OCR Write and Compare-Match

6.7.4 Increment Caused by Changing of Internal Clock Source

When an internal clock source is changed, the changeover may cause the FRC to increment. This depends on the time at which the clock select bits (CKS1 and CKS0) are rewritten, as shown in table 6-4.

The pulse that increments the FRC is generated at the falling edge of the internal clock source. If clock sources are changed when the old source is high and the new source is low, as in case No. 3 in table 6-5, the changeover generates a falling edge that triggers the FRC increment clock pulse.

Switching between an internal and external clock source can also cause the FRC to increment.

Table 6-5 Effect of Changing Internal Clock Sources

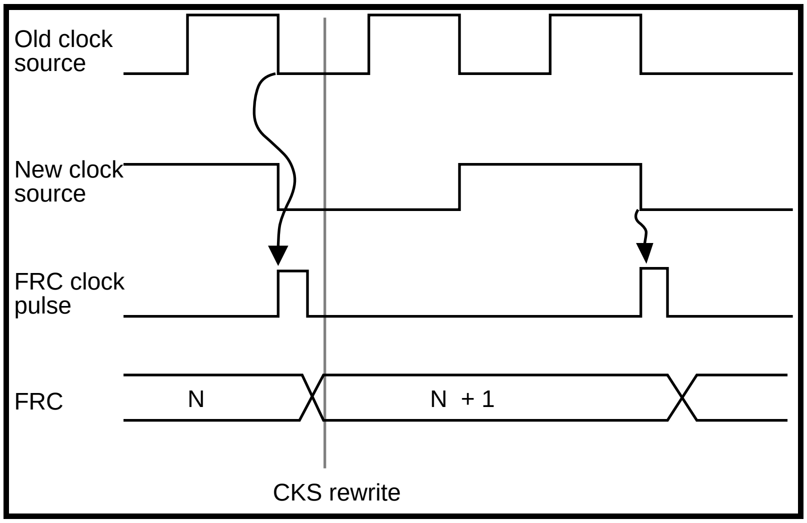
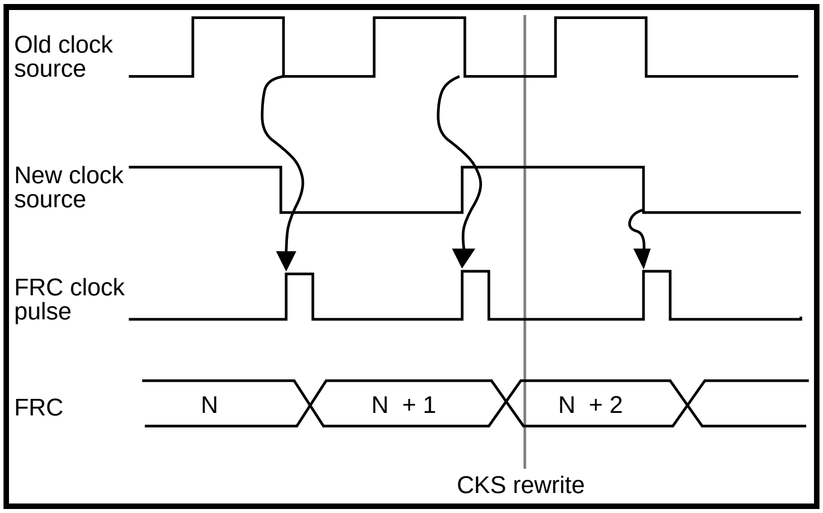
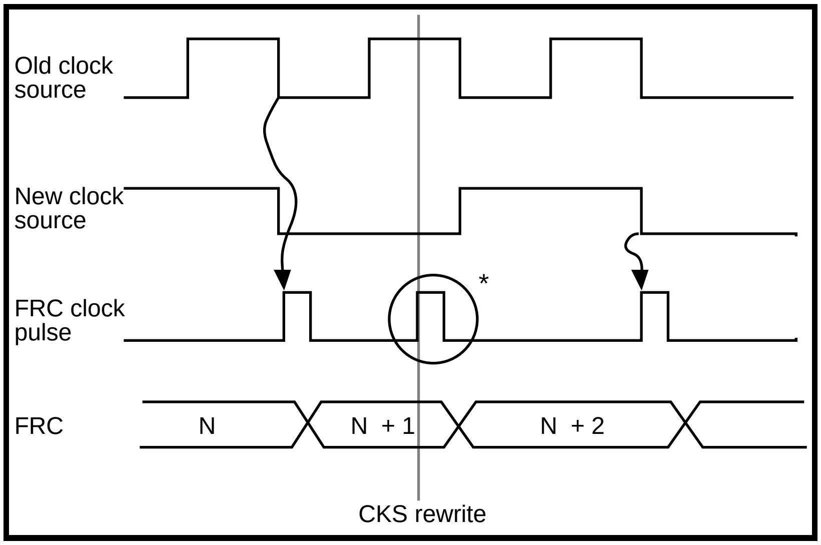
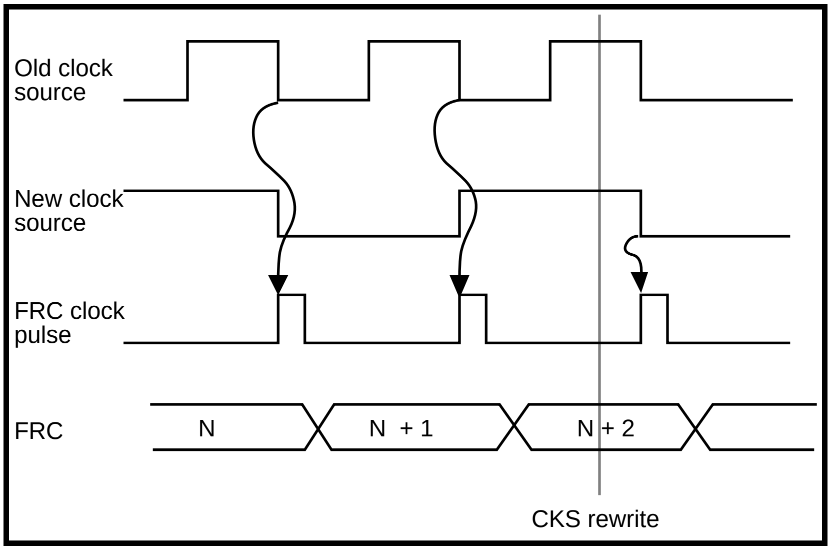
No.	Description	Timing chart
1	Low → low: CKS1 and CKS0 are rewritten while both clock sources are low.	 Old clock source New clock source FRC clock pulse FRC N N + 1 CKS rewrite
2	Low → high: CKS1 and CKS0 are rewritten while old clock source is low and new clock source is high.	 Old clock source New clock source FRC clock pulse FRC N N + 1 N + 2 CKS rewrite

Table 6-5 Effect of Changing Internal Clock Sources (cont)

No.	Description	Timing chart
3	High → low: CKS1 and CKS0 are rewritten while old clock source is high and new clock source is low.	 Old clock source New clock source FRC clock pulse * FRC N N + 1 N + 2 CKS rewrite
4	High → high: CKS1 and CKS0 are rewritten while both clock sources are high.	 Old clock source New clock source FRC clock pulse FRC N N + 1 N + 2 CKS rewrite

* The switching of clock sources is regarded as a falling edge that increments the FRC.

Section 7 8-Bit Timers

7.1 Overview

The H8/3332 includes an 8-bit timer module with two channels (TMR0 and TMR1). Each channel has an 8-bit counter (TCNT) and two time constant registers (TCORA and TCORB). TCORA and TCORB are constantly compared with the TCNT value to detect compare-match events. One application of the 8-bit timer module is to generate a rectangular-wave output with an arbitrary duty factor.

7.1.1 Features

- Seven selectable clock sources
  The counters can be driven by one of six internal clock signals or an external clock input (enabling use as an external event counter).

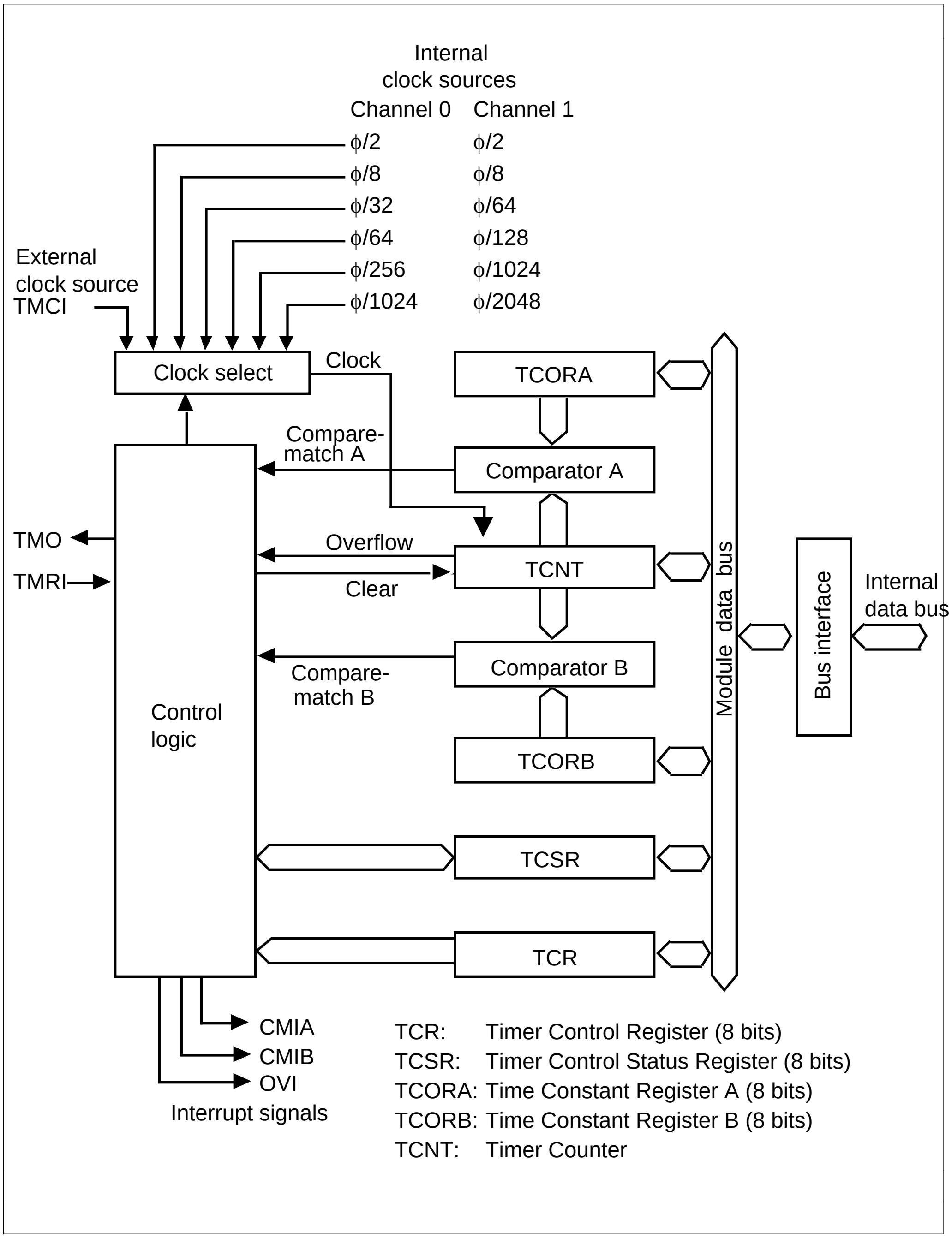
- Three selectable ways to clear the counters
  The counters can be cleared on compare-match A or B, or by an external reset signal.

- Timer output controlled by two time constants
  The timer output signal in each channel is controlled by two independent time constants, enabling the timer to generate output waveforms with an arbitrary duty factor.

- Three independent interrupts
  Compare-match A and B and overflow interrupts can be requested independently.

7.1.2 Block Diagram

Figure 7-1 shows a block diagram of one channel in the 8-bit timer module. The other channel is identical.



TCR: Timer Control Register (8 bits)
TCSR: Timer Control Status Register (8 bits)
TCORA: Time Constant Register A (8 bits)
TCORB: Time Constant Register B (8 bits)
TCNT: Timer Counter

Figure 7-1 Block Diagram of 8-Bit Timer

7.1.3 Input and Output Pins

Table 7-1 lists the input and output pins of the 8-bit timer.

Table 7-1 Input and Output Pins of 8-Bit Timer

	Abbreviation			
Name	**TMR0**	**TMR1**	**I/O**	**Function**
Timer output	TMO$_0$	TMO$_1$	Output	Output controlled by compare-match
Timer clock input	TMCI$_0$	TMCI$_1$	Input	External clock source for the counter
Timer reset input	TMRI$_0$	TMRI$_1$	Input	External reset signal for the counter

7.1.4 Register Configuration

Table 7-2 lists the registers of the 8-bit timer module. Each channel has an independent set of registers.

Table 7-2 8-Bit Timer Registers

				Address	
Name	**Abbreviation**	**R/W**	**Initial Value**	**TMR0**	**TMR1**
Timer control register	TCR	R/W	H'00	H'FFC8	H'FFD0
Timer control/status register	TCSR	R/(W) (Note)	H'10	H'FFC9	H'FFD1
Timer constant register A	TCORA	R/W	H'FF	H'FFCA	H'FFD2
Timer constant register B	TCORB	R/W	H'FF	H'FFCB	H'FFD3
Timer counter	TCNT	R/W	H'00	H'FFCC	H'FFD4
Serial/timer control register	STCR	R/W	H'F8	H'FFC3	H'FFC3

Note: Software can write a 0 to clear bits 7 to 5, but cannot write a 1 in these bits.

7.2 Register Descriptions

7.2.1 Timer Counter (TCNT)—H'FFCC (TMR0), H'FFD4 (TMR1)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The timer counters (TCNT) are 8-bit incrementing registers that increment on a pulse generated from one of four clock sources. The clock source is selected by clock select bits 2–0

(CKS2–CKS0) of the timer control register (TCR). The CPU can always read or write the timer counter.

A timer counter can be cleared by an external reset input or by an internal compare-match signal generated at a compare-match event. Clock clear bits 1 and 0 (CCLR1 and CCLR0) of the timer control register select the method of clearing.

When a timer counter overflows from H'FF to H'00, the overflow flag (OVF) in the timer control/status register (TCSR) is set to 1.

The timer counters are initialized to H'00 at a reset and in the standby modes.

7.2.2 Time Constant Registers A and B (TCORA and TCORB)

—H'FFCA and H'FFCB (TMR0), H'FFD2 and H'FFD3 (TMR1)

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCORA and TCORB are 8-bit read/write registers. The timer count is continually compared with the constants written in these registers. When a match is detected, the corresponding compare-match flag (CMFA or CMFB) is set in the timer control/status register (TCSR).

The timer output signal (TMO0 or TMO1) is controlled by these compare-match signals as specified by output select bits 3 to 0 (OS3 to OS0) in the timer control/status register (TCSR).

TCORA and TCORB are initialized to H'FF at a reset and in the standby modes.

Compare-match is not detected during the T3 state of a write cycle to TCORA or TCORB. See section 7.6.3, Contention between TCOR Write and Compare-Match.

7.2.3 Timer Control Register (TCR)

—H'FFC8 (TMR0), H'FFD0 (TMR1)

Bit	7	6	5	4	3	2	1	0
	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Each TCR is an 8-bit read/write register that selects the clock source and the time at which the timer counter is cleared, and enables interrupts.

The TCRs are initialized to H'00 at a reset and in the standby modes.

For timing diagrams, see section 7.3, Operation.

Bit 7: Compare-Match Interrupt Enable B (CMIEB): Selects whether to request compare-match interrupt B (CMIB) when compare-match flag B (CMFB) in the timer control/status register (TCSR) is set to 1.

Bit 7: CMIEB	Description	
0	Compare-match interrupt request B (CMIB) is disabled	(Initial value)
1	Compare-match interrupt request B (CMIB) is enabled	

Bit 6: Compare-Match Interrupt Enable A (CMIEA): Selects whether to request compare-match interrupt A (CMIA) when compare-match flag A (CMFA) in the timer control/status register (TCSR) is set to 1.

Bit 6: CMIEA	Description	
0	Compare-match interrupt request A (CMIA) is disabled	(Initial value)
1	Compare-match interrupt request A (CMIA) is enabled	

Bit 5: Timer Overflow Interrupt Enable (OVIE): Selects whether to request a timer overflow interrupt (OVI) when the overflow flag (OVF) in the timer control/status register (TCSR) is set to 1.

Bit 5: OVIE	Description	
0	The timer overflow interrupt request (OVI) is disabled	(Initial value)
1	The timer overflow interrupt request (OVI) is enabled.	

Bits 4 and 3: Counter Clear 1 and 0 (CCLR1 and CCLR0): Select how the timer counter is cleared: by compare-match A or B or by an external reset input.

Bit 4: CCLR1	Bit 3: CCLR0	Description	
0	0	Not cleared	(Initial value)
0	1	Cleared on compare-match A	
1	0	Cleared on compare-match B	
1	1	Cleared on rising edge of external reset input signal	

Bits 2, 1, and 0: Clock Select (CKS2, CKS1, and CKS0): With ICKS1 and ICKS0 of the serial/timer control register, CKS2, CKS1, and CKS0 select the internal or external clock source for the timer counter. Six internal clock sources, derived by prescaling the system clock, are available for each timer channel. For the internal clock sources, the counter is incremented on the falling edge of the internal clock. For the external clock source, CKS2–

CKS0 select whether to increment the counter on the rising or falling edge of the clock input, or on both edges.

	TCR			STCR		Description	
Channel	Bit 2: CKS2	Bit 1: CKS1	Bit 0: CKS0	Bit 1: ICKS1	Bit 0: ICKS0	Clock Source	Counted on
0	0	0	0	—	—	No clock source (Initial value)	Timer stopped
	0	0	1	—	0	ϕ/8 Internal	Falling edge
	0	0	1	—	1	ϕ/2 Internal	Falling edge
	0	1	0	—	0	ϕ/64 Internal	Falling edge
	0	1	0	—	1	ϕ/32 Internal	Falling edge
	0	1	1	—	0	ϕ/1024 Internal	Falling edge
	0	1	1	—	1	ϕ/256 Internal	Falling edge
	1	0	0	—	—	No clock source	Timer stopped
	1	0	1	—	—	External	Rising edge
	1	1	0	—	—	External	Falling edge
	1	1	1	—	—	External	Both rising and falling edges
1	0	0	0	—	—	No clock source (Initial value)	Timer stopped
	0	0	1	0	—	ϕ/8 Internal	Falling edge
	0	0	1	1	—	ϕ/2 Internal	Falling edge
	0	1	0	0	—	ϕ/64 Internal	Falling edge
	0	1	0	1	—	ϕ/128 Internal	Falling edge
	0	1	1	0	—	ϕ/1024 Internal	Falling edge
	0	1	1	1	—	ϕ/2048 Internal	Falling edge
	1	0	0	—	—	No clock source	Timer stopped
	1	0	1	—	—	External	Rising edge
	1	1	0	—	—	External	Falling edge
	1	1	1	—	—	External	Both the rising and falling edges

7.2.4 Timer Control/Status Register (TCSR)

—H'FFC9 (TMR0), H'FFD1 (TMR1)

Bit	7	6	5	4	3	2	1	0
	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0
Initial value	0	0	0	1	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	—	R/W	R/W	R/W	R/W

Note: * Software can write a 0 in bits 7 to 5 to clear the flags, but cannot write a 1 in these bits.

The TCSR is an 8-bit readable and partially writeable register that indicates compare-match and overflow status and selects the effect of compare-match events on the timer output signal.

The TCSR is initialized to H'10 at a reset and in the standby modes.

Bit 7: Compare-Match Flag B (CMFB): Set to 1 when the timer count matches the time constant set in TCORB. CMFB must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 7: CMFB	Description
0	To clear CMFB, the CPU must read CMFB after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when TCNT = TCORB

Bit 6: Compare-Match Flag A (CMFA): Set to 1 when the timer count matches the time constant set in TCORA. CMFA must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 6: CMFA	Description
0	To clear CMFA, the CPU must read CMFA after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when TCNT = TCORA

Bit 5: Timer Overflow Flag (OVF): Set to 1 when the timer count overflows (changes from H'FF to H'00). OVF must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 5: OVF	Description
0	To clear OVF, the CPU must read OVF after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when TCNT changes from H'FF to H'00

Bit 4: Reserved: This bit is always read as 1. It cannot be written.

Bits 3 to 0: Output Select 3 to 0 (OS3 to OS0): Specify the effect of compare-match events on the timer output signal (TCOR or TCNT). Bits OS3 and OS2 control the effect of compare-match B on the output level. Bits OS1 and OS0 control the effect of compare-match A on the output level.

If compare-match A and B occur simultaneously, any conflict is resolved as explained in section 7.6.4, Contention between Compare-Match A and Compare-Match B.

After a reset, the timer output is 0 until the first compare-match event.

When all four output select bits are cleared to 0 the timer output signal is disabled.

Bit 3: OS3	**Bit 2: OS2**	**Description**
0	0	No change when compare-match B occurs (Initial value)
0	1	Output changes to 0 when compare-match B occurs
1	0	Output changes to 1 when compare-match B occurs
1	1	Output inverts (toggles) when compare-match B occurs

Bit 1: OS1	**Bit 0: OS0**	**Description**
0	0	No change when compare-match A occurs (Initial value)
0	1	Output changes to 0 when compare-match A occurs
1	0	Output changes to 1 when compare-match A occurs
1	1	Output inverts (toggles) when compare-match A occurs

7.2.5 Serial/Timer Control Register (STCR)—H'FFC3

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	—	—	—	—	—	MPE	ICKS1	ICKS0
Initial value	1	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	R/W	R/W	R/W

The STCR is an 8-bit read/write register that controls the serial communication interface and selects internal clock sources for the timer counters.

The STCR is initialized to H'F8 at a reset.

Bits 7–3: Reserved: Cannot be modified and are always read as 1.

Bit 2: Multiprocessor Enable (MPE): Controls the operating mode of serial communication interfaces 0 and 1. See section 9, Serial Communication Interface.

Bits 1 and 0: Internal Clock Source Select 1 and 0 (ICKS1 and ICKS0): With bits CKS2–CKS0 of the TCR, ICKS1 and ICKS0 select the clock sources for the timer counters. See section 7.2.3, Timer Control Register.

7.3 Operation

7.3.1 TCNT Increment Timing

The timer counter increments on a pulse generated once for each period of the clock source selected by bits CKS2 to CKS0 of the TCR.

Internal Clock: Internal clock sources are created from the system clock by a prescaler. The counter increments on an internal TCNT clock pulse generated from the falling edge of the prescaler output, as shown in figure 7-2. Bits CKS2 to CKS0 of the TCR and ICKS1 and ICKS0 of STCR can select one of the six internal clocks.

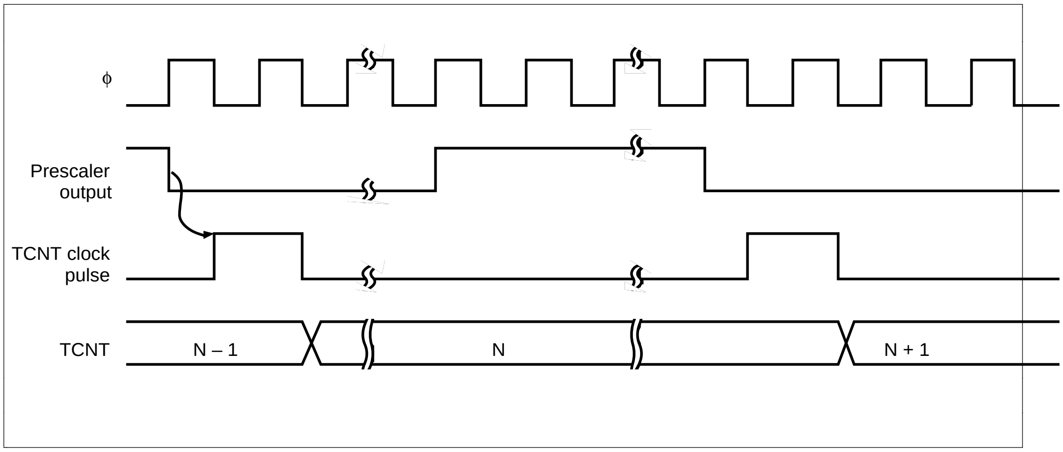


Figure 7-2 Count Timing for Internal Clock Input

External Clock: If external clock input (TMCI) is selected, the timer counter can increment on the rising edge, the falling edge, or both edges of the external clock signal. Figure 7-3 shows incrementing on both edges of the external clock signal.

The external clock pulse width must be at least 1.5 system clock periods for incrementing on a single edge, and at least 2.5 system clock periods for increment on both edges. See figure 7-4. The counter will not increment correctly if the pulse width is shorter than these values.

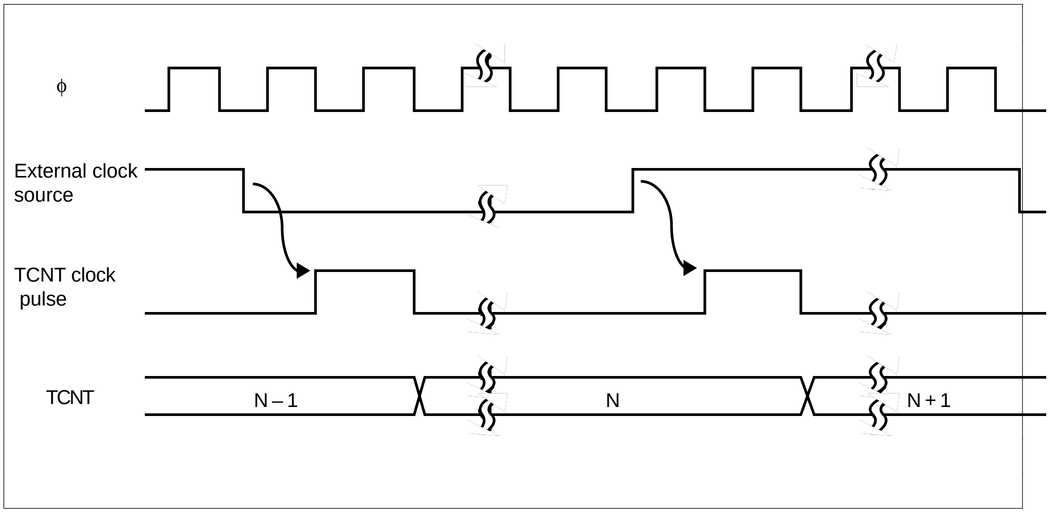


Figure 7-3 Count Timing for External Clock Input

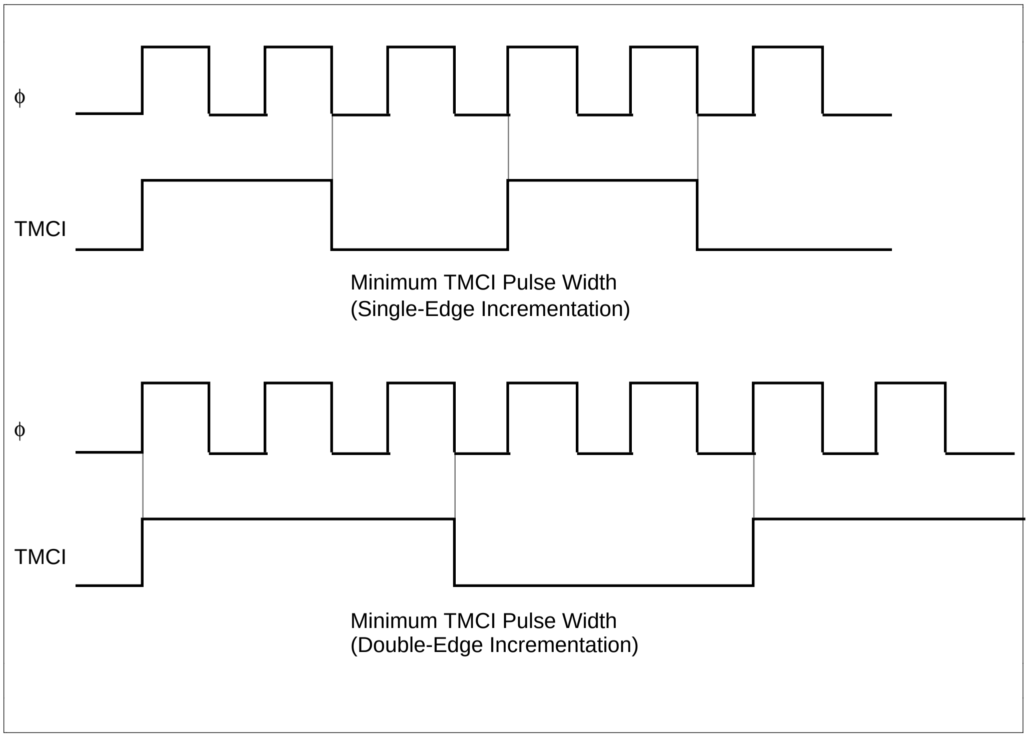


Figure 7-4 Minimum External Clock Pulse Widths (Example)

7.3.2 Compare Match Timing

Setting the Compare-Match Flags A and B (CMFA and CMFB): The compare-match flags are set to 1 by an internal compare-match signal generated when the timer count matches the time constant in TCNT or TCOR. The compare-match signal is generated at the last state in which the match is true, just before the timer counter increments to a new value.

Accordingly, when the timer count matches one of the time constants, the compare-match signal is not generated until the next period of the clock source. Figure 7-5 shows the timing of the setting of the compare-match flags.

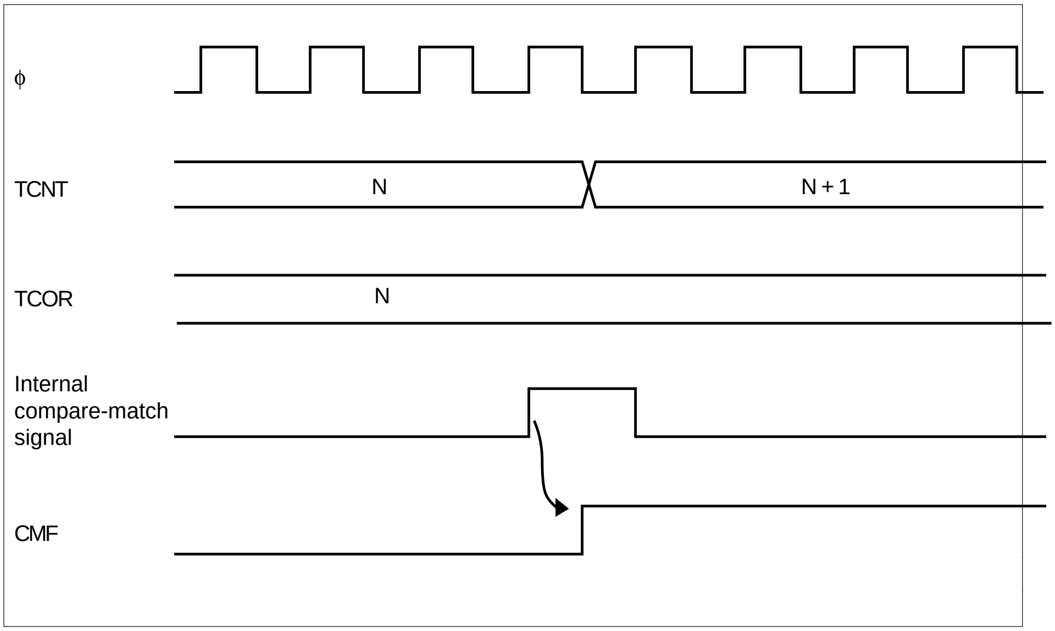


Figure 7-5 Setting the Compare-Match Flags

Output Timing: When a compare-match event occurs, the timer output (TMO0 or TMO1) changes as specified by the output select bits (OS3 to OS0) in the TCSR. Depending on these bits, the output can remain the same, change to 0, change to 1, or toggle.

Figure 7-6 shows the timing when the output is set to toggle on compare-match A.

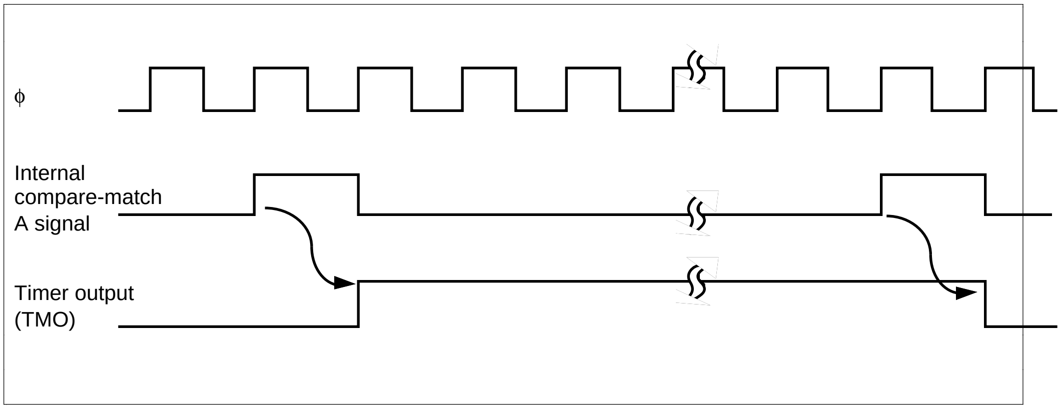


Figure 7-6 Timing of Timer Output

Timing of Compare-Match Clear: Depending on the CCLR1 and CCLR0 bits in the TCR, the timer counter can be cleared when compare-match A or B occurs. Figure 7-7 shows the timing of this operation.

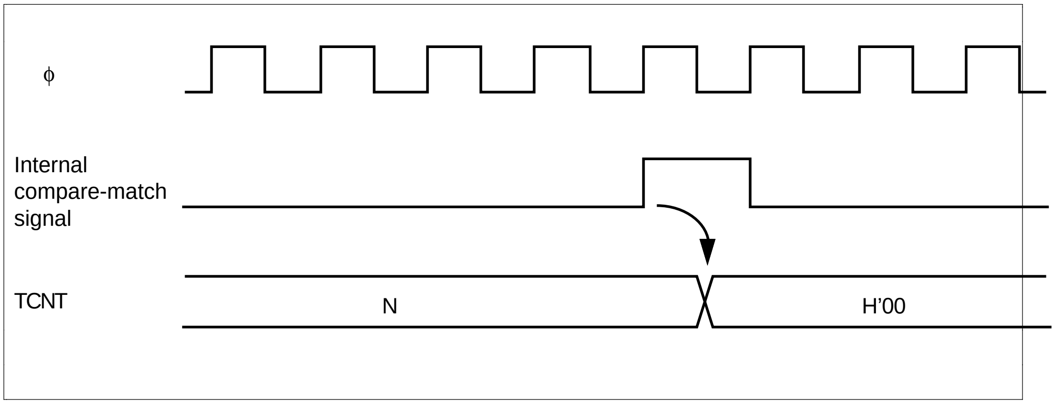


Figure 7-7 Timing of Compare-Match Clear

7.3.3 External Reset of TCNT

When the CCLR1 and CCLR0 bits in the TCR are both set to 1, the timer counter is cleared on the rising edge of an external reset input. Figure 7-8 shows the timing of this operation. The timer reset pulse width must be at least 1.5 system clock periods.

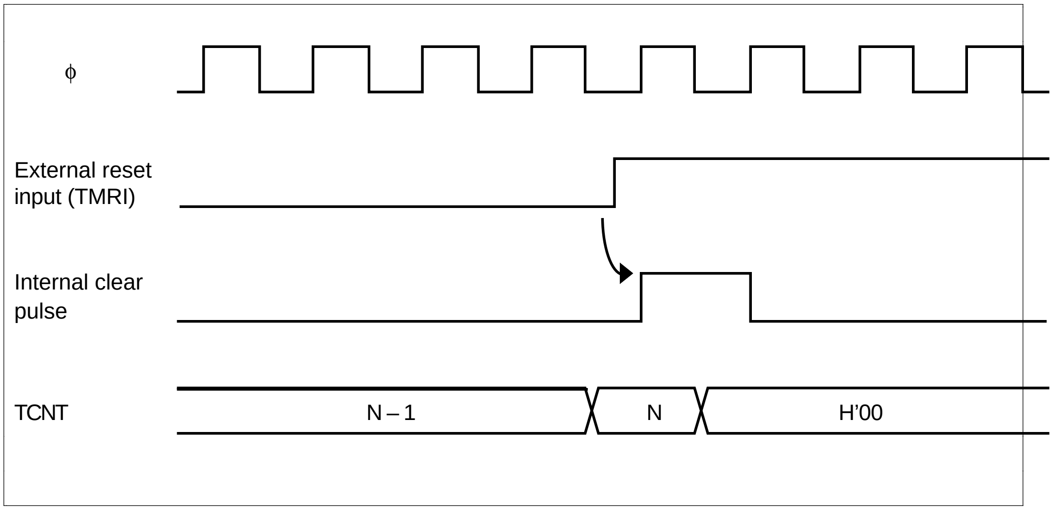


Figure 7-8 Timing of External Reset

7.3.4 Setting the TCSR Overflow Flag (OVF)

The overflow flag (OVF) is set to 1 when the timer count overflows (changes from H'FF to H'00). Figure 7-9 shows the timing of this operation.

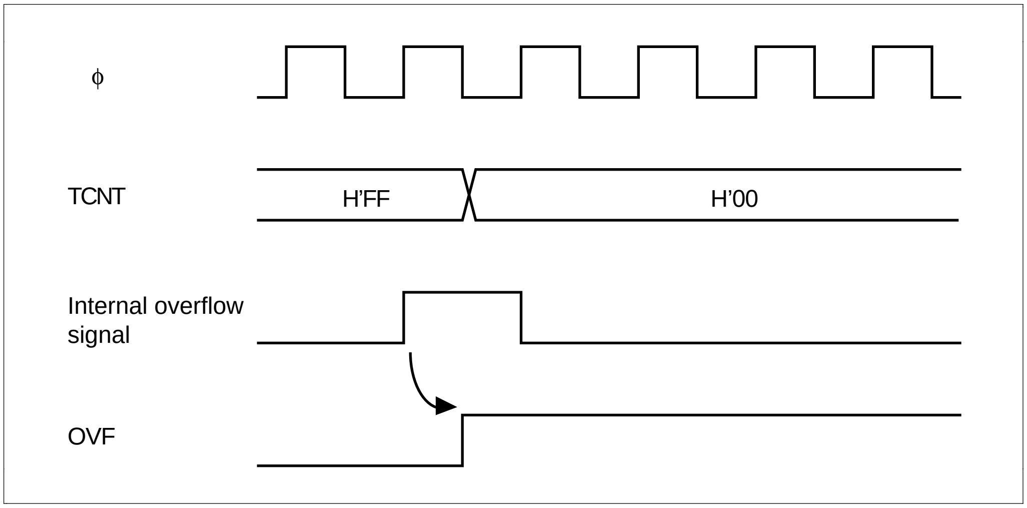


Figure 7-9 Setting the Overflow Flag (OVF)

7.4 Interrupts

Each channel in the 8-bit timer can generate three types of interrupts: compare-match A and B (CMIA and CMIB), and overflow (OVI). Each interrupt is requested when the corresponding enable bits are set in the TCR and TCSR. Independent signals are sent to the interrupt controller for each interrupt. Table 7-3 lists information about these interrupts.

Table 7-3 8-Bit Timer Interrupts

Interrupt	Description	Priority
CMIA	Requested when CMFA and CMIEA are set	High
CMIB	Requested when CMFB and CMIEB are set	↑
OVI	Requested when OVF and OVIE are set	Low

7.5 Sample Application

In the example below, the 8-bit timer generates a pulse output with a selected duty factor. The control bits are set as follows:

- In the TCR, CCLR1 is cleared to 0 and CCLR0 is set to 1 so that the timer counter is cleared when its value matches the constant in TCORA.

- In the TCSR, bits OS3 to OS0 are set to 0110, causing the output to change to 1 on compare-match A and to 0 on compare-match B.

With these settings, the 8-bit timer provides output of pulses at a rate determined by TCORA with a pulse width determined by TCORB (figure 7-10). No software intervention is required.

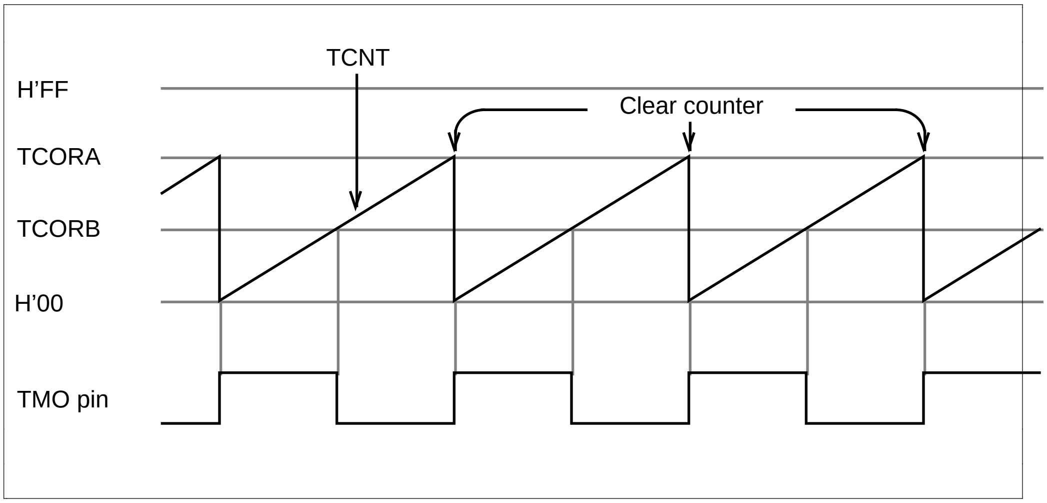


Figure 7-10 Example of Pulse Output

7.6 Application Notes

Application programmers should note that the following types of contention can occur in the 8-bit timer.

7.6.1 Contention between TCNT Write and Clear

If an internal counter clear signal is generated during the T3 state of a write cycle to the timer counter, the clear signal takes priority and the write is not performed.

Figure 7-11 shows this type of contention.

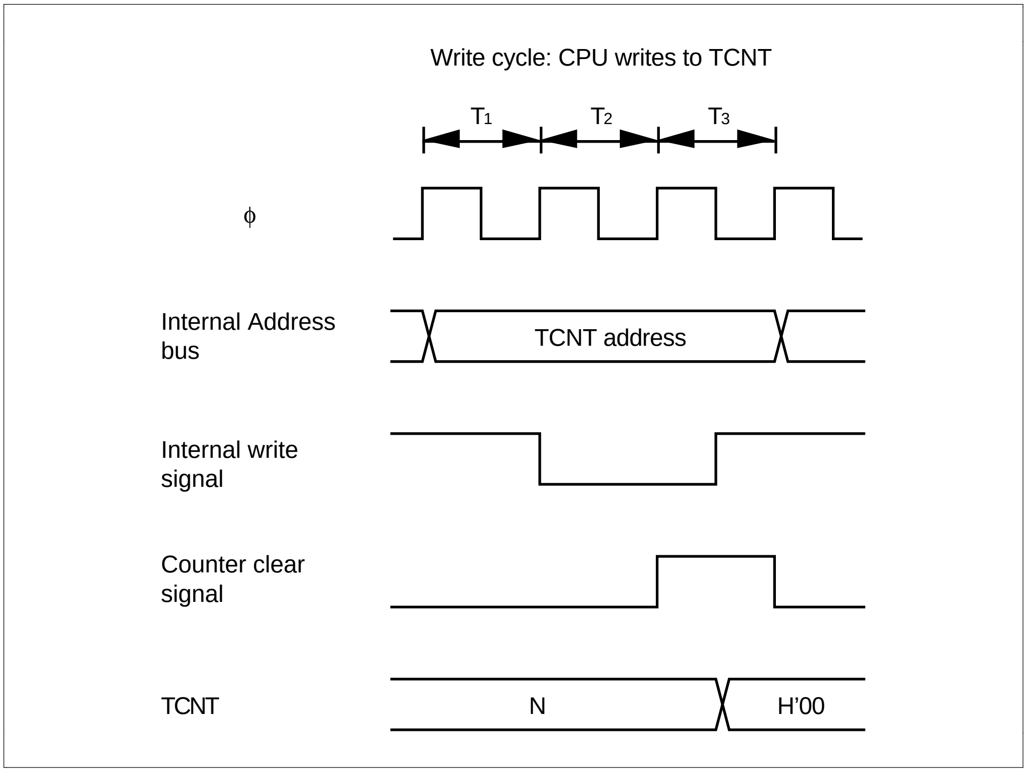


Figure 7-11 TCNT Write-Clear Contention

7.6.2 Contention between TCNT Write and Increment

If a timer counter increment pulse is generated during the T3 state of a write cycle to the timer counter, the write takes priority and the timer counter is not incremented.

Figure 7-12 shows this type of contention.

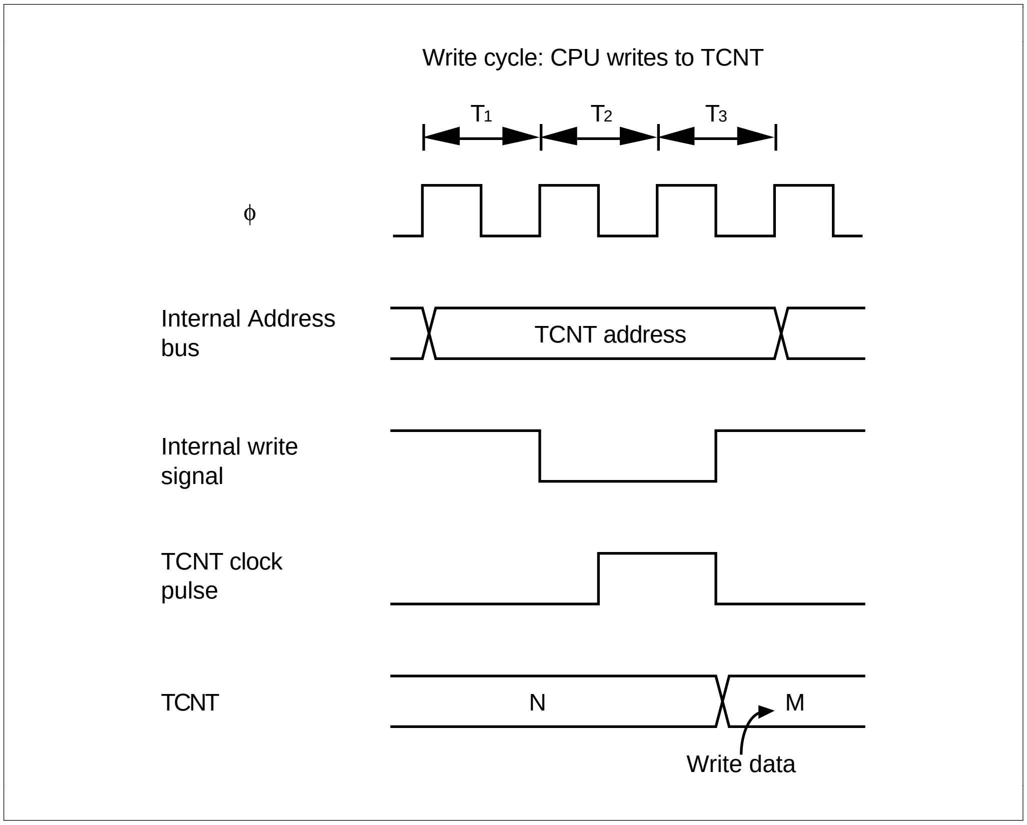


Figure 7-12 TCNT Write-Increment Contention

7.6.3 Contention between TCOR Write and Compare-Match

If a compare-match occurs during the T3 state of a write cycle to TCORA or TCORB, the write takes precedence and the compare-match signal is inhibited.

Figure 7-13 shows this type of contention.

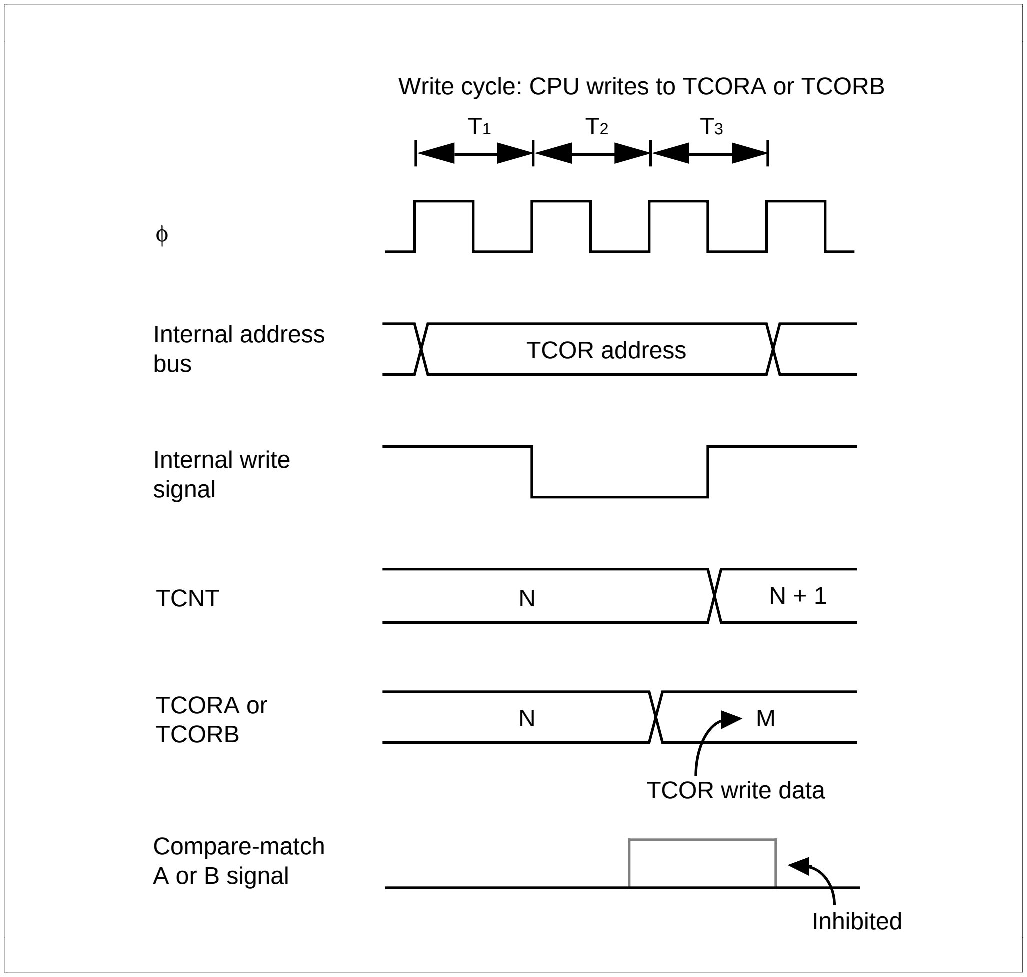


Figure 7-13 Contention between TCOR Write and Compare-Match

7.6.4 Contention between Compare-Match A and Compare-Match B

If identical time constants are written in TCORA and TCORB, causing compare-match A and B to occur simultaneously, any conflict between the output selections for compare-match A and B is resolved by following the priority order in table 7-4.

Table 7-4 Priority of Timer Output

Output Selection	Priority
Toggle	High
1 output	↑
0 output	↓
No change	Low

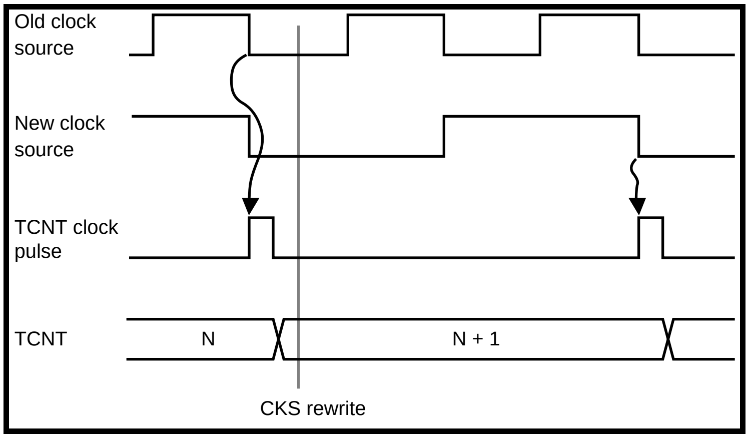
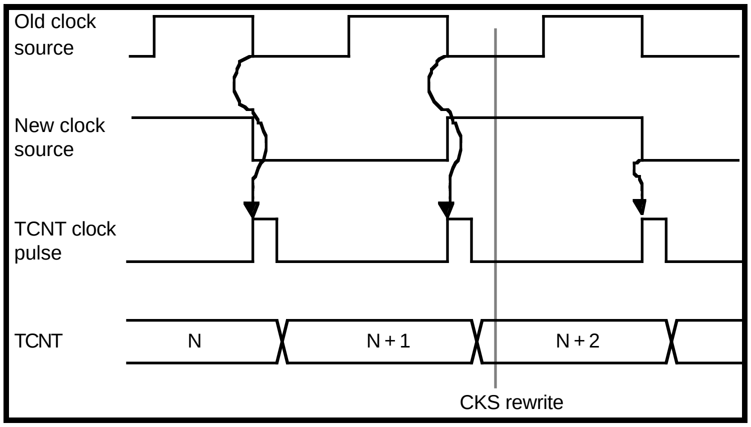
7.6.5 Increment Caused by Changing of Internal Clock Source

When an internal clock source is changed, the changeover may cause the timer counter to increment. This depends on the time at which the clock select bits (CKS2 to CKS0) are rewritten, as shown in table 7-5.

The pulse that increments the timer counter is generated at the falling edge of the internal clock source signal. If clock sources are changed when the old source is high and the new source is low, as in case 3 in table 7-5, the changeover generates a falling edge that triggers the TCNT clock pulse and increments the timer counter.

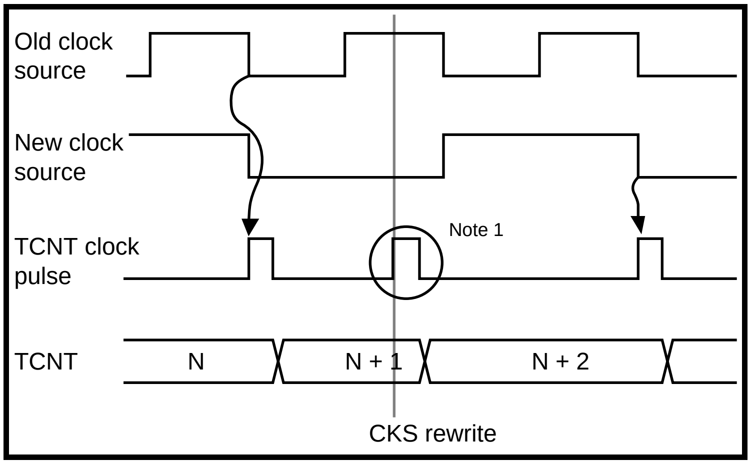
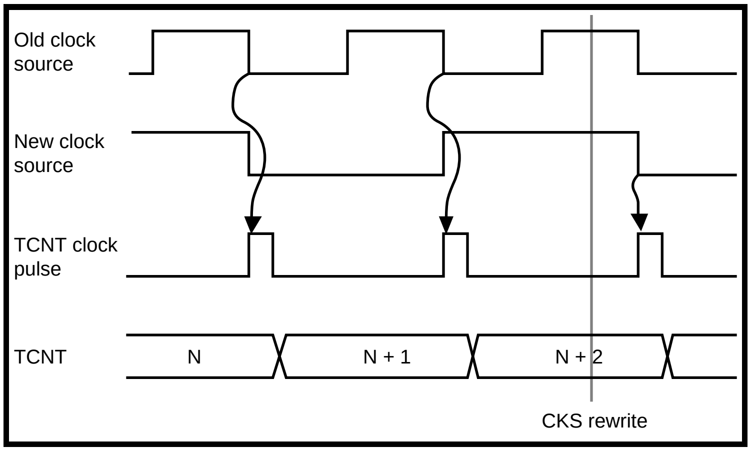
Switching between an internal and external clock source can also cause the timer counter to increment. This type of switching should be avoided at external clock edges.

Table 7-5 Effect of Changing Internal Clock Sources

No.	Description	Timing Chart
1	Low → Low [Note 1]: Clock select bits are rewritten while both clock sources are low	 Old clock source New clock source TCNT clock pulse TCNT N N + 1 CKS rewrite
2	Low → High [Note 2]: Clock select bits are rewritten while old clock source is low and new clock source is high	 Old clock source New clock source TCNT clock pulse TCNT N N + 1 N + 2 CKS rewrite

Notes
1. Including a transition from low to the stopped state (CKS1 = 0, CKS0 = 0), or a transition from the stopped state to low.
2. Including a transition from the stopped state to high.

Table 7-5 Effect of Changing Internal Clock Sources (cont)

No.	Description	Timing Chart
3	High → Low Note 1: Clock select bits are rewritten while old clock source is high and new clock source is low	 Old clock source New clock source TCNT clock pulse Note 1 TCNT N N + 1 N + 2 CKS rewrite
4	High → High Note 2: Clock select bits are rewritten while both clock sources are high	 Old clock source New clock source TCNT clock pulse TCNT N N + 1 N + 2 CKS rewrite

Notes

1. Including a transition from high to the stopped state.
2. The switching of clock sources is regarded as a falling edge that increments the TCNT.

Section 8 PWM Timers

8.1 Overview

The H8/3332 has an on-chip pulse-width modulation (PWM) timer module with two independent channels (PWM0 and PWM1). Both channels are functionally identical. Each PWM channel generates a rectangular output pulse with a duty factor of 0 to 100%. The duty factor is specified in an 8-bit duty register (DTR).

8.1.1 Features

The PWM timer module has the following features:

- Eight selectable clock sources
- Duty factors from 0 to 100% with 1/250 resolution
- Output with positive or negative logic and software enable/disable control

8.1.2 Block Diagram

Figure 8-1 shows a block diagram of one PWM timer channel.

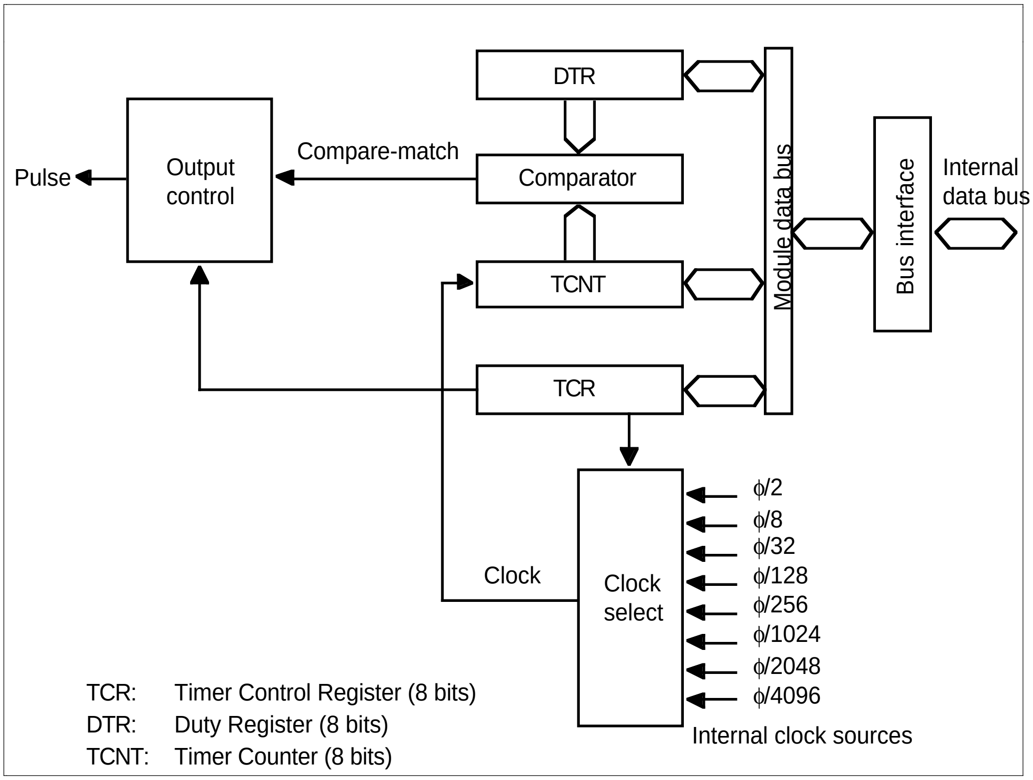


Figure 8-1 Block Diagram of PWM Timer

8.1.3 Output Pins

Table 8-1 lists the output pins of the PWM timer module. There are no input pins.

Table 8-1 Output Pins of PWM Timer Module

Name	Abbreviation	I/O	Function
PWM0 output	PW0	Output	Pulse output from PWM timer channel 0
PWM1 output	PW1	Output	Pulse output from PWM timer channel 1

8.1.4 Register Configuration

The PWM timer module has three registers for each channel as listed in table 8-2.

Table 8-2 PWM Timer Registers

				Address	
Name	**Abbreviation**	**R/W**	**Initial Value**	**PWM0**	**PWM1**
Timer control register	TCR	R/W	H'38	H'FFA0	H'FFA4
Duty register	DTR	R/W	H'FF	H'FFA1	H'FFA5
Timer counter	TCNT	R/W	H'00	H'FFA2	H'FFA6

8.2 Register Descriptions

8.2.1 Timer Counter (TCNT)—H'FFA2 (PWM0), H'FFA6 (PWM1)

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The PWM timer counters (TCNT) are 8-bit incrementing registers. When the output enable bit (OE) in the timer control register (TCR) is set to 1, the timer counter starts counting pulses of an internal clock source selected by clock select bits 2 to 0 (CKS2 to CKS0). After counting from H'00 to H'F9, the timer counter repeats from H'00.

The PWM timer counters are initialized to H'00 at a reset and in the standby modes, and when the OE bit is cleared to 0.

8.2.2 Duty Register (DTR)—H'FFA1 (PWM0), H'FFA5 (PWM1)

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The duty registers (DTR) are 8-bit read/write registers that specify the duty factor of the output pulse. Any duty factor from 0 to 100% can be selected, with a resolution of 1/250. Writing 0 (H'00) in a DTR gives a 0% duty factor; writing 125 (H'7D) gives a 50% duty factor; writing 250 (H'FA) gives a 100% duty factor.

The timer count is continually compared with the DTR contents. If the DTR value is not 0, when the count increments from H'00 to H'01 the PWM output signal is set to 1. When the count increments past the DTR value, the PWM output returns to 0. If the DTR value is 0 (duty factor 0%), the PWM output remains constant at 0.

The DTRs are double-buffered. A new value written in a DTR while the timer counter is running does not become valid until after the count changes from H'F9 to H'00. When the timer counter is stopped (while the OE bit is 0), new values become valid as soon as written. When a DTR is read, the value read is the currently valid value.

The DTRs are initialized to H'FF at a reset and in the standby modes.

8.2.3 Timer Control Register (TCR)—H'FFA0 (PWM0), H'FFA4 (PWM1)

Bit	7	6	5	4	3	2	1	0
	OE	OS	—	—	—	CKS2	CKS1	CKS0
Initial value	0	0	1	1	1	0	0	0
Read/Write	R/W	R/W	—	—	—	R/W	R/W	R/W

The TCRs are 8-bit read/write registers that select the clock source and control the PWM outputs.

The TCRs are initialized to H'38 at a reset and in the standby modes.

Bit 7: Output Enable (OE): Enables the timer counter and the PWM output.

Bit 7: OE	Description	
0	PWM output is disabled; TCNT is cleared to H'00 and stopped	(Initial value)
1	PWM output is enabled; TCNT runs	

Bit 6: Output Select (OS): Selects positive or negative logic for the PWM output.

Bit 6: OS	Description	
0	Positive logic; positive-going PWM pulse, 1 = high	(Initial value)
1	Negative logic; negative-going PWM pulse, 1 = low	

Bits 5 to 3: Reserved: Cannot be modified and are always read as 1.

Bits 2, 1, and 0: Clock Select (CKS2, CKS1, and CKS0): Select one of eight internal clock sources obtained by dividing the system clock (ϕ).

Bit 2: CKS2	Bit 1: CKS1	Bit 0: CKS0	Description	
0	0	0	ϕ/2	(Initial value)
0	0	1	ϕ/8	
0	1	0	ϕ/32	
0	1	1	ϕ/128	
1	0	0	ϕ/256	
1	0	1	ϕ/1024	
1	1	0	ϕ/2048	
1	1	1	ϕ/4096	

From the clock source frequency, the resolution, period, and frequency of the PWM output can be calculated as follows.

Resolution = 1/clock source frequency
PWM period = Resolution × 250
PWM frequency = 1/PWM period

If the system clock frequency is 10 MHz, then the resolution, period, and frequency of the PWM output for each clock source are given in table 8-3.

Table 8-3 PWM Timer Parameters for 10-MHz System Clock

Internal Clock Frequency	Resolution	PWM period	PWM frequency
ϕ/2	200 ns	50 µs	20 kHz
ϕ/8	800 ns	200 µs	5 kHz
ϕ/32	3.2 µs	800 µs	1.25 kHz
ϕ/128	12.8 µs	3.2 ms	312.5 Hz
ϕ/256	25.6 µs	6.4 ms	156.3 Hz
ϕ/1024	102.4 µs	25.6 ms	39.1 Hz
ϕ/2048	204.8 µs	51.2 ms	19.5 Hz
ϕ/4096	409.6 µs	102.4 ms	9.8 Hz

8.3 Operation

8.3.1 Timer Increment

The PWM clock source is created from the system clock (ϕ) by a prescaler. The timer counter increments on a TCNT clock pulse generated from the falling edge of the prescaler output as shown in figure 8-2.

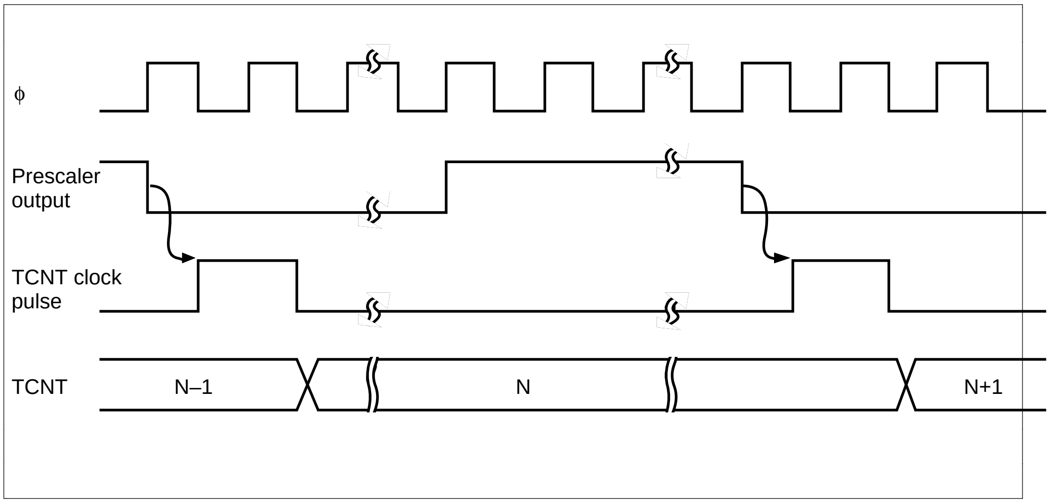
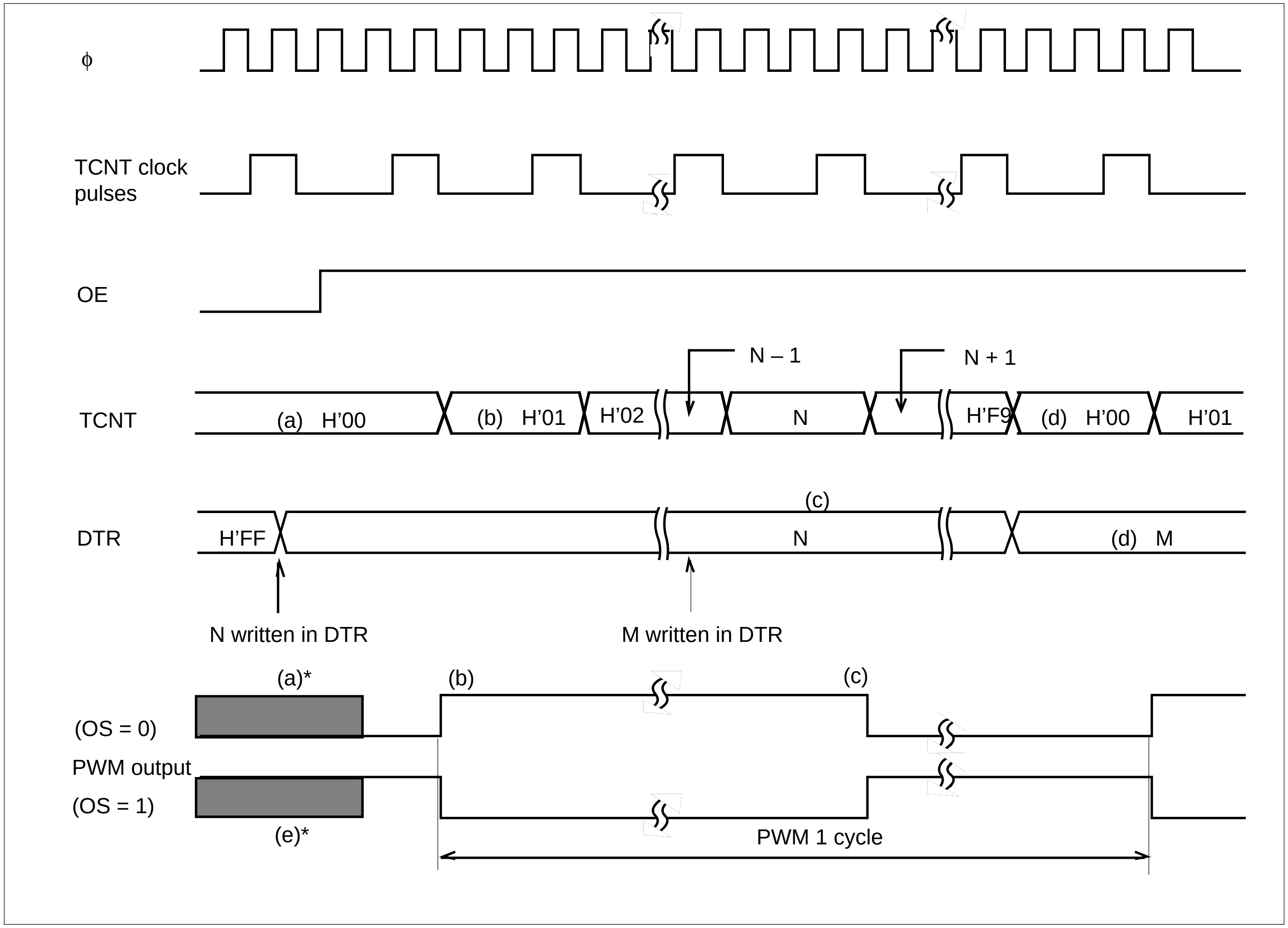


Figure 8-2 TCNT Increment Timing

8.3.2 PWM Operation

Figure 8-3 is a timing chart of the PWM operation.



Note: * Used for port 4 input/output: state depends on values in data register and data direction register.

Figure 8-3 PWM Timing

- Positive logic (OS = 0)

  — When OE = 0 ((a) in figure 8-3): The timer count is held at H'00 and PWM output is inhibited. (Pin 4_6 (for PW0) or pin 4_7 (for PW1)is used for port 4 input/output. Its state depends on the corresponding port 4 data register and data direction register.) Any value (such as N in figure 8-3) written in the DTR becomes valid immediately.

  — When OE = 1:
    - The timer counter begins incrementing. The PWM output goes high when TCNT changes from H'00 to H'01, unless DTR = H'00 [(b) in Figure 8-3].
    - When the count passes the DTR value, the PWM output goes low [(c) in Figure 8-3].
    - If the DTR value is changed (by writing the data "M" in Figure 8-3), the new value becomes valid after the timer count changes from H'F9 to H'00 [(d) in Figure 8-3].

- Negative logic (OS = 1) ((e) in figure 8-3): The operation is the same except that high and low are reversed in the PWM output.

8.4 Application Notes

- Any necessary changes to the clock select bits (CKS2 to CKS0) and output select bit (OS) should be made before the output enable bit (OE) is set to 1.

- If the DTR value is H'00, the duty factor is 0% and PWM output remains constant at 0. If the DTR value is H'FA to H'FF, the duty factor is 100% and PWM output remains constant at 1.

  (For positive logic, 0 is low and 1 is high. For negative logic, 0 is high and 1 is low.)

Section 9 Serial Communication Interface

9.1 Overview

The H8/3332 includes a serial communication interface channel (SCI) for transferring serial data to and from other chips. Either synchronous or asynchronous communication can be selected.

9.1.1 Features

The features of the on-chip serial communication interface are:

- Asynchronous mode
  The H8/3332 can communicate with a UART (Universal Asynchronous Receiver/Transmitter), ACIA (Asynchronous Communication Interface Adapter), or other chip that employs standard asynchronous serial communication. It also has a multiprocessor communication function for communication with other processors. Twelve data formats are available.
  - Data length: 7 or 8 bits
  - Stop bit length: 1 or 2 bits
  - Parity: Even, odd, or none
  - Multiprocessor bit: 1 or 0
  - Error detection: Parity, overrun, and framing errors
  - Break detection: When a framing error occurs, the break condition can be detected by reading the level of the RxD line directly.

- Synchronous mode
  The SCI can communicate with chips able to perform clocked synchronous data transfer.
  - Data length: 8 bits
  - Error detection: Overrun errors

- Full duplex communication
  The transmitting and receiving sections are independent, so each channel can transmit and receive simultaneously. Both the transmit and receive sections use double buffering, so continuous data transfer is possible in either direction.

- Built-in baud rate generator
  Any specified baud rate can be generated.

- Internal or external clock source
  The SCI can operate on an internal clock signal from the baud rate generator, or an external clock signal input at the SCK pin.

- Four interrupts
  TDR-empty, TSR-empty, receive-end, and receive-error interrupts are requested independently.

9.1.2 Block Diagram

Figure 9-1 shows a block diagram of the serial communication interface.

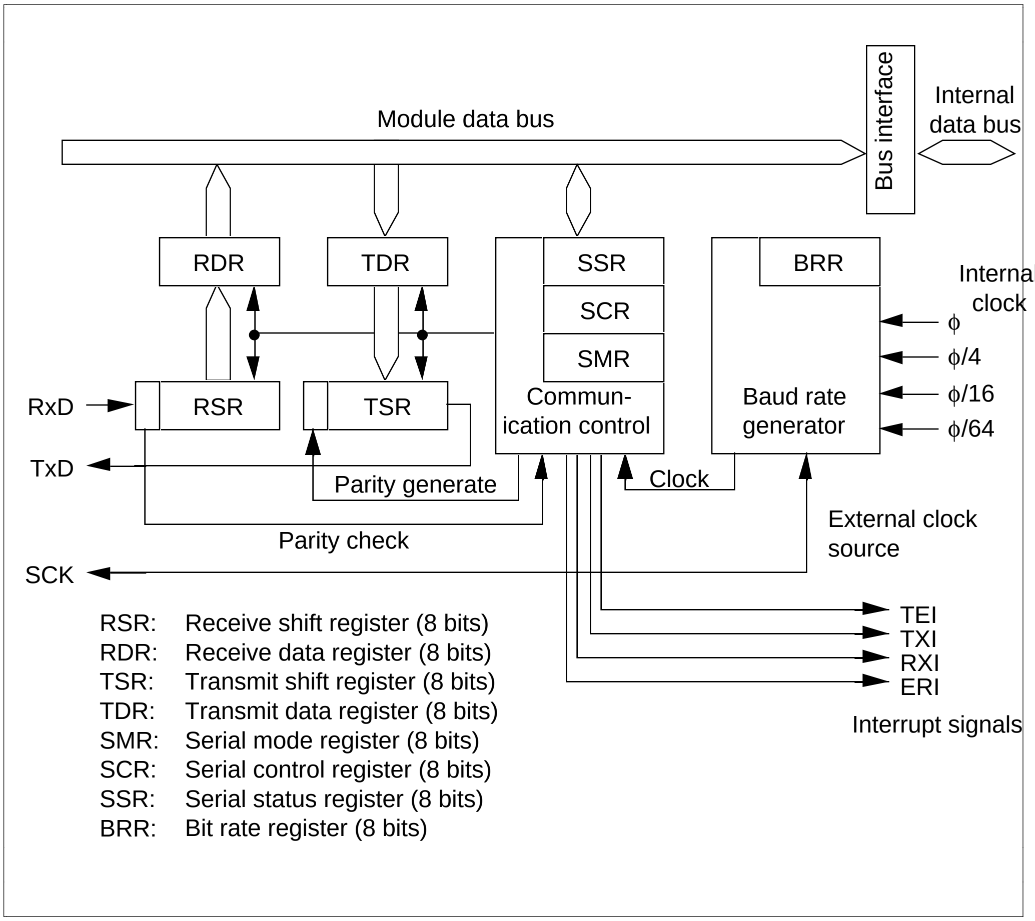

Module data bus
Bus interface
Internal data bus
RDR
TDR
SSR
SCR
SMR
BRR
Internal clock
ϕ
ϕ/4
ϕ/16
ϕ/64
RxD
RSR
TSR
Commun-ication control
Baud rate generator
TxD
Parity generate
Clock
Parity check
External clock source
SCK
TEI
TXI
RXI
ERI
Interrupt signals
RSR: Receive shift register (8 bits)
RDR: Receive data register (8 bits)
TSR: Transmit shift register (8 bits)
TDR: Transmit data register (8 bits)
SMR: Serial mode register (8 bits)
SCR: Serial control register (8 bits)
SSR: Serial status register (8 bits)
BRR: Bit rate register (8 bits)

Figure 9-1 Block Diagram of Serial Communication Interface

9.1.3 Input and Output Pins

Table 9-1 lists the input and output pins used by the SCI module.

Table 9-1 SCI Input/Output Pins

Name	Abbreviation	I/O	Function
Serial clock	SCK	Input/output	Serial clock input and output
Receive data	RxD	Input	Receive data input
Transmit data	TxD	Output	Transmit data output

9.1.4 Register Configuration

Table 9-2 lists the SCI registers. These registers specify the operating mode (synchronous or asynchronous), data format and bit rate, and control the transmit and receive sections.

Table 9-2 SCI Registers

Name	Abbreviation	R/W	Value	Address
Receive shift register	RSR	—	—	—
Receive data register	RDR	R	H'00	H'FFDD
Transmit shift register	TSR	—	—	—
Transmit data register	TDR	R/W	H'FF	H'FFDB
Serial mode register	SMR	R/W	H'00	H'FFD8
Serial control register	SCR	R/W	H'00	H'FFDA
Serial status register	SSR	R/(W)*	H'84	H'FFDC
Bit rate register	BRR	R/W	H'FF	H'FFD9
Serial/timer control register	STCR	R/W	H'F8	H'FFC3

Note: *: Software can write a 0 to clear the flags in bits 7 to 3, but cannot write 1 in these bits.

9.2 Register Descriptions

9.2.1 Receive Shift Register (RSR)

Bit	7	6	5	4	3	2	1	0
Read/Write	—	—	—	—	—	—	—	—

The RSR is a shift register that converts incoming serial data to parallel data. When one data character has been received, it is transferred to the receive data register (RDR).

The CPU cannot read or write the RSR directly.

9.2.2 Receive Data Register (RDR)—H'FFDD

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

The RDR stores received data. As each character is received, it is transferred from the RSR to the RDR, enabling the RSR to receive the next character. This double-buffering allows the SCI to receive data continuously.

The CPU can read but not write the RDR. The RDR is initialized to H'00 at a reset and in the standby modes.

9.2.3 Transmit Shift Register (TSR)

Bit	7	6	5	4	3	2	1	0
Read/Write	—	—	—	—	—	—	—	—

The TSR is a shift register that converts parallel data to serial transmit data. When transmission of this character is completed, the next character is moved from the transmit data register (TDR) to the TSR and transmission of that character begins. If the TDRE bit is still set to 1, however, nothing is transferred to the TSR.

The CPU cannot read or write the TSR directly.

9.2.4 Transmit Data Register (TDR)—H'FFDB

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The TDR is an 8-bit readable/writeable register that holds the next character to be transmitted. When the TSR becomes empty, the character written in the TDR is transferred to the TSR. Continuous data transmission is possible by writing the next byte in the TDR while the current byte is being transmitted from the TSR.

The TDR is initialized to H'FF at a reset and in the standby modes.

9.2.5 Serial Mode Register (SMR)—H'FFD8

Bit	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The SMR is an 8-bit readable/writeable register that controls the communication format and selects the clock rate for the internal clock source. It is initialized to H'00 at a reset and in the standby modes. For further information on the SMR settings and communication formats, see tables 9-5 and 9-7 in section 9.3, “Operation.”

Bit 7: Communication Mode (C/$\overline{A}$): Selects the asynchronous or clocked synchronous communication mode.

Bit 7: C/$\overline{A}$	Description	
0	Asynchronous communication	(Initial value)
1	Clock synchronous communication	

Bit 6: Character Length (CHR): Selects the character length in asynchronous mode. CHR is ignored in synchronous mode.

Bit 6: CHR	Description	
0	8 bits per character	(Initial value)
1	7 bits per character (Bits 0 to 6 of TDR and RDR are used for transmitting and receiving, respectively.)	

Bit 5: Parity Enable (PE): Selects whether to add a parity bit in asynchronous mode. PE is ignored in synchronous mode, and when a multiprocessor format is used.

Bit 5: PE	Description	
0	Transmit: No parity bit is added Receive: Parity is not checked	(Initial value)
1	Transmit: A parity bit is added Receive: Parity is checked	

Bit 4: Parity Mode (O/$\overline{E}$): In asynchronous mode, when parity is enabled (PE = 1), O/$\overline{E}$ selects even or odd parity.

Even parity means that a parity bit is added to the data bits for each character to make the total number of 1s even. Odd parity means that the total number of 1s is made odd.

This bit is ignored when PE = 0, in the synchronous mode, and when a multiprocessor format is used.

Bit 4: O/$\overline{E}$	Description	
0	Even parity	(Initial value)
1	Odd parity	

Bit 3: Stop Bit Length (STOP): Selects the number of stop bits. STOP is ignored in the synchronous mode.

Bit 3: STOP	Description	
0	One stop bit. Transmit: One stop bit is added. Receive: One stop bit is checked to detect framing errors.	(Initial value)
1	Two stop bits Transmit: Two stop bits are added. Receive: The first stop bit is checked to detect framing errors. If the second stop bit is a space (0), it is regarded as the next start bit.	

Bit 2: Multiprocessor Mode (MP): Selects the multiprocessor format in asynchronous communication. When multiprocessor format is selected, the parity settings of the parity enable bit (PE) and parity mode bit (O/$\overline{E}$) are ignored. The MP bit is ignored in synchronous communication.

The MP bit is valid only when the MPE bit in the serial/timer control register (STCR) is set to 1. When the MPE bit is cleared to 0, the multiprocessor communication function is disabled regardless of the setting of the MP bit.

Bit 2: MP	Description	
0	Multiprocessor communication function is disabled	(Initial value)
1	Multiprocessor communication function is enabled	

Bits 1 and 0: Clock Select 1 and 0 (CKS1 and CKS0): Select the internal clock source when the baud rate generator is clocked from within the chip.

Bit 1: CKS1	Bit 0: CKS0	Description	
0	0	ϕ clock	(Initial value)
0	1	ϕ/4 clock	
1	0	ϕ/16 clock	
1	1	ϕ/64 clock	

9.2.6 Serial Control Register (SCR)—H'FFDA

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The SCR is an 8-bit readable/writeable register that enables or disables various SCI functions. It is initialized to H'00 at a reset and in the standby modes.

Bit 7: Transmit Interrupt Enable (TIE): Enables or disables the TDR-empty interrupt (TxI) requested when the transmit data register empty (TDRE) bit in the serial status register (SSR) is set to 1.

Bit 7: TIE	Description
0	The TDR-empty interrupt request (TXI) is disabled (Initial value)
1	The TDR-empty interrupt request (TXI) is enabled

Bit 6: Receive Interrupt Enable (RIE): Enables or disables the receive-end interrupt (RXI) requested when the receive data register full (RDRF) bit in the serial status register (SSR) is set to 1, and the receive error interrupt (ERI) requested when the overrun error (ORER), framing error (FER), or parity error (PER) bit in the serial status register (SSR) is set to 1.

Bit 6: RIE	Description
0	The receive-end interrupt (RXI) and receive-error (ERI) requests are disabled (Initial value)
1	The receive-end interrupt (RXI) and receive-error (ERI) requests are enabled

Bit 5: Transmit Enable (TE): Enables or disables the transmit function. When the transmit function is enabled, the TxD pin is automatically used for output. When the transmit function is disabled, the TxD pin can be used as a general-purpose I/O port.

Bit 5: TE	Description
0	The transmit function is disabled. The TxD pin can be used for general-purpose I/O. (Initial value)
1	The transmit function is enabled. The TxD pin is used for output.

Bit 4: Receive Enable (RE): Enables or disables the receive function. When the receive function is enabled, the RxD pin is automatically used for input. When the receive function is disabled, the RxD pin is available as a general-purpose I/O port.

Bit 4: RE	Description
0	The receive function is disabled. The RxD pin can be used for general-purpose I/O. (Initial value)
1	The receive function is enabled. The RxD pin is used for input.

Bit 3—Multiprocessor Interrupt Enable (MPIE): When serial data are received in a multiprocessor format, MPIE enables or disables the receive-end interrupt (RXI) and receive-error interrupt (ERI) until data with the multiprocessor bit set to 1 are received. It also enables or disables the transfer of received data from the RSR to the RDR, and enables or disables setting of the RDRF, FER, PER, and ORER bits in the serial status register (SSR).

The MPIE bit is ignored when the MP bit is cleared to 0, and in synchronous mode.

Clearing the MPIE bit to 0 disables the multiprocessor receive interrupt function. In this condition data are received regardless of the value of the multiprocessor bit in the receive data.

Setting the MPIE bit to 1 enables the multiprocessor receive interrupt function. In this condition, if the multiprocessor bit in the receive data is 0, the receive-end interrupt (RXI) and receive-error interrupt (ERI) are disabled, the receive data are not transferred from the RSR to the RDR, receive errors are not detected, and the RDRF, FER, PER, and ORER bits in the serial status register (SSR) are not set. If the multiprocessor bit is 1, however, the MPB bit in the SSR is set to 1, the MPIE bit is cleared to 0, the receive data are transferred from the RSR to the RDR, the FER, PER, and ORER bits can be set, and the receive-end and receive-error interrupts are enabled.

Bit 3: MPIE	Description	
0	The multiprocessor receive interrupt function is disabled (Normal receive operation)	(Initial value)
1	The multiprocessor receive interrupt function is enabled. During the interval before data with the multiprocessor bit set to 1 are received, the receive interrupt request (RXI) and receive-error interrupt request (ERI) are disabled, the RDRF, FER, PER, and ORER bits are not set in the serial status register (SSR), and no data are transferred from the RSR to the RDR. The MPIE bit is cleared at the following times: 1. When 0 is written in MPIE 2. When data with the multiprocessor bit set to 1 are received.	

Bit 2: Transmit-End Interrupt Enable (TEIE): Enables or disables the TSR-empty interrupt (TEI) requested when the transmit-end bit (TEND) in the serial register (SSR) is set to 1.

Bit 2: TEIE	Description	
0	The TSR-empty interrupt request (TEI) is disabled	(Initial value)
1	The TSR-empty interrupt request (TEI) is enabled	

Bit 1: Clock Enable 1 (CKE1): Selects the internal or external clock source for the baud rate generator. When the external clock source is selected, the SCK pin is automatically used for input of the external clock signal.

Bit 1: CKE1	Description
0	Internal clock source (Initial value) When $C/\overline{A}$ = 1, the serial clock signal is output at the SCK pin. When $C/\overline{A}$ = 0, output depends on the CKE0 bit.
1	External clock source, the SCK pin is used for input

Bit 0—Clock Enable 0 (CKE0): When an internal clock source is used in asynchronous mode, CKE0 enables or disables serial clock output at the SCK pin.

This bit is ignored when the external clock is selected, or when synchronous mode is selected.

For further information on the communication format and clock source selection, see table 9-7 in section 9.3, Operation.

Bit 0: CKE0	Description
0	The SCK pin is not used by the SCI (and is available as a general-purpose I/O port) (Initial value)
1	The SCK pin is used for serial clock output.

9.2.7 Serial Status Register (SSR)—H'FFDC

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Software can write a 0 to clear the flags, but cannot write a 1 in these bits.

The SSR is an 8-bit register that indicates transmit and receive status. It is initialized to H'84 at a reset and in the standby modes.

Bit 7: Transmit Data Register Empty (TDRE): Indicates when the TDR contents have been transferred to the TSR and the next character can safely be written in the TDR.

Bit 7: TDRE	Description
0	To clear TDRE, the CPU must read TDRE after it has been set to 1, then write a 0 in this bit
1	Set to 1 at the following times: 1. When TDR contents are transferred to the TSR 2. When the TE bit in the SCR is cleared to 0 (Initial value)

Bit 6: Receive Data Register Full (RDRF): Indicates when one character has been received and transferred to the RDR.

Bit 6: RDRF	Description
0	To clear RDRF, the CPU must read RDRF after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when one character is received without error and transferred from the RSR to the RDR

Bit 5: Overrun Error (ORER): Indicates an overrun error during reception.

Bit 5: ORER	Description
0	To clear ORER, the CPU must read ORER after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 if reception of the next character ends while the receive data register is still full (RDRF = 1)

Bit 4: Framing Error (FER): Indicates a framing error during data reception in asynchronous mode. It has no meaning in synchronous mode.

Bit 4: FER	Description
0	To clear FER, the CPU must read FER after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 if a framing error occurs (stop bit = 0)

Bit 3: Parity Error (PER): Indicates a parity error during data reception in the asynchronous mode, when a communication format with parity bits is used.

PER has no meaning in the synchronous mode, or when a communication format without parity bits is used.

Bit 3: PER	Description
0	To clear PER, the CPU must read PER after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when a parity error occurs (the parity of the received data does not match the parity selected by the O/E bit in SMR)

Bit 2: Transmit End (TEND): Indicates that the serial communication interface has stopped transmitting because there was no valid data in the TDR when the last bit of the current character was transmitted. The TEND bit is also set to 1 when the TE bit in the serial control register (SCR) is cleared to 0.

The TEND bit can be read but not written. To clear TEND to 0, software must read the serial status register while TDRE = 1, then write 0 in TDRE.

Bit 2: TEND	Description
0	To clear TEND, the CPU must read TDRE after it has been set to 1, then write a 0 in TDRE (Initial value)
1	This bit is set to 1 when: 1. TE = 0 2. TDRE = 1 at the end of transmission of a character

Bit 1: Multiprocessor Bit (MPB): Stores the value of the multiprocessor bit in data received in a multiprocessor format in asynchronous communication mode. MPB is cleared to 0 in synchronous mode, or when a multiprocessor format is not used. If the RE bit is cleared to 0 when a multiprocessor format is used, the MPB bit retains its previous value.

MPB can be read but not written.

Bit 1: MPB	Description
0	Multiprocessor bit = 0 in receive data (Initial value)
1	Multiprocessor bit = 1 in receive data

Bit 0: Multiprocessor Bit Transfer (MPBT): Stores the value of the multiprocessor bit inserted in transmit data when a multiprocessor format is used in asynchronous communication mode. The MPBT bit has no effect in synchronous mode, or when a multiprocessor format is not used. It is not used in receiving data.

Bit 0: MPBT	Description
0	Multiprocessor bit = 0 in transmit data (Initial value)
1	Multiprocessor bit = 1 in transmit data

9.2.8 Bit Rate Register (BRR)—H'FFD9

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The BRR is an 8-bit register that, together with the CKS1 and CKS0 bits in the SMR, determines the baud rate output by the baud rate generator.

The BRR is initialized to H'FF (the slowest rate) at a reset and in the standby modes.

Tables 9-3 and 9-4 show examples of BRR (N) and CKS (n) settings for commonly used bit rates. Table 9-5 lists the maximum bit rates in asynchronous mode.

Table 9-3 Examples of BRR Settings in Asynchronous Mode

	XTAL Frequency (MHz)											
	2			2.4576			4			4.194304		
Bit Rate			Error			Error			Error			Error
	n	N	(%)	n	N	(%)	n	N	(%)	n	N	(%)
110	1	70	+0.03	1	86	+0.31	1	141	+0.03	1	148	–0.04
150	0	207	+0.16	0	255	0	1	103	+0.16	1	108	+0.21
300	0	103	+0.16	0	127	0	0	207	+0.16	0	217	+0.21
600	0	51	+0.16	0	63	0	0	103	+0.16	0	108	+0.21
1200	0	25	+0.16	0	31	0	0	51	+0.16	0	54	–0.70
2400	0	12	+0.16	0	15	0	0	25	+0.16	0	26	+1.14
4800	—	—	—	0	7	0	0	12	+0.16	0	13	–2.48
9600	—	—	—	0	3	0	—	—	—	—	—	—
19200	—	—	—	0	1	0	—	—	—	—	—	—
31250	—	—	—	—	—	—	0	1	0	—	—	—
38400	—	—	—	0	0	0	—	—	—	—	—	—

Table 9-3 Examples of BRR Settings in Asynchronous Mode (cont)

	XTAL Frequency (MHz)											
	4.9152			6			7.3728			8		
Bit Rate	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	1	174	–0.26	2	52	+0.50	2	64	+0.70	2	70	+0.03
150	1	127	0	1	155	+0.16	1	191	0	1	207	+0.16
300	0	255	0	1	77	+0.16	1	95	0	1	103	+0.16
600	0	127	0	0	155	+0.16	0	191	0	0	207	+0.16
1200	0	63	0	0	77	+0.16	0	95	0	0	103	+0.16
2400	0	31	0	0	38	+0.16	0	47	0	0	51	+0.16
4800	0	15	0	0	19	–2.34	0	23	0	0	25	+0.16
9600	0	7	0	—	—	—	0	11	0	0	12	+0.16
19200	0	3	0	—	—	—	0	5	0	—	—	—
31250	—	—	—	0	2	0	—	—	—	0	3	0
38400	0	1	0	—	—	—	0	2	0	—	—	—

Table 9-3 Examples of BRR Settings in Asynchronous Mode (cont)

	XTAL Frequency (MHz)											
	9.8304			10			12			12.288		
Bit Rate	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	86	+0.31	2	88	–0.25	2	106	–0.44	2	108	+0.08
150	1	255	0	2	64	+0.16	2	77	0	2	79	0
300	1	127	0	1	129	+0.16	1	155	0	1	159	0
600	0	255	0	1	64	+0.16	1	77	0	1	79	0
1200	0	127	0	0	129	+0.16	0	155	+0.16	0	159	0
2400	0	63	0	0	64	+0.16	0	77	+0.16	0	79	0
4800	0	31	0	0	32	–1.36	0	38	+0.16	0	39	0
9600	0	15	0	0	15	+1.73	0	19	–2.34	0	19	0
19200	0	7	0	0	7	+1.73	—	—	—	0	4	0
31250	0	4	–1.70	0	4	0	0	5	0	0	5	+2.40
38400	0	3	0	0	3	+1.73	—	—	—	—	—	—

Table 9-3 Examples of BRR Settings in Asynchronous Mode (cont)

	XTAL Frequency (MHz)											
	14.7456			16			19.6608			20		
Bit Rate	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
110	2	130	–0.07	2	141	+0.03	2	174	–0.26	3	43	+0.88
150	2	95	0	2	103	+0.16	2	127	0	2	129	+0.16
300	1	191	0	1	207	+0.16	1	255	0	2	64	+0.16
600	1	95	0	1	103	+0.16	1	127	0	1	129	+0.16
1200	0	191	0	0	207	+0.16	0	255	0	1	64	+0.16
2400	0	95	0	0	103	+0.16	0	127	0	0	129	+0.16
4800	0	47	0	0	51	+0.16	0	63	0	0	64	+0.16
9600	0	23	0	0	25	+0.16	0	31	0	0	32	–1.36
19200	0	11	0	0	12	+0.16	0	15	0	0	15	+1.73
31250	—	—	—	0	7	0	0	9	–1.70	0	9	0
38400	0	5	0	—	—	—	0	7	0	0	7	+1.73

Note: If possible, the error should be within 1%.

$B = OSC \times 10^6/[64 \times 2^{2n} \times (N + 1)]$

N: BRR value ($0 \le N \le 255$)

OSC: Crystal oscillator frequency in MHz

B: Bit rate (bits/second)

n: Internal clock source (0, 1, 2, or 3) as shown in the table below:

n	CKS1	CKS0	Clock
0	0	0	ϕ
1	0	1	$\phi/4$
2	1	0	$\phi/16$
3	1	1	$\phi/64$

Table 9-4 Examples of BRR Settings in Synchronous Mode

	XTAL Frequency (MHz)											
Bit	2		4		8		10		16		20	
rate	n	N	n	N	n	N	n	N	n	N	n	N
100	—	—	—	—	—	—	—	—	—	—	—	—
250	1	249	2	124	2	249	—	—	3	124	—	—
500	1	124	1	249	2	124	—	—	2	249	—	—
1k	0	249	1	124	1	249	—	—	2	124	—	—
2.5k	0	99	0	199	1	99	1	124	1	199	1	249
5k	0	49	0	99	0	199	0	249	1	99	1	124
10k	0	24	0	49	0	99	0	124	0	199	0	249
25k	0	9	0	19	0	39	0	49	0	79	0	99
50k	0	4	0	9	0	19	0	24	0	39	0	49
100k	—	—	0	4	0	9	—	—	0	19	0	24
250k	0	0*	0	1	0	3	0	4	0	7	0	9
500k			0	0*	0	1	—	—	0	3	0	4
1M					0	0*	—	—	0	1	—	—
2.5M											0	0*

Notes: Blank: No setting is available.

—: A setting is available, but the bit rate is inaccurate.

*: Continuous transfer is not possible.

$B = OSC \times 10^6/[8 \times 2^{2n} \times (N + 1)]$

N: BRR value ($0 \leq N \leq 255$)

OSC: Crystal oscillator frequency in MHz

B: Bit rate (bits per second)

n: Internal clock source (0, 1, 2, or 3) as shown in the table below:

n	CKS1	CKS0	Clock
0	0	0	φ
1	0	1	φ/4
2	1	0	φ/16
3	1	1	φ/64

9.2.9 Serial/Timer Control Register (STCR)—H'FFC3

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	MPE	ICKS1	ICKS0
Initial value	1	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	R/W	R/W	R/W

The STCR is an 8-bit readable/writeable register that controls the operating mode of the serial communication interface and selects input clock sources for the 8-bit timer counters (TCNT). The STCR is initialized to H'F8 by a reset.

Bits 7 to 3: Reserved: Cannot be modified and are always read as 1.

Bit 2: Multiprocessor Enable (MPE): Enables or disables the multiprocessor communication function.

Bit 2: MPE	Description
0	The multiprocessor communication function is disabled, regardless of the setting of the MP bit in SMR (Initial value)
1	The multiprocessor communication function is enabled. The multiprocessor format can be selected by setting the MP bit in SMR to 1

Bits 1 and 0: Internal Clock Source Select 1 and 0 (ICKS1, ICKS0): Select the clock input to the timer counters (TCNT) in the 8-bit timers. For further information see section 7, 8-Bit Timers.

9.3 Operation

9.3.1 Overview

The SCI supports serial data transfer in two modes. In asynchronous mode each character is synchronized individually. In synchronous mode communication is synchronized with a clock signal.

The selection of asynchronous or synchronous mode and the communication format depend on settings in the SMR as indicated in table 9-5. The clock source depends on the settings of the C/A bit in the SMR and the CKE1 and CKE0 bits in the SCR as indicated in table 9-6.

Asynchronous Mode: Data lengths of seven or eight bits can be selected. A parity bit or multiprocessor bit can be added, and stop bit lengths of one or two bits can be selected. These selections determine the communication format and character length. Framing errors (FER), parity errors (PER) and overrun errors (ORER) can be detected in receive data, and the line-break condition can be detected.

An internal or external clock source can be selected for the serial clock. When an internal clock source is selected, the SCI is clocked by the on-chip baud rate generator and can output a clock signal at the bit-rate frequency. When the external clock source is selected, the on-chip baud rate generator is not used. The external clock frequency must be 16 times the bit rate.

Synchronous Mode: The transmit data length is eight bits. Overrun errors (ORER) can be detected in receive data.

An internal or external clock source can be selected for the serial clock. When an internal clock source is selected, the SCI is clocked by the on-chip baud rate generator and outputs a serial clock signal. When the external clock source is selected, the on-chip baud rate generator is not used and the SCI operates on the input serial clock.

Table 9-5 Communication Formats Used by SCI

SMR						Communication Format			
Bit 7: C/A	**Bit 6: CHR**	**Bit 2: MP**	**Bit 5: PE**	**Bit 3: STOP**	**Mode**	**Data Length**	**MP Bit**	**Parity Bit**	**Stop Bit Length**
0	0	0	0	0	Asynchronous	8 bits	No	No	1 bits
				1					2 bits
			1	0				Yes	1 bits
				1					2 bits
	1		0	0		7 bits		No	1 bits
				1					2 bits
			1	0				Yes	1 bits
				1					2 bits
	0	1	—	0	Asynchronous (Multiprocessor format)	8 bits	Yes	No	1 bits
				1					2 bits
	1			0		7 bits			1 bits
				1					2 bits
1	—	—	—	—	Synchronous	8 bits	No	—	None

Table 9-6 SCI Clock Source Selection

SMR	SCR			Serial Transmit/Receive Clock	
Bit 7:	Bit 1:	Bit 0:		Clock	
C/A	CKE1	CKE0	Mode	Source	SCK Pin
0	0	0	Async	Internal	Input/output port (Not used by the SCI)
		1			Serial clock output at bit rate
	1	0		External	Serial clock input at 16 × bit rate
		1			
1	0	0	Sync	Internal	Serial clock output
		1			
	1	0		External	Serial clock input
		1			

9.3.2 Asynchronous Mode

In asynchronous mode, each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible because the SCI has independent transmit and receive sections. Double buffering in both sections enables the SCI to be programmed for continuous data transfer.

Figure 9-2 shows the general format of one character sent or received in asynchronous mode. The communication channel is normally held in the mark state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity or multiprocessor bit, if present, then the stop bit or bits (high) confirming the end of the frame.

In receiving, the SCI synchronizes on the falling edge of the start bit, and samples each bit at the center of the bit (at the eighth cycle of the internal serial clock, which runs at 16 times the bit rate).

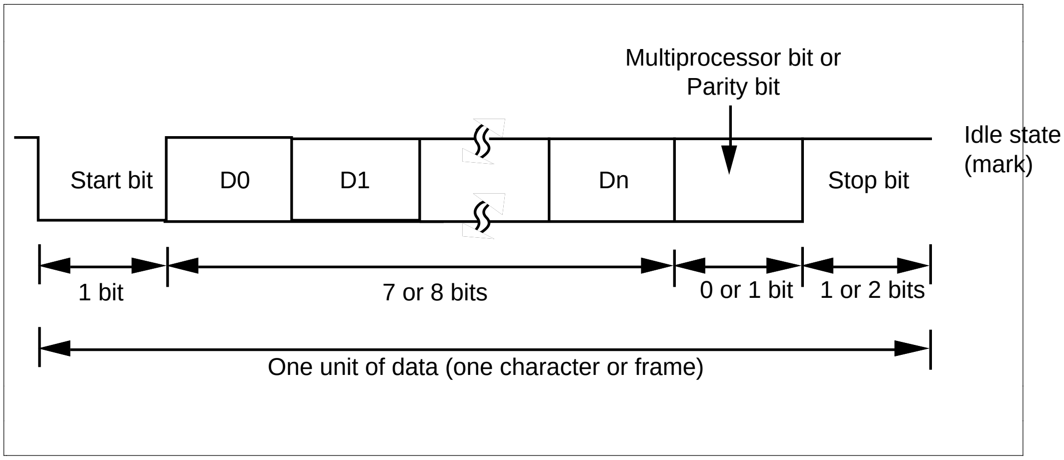


Figure 9-2 Data Format in Asynchronous Mode

Data Format: Table 9-7 lists the data formats that can be sent and received in asynchronous mode. Twelve formats can be selected by bits in the SMR.

Table 9-7 Data Formats in Asynchronous Mode

SMR Bits															
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	0	START	8-Bit data								STOP		
0	0	0	1	START	8-Bit data								STOP	STOP	
0	1	0	0	START	8-Bit data								P	STOP	
0	1	0	1	START	8-Bit data								P	STOP	STOP
1	0	0	0	START	7-Bit data							STOP			
1	0	0	1	START	7-Bit data							STOP	STOP		
1	1	0	0	START	7-Bit data							P	STOP		
1	1	0	1	START	7-Bit data							P	STOP	STOP	
0	—	1	0	START	8-Bit data								MPB	STOP	
0	—	1	1	START	8-Bit data								MPB	STOP	STOP
1	—	1	0	START	7-Bit data							MPB	STOP		
1	—	1	1	START	7-Bit data							MPB	STOP	STOP	

Note: START: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multiprocessor bit

Clock: In asynchronous mode it is possible to select either an internal clock created by the on-chip baud rate generator, or an external clock input at the SCK pin. The selection is made by the $C/\overline{A}$ bit in the serial mode register (SMR) and the CKE1 and CKE0 bits in the serial control register (SCR). Refer to table 9-7.

If an external clock is input at the SCK pin, its frequency should be 16 times the desired bit rate.

If the internal clock provided by the on-chip baud rate generator is selected and the SCK pin is used for clock output, the output clock frequency is equal to the bit rate, and the clock pulse rises at the center of the transmit data bits. Figure 9-3 shows the phase relationship between the output clock and transmit data.

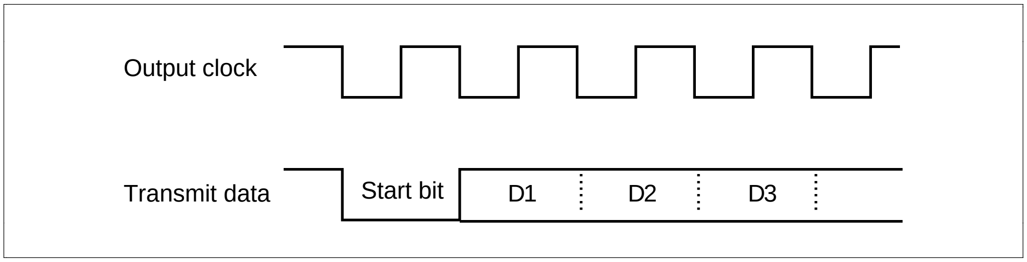


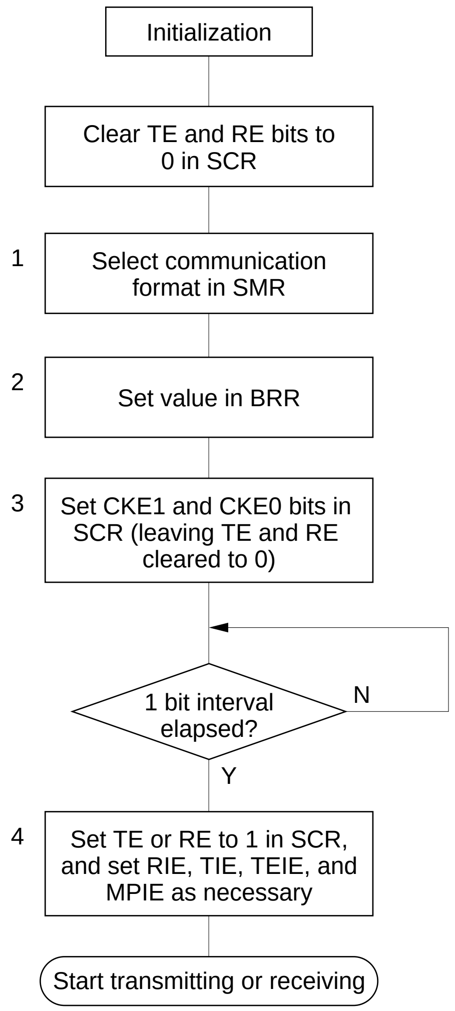
Figure 9-3 Phase Relationship between Clock Output and Transmit Data (Asynchronous Mode)

Transmitting and Receiving Data:

- **SCI Initialization:** Before transmitting or receiving, software must clear the TE and RE bits to 0 in the serial control register (SCR), then initialize the SCI as follows.

  Note: When changing the communication mode or format, always clear the TE and RE bits to 0 before following the procedure given below. Clearing TE to 0 sets TDRE to 1 and initializes the transmit data register (TDR) and transmit shift register (TSR). Clearing RE to 0, however, does not initialize the RDRF, PER, FER, and ORER flags and receive data register (RDR), which retain their previous contents.

  When an external clock is used, the clock should not be stopped during initialization or subsequent operation. SCI operation becomes unreliable if the clock is stopped.


Initialization
Clear TE and RE bits to 0 in SCR
1
Select communication format in SMR
2
Set value in BRR
3
Set CKE1 and CKE0 bits in SCR (leaving TE and RE cleared to 0)
1 bit interval elapsed?
N
Y
4
Set TE or RE to 1 in SCR, and set RIE, TIE, TEIE, and MPIE as necessary
Start transmitting or receiving

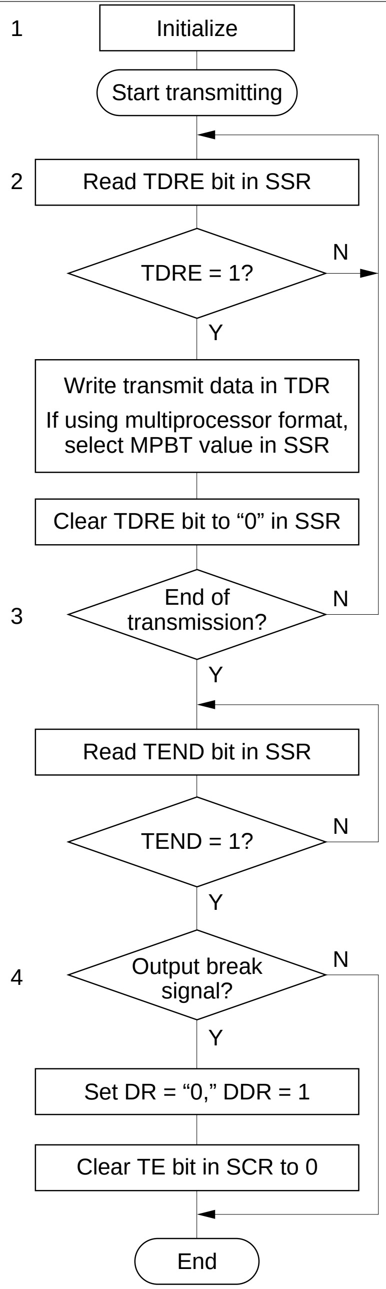
1. Select the communication format in the serial mode register (SMR).
2. Write the value corresponding to the bit rate in the bit rate register (BRR). This step is not necessary when an external clock is used.
3. Select interrupts and the clock source in the serial control register (SCR). Leave TE and RE cleared to 0. If clock output is selected, clock output starts immediately after the setting is made in SCR.
4. Wait for at least the interval required to transmit or receive one bit, then set TE or RE in the serial control register (SCR).

   Setting TE or RE enables the SCI to use the TxD or RxD pin.

   Also set the RIE, TIE, TEIE, and MPIE bits as necessary to enable interrupts. The initial states are the mark transmit state, and the idle receive state (waiting for a start bit).

Figure 9-4 Sample Flowchart for SCI Initialization

- **Transmitting Serial Data:** Follow the procedure below for transmitting serial data.



1. SCI initialization: the transmit data output function of the TxD pin is selected automatically.
2. SCI status check and transmit data write: read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR) and clear TDRE to 0.

   If a multiprocessor format is selected, after writing the transmit data write 0 or 1 in the multiprocessor bit transfer (MPBT) in SSR. Transition of the TDRE bit from 0 to 1 can be reported by an interrupt.
3. a. To continue transmitting serial data: read the TDRE bit to check whether it is safe to write; if so, write data in TDR, then clear TDRE to 0.

   b. To end serial transmission: end of transmission can be confirmed by checking transition of the TEND bit from 0 to 1. This can be reported by a TEI interrupt.
4. To output a break signal at the end of serial transmission: set the DDR bit to 1 and the DR bit to 0 (DDR and DR are I/O port registers), then clear TE to 0 in SCR.

Figure 9-5 Sample Flowchart for Transmitting Serial Data

In transmitting serial data, the SCI operates as follows.

1. The SCI monitors the TDRE bit in SSR. When TDRE is cleared to 0 the SCI recognizes that the transmit data register (TDR) contains new data, and loads this data from TDR into the transmit shift register (TSR).

2. After loading the data from TDR into TSR, the SCI sets the TDRE bit to 1 and starts transmitting. If the TIE bit (TDR-empty interrupt enable) is set to 1 in SCR, the SCI requests a TXI interrupt (TDR-empty interrupt) at this time.

   Serial transmit data are transmitted in the following order from the TxD pin:

   a. Start bit: one 0 bit is output.

   b. Transmit data: seven or eight bits are output, LSB first.

   c. Parity bit or multiprocessor bit: one parity bit (even or odd parity) or one multiprocessor bit is output. Formats in which neither a parity bit nor a multiprocessor bit is output can also be selected.

   d. Stop bit: one or two 1 bits (stop bits) are output.

   e. Mark state: output of 1 bits continues until the start bit of the next transmit data.

3. The SCI checks the TDRE bit when it outputs the stop bit. If TDRE is 0, the SCI loads new data from TDR into TSR, outputs the stop bit, then begins serial transmission of the next frame. If TDRE is 1, the SCI sets the TEND bit to 1 in SSR, outputs the stop bit, then continues output of 1 bits in the mark state. If the TEIE bit (TSR-empty interrupt enable) in SCR is set to 1, a TEI interrupt (TSR-empty interrupt) is requested.

Figure 9-6 shows an example of SCI transmit operation in asynchronous mode.

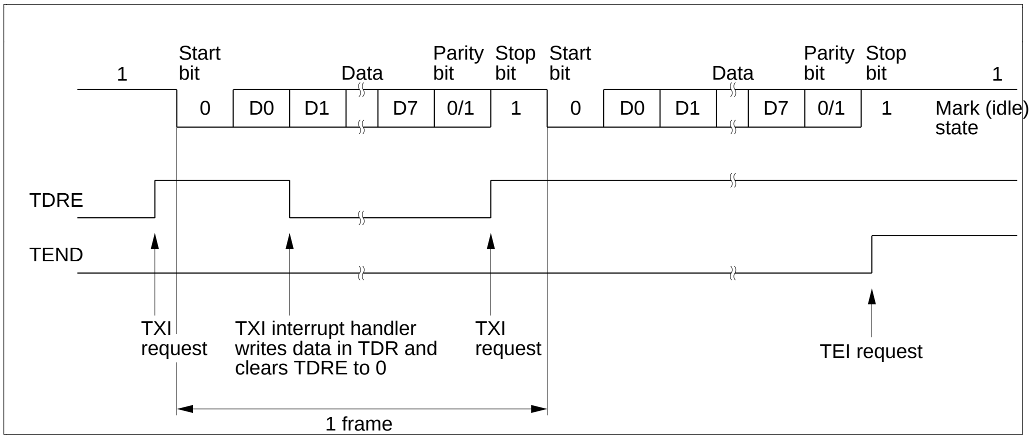
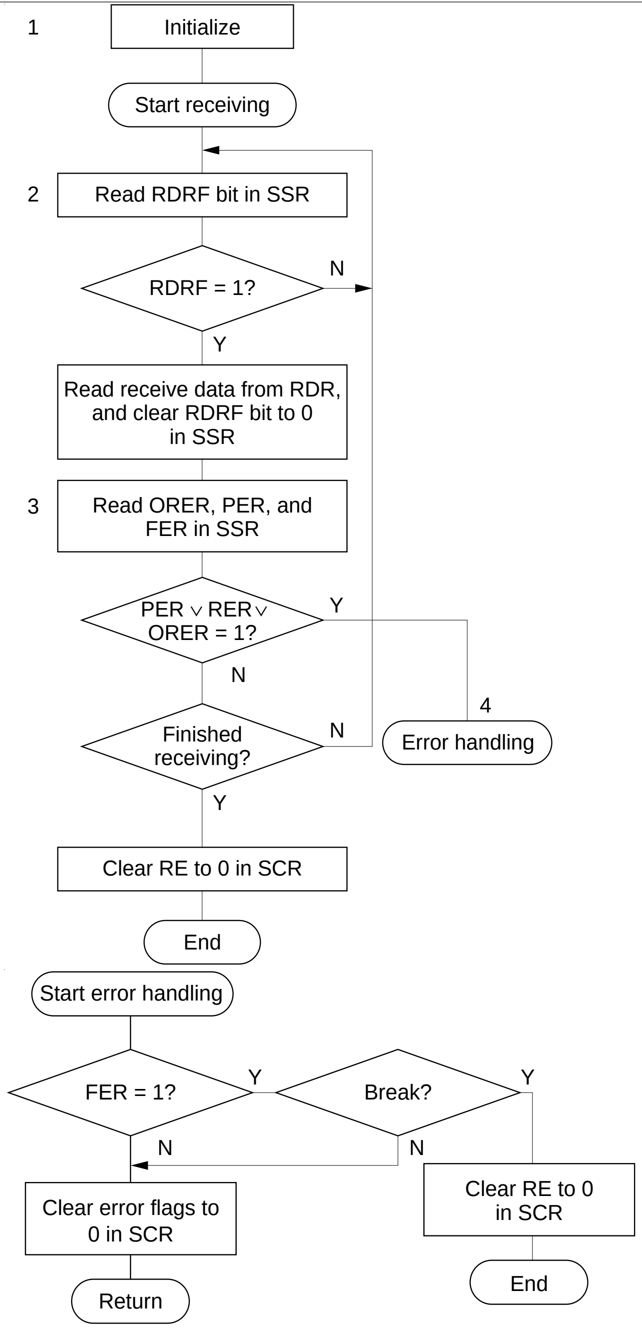


Figure 9-6 Example of SCI Transmit Operation (8-Bit Data with Parity and One Stop Bit)

- **Receiving Serial Data:** Follow the procedure in figure 9-7 for receiving serial data.



1. SCI initialization: the receive data function of the RxD pin is selected automatically.
2. SCI status check and receive data read: read the serial status register (SSR), check that RDRF is set to 1, then read receive data from the receive data register (RDR) and clear RDRF to 0.

   Transition of the RDRF bit from 0 to 1 can be reported by an RXI interrupt.
3. To continue receiving serial data: read RDR and clear RDRF to 0 before the stop bit of the current frame is received.
4. Receive error handling and break detection: if a receive error occurs, read the ORER, PER, and FER bits in SSR to identify the error. After executing the necessary error handling, clear ORER, PER, and FER all to 0. Transmitting and receiving cannot resume if ORER, PER, or FER remains set to 1.

   When a framing error occurs, the RxD pin can be read to detect the break state.

Figure 9-7 Sample Flowchart for Receiving Serial Data

In receiving, the SCI operates as follows.

1. The SCI monitors the receive data line and synchronizes internally when it detects a start bit.

2. Receive data are shifted into RSR in order from LSB to MSB.

3. The parity bit and stop bit are received.

   After receiving these bits, the SCI makes the following checks:

   a. Parity check: the number of 1s in the receive data must match the even or odd parity setting of the O/$\overline{\text{E}}$ bit in SMR.

   b. Stop bit check: the stop bit value must be 1. If there are two stop bits, only the first stop bit is checked.

   c. Status check: RDRF must be 0 so that receive data can be loaded from RSR into RDR.

   If these checks all pass, the SCI sets RDRF to 1 and stores the received data in RDR. If one of the checks fails (receive error), the SCI operates as indicated in table 9-8.

   Note: When a receive error flag is set, further receiving is disabled. The RDRF bit is not set to 1. Be sure to clear the error flags.

4. After setting RDRF to 1, if the RIE bit (receive-end interrupt enable) is set to 1 in SCR, the SCI requests an RXI (receive-end) interrupt. If one of the error flags (ORER, PER, or FER) is set to 1 and the RIE bit in SCR is also set to 1, the SCI requests an ERI (receive-error) interrupt.

Figure 9-8 shows an example of SCI receive operation in asynchronous mode.

Table 9-8 Receive Error Conditions and SCI Operation

Receive error	Abbreviation	Condition	Data transfer
Overrun error	ORER	Receiving of next data ends while RDRF is still set to 1 in SSR	Receive data not loaded from RSR into RDR
Framing error	FER	Stop bit is 0	Receive data loaded from RSR into RDR
Parity error	PER	Parity of receive data differs from even/odd parity setting in SMR	Receive data loaded from RSR into RDR

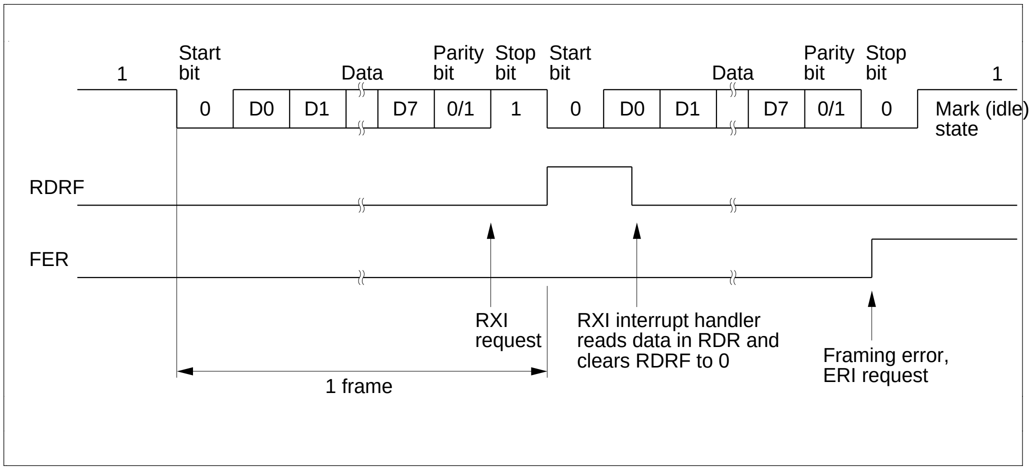


Figure 9-8 Example of SCI Receive Operation (8-Bit Data with Parity and One Stop Bit)

Multiprocessor Communication: The multiprocessor communication function enables several processors to share a single serial communication line. The processors communicate in asynchronous mode using a format with an additional multiprocessor bit (multiprocessor format).

In multiprocessor communication, each receiving processor is addressed by an ID.

A serial communication cycle consists of two cycles: an ID-sending cycle that identifies the receiving processor, and a data-sending cycle. The multiprocessor bit distinguishes ID-sending cycles from data-sending cycles.

The transmitting processor starts by sending the ID of the receiving processor with which it wants to communicate as data with the multiprocessor bit set to 1. Next the transmitting processor sends transmit data with the multiprocessor bit cleared to 0.

Receiving processors skip incoming data until they receive data with the multiprocessor bit set to 1.

After receiving data with the multiprocessor bit set to 1, the receiving processor with an ID matching the received data continues to receive further incoming data. Multiple processors can send and receive data in this way.

Four formats are available. Parity-bit settings are ignored when a multiprocessor format is selected. For details see table 9-7.

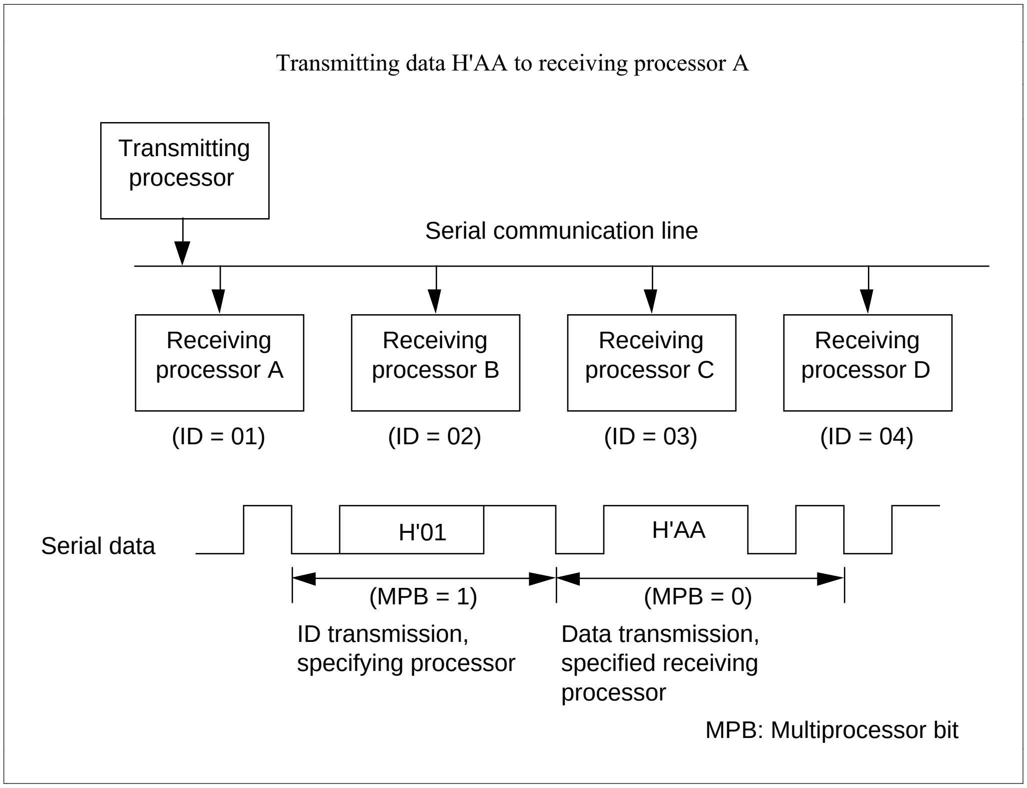
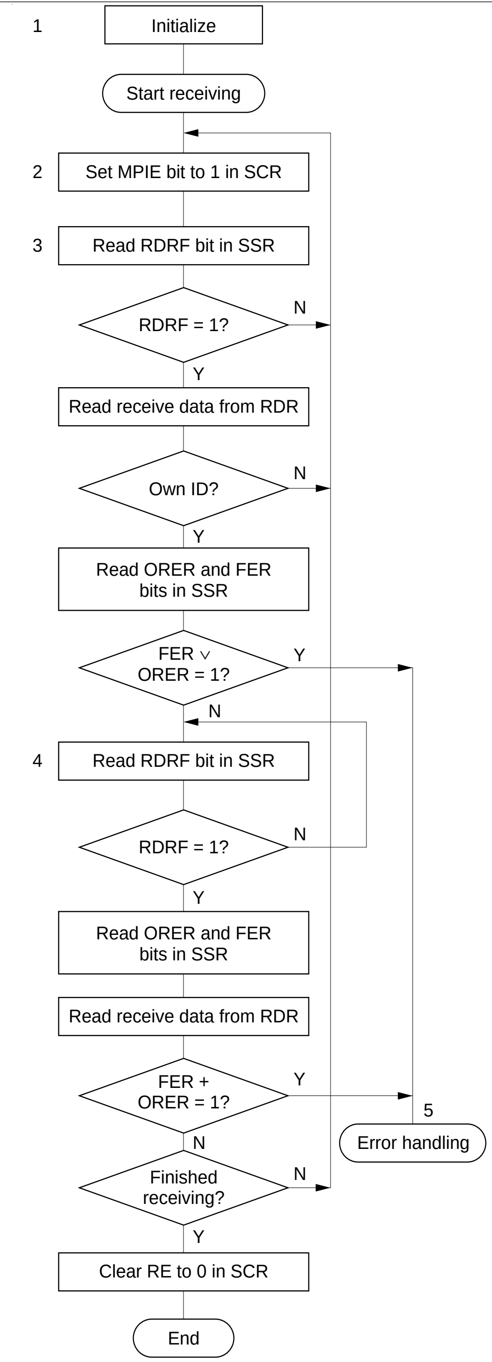


Figure 9-9 Example of Communication among Processors using Multiprocessor Format

Transmitting Multiprocessor Serial Data: See figures 9-5 and 9-6.

Receiving Multiprocessor Serial Data: Follow the procedure in figure 9-10 for receiving multiprocessor serial data.



1. SCI initialization: the receive data function of the RxD pin is selected automatically.
2. ID receive cycle: Set the MPIE bit in the serial control register to 1.
3. SCI status check and ID check: read the serial status register (SSR), check that RDRF is set to 1, then read receive data from the receive data register (RDR) and compare with the processor's own ID. Transition of the RDRF bit from 0 to 1 can be reported by an RXI interrupt. If the ID does not match the receive data, set MPIE to 1 again and clear RDRF to 0. If the ID matches the receive data, clear RDRF to 0.
4. SCI status check and data receiving: read SSR, check that RDRF is set to 1, then read data from the receive data register (RDR) and write 0 in the RDRF bit. Transition of the RDRF bit from 0 to 1 can be reported by an RXI interrupt.
5. Receive error handling and break detection: if a receive error occurs, read the ORER and FER bits in SSR to identify the error.

   After executing the necessary error handling, clear both ORER and FER to 0. Receiving cannot resume while ORER or FER remains set to 1. When a framing error occurs, the RxD pin can be read to detect the break state.

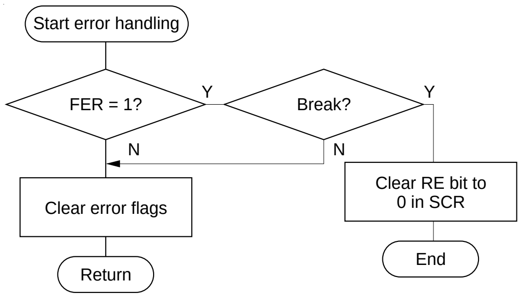


Figure 9-10   Sample Flowchart for Receiving Multiprocessor Serial Data

Figure 9-11 shows an example of SCI receive operation using a multiprocessor format.

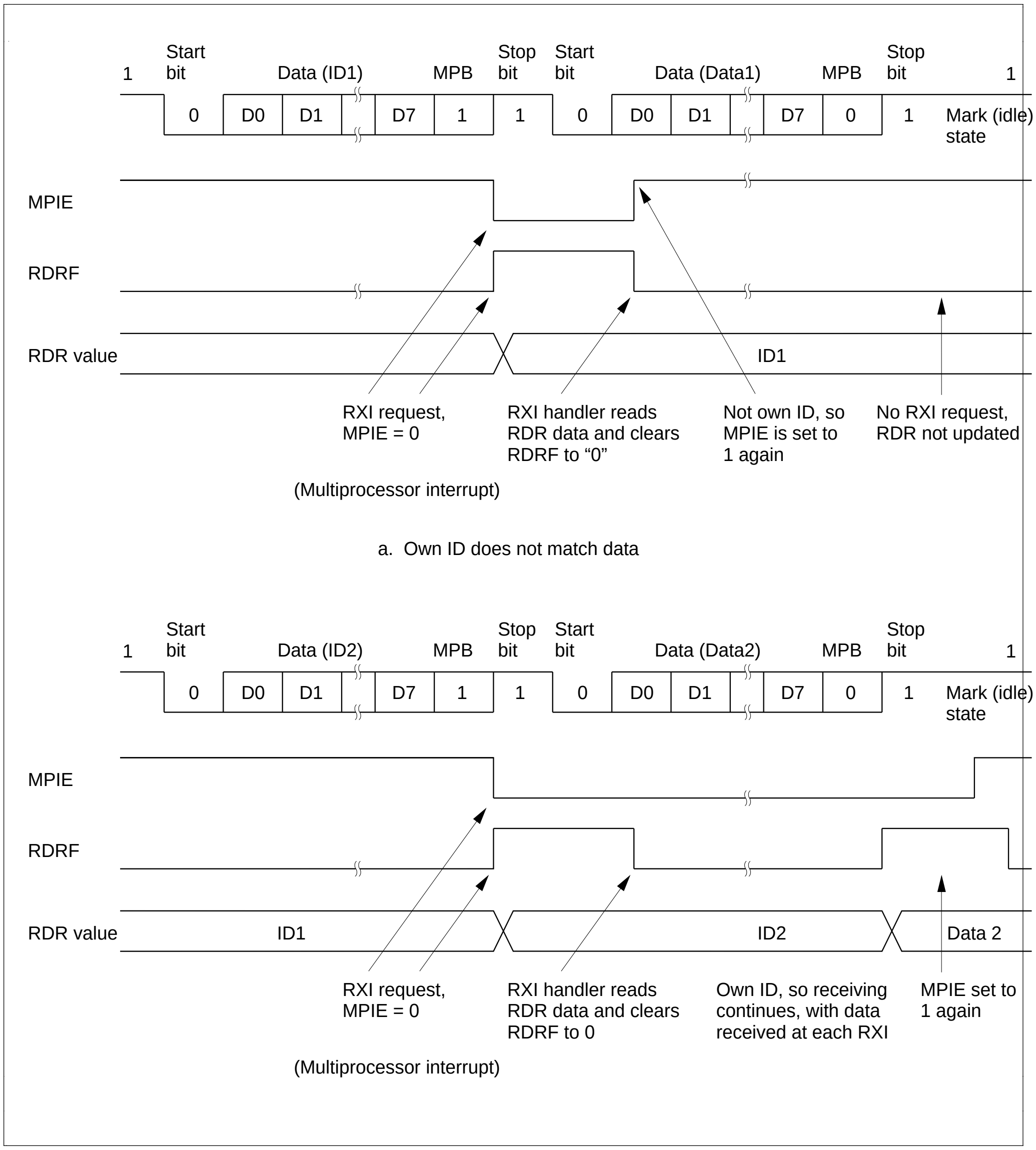


Figure 9-11 Example of SCI Receive Operation
(Eight-Bit Data with Multiprocessor Bit and One Stop Bit)

9.3.3 Synchronous Mode

In clocked synchronous mode, the SCI transmits and receives data in synchronization with clock pulses. This mode is suitable for high-speed serial communication.

The SCI transmitter and receiver share the same clock but are otherwise independent, so full duplex communication is possible. The transmitter and receiver are also double buffered, so continuous transmitting or receiving is possible by reading or writing data while transmitting or receiving is in progress.

Figure 9-12 shows the general format in clocked synchronous serial communication.

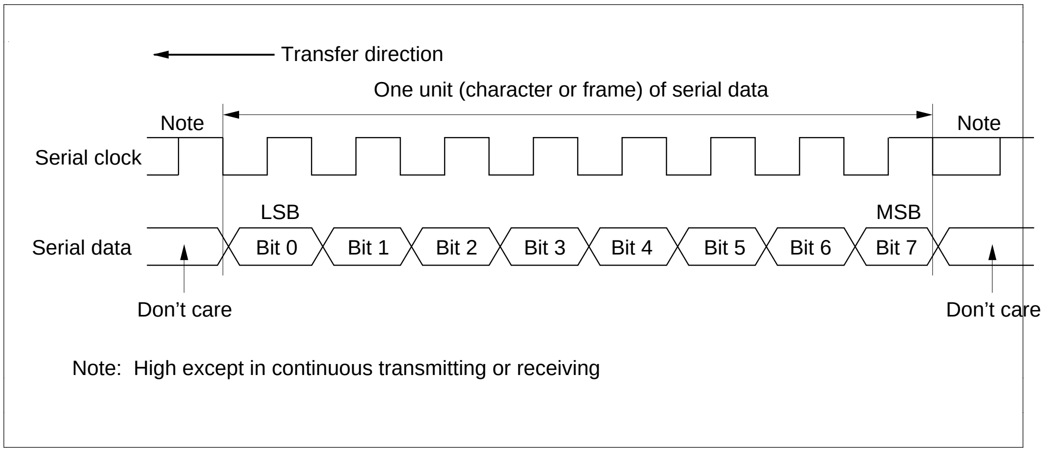


Figure 9-12 Data Format in Clocked Synchronous Communication

In clocked synchronous serial communication, each data bit is sent on the communication line from one falling edge of the serial clock to the next. Data are also received in synchronization with the rising edge of the serial clock.

In each character, the serial data bits are transmitted in order from LSB (first) to MSB (last). After output of the MSB, the communication line remains in the state of the MSB.

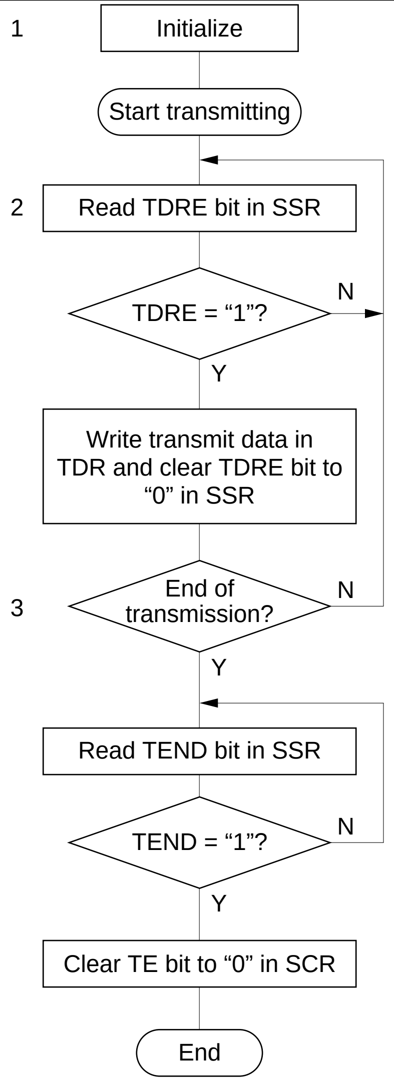
Communication Format: The data length is fixed at eight bits. No parity bit or multiprocessor bit can be added.

Clock: An internal clock generated by the on-chip baud rate generator or an external clock input from the SCK pin can be selected by clearing or setting the CKE1 bit in the serial control register (SCR). See table 9-6.

When the SCI operates on an internal clock, it outputs the clock signal at the SCK pin. Eight clock pulses are output per transmitted or received character. When the SCI is not transmitting or receiving, the clock signal remains at the high level.

SCI Initialization: The SCI must be initialized in the same way as in asynchronous mode. See figure 9-4. When switching from asynchronous mode to clocked synchronous mode, check that the ORER, FER, and PER bits are cleared to 0. Transmitting and receiving cannot begin if ORER, FER, or PER is set to 1.

Transmitting Serial Data: Follow the procedure below for transmitting serial data.



1. SCI initialization: the transmit data output function of the TxD pin is selected automatically.
2. SCI status check and transmit data write: read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR) and clear TDRE to 0.

   Transition of the TDRE bit from 0 to 1 can be reported by a TXI interrupt.
3. a. To continue transmitting serial data: read the TDRE bit to check whether it is safe to write; if so, write data in TDR, then clear TDRE to 0.

   b. To end serial transmission: end of transmission can be confirmed by checking transition of the TEND bit from 0 to 1. This can be reported by a TEI interrupt.

Figure 9-13 Sample Flowchart for Serial Transmitting

In transmitting serial data, the SCI operates as follows.

1. The SCI monitors the TDRE bit in SSR. When TDRE is cleared to 0 the SCI recognizes that the transmit data register (TDR) contains new data, and loads this data from TDR into the transmit shift register (TSR).

2. After loading the data from TDR into TSR, the SCI sets the TDRE bit to 1 and starts transmitting. If the TIE bit (TDR-empty interrupt enable) in SCR is set to 1, the SCI requests a TXI interrupt (TDR-empty interrupt) at this time.

If clock output is selected the SCI outputs eight serial clock pulses, triggered by the clearing of the TDRE bit to 0. If an external clock source is selected, the SCI outputs data in synchronization with the input clock.

Data are output from the TxD pin in order from LSB (bit 0) to MSB (bit 7).

3. The SCI checks the TDRE bit when it outputs the MSB (bit 7). If TDRE is 0, the SCI loads data from TDR into TSR, transmits the MSB, then begins serial transmission of the next frame. If TDRE is 1, the SCI sets the TEND bit in SSR to 1, transmits the MSB, then holds the output in the MSB state. If the TEIE bit (transmit-end interrupt enable) in SCR is set to 1, a TEI interrupt (TSR-empty interrupt) is requested at this time.
4. After the end of serial transmission, the SCK pin is held at the high level.

Figure 9-14 shows an example of SCI transmit operation.

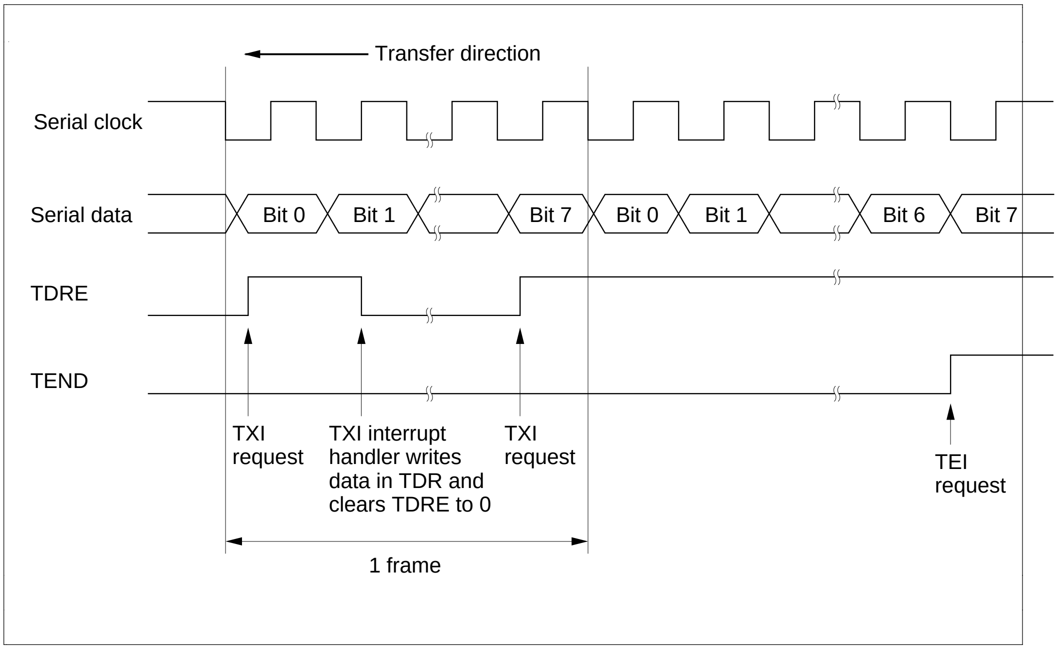
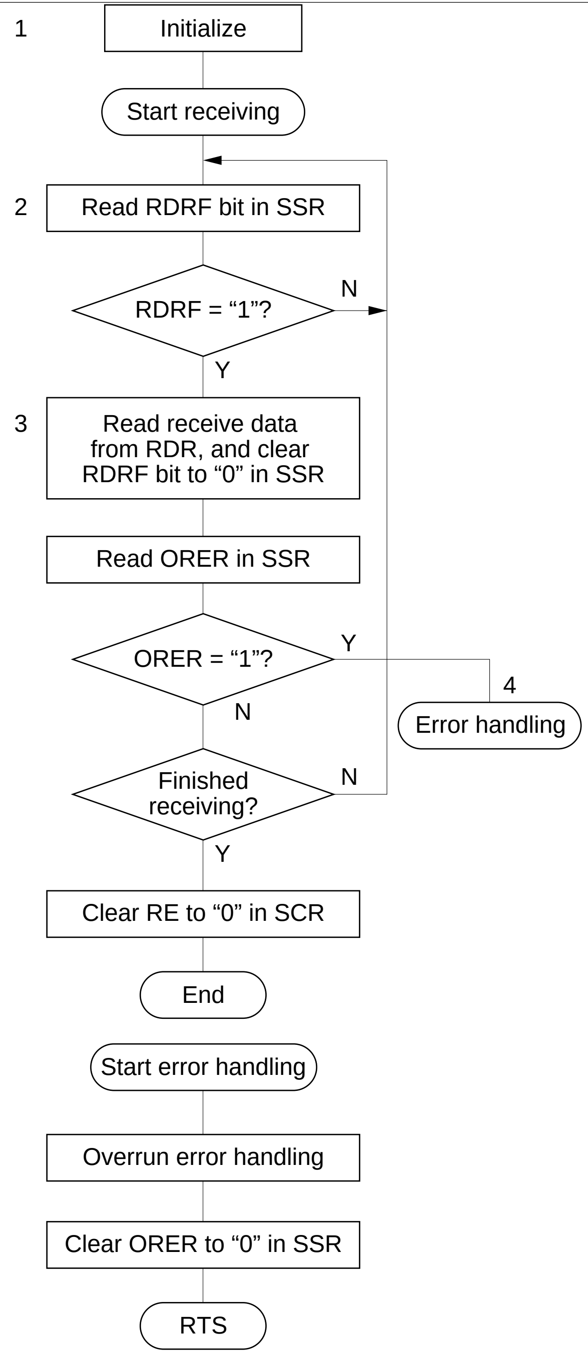


Figure 9-14 Example of SCI Transmit Operation

Receiving Serial Data: Follow the procedure in figure 9-15 for receiving serial data. When switching from asynchronous mode to clocked synchronous mode, be sure to check that PER and FER are cleared to 0. If PER or FER is set to 1 the RDRF bit will not be set and *both transmitting and receiving will be disabled*.



1. SCI initialization: the receive data function of the RxD pin is selected automatically.
2. SCI status check and receive data read: read the serial status register (SSR), check that RDRF is set to 1, then read receive data from the receive data register (RDR) and clear RDRF to 0.

   Transition of the RDRF bit from 0 to 1 can be reported by an RXI interrupt.
3. To continue receiving serial data: read RDR and clear RDRF to 0 before the MSB (bit 7) of the current frame is received.
4. Receive error handling: if a receive error occurs, read the ORER bit in SSR then, after executing the necessary error handling, clear ORER to 0. Neither transmitting nor receiving can resume while ORER remains set to 1. When clock output mode is selected, receiving can be halted temporarily by receiving one dummy byte and causing an overrun error. When preparations to receive the next data are completed, clear the ORER bit to 0. This causes receiving to resume, so return to the step marked 2 in the flowchart.

Figure 9-15 Sample Flowchart for Serial Receiving

In receiving, the SCI operates as follows.

1. If an external clock is selected, data are input in synchronization with the input clock. If clock output is selected, as soon as the RE bit is set to 1 the SCI begins outputting the serial clock and inputting data. If clock output is stopped because the ORER bit is set to 1, output of the serial clock and input of data resume as soon as the ORER bit is cleared to 0.
2. Receive data are shifted into RSR in order from LSB to MSB.

   After receiving the data, the SCI checks that RDRF is 0 so that receive data can be loaded from RSR into RDR. If this check passes, the SCI sets RDRF to 1 and stores the received data in RDR. If the check does not pass (receive error), the SCI operates as indicated in table 9-8.

   Note: *Both transmitting and receiving are disabled while a receive error flag is set.* The RDRF bit is not set to 1. Be sure to clear the error flag.
3. After setting RDRF to 1, if the RIE bit (receive-end interrupt enable) is set to 1 in SCR, the SCI requests an RXI (receive-end) interrupt. If the ORER bit is set to 1 and the RIE bit in SCR is set to 1, the SCI requests an ERI (receive-error) interrupt.

   When clock output mode is selected, clock output stops when the RE bit is cleared to 0 or the ORER bit is set to 1. To prevent clock count errors, it is safest to receive one dummy byte and generate an overrun error.

Figure 9-16 shows an example of SCI receive operation.

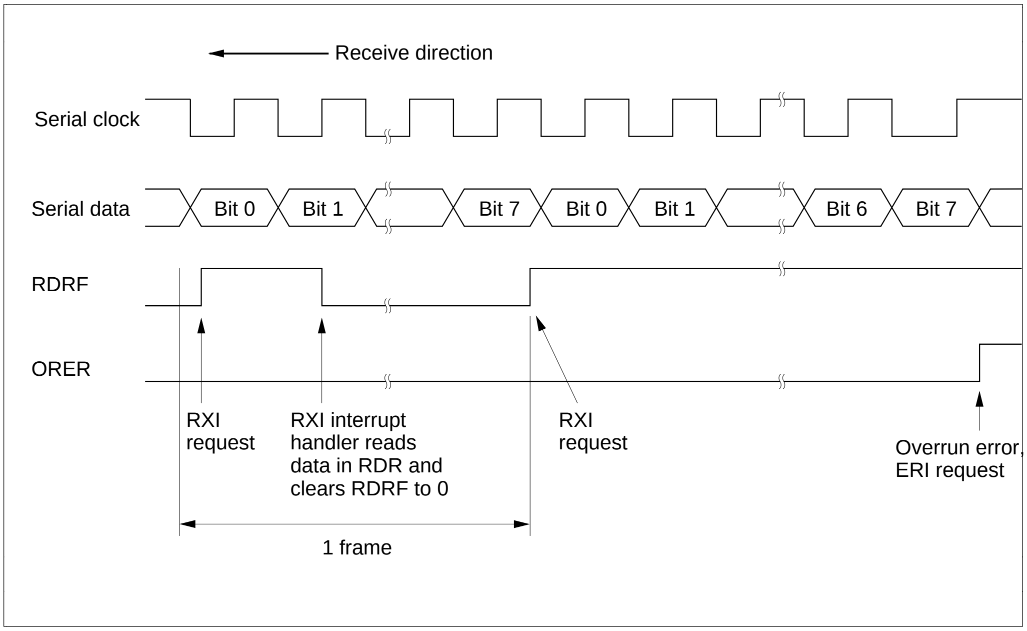
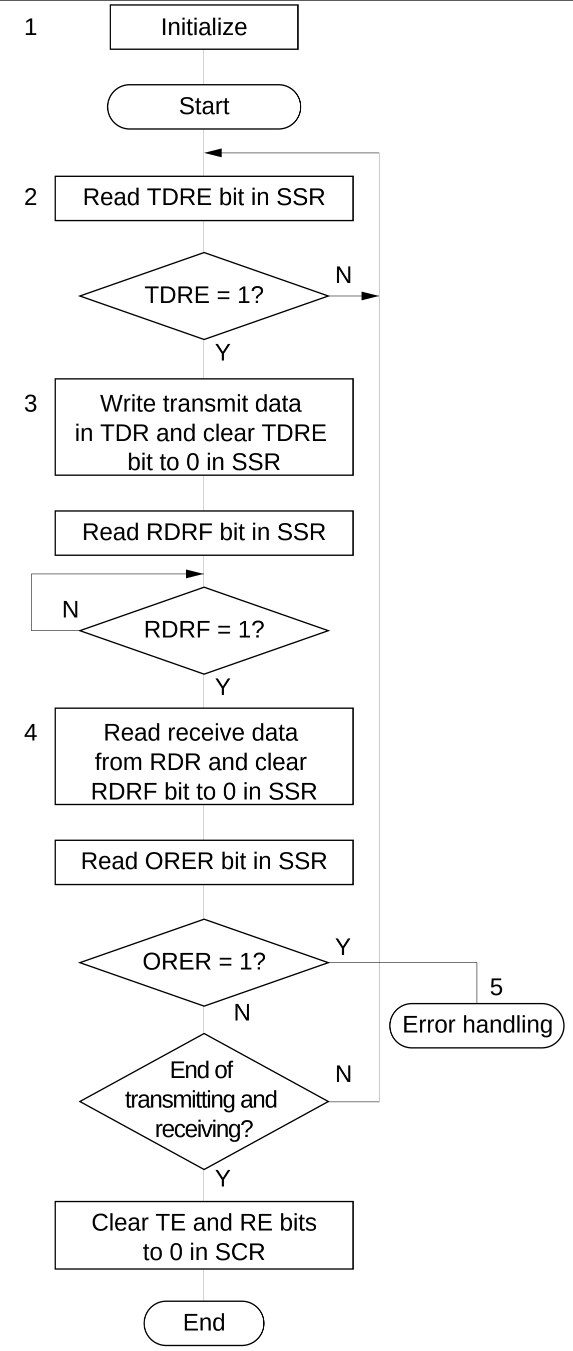


Figure 9-16 Example of SCI Receive Operation

Transmitting and Receiving Serial Data Simultaneously: Follow the procedure in figure 9-17 for transmitting and receiving serial data simultaneously. If clock output mode is selected, output of the serial clock begins simultaneously with serial transmission.


1
Initialize
Start
2
Read TDRE bit in SSR
TDRE = 1?
N
Y
3
Write transmit data in TDR and clear TDRE bit to 0 in SSR
Read RDRF bit in SSR
N
RDRF = 1?
Y
4
Read receive data from RDR and clear RDRF bit to 0 in SSR
Read ORER bit in SSR
ORER = 1?
Y
5
Error handling
N
End of transmitting and receiving?
N
Y
Clear TE and RE bits to 0 in SCR
End

1. SCI initialization: the transmit data output function of the TxD pin and receive data input function of the RxD pin are selected, enabling simultaneous transmitting and receiving.
2. SCI status check and transmit data write: read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR) and clear TDRE to 0. Transition of the TDRE bit from 0 to 1 can be reported by a TXI interrupt.
3. SCI status check and receive data read: read the serial status register (SSR), check that the RDRF bit is 1, then read receive data from the receive data register (RDR) and clear RDRF to 0. Transition of the RDRF bit from 0 to 1 can be reported by an RXI interrupt.
4. To continue transmitting and receiving serial data: read RDR and clear RDRF to 0 before the MSB (bit 7) of the current frame is received. Also read the TDRE bit and check that it is set to 1, indicating that it is safe to write; then write data in TDR and clear TDRE to 0 before the MSB (bit 7) of the current frame is transmitted.
5. Receive error handling: if a receive error occurs, read the ORER bit in SSR then, after executing the necessary error handling, clear ORER to 0. Neither transmitting nor receiving can resume while ORER remains set to 1.

Figure 9-17 Sample Flowchart for Serial Transmitting and Receiving

Note: In switching from transmitting or receiving to simultaneous transmitting and receiving, follow one of the procedures given next:

1. Clear both TE and RE to 0, then set both TE and RE to 1.
2. When TE = 1 (transmitting): Check that the SCI is in the idle state waiting for transmit data (TDRE = 1), then set RE to 1.
3. When RE = 1 (receiving): Check that the SCI has finished receiving (RDRF = 1) and is in the idle state, then set TE to 1.

9.4 Interrupts

The SCI can request four types of interrupts: ERI, RXI, TXI, and TEI. Table 9-9 indicates the source and priority of these interrupts. The interrupt sources can be enabled or disabled by the TIE, RIE, and TEIE bits in the SCR. Independent signals are sent to the interrupt controller for each interrupt source, except that the receive-error interrupt (ERI) is the logical OR of three sources: overrun error, framing error, and parity error.

The TXI interrupt indicates that the next transmit data can be written. The TEI interrupt indicates that the SCI has stopped transmitting data.

Table 9-9 SCI Interrupt Sources

Interrupt	Description	Priority
ERI	Receive-error interrupt (ORER, FER, or PER)	High
RXI	Receive-end interrupt (RDRF)	↑
TXI	TDR-empty interrupt (TDRE)	↓
TEI	TSR-empty interrupt (TEND)	Low

9.5 Application Notes

Application programmers should note the following features of the SCI.

9.5.1 TDR Write

The TDRE bit in the SSR is simply a flag that indicates that the TDR contents have been transferred to the TSR. The TDR contents can be rewritten regardless of the TDRE value. If a new byte is written in the TDR while the TDRE bit is 0, before the old TDR contents have been moved into the TSR, the old byte will be lost. Software should check that the TDRE bit is set to 1 before writing to the TDR.

9.5.2 Multiple Receive Errors

Table 9-10 lists the values of flag bits in the SSR when multiple receive errors occur, and indicates whether the RSR contents are transferred to the RDR.

Table 9-10 SSR Bit States and Data Transfer When Multiple Receive Errors Occur

	SSR Bits				
Receive Error	**RDRF**	**ORER**	**FER**	**PER**	**RSR → RDR** [Note 2]
Overrun error	1 [Note 1]	1	0	0	No
Framing error	0	0	1	0	Yes
Parity error	0	0	0	1	Yes
Overrun + framing errors	1 [Note 1]	1	1	0	No
Overrun + parity errors	1 [Note 1]	1	0	1	No
Framing + parity errors	0	0	1	1	Yes
Overrun + framing + parity errors	1 [Note 1]	1	1	1	No

Notes: 1. Set to 1 before the overrun error occurs.

2. Yes: The RSR contents are transferred to the RDR.

No: The RSR contents are not transferred to the RDR.

9.5.3 Line Break Detection

When the RxD pin receives a continuous stream of 0s in asynchronous mode (line-break state), a framing error occurs because the SCI detects a 0 stop bit. The value H'00 is transferred from the RSR to the RDR. Software can detect the line-break state as a framing error accompanied by H'00 data in the RDR.

The SCI continues to receive data, so if the FER bit is cleared to 0 another framing error will occur.

9.5.4 Sampling Timing and Receive Margin in Asynchronous Mode

The serial clock used by the SCI in asynchronous mode runs at 16 times the baud rate. The falling edge of the start bit is detected by sampling the RxD input on the falling edge of this clock. After the start bit is detected, each bit of receive data in the frame (including the start bit, parity bit, and stop bit or bits) is sampled on the rising edge of the serial clock pulse at the center of the bit. See figure 9-18.

It follows that the receive margin can be calculated as in equation (1).

When the absolute frequency deviation of the clock signal is 0 and the clock duty factor is 0.5, data can theoretically be received with distortion up to the margin given by equation (2). This is a theoretical limit, however. In practice, system designers should allow a margin of 20% to 30%.

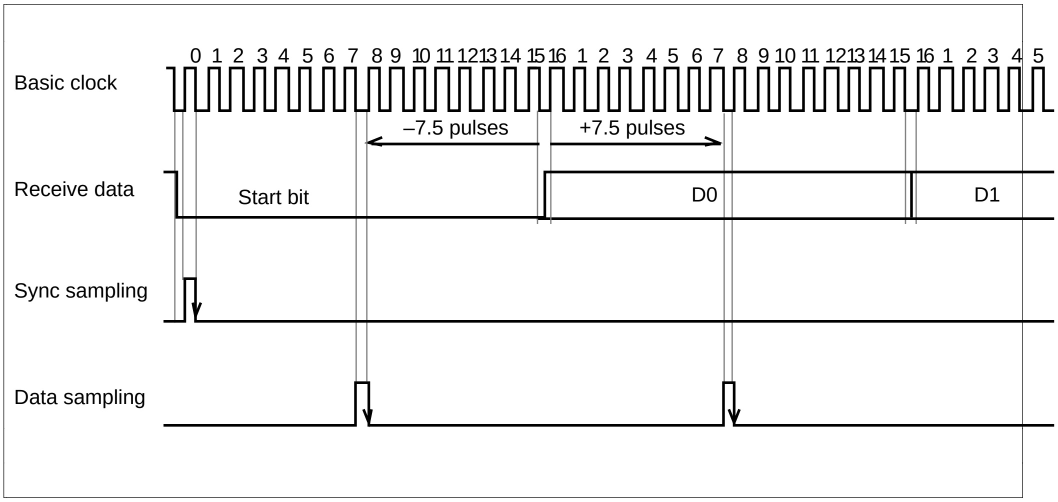


Figure 9-18 Sampling Timing (Asynchronous Mode)

$M = \{(0.5 - 1/2N) - (D - 0.5)/N - (L - 0.5)F\} \times 100$ [%] (1)

M: Receive margin
N: Ratio of basic clock to baud rate (N=16)
D: Duty factor of clock—ratio of high pulse width to low width (0.5 to 1.0)
L: Frame length (9 to 12)
F: Absolute clock frequency deviation

When D = 0.5 and F = 0:

$M = (0.5 - 1/2 \times 16) \times 100$ [%] = 46.875% (2)

Section 10 A/D Converter

10.1 Overview

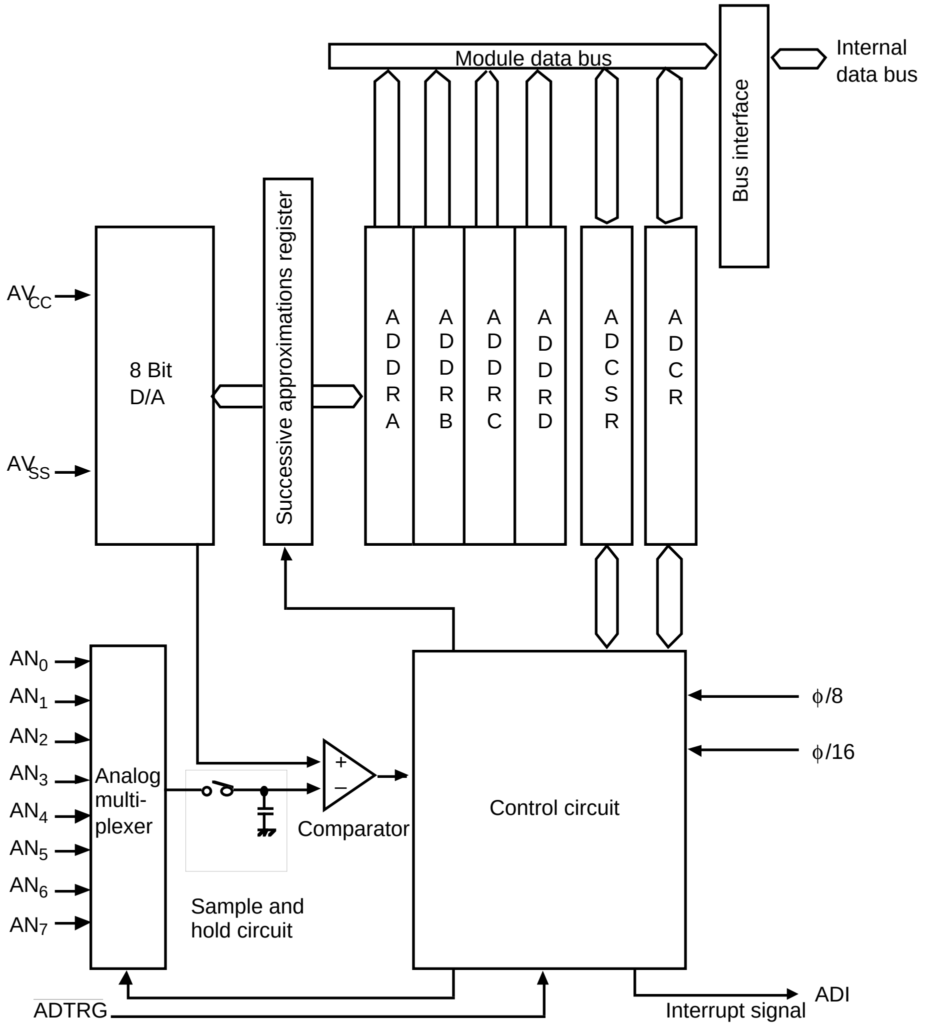
The H8/3332 includes an analog-to-digital converter module with eight input channels. A/D conversion is performed by the successive approximations method with 8-bit resolution.

10.1.1 Features

The features of the on-chip A/D module are:

- 8-bit resolution
- Eight analog input channels
- Rapid conversion
  Conversion time is 12.2 µs per channel (minimum) with a 10 MHz system clock
- Single and scan modes
  - Single mode: A/D conversion is performed once
  - Scan mode: A/D conversion is performed in a repeated cycle on one to four channels
- Four 8-bit data registers
  Store A/D conversion results for up to four channels
- A CPU interrupt (ADI) can be requested at the completion of each A/D conversion cycle.
- External triggering can be selected

10.1.2 Block Diagram



ADCR:	A/D Control Register (8 bits)
ADCSR:	A/D Control/Status Register (8 bits)
ADDRA:	A/D Data Register A (8 bits)
ADDRB:	A/D Data Register B (8 bits)
ADDRC:	A/D Data Register C (8 bits)
ADDRD:	A/D Data Register D (8 bits)

Figure 10-1 Block Diagram of A/D Converter

10.1.3 Input Pins

Table 10-1 lists the input pins used by the A/D converter module.

The eight analog input pins are divided into two groups, consisting of analog inputs 0 to 3 (AN_0 to AN_3) and analog inputs 4 to 7 (AN_4 to AN_7), respectively.

Table 10-1 A/D Input Pins

Name	Abbreviation	I/O	Function
Analog supply voltage	AV_{CC}	Input	Power supply and reference voltage for the analog circuits
Analog ground	AV_{SS}	Input	Ground and reference voltage for the analog circuits
Analog input 0	AN_0	Input	Analog input pins, group 0
Analog input 1	AN_1	Input	
Analog input 2	AN_2	Input	
Analog input 3	AN_3	Input	
Analog input 4	AN_4	Input	Analog input pins, group 1
Analog input 5	AN_5	Input	
Analog input 6	AN_6	Input	
Analog input 7	AN_7	Input	
A/D external trigger	$\overline{\text{ADTRG}}$	Input	External trigger for starting A/D conversion

10.1.4 Register Configuration

Table 10-2 lists the registers of the A/D converter module.

Table 10-2 A/D Registers

Name	Abbreviation	R/W	Initial Value	Address
A/D data register A	ADDRA	R	H'00	H'FFE0
A/D data register B	ADDRB	R	H'00	H'FFE2
A/D data register C	ADDRC	R	H'00	H'FFE4
A/D data register D	ADDRD	R	H'00	H'FFE6
A/D control/status register	ADCSR	R/(W) Note	H'00	H'FFE8
A/D control register	ADCR	R/W	H'7E	H'FFEA

Note: Software can write a 0 to clear bit 7, but cannot write a 1 in this bit.

10.2 Register Descriptions

10.2.1 A/D Data Registers (ADDRA–ADDRD)—H'FFE0 to H'FFE6

Bit	7	6	5	4	3	2	1	0
ADDRn								
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Note: n = A, B, C, D

The four A/D data registers (ADDRA to ADDRD) are 8-bit read-only registers that store the results of A/D conversion. Each data register is assigned to two analog input channels as indicated in table 10-3.

The A/D data registers can always be read by the CPU.

The A/D data registers are initialized to H'00 at a reset and in the standby modes.

Table 10-3 Assignment of Data Registers to Analog Input Channels

Analog Input Channel		
Group 0	**Group 1**	**A/D data register**
AN_0	AN_4	ADDRA
AN_1	AN_5	ADDRB
AN_2	AN_6	ADDRC
AN_3	AN_7	ADDRD

10.2.2 A/D Control/Status Register (ADCSR)—H'FFE8

Bit	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Software can write a 0 in bit 7 to clear the flag, but cannot write a 1 in this bit.

The A/D control/status register (ADCSR) is an 8-bit read/write register that controls the operation of the A/D converter module.

The ADCSR is initialized to H'00 at a reset and in the standby modes.

Bit 7: A/D End Flag (ADF): The ADF status flag indicates the end of one cycle of A/D conversion.

Bit 7: ADF	Description
0	To clear ADF, the CPU must read ADF after it has been set to 1, then write a 0 in this bit (Initial value)
1	ADF is set to 1 at the following times: 1. Single mode: when one A/D conversion is completed 2. Scan mode: when inputs on all selected channels have been converted

Bit 6: A/D Interrupt Enable (ADIE): Selects whether to request an A/D interrupt (ADI) when A/D conversion is completed.

Bit 6: ADIE	Description
0	The A/D interrupt request (ADI) is disabled (Initial value)
1	The A/D interrupt request (ADI) is enabled

Bit 5: A/D Start (ADST): The A/D converter operates while ADST is set to 1. In the single mode, this bit is automatically cleared to 0 at the end of each A/D conversion.

Bit 5: ADST	Description
0	A/D conversion is halted (Initial value)
1	1. Single mode: One A/D conversion is performed. The ADST bit is automatically cleared to 0 at the end of the conversion. 2. Scan mode: A/D conversion starts and continues cyclically on the selected channels until the ADST bit is cleared to 0 by software (or a reset, or by entry to a standby mode)

Bit 4: Scan Mode (SCAN): Selects the scan mode or single mode of operation. See Section 10.3, Operation, for descriptions of these modes.

The mode should be changed only when the ADST bit is cleared to 0.

Bit 4: SCAN	Description
0	Single mode (Initial value)
1	Scan mode

Bit 3: Clock Select (CKS): Controls the A/D conversion time.

The conversion time should be changed only when the ADST bit is cleared to 0.

Bit 3: CKS	Description	
0	Conversion time = 242 states (max.)	(Initial value)
1	Conversion time = 122 states (max.)	

Bits 2 to 0: Channel Select 2 to 0 (CH2 to CH0): CH2–CH0 and the SCAN bit combine to select one or more analog input channels.

The channel selection should be changed only when the ADST bit is cleared to 0.

Group Select	Channel Select		Selected Channels	
CH2	**CH1**	**CH0**	**Single Mode**	**Scan Mode**
0	0	0	AN_0 (Initial value)	AN_0
	0	1	AN_1	AN_0, AN_1
	1	0	AN_2	AN_0 to AN_2
	1	1	AN_3	AN_0 to AN_3
1	0	0	AN_4	AN_4
	0	1	AN_5	AN_4, AN_5
	1	0	AN_6	AN_4 to AN_6
	1	1	AN_7	AN_4 to AN_7

10.2.3 A/D Control Register (ADCR)—H'FFEA

Bit	7	6	5	4	3	2	1	0
	TRGE	—	—	—	—	—	—	CHS
Initial value	0	1	1	1	1	1	1	0
Read/Write	R/W	—	—	—	—	—	—	R/W

The A/D control register (ADCR) is an 8-bit read/write register that enables or disables the A/D external trigger signal.

The ADCR is initialized to H'7E at a reset and in the standby modes.

Bit 7: Trigger Enable (TRGE): Enables the $\overline{\text{ADTRG}}$ (A/D external trigger) signal to set the ADST bit and start A/D conversion.

Bit 7: TRGE	Description
0	A/D external trigger is disabled. $\overline{\text{ADTRG}}$ does not set the ADST bit (Initial value)
1	A/D external trigger is enabled. $\overline{\text{ADTRG}}$ sets the ADST bit (The ADST bit can also be set by software)

Bits 6 to 1: Reserved: Cannot be modified and are always read as 1.

Bit 0: Channel Set Select (CHS): Reserved. Does not affect any operation of the H8/3332.

10.3 Operation

The A/D converter performs 8 successive approximations to obtain a result ranging from H'00 (corresponding to AVSS) to H'FF (corresponding to AVCC).

The A/D converter module can be programmed to operate in single mode or scan mode as explained below.

10.3.1 Single Mode (SCAN = 0)

The single mode is suitable for obtaining a single data value from a single channel. A/D conversion starts when the ADST bit is set to 1, either by software or by a high-to-low transition of the $\overline{\text{ADTRG}}$ signal (if enabled). During the conversion process the ADST bit remains set to 1. When conversion is completed, the ADST bit is automatically cleared to 0.

When the conversion is completed, the ADF bit is set to 1. If the interrupt enable bit (ADIE) is also set to 1, an A/D conversion end interrupt (ADI) is requested, so that the converted data can be processed by an interrupt-handling routine. The ADF bit is cleared when software reads the A/D control/status register (ADCSR), then writes a 0 in this bit.

Before selecting the single mode, clock, and analog input channel, software should clear the ADST bit to 0 to make sure the A/D converter is stopped. Changing the mode, clock, or channel selection while A/D conversion is in progress can lead to conversion errors. A/D conversion begins when the ADST bit is set to 1 again. The same instruction can be used to alter the mode and channel selection and set ADST to 1.

The following example explains the A/D conversion process in single mode when channel 1 (AN1) is selected and the external trigger is disabled. Figure 10-2 shows the corresponding timing chart.

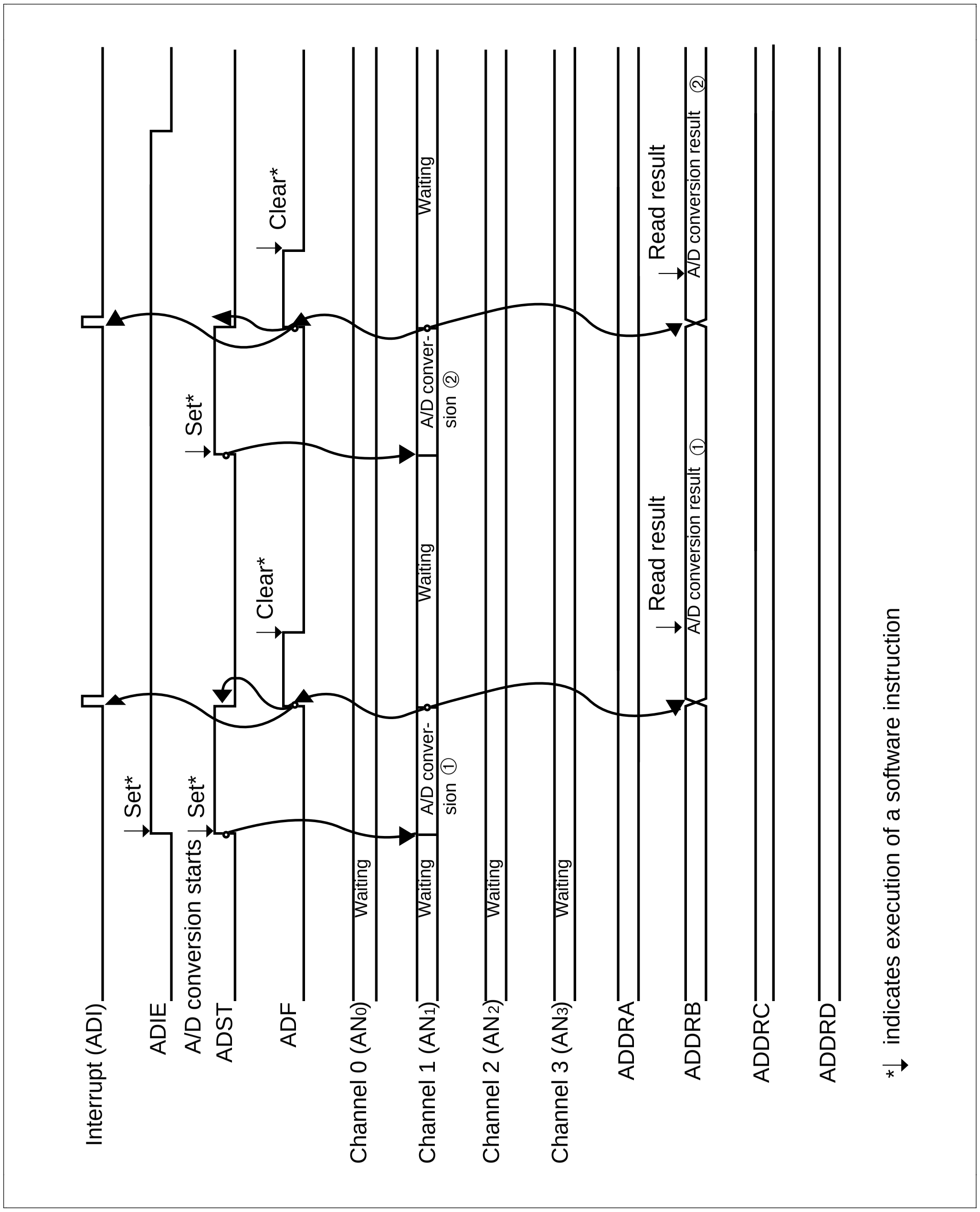


Figure 10-2 A/D Operation in Single Mode (Channel 1 Selected)

1. Software clears the ADST bit to 0, then selects the single mode (SCAN = 0) and channel 1 (CH2 to CH0 = “001”), enables the A/D interrupt request (ADIE = 1), and sets the ADST bit to 1 to start A/D conversion.

   Coding example (when using the slow clock, CKS = 0):

```
BCLR #5, @H'FFE8      ;Clear ADST
MOV.B #H'7F, ROL
MOV.B ROL, @H'FFEA  ;Disable external trigger
MOV.B #H'61, ROL
MOV.B ROL, @H'FFE8  ;Select mode and channel and set ADST to 1
```

Value set in ADCSR:

ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
0	1	1	0	0	0	0	1

2. The A/D converter converts the voltage level at the AN$_1$ input pin to a digital value. At the end of the conversion process the A/D converter transfers the result to register ADDRB, sets the ADF bit is set to 1, clears the ADST bit to 0, and halts.

3. ADF = 1 and ADIE = 1, so an A/D interrupt is requested.

4. The user-coded A/D interrupt-handling routine is started.

5. The interrupt-handling routine reads the ADCSR value, then writes a 0 in the ADF bit to clear this bit to 0.

6. The interrupt-handling routine reads and processes the A/D conversion result.

7. The routine ends.

Steps 2 to 7 can now be repeated by setting the ADST bit to 1 again.

10.3.2 Scan Mode (SCAN = 1)

The scan mode can be used to monitor analog inputs on one or more channels. When the ADST bit is set to 1, either by software or by a high-to-low transition of the $\overline{\text{ADTRG}}$ signal (if enabled), A/D conversion starts from the first channel selected by the CH bits. When CH2 = 0 the first channel is AN$_0$. When CH2 = 1 the first channel is AN$_4$.

If the scan group includes more than one channel (that is, if bit CH1 or CH0 is set), conversion of the next channel begins as soon as conversion of the first channel ends.

Conversion of the selected channels continues cyclically until the ADST bit is cleared to 0. The conversion results are placed in the data registers corresponding to the selected channels. The A/D data registers are readable by the CPU.

Before selecting the scan mode, clock, and analog input channels, software should clear the ADST bit to 0 to make sure the A/D converter is stopped. Changing the mode, clock, or channel selection while A/D conversion is in progress can lead to conversion errors. A/D conversion begins when the ADST bit is set to 1 again. The same instruction can be used to alter the mode and channel selection and set ADST to 1.

The following example explains the A/D conversion process when three channels in group 0 are selected (AN_0, AN_1, and AN_2) and the external trigger is disabled. Figure 10-3 shows the corresponding timing chart.

1. Software clears the ADST bit to 0, then selects the scan mode (SCAN = 1), scan group 0 (CH2 = 0), and analog input channels AN_0 to AN_2 (CH1 and CH0 = 0) and sets the ADST bit to 1 to start A/D conversion.

   Coding example (with slow clock and ADI interrupt enabled):

   ```
   BCLR #5, @H'FFE8    ;Clear ADST
   MOV.B #H'7F, R0L
   MOV.B R0L, @H'FFEA  ;Disable external trigger
   MOV.B #H'72, R0L
   MOV.B R0L, @H'FFE8  ; Select mode and channels and set ADST to 1
   ```

   Value set in ADCSR:

ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
0	1	1	1	0	0	1	0

2. The A/D converter converts the voltage level at the AN_0 input pin to a digital value, and transfers the result to register ADDRA.

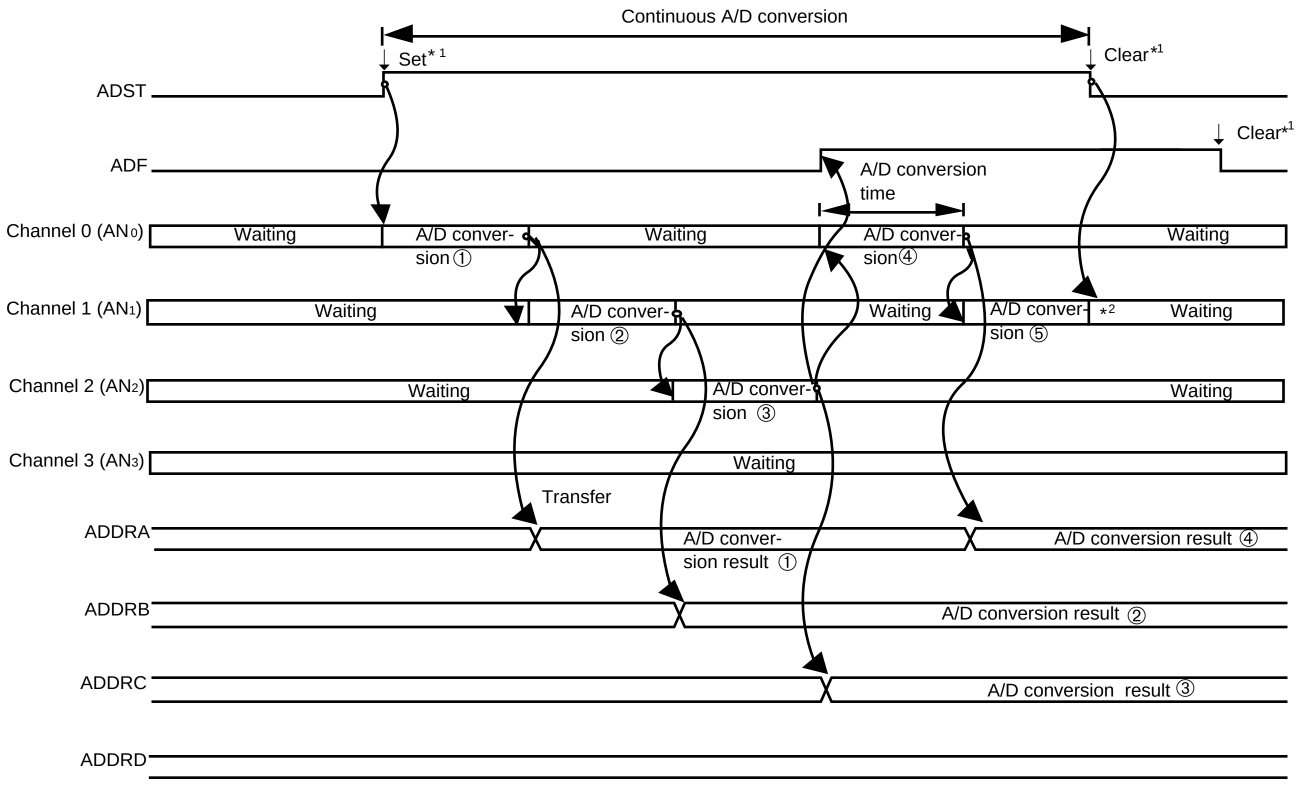
3. Next the A/D converter converts AN_1 and transfers the result to ADDRB. Then it converts AN2 and transfers the result to ADDRC.

4. After all selected channels (AN_0 to AN_2) have been converted, the AD converter sets the ADF bit to 1. If the ADIE bit is set to 1, an A/D interrupt (ADI) is requested. Then the A/D converter begins converting AN_0 again.

5. Steps 2 to 4 are repeated cyclically as long as the ADST bit remains set to 1.

To stop the A/D converter, software must clear the ADST bit to 0.

Regardless of which channel is being converted when the ADST bit is cleared to 0, when the ADST bit is set to 1 again, conversion begins from the first selected channel (AN_0 or AN_4).



*1 ↓ indicates execution of a software instruction

*2 Data undergoing conversion when ADST bit is cleared are ignored.

Figure 10-3 A/D Operation in Scan Mode (When Channels 0 to 2 are Selected)

Note: If the ADST bit is cleared to 0 when two or more channels are selected in the scan mode, incorrect values may be left in the A/D data registers. For this reason, in the scan mode the A/D data registers should be read while the ADST bit is still set to 1.

Example: The following coding example sets up a four-channel A/D scan, and shows the first part of an ADI interrupt handler for reading the converted data. Note that the data are read before the ADST bit is cleared.

```
MOV.B      #5B   , R0L
MOV.B      R0L   , @ADCSR      ; Four-channel scan mode
BSET #5    , @ADCSR      ; Start conversion (set ADST)
```

(Conversion of four channels)

```
ADI:  MOV.B   @ADDRA     , R1               ; Read ADDRA
      MOV.B   @ADDRB     , R2               ; Read ADDRB
      MOV.B   @ADDRC     , R3               ; Read ADDRC
      MOV.B   @ADDRD     , R4               ; Read ADDRD
      BCLR    #5         , @ADCSR           ; Clear ADST
      BCLR    #7         , @ADCSR           ; Clear ADF
```

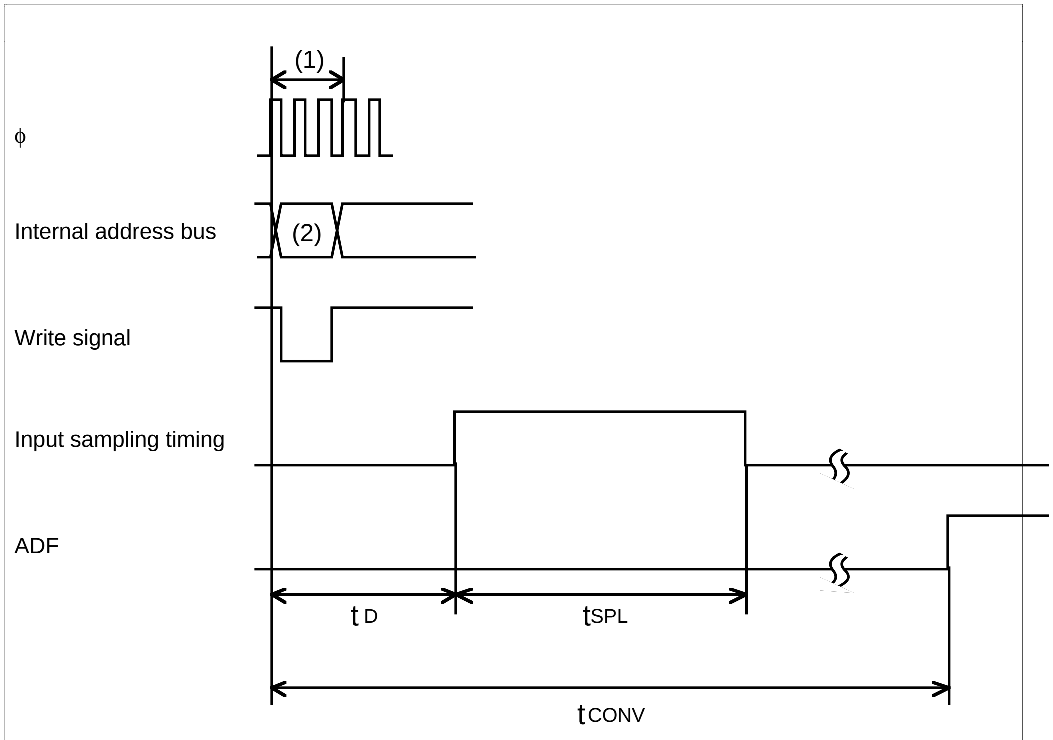
(It is not necessary to clear the ADST bit in order to read ADDRA to ADDRD.)

10.3.3 Input Sampling Time and A/D Conversion Time

The A/D converter includes a built-in sample-and-hold circuit. Sampling of the input starts at a time tD after the ADST bit is set to 1. The sampling process lasts for a time tSPL. The actual A/D conversion begins after sampling is completed. Figure 10-4 shows the timing of these steps. Table 10-4 lists the conversion times for the single mode. Table 10-5 lists the conversion times for the scan mode.

The total conversion time (tCONV) includes tD and tSPL. The purpose of tD is to synchronize the ADCSR write time with the A/D conversion process, so the length of tD is variable. The total conversion time therefore varies within the minimum to maximum ranges indicated in tables 10-4 and 10-5.

In the scan mode, the ranges given in table 10-5 apply to the first conversion. The length of the second and subsequent conversion processes is fixed at 256 states (when CKS = 0) or 128 states (when CKS = 1).



(1): ADCSR write cycle

(2): ADCSR address

t_D: Synchronization delay

t_{SPL}: Input sampling time

t_{CONV}: Total A/D conversion time

Figure 10-4 A/D Conversion Timing

Table 10-4 A/D Conversion Time (Single Mode)

		CKS = 0			**CKS = 1**		
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
Synchronization delay	t_D	18	—	33	10	—	17
Input sampling time	t_{SPL}	—	63	—	—	31	—
Total A/D conversion time	t_{CONV}	227	—	242	115	—	122

Note: Values in the table above are numbers of states.

Table 10-5 A/D Conversion Time (Scan Mode)

		CKS = 0			CKS = 1		
Item	Symbol	Min	Typ	Max	Min	Typ	Max
Synchronization delay	t_D	18	—	33	10	—	17
Input sampling time	t_{SPL}	—	63	—	—	31	—
Total A/D conversion time	t_{CONV}	259	—	274	131	—	138

Note: Values in the tables above are numbers of states.

10.3.4 External Trigger Input Timing

A/D conversion can be started by external trigger input at the $\overline{\text{ADTRG}}$ pin. This input is enabled or disabled by the TRGE bit in the A/D control register (ADCR). If the TRGE bit is set to 1, when a falling edge of $\overline{\text{ADTRG}}$ is detected the ADST bit is set to 1 and A/D conversion begins. Subsequent operation in both single and scan mode is the same as when the ADST bit is set to 1 by software.

Figure 10-5 shows the trigger timing.

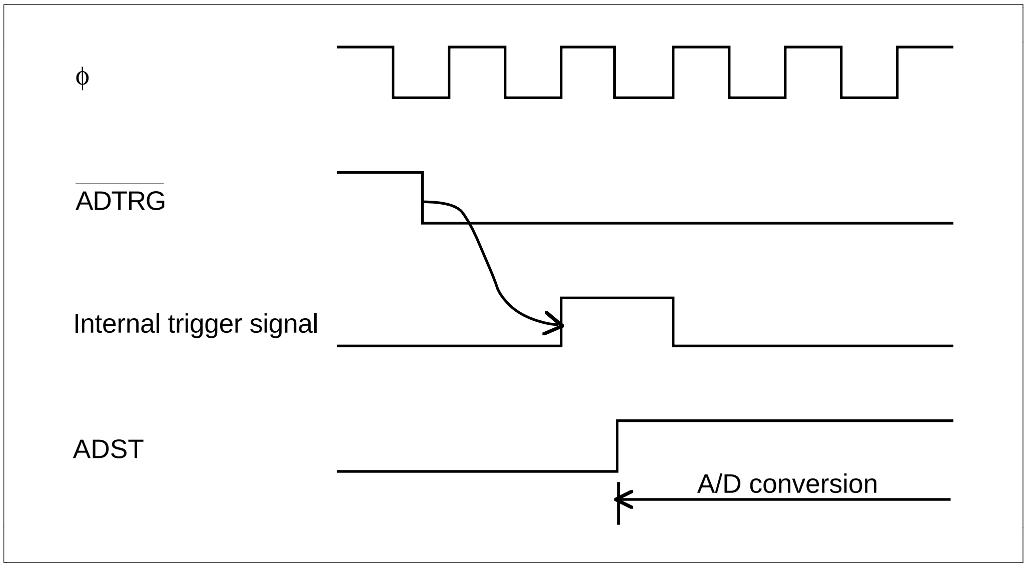


Figure 10-5 External Trigger Input Timing

10.4 Interrupts

The A/D conversion module generates an A/D-end interrupt request (ADI) at the end of A/D conversion.

The ADI interrupt request can be enabled or disabled by the ADIE bit in the A/D control/status register (ADCSR).

Section 11 Watchdog Timer

11.1 Overview

The H8/3332 on-chip watchdog timer (WDT) module can monitor system operation by requesting a nonmaskable interrupt internally if a system crash allows the timer count to overflow. It can also generate an internal chip reset instead of a nonmaskable interrupt.

When this watchdog function is not needed, the WDT module can be used as an interval timer. In the interval timer mode, it requests an OVF interrupt at each counter overflow.

11.1.1 Features

- Selection of eight clock sources
- Selection of two modes:
  - Watchdog timer mode
  - Interval timer mode
- Counter overflow generates an interrupt request or reset:
  - Reset or NMI request in the watchdog timer mode
  - OVF interrupt request in the interval timer mode

11.1.2 Block Diagram

Figure 11-1 is a block diagram of the watchdog timer.

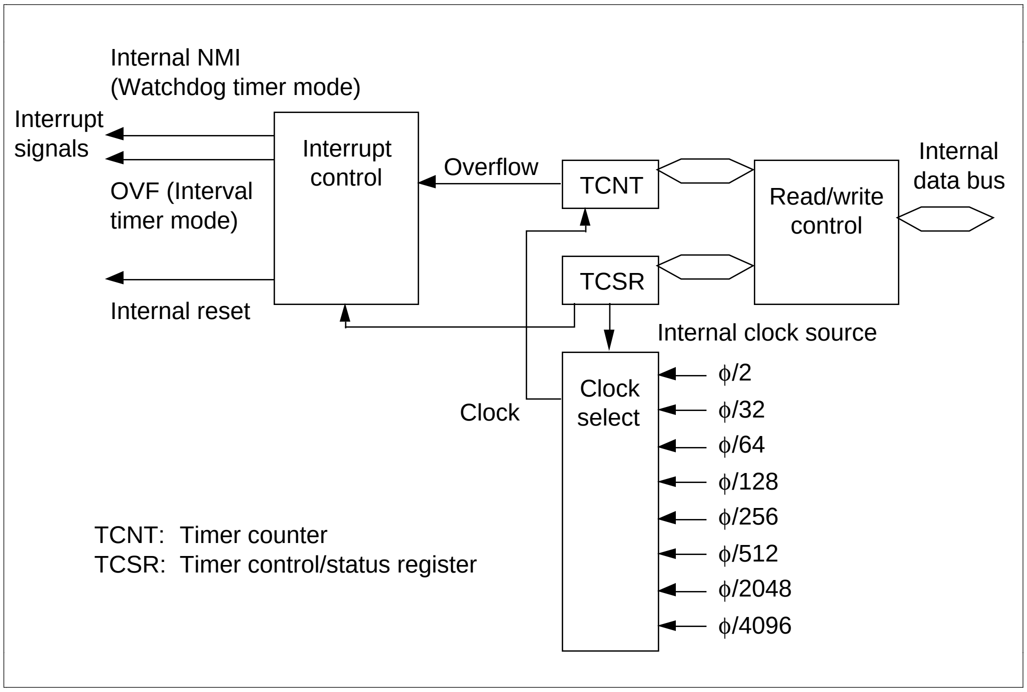


Figure 11-1 Block Diagram of Watchdog Timer

11.1.3 Register Configuration

Table 11-1 lists information on the watchdog timer registers.

Table 11-1 Register Configuration

				Addresses	
Name	**Abbreviation**	**RW**	**Initial Value**	**Write**	**Read**
Timer counter	TCNT	R/W	H'00	H'FFA9	H'FFA9
Timer control/status register	TCSR	R/(W)*	H'18	H'FFA9	H'FFA8

Note: *: Software can write a 0 to clear the status flag bits, but cannot write 1.

11.2 Register Descriptions

11.2.1 Timer Counter (TCNT)—H'FFA9

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The watchdog timer counter (TCNT) is a read/write 8-bit up-counter. (TCNT is write-protected by a password. See section 11.2.3, Register Access, for details.) When the timer enable bit (TME) in the timer control/status register (TCSR) is set to 1, the timer counter starts counting pulses of an internal clock source selected by clock select bits 2 to 0 (CKS$_2$ to CKS$_0$) in the TCSR. When the count overflows (changes from H'FF to H'00), an overflow flag (OVF) in the TCSR is set to 1.

The watchdog timer counter is initialized to H'00 at a reset and when the TME bit is cleared to 0.

Note: TCNT is more difficult to write to than other registers. See Section 11.2.3, Register Access, for details.

11.2.2 Timer Control/Status Register (TCSR—H'FFA8 (Read), H'FFA9 (Write)

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{\text{IT}}$	TME	—	RST/$\overline{\text{NMI}}$	CKS2	CKS1	CKS0
Initial value	0	0	0	1	0	0	0	0
Read/Write	R/(W*)	R/W	R/W	—	R/W	R/W	R/W	R/W

Note: *: Software can write a 0 in bit 7 to clear the flag, but cannot write a 1 in this bit. TCSR is more difficult to write to than other registers. See Section 11.2.3, Register Access, for details.

The watchdog timer control/status register (TCSR) is an 8-bit read/write register that selects the timer mode and clock source and performs other functions. (The TCST is write-protected by a password. See section 11.2.3, Register Access, for details.)

Bits 7 to 5 and bit 3 are initialized to 0 at a reset and in the standby modes. Bits 2 to 0 are initialized to 0 at a reset, but retain their values in the standby modes.

Bit 7: Overflow Flag (OVF): Indicates that the watchdog timer count has overflowed.

Bit 7: OVF	Description
0	To clear OVF, the CPU must read OVF after it has been set to 1, then write a 0 in this bit (Initial value)
1	Set to 1 when TCNT changes from H'FF to H'00

Bit 6: Timer Mode Select (WT/$\overline{\text{IT}}$): Selects whether to operate in the watchdog timer mode or interval timer mode.

Bit 6: WT/$\overline{\text{IT}}$	Description
0	Interval timer mode (OVF request) (Initial value)
1	Watchdog timer mode (reset or NMI request)

Bit 5: Timer Enable (TME): Enables or disables the timer.

Bit 5: TME	Description
0	TCNT is initialized to H'00 and stopped (Initial value)
1	TCNT runs and requests a reset or an interrupt when it overflows

Bit 4: Reserved: Cannot be modified and is always read as 1.

Bit 3: Reset or NMI Select (RST/$\overline{\text{NMI}}$): Selects either internal reset or NMI function enabled during watchdog timer overflow.

Bit 3: RST/$\overline{\text{NMI}}$	Description
0	NMI function enabled (Initial value)
1	Reset function enabled

Note: There is no reset output issued to external from this LSI during watchdog reset is active.

Bits 2–0: Clock Select (CKS2–CKS0): Select one of eight clock sources obtained by dividing the system clock (ϕ).

The overflow interval listed in table 11-2 is the time from when the watchdog timer counter begin counting from H'00 until an overflow occurs.

In the interval timer mode, OVF interrupts are requested at this interval.

Table 11-2 Timer Overflow Interval

Bit 2: CKS2	Bit 1: CKS1	Bit 0: CKS0	Clock Source	Overflow Interval (ϕ = 10 MHz)
0	0	0	ϕ/2	51.2 µs (Initial value)
0	0	1	ϕ/32	819.2 µs
0	1	0	ϕ/64	1.6 ms
0	1	1	ϕ/128	3.3 ms
1	0	0	ϕ/256	6.6 ms
1	0	1	ϕ/512	13.1 ms
1	1	0	ϕ/2048	52.4 ms
1	1	1	ϕ/4096	104.9 ms

11.2.3 Register Access

The watchdog timer's TCNT and TCSR registers are more difficult to write than other registers. The procedures for writing and reading these registers are given below.

Writing to TCNT and TCSR: The TCNT and TCSR registers must be written by word access. The write data must be contained in the lower byte of the word written at this address. The upper byte must contain H'5A (password for TCNT) or H'A5 (password for TCSR). See figure 11-2.

The result of the access depicted in figure 11-2 is to transfer the write data from the lower byte to the TCNT or TCSR.

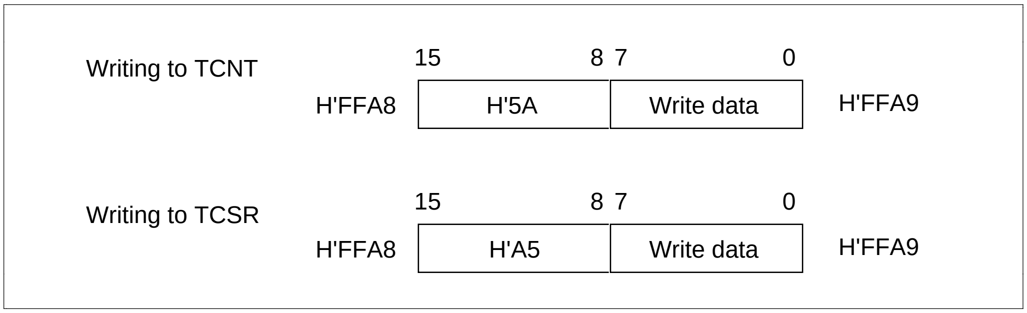


Figure 11-2 Writing to TCNT and TCSR

Reading TCNT and TCSR: The read addresses are H’FFA8 for TCSR and H’FFA9 for TCNT, as indicated in table 11-3.

These two registers are read like other registers. Byte access instructions can be used.

Table 11-3 Read Addresses of TCNT and TCSR

Read Address	Register
H'FFA8	TCSR
H'FFA9	TCNT

11.3 Operation

11.3.1 Watchdog Timer Mode

The watchdog timer function begins operating when software sets the WT/$\overline{\text{IT}}$ and TME bits to 1 in the TCSR. Thereafter, software should periodically rewrite the contents of the timer counter (normally by writing H’00) to prevent the count from overflowing. If a program crash allows the timer count to overflow, the watchdog timer requests either a nonmaskable interrupt (NMI) or a reset, depending on the status of bit 3 of register TCSR. Figure 11-3 shows the operation.

NMI requests from the watchdog timer have the same vector as NMI requests from the $\overline{\text{NMI}}$ pin, so the NMI interrupt-handling routine must check the OVF bit in the TCSR to determine the source of the interrupt.

Reset from the watchdog timer has the same vector as external reset from the $\overline{\text{RES}}$ pin. The reset source can be determined by the XRST bit in SYSCR.

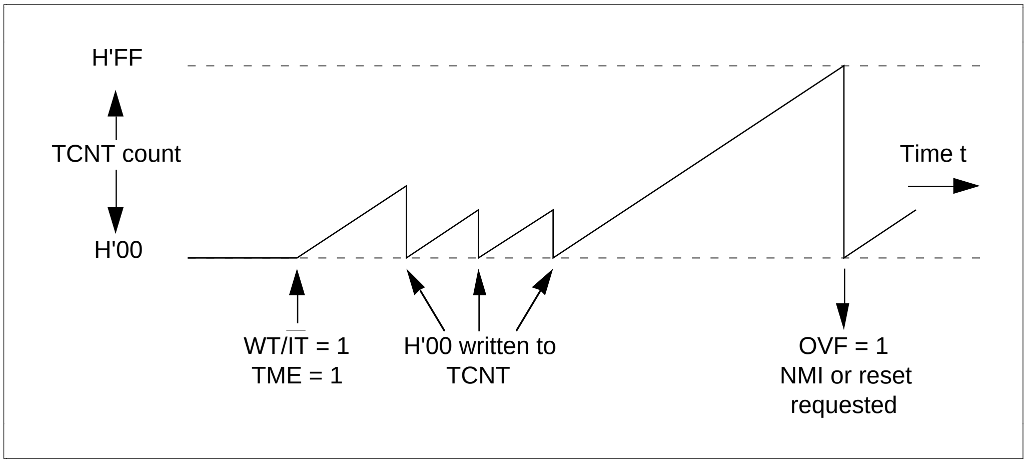


Figure 11-3 Operation in Watchdog Timer Mode

11.3.2 Interval Timer Mode

Interval timer operation begins when the WT/$\overline{\text{IT}}$ bit is cleared to 0 and the TME bit is set to 1.

In the interval timer mode, an OVF request is generated each time the timer count overflows. This function can be used to generate OVF requests at regular intervals. See figure 11-4.

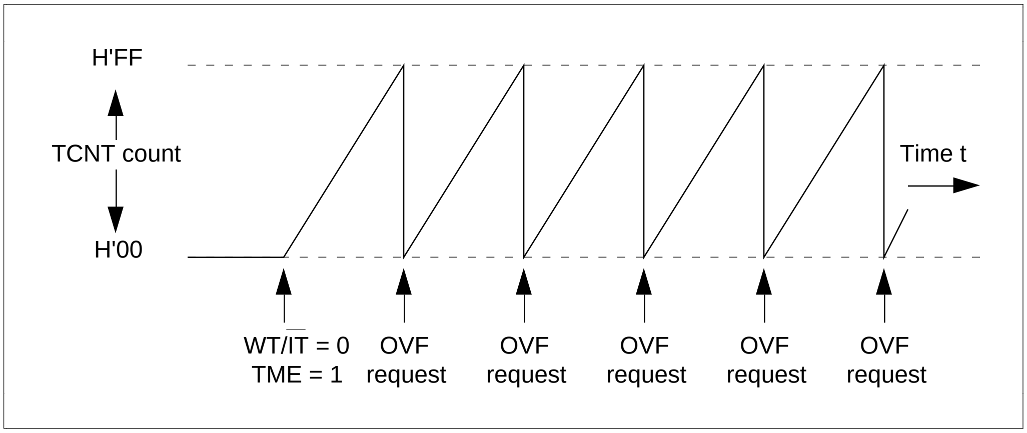


Figure 11-4 Operation in Interval Timer Mode

11.3.3 Setting the Overflow Flag

The OVF bit is set to 1 when the timer count overflows. Simultaneously, the WDT module requests an internal reset, NMI, or OVF interrupt. The timing is shown in figure 11-5.

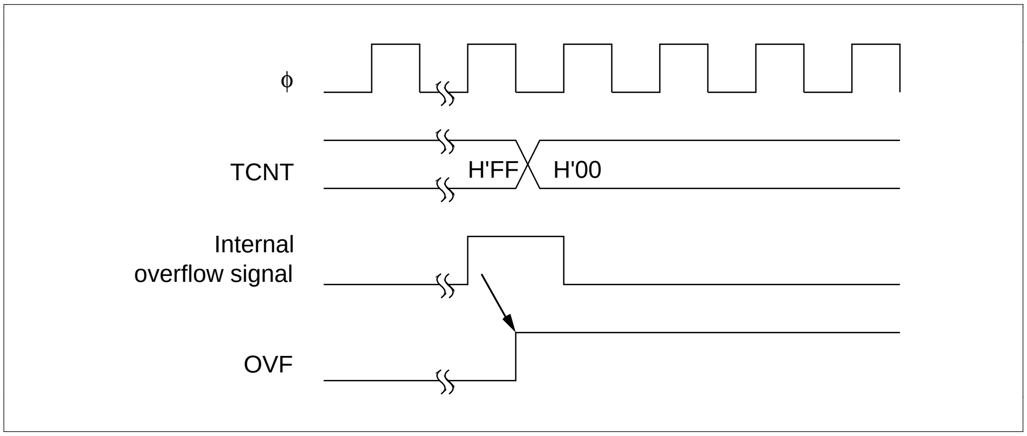


Figure 11-5 Setting the OVF Bit

11.4 Application Notes

11.4.1 Contention between TCNT Write and Increment

If a timer counter clock pulse is generated during the T3 state of a write cycle to the timer counter, the write takes priority and the timer counter is not incremented. See figure 11-6.

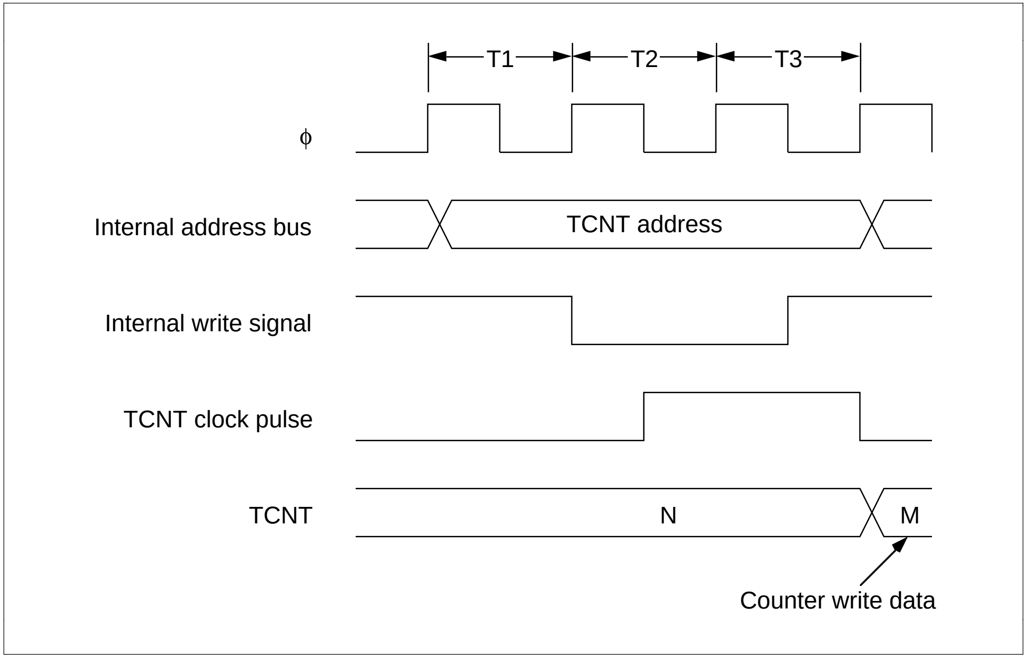


Figure 11-6 TCNT Write-Increment Contention

11.4.2 Changing the Clock Select Bits (CKS2 to CKS0)

Software should stop the watchdog timer (by clearing the TME bit to 0) before changing the value of the clock select bits. If the clock select bits are modified while the watchdog timer is running, the timer count may be incremented incorrectly.

11.4.3 Recovery from Software Standby Mode

TCSR bits, except bits 0–2, and the TCNT counter are reset when the LSI recovers from software standby mode. Based on the application, re-initialize the watchdog timer to the proper state to secure its normal operation.

Section 12 Host Interface

12.1 Overview

The host interface provides dual-channel host CPU to H8/3332 CPU slave interface capability. It can be used only during single chip mode operation, and only when the HIE bit in the SYSCR register is set to 1. This mode is called the slave mode, because it is designed for master-slave system communication with a master CPU.

This block includes 4 data registers, 2 status registers, 1 control register, 1 interrupt mask register, and fast GATE A_{20} control logic. It communicates to the host via five control signals ($\overline{CS}_1$, $\overline{CS}_2$, HA_0, $\overline{IOR}$, and $\overline{IOW}$) from the host, four output signals (GA_{20}, $HIRQ_1$, $HIRQ_{11}$, and $HIRQ_{12}$) to the host, and an 8-bit data bus (HDB_0–HDB_7) as command/data I/O buses. $\overline{CS}_1$ and $\overline{CS}_2$ are provided by host to selectively activate one of the 2 interface channels.

Note: If one of the interface channels is not needed, tie the corresponding $\overline{CS}_1$ pin to V_{CC}. For example, if interface channel 2 (IDR2, ODR2, STR2) is unused, tie $\overline{CS}_2$ to V_{CC}.)

Table 12-1 shows how the host interface interprets each control condition.

Table 12-1 Host Interface Operation

$\overline{CS}_2$	$\overline{CS}_1$	$\overline{IOR}$	$\overline{IOW}$	HA_0	Operation
1	0	0	0	0	Prohibited
1	0	0	0	1	Prohibited
1	0	0	1	0	Data read (from output data register 1, ODR1)
1	0	0	1	1	Status read (from status register 1, STR1)
1	0	1	0	0	Data write (to input data register 1, IDR1)
1	0	1	0	1	Command write (to input data register 1, IDR1)
1	0	1	1	0	No R/W activity
1	0	1	1	1	No R/W activity
0	1	0	0	0	Prohibited
0	1	0	0	1	Prohibited
0	1	0	1	0	Data read (from output data register 2, ODR2)
0	1	0	1	1	Status read (from status register 2, STR2)
0	1	1	0	0	Data write (to input data register 2, IDR2)
0	1	1	0	1	Command write (to input data register 2, IDR2)
0	1	1	1	0	No R/W activity
0	1	1	1	1	No R/W activity

12.1.1 Block Diagram

Figure 12-1 is a block diagram of the host interface.

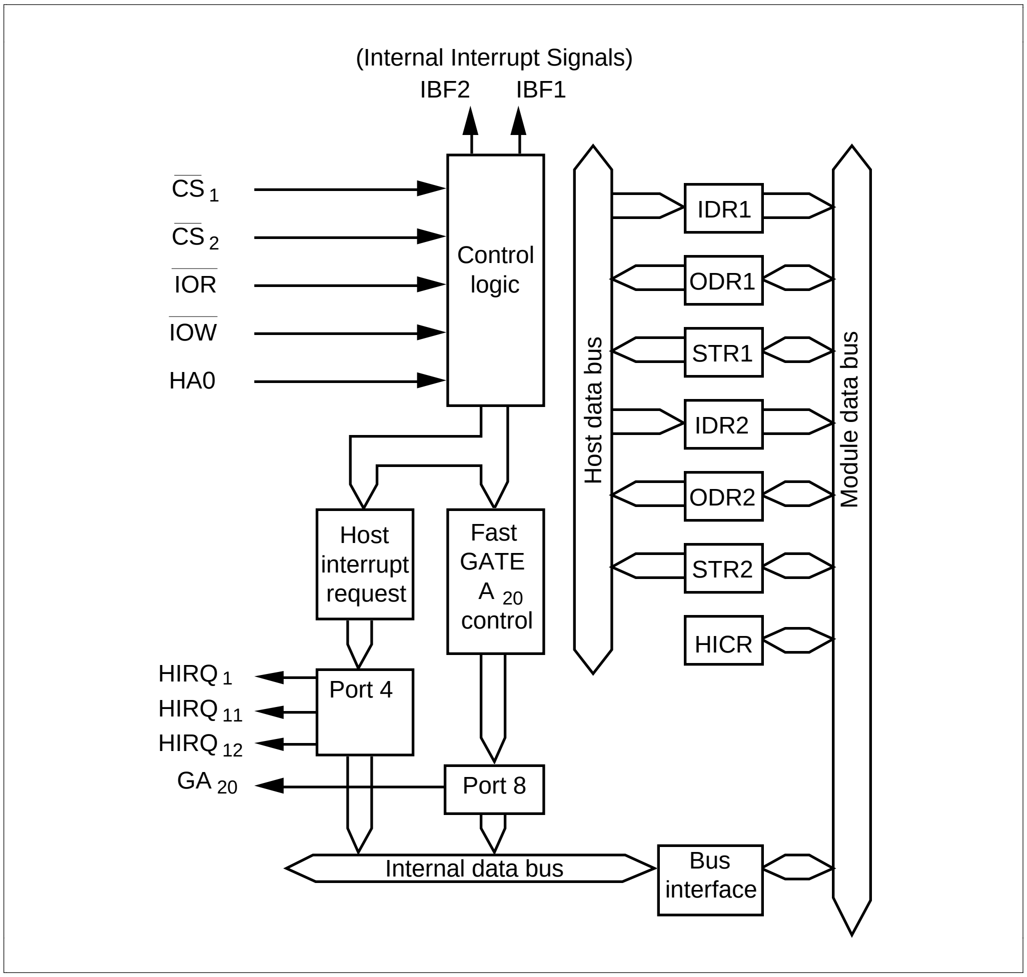


Figure 12-1 Host Interface Block Diagram

12.1.2 Input and Output Pins

Table 12-2 lists the input and output pins of the host interface module.

Table 12-2 Input/Output Pins of the Host Interface Module

Name	Abbreviation	Port	I/O	Function
I/O read	$\overline{IOR}$	$P8_3$	Input	Host interface read signal
I/O write	$\overline{IOW}$	$P8_4$	Input	Host interface write signal
Chip select 1	$\overline{CS}_1$	$P8_2$	Input	Host interface chip select signal for IDR1, ODR1, STR1
Chip select 2	$\overline{CS}_2$	$P8_5$	Input	Host interface chip select signal for IDR2, ODR2, STR2
Command/data	HA_0	$P8_0$	Input	Host interface address select input. HA_0 high selects the status register. HA_0 low selects the data registers.
Data bus	HDB_7–HDB_0	$P3_7$–$P3_0$	I/O	Host interface data bus
Host interrupt 1	$HIRQ_1$	$P4_4$	Output	Interrupt output 1 to host
Host interrupt 11	$HIRQ_{11}$	$P4_3$	Output	Interrupt output 11 to host
Host interrupt 12	$HIRQ_{12}$	$P4_5$	Output	Interrupt output 12 to host
Gate A_{20}	GA_{20}	$P8_1$	Output	GATE A_{20} control signal output

12.2 Operation

12.2.1 Expanded Modes (Modes 1 and 2)

The host interface registers are accessible to the slave CPU in expanded mode. However, host CPU access is disabled.

12.2.2 Single Chip Mode (Mode 3)

Activate host interface (slave mode) by setting the HIE bit (bit 1) of the SYSCR register to 1 in single chip mode operation. All related I/O ports (port 3 for data, port 8 for controls, and port 4 for host interrupts) become dedicated to host control signals and the host data path, making the host interface ready for slave mode operation.

Refer to section 17.3.8 for host read and write operation timing.

12.3 System Control Register (SYSCR)—H'FFC4

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	XRST	NMIEG	HIE	RAME
Initial value	0	0	0	0	1	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Note: The SYSCR is an 8-bit read/write register which controls the operations of the LSI. Host interface functions are enabled or disabled by the HIE bit of the SYSCR See Section 2.2, System Control Register, for information on other SYSCR bits. The SYSCR is initialized to H’09 by an external reset or during standby mode.

Bit 1: Host Interface Enable (HIE): In the single chip mode, HIE enables or disables the host interface. When enabled, this LSI behaves like a slave processor, handling any activity between the slave and the host.

HIE	Description
0	The host interface is disabled (Initial value)
1	• Single chip mode: The host interface is enabled (slave mode) • Expanded mode: The host interface is disabled

12.4 Host Interface Control Register (HICR)—H'FFF0

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	IBFIE2	IBFIE1	FGA20E
Initial value	1	1	1	1	1	0	0	0
Slave Read/Write	—	—	—	—	—	R/W	R/W	R/W
Host Read/Write	—	—	—	—	—	—	—	—

Note: The HICR is an 8-bit read/write register which controls host interface interrupts and Fast Gate A20 functions. The HICR is initialized to H’F8 by a reset or during standby mode.

Bit 2: Input Data Register Full Interrupt Enable (IBFIE2): Enables or disables the IBF interrupt to the slave CPU.

IBFIE2	Description
0	Input data register IDR2 full interrupt is disabled (Initial value)
1	Input data register IDR2 full interrupt is enabled

Bit 1: Input Data Register Full Interrupt Enable (IBFIE1): Enables or disables the IBF interrupt to the slave CPU.

IBFIE1	Description	
0	Input data register IDR1 full interrupt is disabled	(Initial value)
1	Input data register IDR1 full interrupt is enabled	

Bit 0: Fast GATE A_{20} Enable (FGA20E): Enables or disables the function of fast GATE A_{20}. However, when fast GATE A_{20} is disabled, regular GATE A_{20} is still available

FGA20E	Description	
0	Disables fast GATE A_{20} function	(Initial value)
1	Enables fast GATE A_{20} function	

12.5 Input Data Register (IDR1)—H'FFF4

Bit	7	6	5	4	3	2	1	0
	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
Initial value	—	—	—	—	—	—	—	—
Slave Read/Write	R	R	R	R	R	R	R	R
Host Read/Write	W	W	W	W	W	W	W	W

The input data register is an 8-bit read-only register to the slave, and a write-only register to the host processor. The $\overline{\text{IOW}}$ active with $\overline{\text{CS}_1}$ low will enable the host to write data into IDR1. Both commands and data from the host are written to the same input register independent of the HA_0 status.

12.6 Output Data Register (ODR1)—H'FFF5

Bit	7	6	5	4	3	2	1	0
	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
Initial value	—	—	—	—	—	—	—	—
Slave Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Host Read/Write	R	R	R	R	R	R	R	R

The output data register is an 8-bit read/write register to the slave, and a read-only register to the host processor. When $HA_0 = 0$, the active $\overline{IOR}$ signal is qualified by $\overline{CS}_1$ low, which will allow data to be read to the host.

12.7 Status Register (STR1)—H'FFF6

Bit	7	6	5	4	3	2	1	0
	DBU	DBU	DBU	DBU	$C/\overline{D}$	DBU	IBF	OBF
Initial value	0	0	0	0	0	0	0	0
Slave Read/Write	R/W	R/W	R/W	R/W	R	R/W	R	R
Host Read/Write	R/W	R/W	R/W	R/W	R	R/W	R	R

The STR1 is an 8-bit register. It displays the status during the host interface process. Bits 3, 1, and 0 are read only to the host and the slave CPU.

Bits 7–4 and 2 (DBU): Defined by the user.

Bit 3: Command or Data ($C/\overline{D}$): Copies the HA_0 input while the host is writing to the input data register (IDR1). It determines whether the existing contents of IDR1 are data or a command.

$C/\overline{D}$	Description
0	Contents of IDR1 are data
1	Contents of IDR1 are a command

Bit 1: Input Data Register Full (IBF): Set by $\overline{IOW}$, which is qualified by $\overline{CS}_1$ low. It is also one of the internal interrupt sources to the slave CPU. A slave CPU read from IDR1 will reset bit IBF of STR1.

IBF	Description	
0	Input data register (IDR1) empty	(initial value)
1	Input data register (IDR1) full	

Bit 0: Output Data Register Full (OBF): Set by a write strobe from the slave CPU to ODR1. An active $\overline{\text{IOR}}$ and $\overline{\text{CS}}_1$ along with HA_0 = 0 will read the output data register and clear the bit OBF of STR1.

OBF	Description	
0	Output data register (ODR1) empty	(initial value)
1	Output data register (ODR1) full	

Table 12-3 shows the conditions for setting and clearing the STR1 flags.

Table 12-3 Setting and Clearing STR1 Flags

Conditions	Operation	C/$\overline{\text{D}}$	IBF	OBF
Single-chip mode, HIE = 1, $\overline{\text{CS}}_1$ = 0, and $\overline{\text{CS}}_2$ = 1	Set by	Rising edge of host write ($\overline{\text{IOW}}$), HA = 1	Rising edge of host write ($\overline{\text{IOW}}$) to IDR1	Rising edge of slave write ($\overline{\text{WR}}$) to ODR1
	Cleared by	Rising edge of host write ($\overline{\text{IOW}}$), HA = 0	Rising edge of slave read ($\overline{\text{RD}}$) from IDR1	Rising edge of host read ($\overline{\text{IOR}}$) from ODR1

12.8 Input Data Register (IDR2)—H'FFFC

Bit	7	6	5	4	3	2	1	0
	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
Initial value	—	—	—	—	—	—	—	—
Slave Read/Write	R	R	R	R	R	R	R	R
Host Read/Write	W	W	W	W	W	W	W	W

The input data register is an 8-bit read-only register to the slave, and a write only register to the host processor. The $\overline{\text{IOW}}$ active with $\overline{\text{CS}}_2$ low will enable the host to write data into IDR2. Both commands and data from the host are written to the same input register independent of the HA_0 status.

The IDR2 initial value is undetermined during a reset or when in standby mode.

12.9 Output Data Register (ODR2)—H'FFFD

Bit	7	6	5	4	3	2	1	0
	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
Initial value	—	—	—	—	—	—	—	—
Slave Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Host Read/Write	R	R	R	R	R	R	R	R

The output data register is an 8-bit read/write register to the slave, and a read only register to the host processor. When HA_0 = 0, the $\overline{IOR}$ active is qualified by $\overline{CS}_2$ low, which will allow data to be read to the host.

12.10 Status Register (STR2)—H'FFFE

Bit	7	6	5	4	3	2	1	0
	DBU	DBU	DBU	DBU	C/$\overline{D}$	DBU	IBF	OBF
Initial value	0	0	0	0	0	0	0	0
Slave Read/Write	R/W	R/W	R/W	R/W	R	R/W	R	R
Host Read/Write	R/W	R/W	R/W	R/W	R	R/W	R	R

The STR2 is an 8-bit register. It displays the status during the host interface process. Bits 3, 1, and 0 are read-only to the host and the slave CPU.

STR2 is initialized to H’00 on reset or in standby mode.

Bits 7–4, and Bit 2 (DBU): Defined by the user.

Bit 3: Command or Data (C/$\overline{D}$): Copies the HA_0 input while the host is writing to the input data register (IDR2). It determines whether the existing contents of IDR2 are data or a command.

C/$\overline{D}$	Description	
0	Contents of IDR2 are data	(initial value)
1	Contents of IDR2 are a command	

Bit 1: Input Data Register Full (IBF): Set by $\overline{IOW}$, which is qualified by $\overline{CS}_2$ at low. It is also one of the internal interrupt sources to the slave CPU. A slave CPU read from IDR2 will reset bit IBF of STR2.

IBF	Description	
0	Input data register (IDR2) empty	(initial value)
1	Input data register (IDR2) full	

Bit 0: Output Data Register Full (OBF): Set by a write strobe from the slave CPU to ODR2. An active $\overline{IOR}$ and $\overline{CS}_2$ along with HA_0 = 0 will read the output data register and clear the bit OBF of STR2.

OBF	Description	
0	Output data register (ODR2) empty	(initial value)
1	Output data register (ODR2) full	

Table 12-4 shows the conditions for setting and clearing the STR2 flags.

Table 12-4 Setting and Clearing STR2 Flags

Conditions	Operation	C/$\overline{D}$	IBF	OBF
Single-chip mode, HIE = 1, $\overline{CS}_1$ = 1, and $\overline{CS}_2$ = 0	Set by	Rising edge of host write ($\overline{IOW}$), HA = 1	Rising edge of host write ($\overline{IOW}$) to IDR2	Rising edge of slave write ($\overline{WR}$) to ODR2
	Cleared by	Rising edge of host write ($\overline{IOW}$), HA = 0	Rising edge of slave read ($\overline{RD}$) from IDR2	Rising edge of host read ($\overline{IOR}$) from ODR2

12.11 GATE A_{20}

GATE A_{20} is part of the control needed to mask address line A_{20} to emulate addressing found on PCs using an 8086 CPU. In this slave mode, this output can be controlled by firmware (regular GATE A20). However, setting the FGA20E bit (bit 0) of HICR (H'FFF0) selects hardware speed-up. This is referred to as fast GATE A_{20}.

Regular GATE A_{20} Operation: When the FGA20E bit is reset to 0, the host system can control the GATE A_{20} output by writing a D1 command followed by data. When the slave CPU receives the data (normally done via an interrupt sequence from the IBF1 interrupt and then reading the IDR1), firmware should copy the value of data bit 1 to the GATEA20 output. Since GA_{20} is 0 after reset, this is the default mode.

Fast GATE A_{20} Operation: When FGA20E bit is set to 1, $P8_1/GA_{20}$ will become a dedicated pin for the fast GA_{20} signal. Update the DDR bit to assign $P8_1$ as output pin. It will output logic 1 first, then the host processor can toggle this pin's output based on its application. In this case, the on-chip logic decodes the incoming command/data from the host system. This logic is available only with the IDR1 register accessed by $\overline{CS}_1$. If a host command D1 is first detected, followed by a data byte, then bit 1 of the data will be output to the current state of GA_{20} output pin. The IBF bit of the STR register is always set by incoming command/data from the host CPU. Figure 12-2 shows the protocol and table 12-5 shows the conditions of operation.

Table 12-5 Setting and Clearing Fast GA_{20} ($P8_1$)

Condition	Setting	Clearing
Single-chip mode, HIE = 1, $FGA_{20}E$ = 1	"D1" host command followed by an 8-bit host data with bit 1 = 1	"D1" host command followed by an 8-bit host data with bit 1 = 0

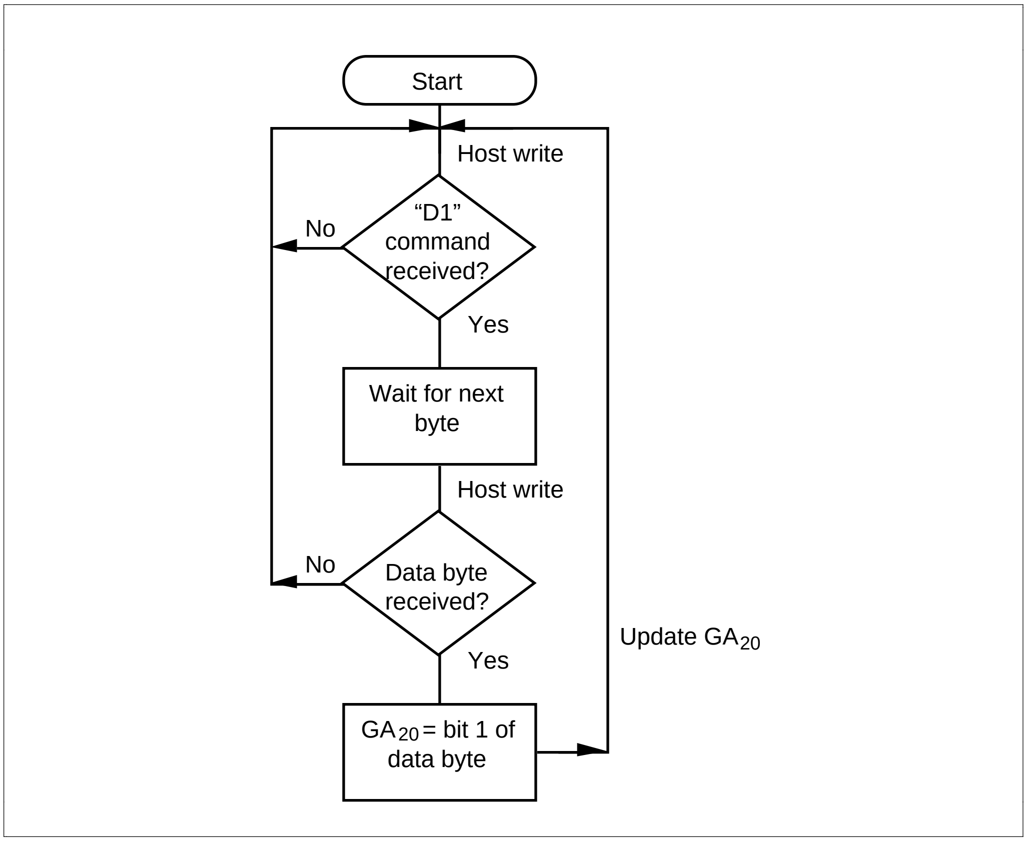


Figure 12-2 GA_{20} Output

12.12 Interrupts

12.12.1 IBF1, IBF2

The host interface can request two types of interrupts to the slave CPU: IBF1, and IBF2. They are input buffer full interrupts for input data registers IDR1 and IDR2 respectively. Each interrupt is requested when the corresponding enable bit is set (table 12-6).

Table 12-6 Input Buffer Full Interrupts

Interrupt	Description
IBF1	Requested when IBFIE1 is set and IDR1 is full
IBF2	Requested when IBFIE2 is set and IDR2 is full

12.12.2 HIRQ$_{11}$, HIRQ$_1$, and HIRQ$_{12}$

In the host interface application (single chip mode, HIE = 1 in the SYSCR register), there are three bits of the PDR4 register that can be used as host interrupt latches. In addition to being P4DR register bits, they can be reset by the host read strobe ($\overline{\text{IOR}}$). Host read strobe $\overline{\text{IOR}}$ with $\overline{\text{CS}}_1$ active and HA0 = 0 will read ODR1 and reset the HIRQ$_1$ and HIRQ$_{12}$ latches. Host read strobe $\overline{\text{IOR}}$ with $\overline{\text{CS}}_2$ active and HA0 = 0 will read ODR2 and reset the HIRQ$_{11}$ latch. Usually, on-chip firmware writes a 1 to the corresponding bit in order to generate a host interrupt. Then the host generates a read strobe to clear the bit right after the host services the interrupt by reading the output data register (ODR1 or ODR2). Table 12-7 shows how to set and clear these bits. Figure 12-3 shows the flowchart for HIRQ usage.

Table 12-7 Setting and Clearing HIRQ Bits

Conditions	Operation	HIRQ$_{11}$ (P4$_3$)	HIRQ$_1$ (P4$_4$)	HIRQ$_{12}$ (P4$_5$)
Single chip mode, HIE = 1	Set: H8 CPU writes 1 to bit	P4DR bit 3	P4DR bit 4	P4DR bit 5
	Clear: By reset or read by host CPU of register	ODR2 register ($\overline{\text{IOR}}$, $\overline{\text{CS}}_2$ all low)	ODR1 register ($\overline{\text{IOR}}$, $\overline{\text{CS}}_1$ all low)	

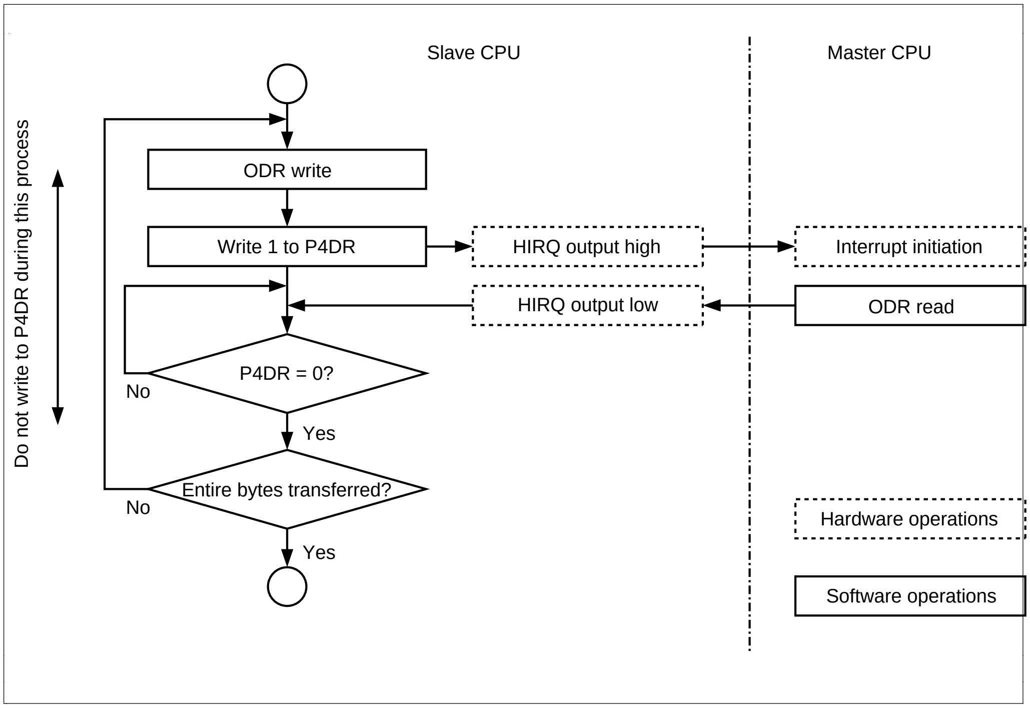


Figure 12-3 HIRQ Output Flowchart

12.13 Application Note

The host interface provides logic that buffers the asynchronous data from the host side and local processor side. A certain protocol for peripheral interface must be followed to get the expected functions and avoid data contention. For example, if host and H8/3332 processors try to access IDR or ODR simultaneously, data may be corrupted. Usually, a simple handshaking procedure, such as the receiving side verifying the STR flags, is necessary before accessing the data in the data registers.

Section 13 RAM

13.1 Overview

The H8/3332 includes 512 bytes of on-chip static RAM. The RAM is connected to the CPU by a 16-bit data bus. Both byte and word access to the on-chip RAM are performed in two states, enabling rapid data transfer and instruction execution.

The on-chip RAM is assigned to addresses H'FD80 to H'FF7F in the address space. The RAME bit in the system control register (SYSCR) can enable or disable the on-chip RAM, permitting these addresses to be allocated to external memory instead, if so desired.

13.2 Block Diagram

Figure 13-1 is a block diagram of the on-chip RAM.

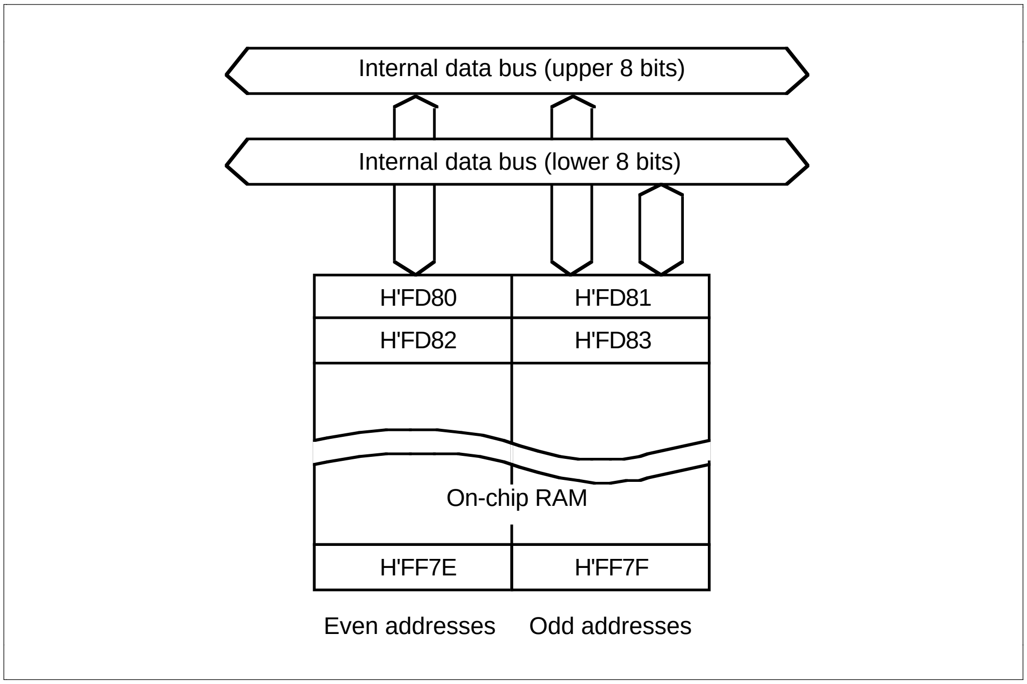


Figure 13-1 Block Diagram of On-Chip RAM (H8/3332)

13.3 RAM Enable Bit (RAME)

The on-chip RAM is enabled or disabled by the RAME (RAM Enable) bit in the system control register (SYSCR). Table 13-1 lists information about the system control register.

Table 13-1 System Control Register

Name	Abbreviation	R/W	Initial Value	Address
System control register	SYSCR	R/W	H'09	H'FFC4

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	XRST	NMIEG	HIE	RAME
Initial value	0	0	0	0	1	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

The only bit in the system control register that concerns the on-chip RAM is the RAME bit. See section 2.4.2, "System Control Register" for the other bits.

Bit 0: RAM Enable (RAME): Enables or disables the on-chip RAM.

The RAME bit is initialized to 1 on the rising edge of the $\overline{\text{RES}}$ signal, so a reset enables the on-chip RAM. The RAME bit is not initialized in the software standby mode.

Bit 7: RAME	Description	
0	On-chip RAM is disabled	
1	On-chip RAM is enabled	(Initial value)

13.4 Operation

13.4.1 Expanded Modes (Modes 1 and 2)

If the RAME bit is set to 1, accesses to addresses H'FD80 to H'FF7F are directed to the on-chip RAM. If the RAME bit is cleared to 0, accesses to addresses H'FD80 to H'FF7F and addresses H'FB80 to H'FD7F (reserved area) are directed to the external data bus.

13.4.2 Single-Chip Mode (Mode 3)

If the RAME bit is set to 1, accesses to addresses H'FD80 to H'FF7F are directed to the on-chip RAM.

If the RAME bit is cleared to 0, the on-chip RAM data cannot be accessed. Attempted write access has no effect. Attempted read access always results in H'FF data being read.

Section 14 ROM

14.1 Overview

The H8/3332 includes 16 kbytes of high-speed, on-chip ROM. The on-chip ROM is connected to the CPU via a 16-bit data bus. Both byte data and word data are accessed in two states, enabling rapid data transfer and instruction fetching.

The H8/3332 is available in two versions: one with one-time programmable ROM (OTP PROM), the other with masked ROM. The PROM version has a PROM mode in which the chip can be programmed with a standard PROM writer.

The on-chip ROM is enabled or disabled depending on the MCU operating mode, which is determined by the inputs at the mode pins (MD_1 and MD_0). See table 14-1.

Table 14-1 On-Chip ROM Use in Each MCU Mode

	Mode Pins		
Mode	**MD_1**	**MD_0**	**On-Chip ROM**
Mode 1 (expanded mode)	0	1	Disabled (external addresses)
Mode 2 (expanded mode)	1	0	Enabled
Mode 3 (single-chip mode)	1	1	Enabled

14.1.1 Block Diagram

Figure 14-1 is a block diagram of the on-chip ROM.

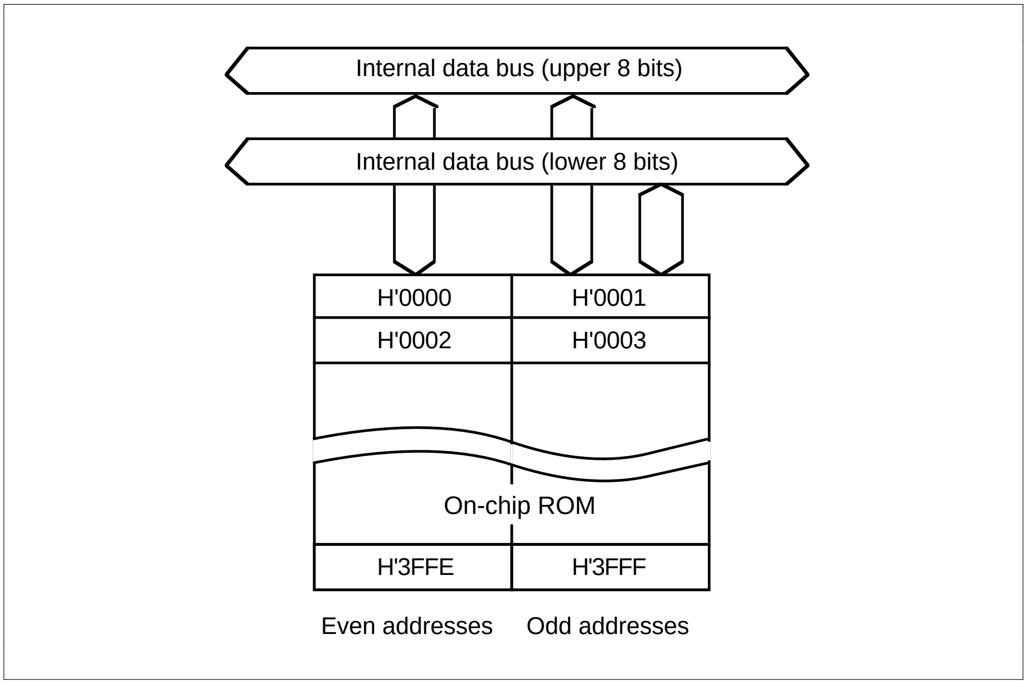


Figure 14-1 Block Diagram of On-Chip ROM (H8/3332)

14.2 PROM Mode

14.2.1 PROM Mode Setup

In the PROM mode of the PROM version of the H8/3332, the usual embedded controller functions are halted to allow the on-chip PROM to be programmed. The programming method is the same as for the HN27C256.

To select the PROM mode, apply the signal inputs listed in table 14-2.

Table 14-2 Selection of PROM Mode

Pin	Input
Mode pin MD1	Low
Mode pin MD0	Low
$\overline{\text{STBY}}$ pin	Low
Pins $P8_0$ and $P8_1$	High

14.2.2 Socket Adapter Pin Assignments and Memory Map

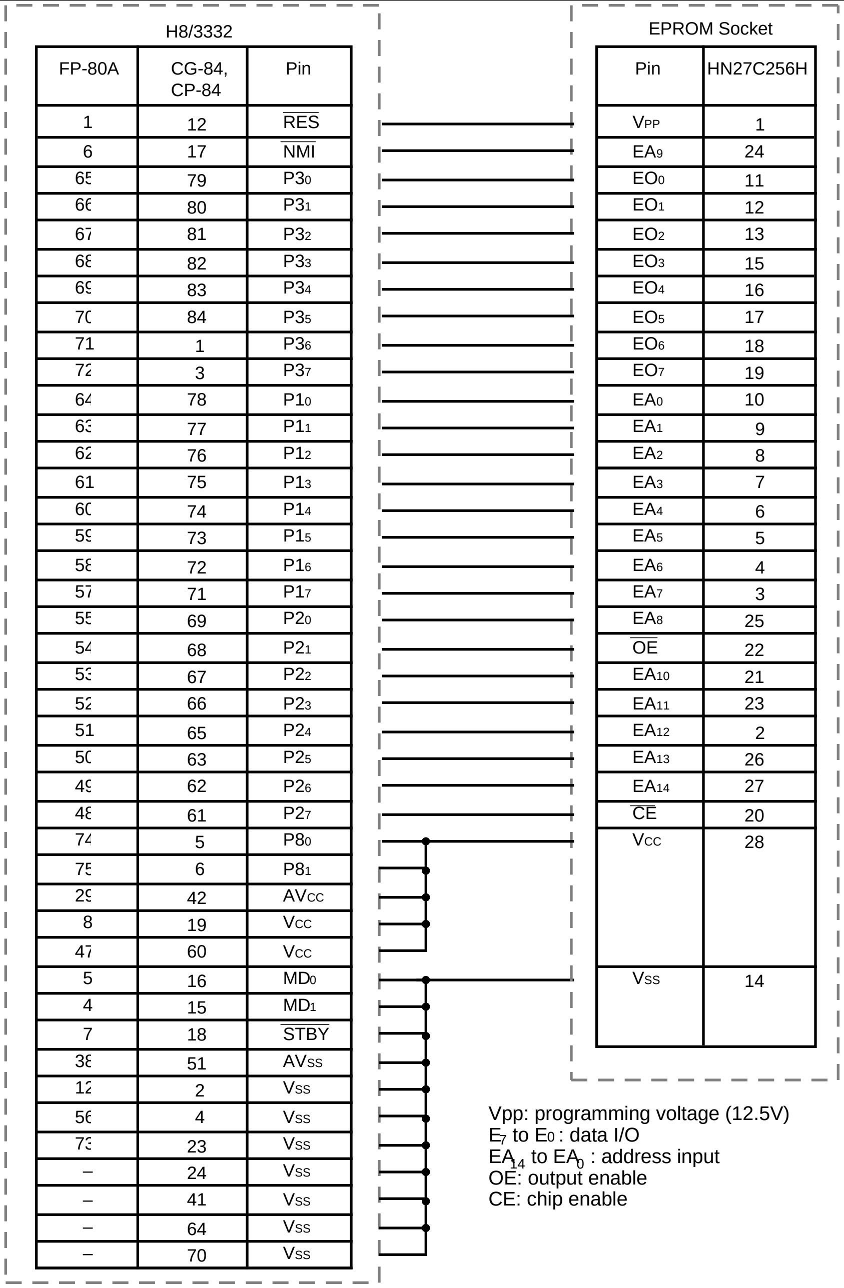
The H8/3332 can be programmed with a general-purpose PROM writer. Since the H8/3332 package has 80 or 84 pins instead of 28, a socket adapter is necessary. Table 14-3 lists recommended socket adapters. Figure 14-2 shows the socket adapter pin assignments by giving the correspondence between H8/3332 pins and HN27C256 pin functions.

Figure 14-3 shows a memory map in the PROM mode. Since the H8/3332 has only 16 kbytes of on-chip PROM, the address range should be specified as H'0000 to H'3FFF. H'FF data should be specified for unused address areas in the on-chip PROM.

It is important to limit the program address range to H'0000 to H'3FFF and specify H'FF data for H'4000 and higher addresses. If data (other than H'FF) are written by mistake in addresses equal to or greater than H'4000 for the H8/3332, it may become impossible to program or verify the PROM data. With a windowed package, it is possible to erase the data and reprogram, but this cannot be done with a plastic package, so particular care is required.

Table 14-3 Recommended Socket Adapters

Package	Recommended Socket Adapter
84-pin PLCC	HS338ESC01H
84-pin windowed LCC	HS338ESG01H
80-pin QFP	HS338ESH01H



H8/3332			EPROM Socket	
FP-80A	CG-84, CP-84	Pin	Pin	HN27C256H
1	12	$\overline{RES}$	V_{PP}	1
6	17	$\overline{NMI}$	EA_9	24
65	79	$P3_0$	EO_0	11
66	80	$P3_1$	EO_1	12
67	81	$P3_2$	EO_2	13
68	82	$P3_3$	EO_3	15
69	83	$P3_4$	EO_4	16
70	84	$P3_5$	EO_5	17
71	1	$P3_6$	EO_6	18
72	3	$P3_7$	EO_7	19
64	78	$P1_0$	EA_0	10
63	77	$P1_1$	EA_1	9
62	76	$P1_2$	EA_2	8
61	75	$P1_3$	EA_3	7
60	74	$P1_4$	EA_4	6
59	73	$P1_5$	EA_5	5
58	72	$P1_6$	EA_6	4
57	71	$P1_7$	EA_7	3
55	69	$P2_0$	EA_8	25
54	68	$P2_1$	$\overline{OE}$	22
53	67	$P2_2$	EA_{10}	21
52	66	$P2_3$	EA_{11}	23
51	65	$P2_4$	EA_{12}	2
50	63	$P2_5$	EA_{13}	26
49	62	$P2_6$	EA_{14}	27
48	61	$P2_7$	$\overline{CE}$	20
74	5	$P8_0$	V_{CC}	28
75	6	$P8_1$		
29	42	AV_{CC}		
8	19	V_{CC}		
47	60	V_{CC}		
5	16	MD_0	V_{SS}	14
4	15	MD_1		
7	18	$\overline{STBY}$		
38	51	AV_{SS}		
12	2	V_{SS}		
56	4	V_{SS}		
73	23	V_{SS}		
–	24	V_{SS}		
–	41	V_{SS}		
–	64	V_{SS}		
–	70	V_{SS}		

Vpp: programming voltage (12.5V)
E_7 to E_0 : data I/O
EA_{14} to EA_0 : address input
$\overline{OE}$: output enable
$\overline{CE}$: chip enable

Note: All pins not listed in this figure should be left open.

Figure 14-2 Socket Adapter Pin Assignments

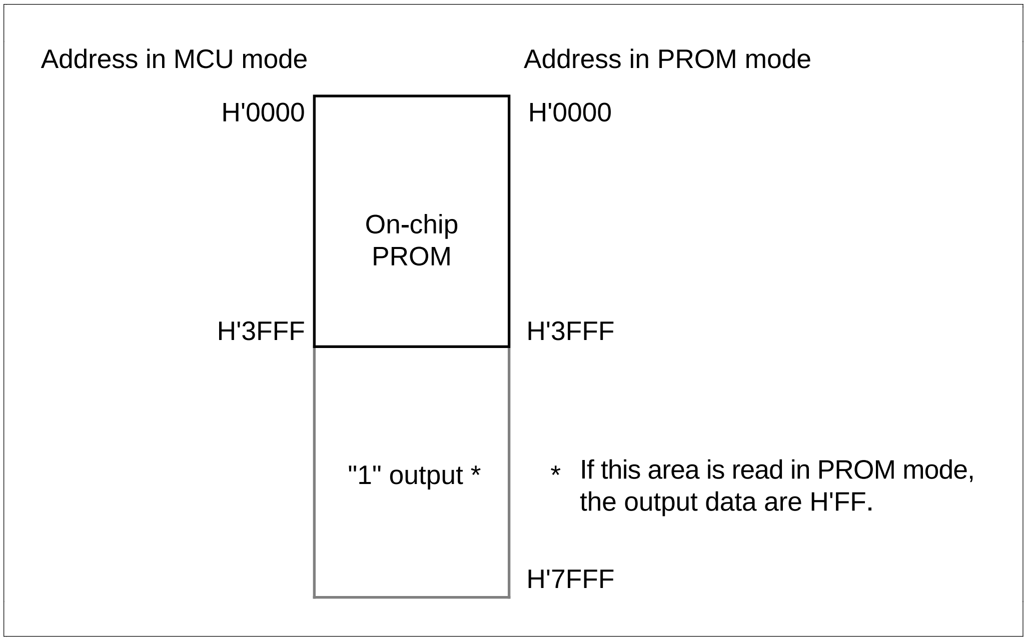


Figure 14-3 H8/3332 Memory Map in PROM Mode

14.3 Programming

The write, verify, inhibited, and read sub-modes of the PROM mode are selected as shown in table 14-4.

Table 14-4 Selection of Sub-Modes in PROM Mode

	Pins					
Sub-Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{CC}	EO_7–EO_0	EA_{14} –EA_0
Write	Low	High	V_{PP}	V_{CC}	Data input	Address input
Verify	High	Low	V_{PP}	V_{CC}	Data output	Address input
Programming inhibited	High	High	V_{PP}	V_{CC}	High-impedance	Address input

Note: The V_{PP} and V_{CC} pins must be held at the V_{PP} and V_{CC} voltage levels.

The H8/3332 PROM uses the same, standard read/write specifications as the HN27C256 and HN27256.

14.3.1 Writing and Verifying

An efficient, high-speed programming procedure can be used to write and verify PROM data. This procedure writes data quickly without subjecting the chip to voltage stress and without sacrificing data reliability. It leaves the data H'FF written in unused addresses.

Figure 14-4 shows the basic high-speed programming flowchart.

Tables 14-5 and 14-6 list the electrical characteristics of the chip in the PROM mode. Figure 14-5 shows a write/verify timing chart.

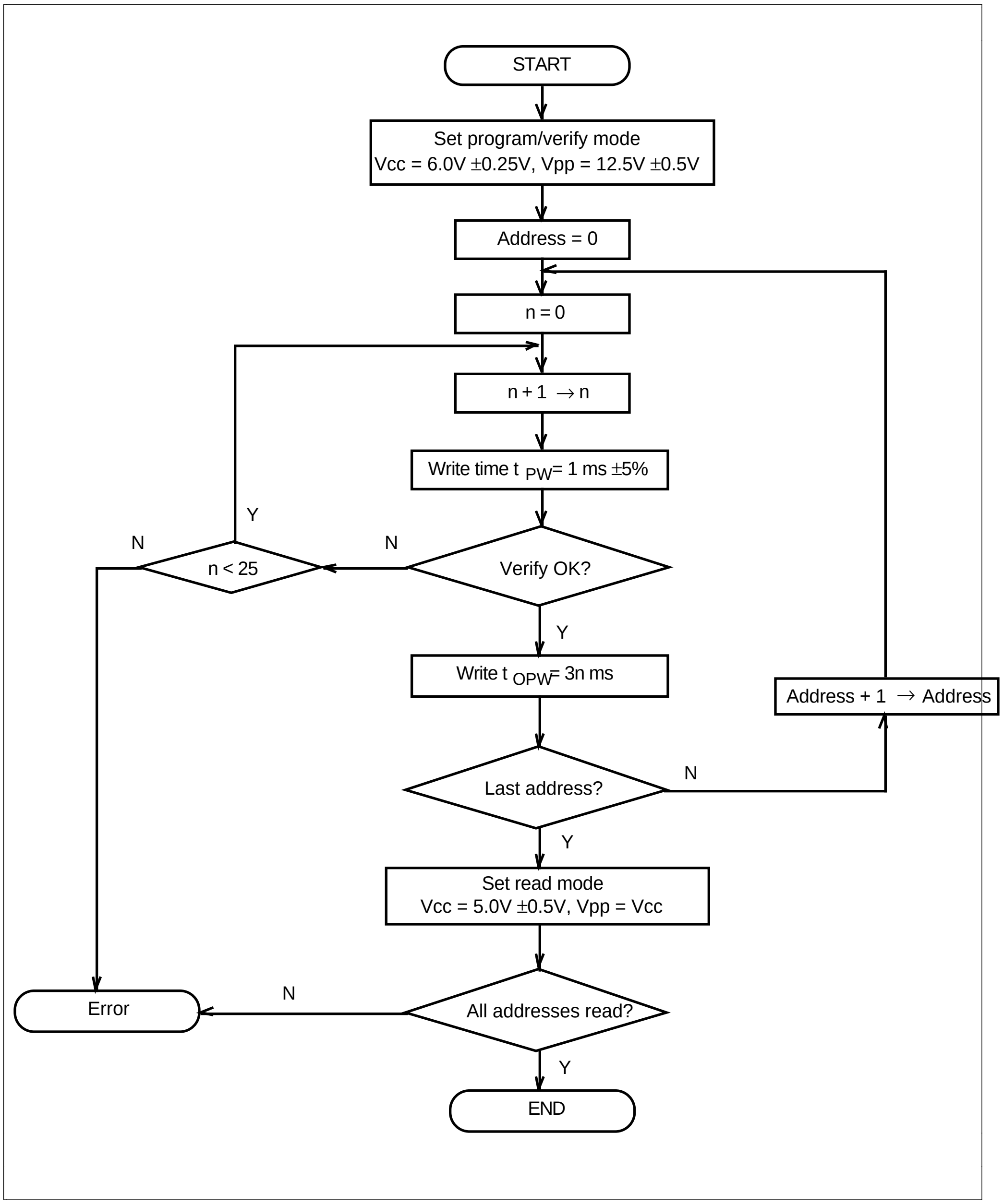


Figure 14-4 High-Speed Programming Flowchart

Table 14-5 DC Characteristics

(When V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V, V_{SS} = 0 V, Ta = 25°C ±5°C)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input high voltage	EO_7–EO_0, EA_{14}–EA_{10}, EA_8–EA_0, $\overline{OE}$, $\overline{CE}$	V_{IH}	2.4	—	V_{CC} + 0.3	V	
Input low voltage	EO_7–EO_0, EA_{14}–EA_0, $\overline{OE}$, $\overline{CE}$	V_{IL}	– 0.3	—	0.8	V	
Output high voltage	EO_7–EO_0	V_{OH}	2.4	—	—	V	I_{OH} = –200 µA
Output low voltage	EO_7–EO_0	V_{OL}	—	—	0.45	V	I_{OL} = 1.6 mA
Input leakage current	EO_7–EO_0, EA_{14}–EA_0, $\overline{OE}$, $\overline{CE}$	$\lvert I_{LI}\rvert$	—	—	2	µA	Vin = 5.25 V/0.5 V
V_{CC} current		I_{CC}	—	—	40	mA	
V_{PP} current		I_{PP}	—	—	40	mA	

Table 14-6 AC Characteristics

(When V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V, Ta = 25°C ±5°C)

Item	Symbol	Min	Typ	Max	Unit	Measurement Conditions
Address setup time	t_{AS}	2	—	—	µs	See figure 14-5 (Note)
OE setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
Data output disable time	t_{DF}	—	—	130	ns	
Vpp setup time	t_{VPS}	2	—	—	µs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
OE pulse width for overwrite-programming	t_{OPW}	2.85	—	78.75	ms	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
Data output delay time	t_{OE}	0	—	500	ns	

Note: Input pulse level: 0.8 V to 2.2 V

Input rise/fall time ≤ 20 ns

Timing reference levels: input—1.0 V, 2.0 V; output—0.8 V, 2.0 V

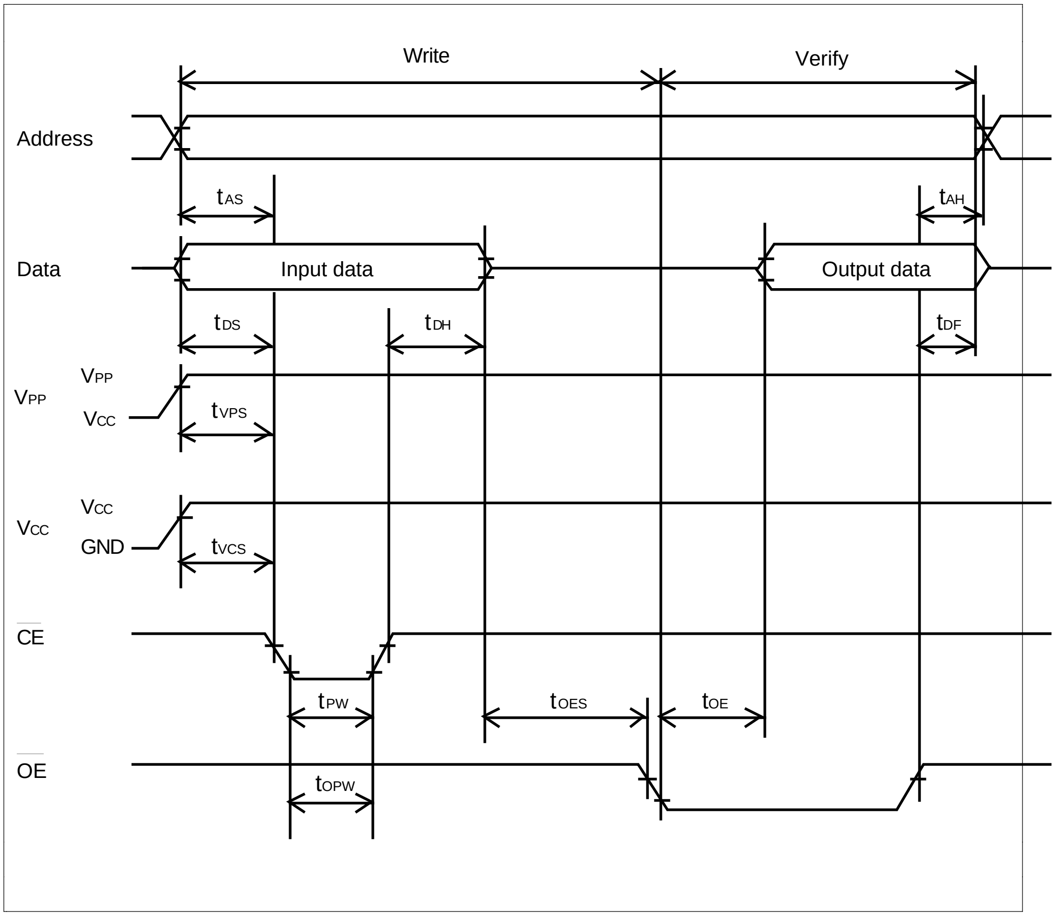


Figure 14-5 PROM Write/Verify Timing

14.3.2 Notes on Writing

1. Write with the specified voltages and timing. The programming voltage (V_{PP}) is 12.5 V.

   Caution: Applied voltages in excess of the specified values can permanently destroy the chip. Be particularly careful about the PROM writer's overshoot characteristics.

   If the PROM writer is set to Intel specifications or Hitachi HN27256 or HN27C256 specifications, V_{PP} will be 12. 5 V.

2. Before writing data, check that the socket adapter and chip are correctly mounted in the PROM writer.

   Overcurrent damage to the chip can result if the index marks on the PROM writer, socket adapter, and chip are not correctly aligned.

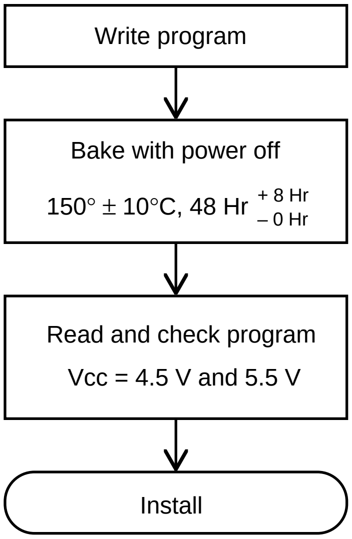
3. Don’t touch the socket adapter or chip during writing.

   Touching either of these can cause contact faults and write errors.

14.3.3 Reliability of Written Data

An effective way to assure the data holding characteristics of the programmed chips is to bake them at 150°C, then screen them for data errors. This procedure quickly eliminates chips with PROM memory cells prone to early failure.

Figure 14-6 shows the recommended screening procedure.



Note: Baking time should be measured from the point when the baking oven reaches 150°C.

Figure 14-6 Recommended Screening Procedure

If a series of write errors occurs while the same PROM writer is in use, stop programming and check the PROM writer and socket adapter for defects, using a embedded controller chip with a windowed package and on-chip EPROM.

Please inform Hitachi of any abnormal conditions noted during programming or in screening of program data after high-temperature baking.

14.3.4 Erasing Data

The windowed package enables data to be erased by illuminating the window with ultraviolet light. Table 14-7 lists the erasing conditions.

Table 14-7 Erasing Conditions

Item	Value
Ultraviolet wavelength	253.7 nm
Minimum illumination	15 W·s/cm^2

The conditions in table 14-7 can be satisfied by placing a 12000 µW/cm^2 ultraviolet lamp 2 or 3 centimeters directly above the chip and leaving it on for about 20 minutes.

14.4 Handling of Windowed Packages

14.4.1 Glass Erasing Window

Rubbing the glass erasing window of a windowed package with a plastic material or touching it with an electrically charged object can create a static charge on the window surface which may cause the chip to malfunction.

If the erasing window becomes charged, the charge can be neutralized by a short exposure to ultraviolet light. This returns the chip to its normal condition, but it also reduces the charge stored in the floating gates of the PROM, so it is recommended that the chip be reprogrammed afterward.

Accumulation of static charge on the window surface can be prevented by the following precautions:

1. When handling the package, ground yourself. Don’t wear gloves. Avoid other possible sources of static charge.

2. Avoid friction between the glass window and plastic or other materials that tend to accumulate static charge.

3. Be careful when using cooling sprays, since they may have a slight ion content.

4. Cover the window with an ultraviolet-shield label, preferably a label including a conductive material. Besides protecting the PROM contents from ultraviolet light, the label protects the chip by distributing static charge uniformly.

14.4.2 Handling after Programming

Fluorescent light and sunlight contain small amounts of ultraviolet, so prolonged exposure to these types of light can cause programmed data to invert. In addition, exposure to any type of intense light can induce photoelectric effects that may lead to chip malfunction. It is recommended that after programming the chip, you cover the erasing window with a light-proof label (such as an ultraviolet-shield label).

14.4.3 84-Pin LCC Package

A socket should always be used when the 84-pin LCC package is mounted on a printed-circuit board. Table 13.8 shows the recommended socket.

Table 14-8 Recommended Socket for Mounting 84-Pin LCC Package

Manufacturer	Code
Sumitomo 3-M	284-1273-00-1102J

Section 15 Power-Down State

15.1 Overview

The H8/3332 has a power-down state that greatly reduces power consumption by stopping some or all of the chip functions. The power-down state includes three modes:

- Sleep mode: a software-triggered mode in which the CPU halts but the rest of the chip remains active
- Software standby mode: a software-triggered mode in which the entire chip is inactive
- Hardware standby mode: a hardware-triggered mode in which the entire chip is inactive

Table 15-1 lists the conditions for entering and leaving the power-down modes. It also indicates the status of the CPU, on-chip supporting modules, etc. in each power-down mode.

Table 15-1 Power-Down State

Mode	Entering Procedure	Clock	CPU	CPU Reg.s	Sup. Mod.	RAM	I/O Ports	Exiting Methods
Sleep mode	Execute SLEEP instruction	Run	Halt	Held	Run	Held	Held	• Interrupt • $\overline{\text{RES}}$ or watchdog reset • $\overline{\text{STBY}}$
Software standby mode	Set SSBY bit in SYSCR to 1, then execute SLEEP instruction	Halt	Halt	Held	Halt and initialized	Held	Held	• $\overline{\text{NMI}}$ • $\overline{\text{IRQ}_0}$–$\overline{\text{IRQ}_2}$, $\overline{\text{IRQ}_6}$ (including $\overline{\text{KEYIN}_0}$–$\overline{\text{KEYIN}_7}$) • $\overline{\text{STBY}}$ • $\overline{\text{RES}}$
Hardware standby mode	Set $\overline{\text{STBY}}$ pin to low level	Halt	Halt	Not held	Halt and initialized	Held	High impedance state	• $\overline{\text{STBY}}$ high, then $\overline{\text{RES}}$ low → high

Notes: SYSCR: System control register

SSBY: Software standby bit

Sup. Mod.: On-chip supporting modules, including the host interface.

15.2 System Control Register: Power-Down Control Bits

Bits 7 to 4 of the system control register (SYSCR) concern the power-down state. Specifically, they concern the software standby mode.

Table 15-2 lists the attributes of the system control register.

Table 15-2 System Control Register

Name	Abbreviation	R/W	Initial Value	Address
System control register	SYSCR	R/W	H'09	H'FFC4

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	XRST	NMIEG	HIE	RAME
Initial value	0	0	0	0	1	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit 7: Software Standby (SSBY): Enables or disables the transition to the software standby mode.

On recovery from the software standby mode by an external interrupt, SSBY remains set to 1. To clear this bit, software must write a 0.

Bit 7: SSBY	Description
0	The SLEEP instruction causes a transition to the sleep mode (Initial value)
1	The SLEEP instruction causes a transition to the software standby mode

Bits 6 to 4: Standby Timer Select 2 to 0 (STS2 to STS0): Select the clock settling time when the chip recovers from the software standby mode by an external interrupt. During the selected time, the clock oscillator runs but clock pulses are not supplied to the CPU or the on-chip supporting modules.

Bit 6: STS2	Bit 5: STS1	Bit 4: STS0	Description
0	0	0	Settling time = 8192 states (Initial value)
0	0	1	Settling time = 16384 states
0	1	0	Settling time = 32768 states
0	1	1	Settling time = 65536 states
1	—	—	Settling time = 131072 states

When this LSI’s on-chip clock pulse generator is used, the STS bits should be set to allow a settling time of at least 10 ms. Table 15-3 lists the settling times selected by these bits at several clock frequencies and indicates the recommended settings.

When this LSI is externally clocked, the STS bits can be set to any value. The minimum value (STS2 = STS1 = STS0 = 0) is recommended.

Table 15-3 Times Set by Standby Timer Select Bits (Unit: ms)

STS2	STS1	STS0	Settling Time (states)	System Clock Frequency (MHz)						
				10	8	6	4	2	1	0.5
0	0	0	8192	0.8	1.0	1.3	2.0	4.1	8.2	**16.4**
0	0	1	16384	1.6	2.0	2.7	4.1	8.2	**16.4**	32.8
0	1	0	32768	3.3	4.1	5.5	8.2	**16.4**	32.8	65.5
0	1	1	65536	6.6	8.2	**10.9**	**16.4**	32.8	65.5	131.1
1	—	—	131072	**13.1**	**16.4**	21.8	32.8	65.5	131.1	262.1

Notes: 1. All times are in milliseconds.

2. Recommended values are printed in boldface.

15.3 Sleep Mode

The sleep mode provides an effective way to conserve power while the CPU is waiting for an external interrupt or an interrupt from an on-chip supporting module.

15.3.1 Transition to Sleep Mode

When the SSBY bit in the system control register is cleared to 0, execution of the SLEEP instruction causes a transition from the program execution state to the sleep mode. After executing the SLEEP instruction, the CPU halts, but the contents of its internal registers remain unchanged. The on-chip supporting modules continue to operate normally.

15.3.2 Exit from Sleep Mode

The chip wakes up from the sleep mode when it receives an internal or external interrupt request, or a low input at the $\overline{\text{RES}}$ or $\overline{\text{STBY}}$ pin.

Wake-Up by Interrupt: An interrupt releases the sleep mode and starts the CPU’s interrupt-handling sequence.

If an interrupt from an on-chip supporting module is disabled by the corresponding enable/disable bit in the module’s control register, the interrupt cannot be requested, so it cannot wake the chip up. Similarly, the CPU cannot be woken by an interrupt other than NMI if the I (interrupt mask) bit in the CCR (condition code register) is set when the SLEEP instruction is executed.

Wake-Up by $\overline{\text{RES}}$ Pin or Reset by Watchdog Overflow: When the $\overline{\text{RES}}$ pin goes low, or when the watchdog timer overflows and causes a reset, the chip exits from the sleep mode to the reset state.

Wake-Up by $\overline{\text{STBY}}$ Pin: When the $\overline{\text{STBY}}$ pin goes low, the chip exits from the sleep mode to the hardware standby mode.

15.4 Software Standby Mode

In the software standby mode, the system clock stops and chip functions halt, including both CPU functions and the functions of the on-chip supporting modules. Power consumption is reduced to an extremely low level. The on-chip supporting modules and their registers are reset to their initial states, but as long as a minimum necessary voltage supply is maintained (at least 2 V), the contents of the CPU registers and on-chip RAM remain unchanged.

15.4.1 Transition to Software Standby Mode

To enter the software standby mode, set the standby bit (SSBY) in the system control register (SYSCR) to 1, then execute the SLEEP instruction.

15.4.2 Exit from Software Standby Mode

The chip can be brought out of the software standby mode by an input at one of six interrupts: $\overline{\text{NMI}}$, $\overline{\text{IRQ}_0}$, $\overline{\text{IRQ}_1}$, $\overline{\text{IRQ}_2}$, $\overline{\text{IRQ}_6}$ (including $\overline{\text{KEYIN}_0}$ to $\overline{\text{KEYIN}_7}$), $\overline{\text{RES}}$, or $\overline{\text{STBY}}$.

Recovery by External Interrupt: When an $\overline{\text{NMI}}$, $\overline{\text{IRQ}_0}$, $\overline{\text{IRQ}_1}$, $\overline{\text{IRQ}_2}$ or $\overline{\text{IRQ}_6}$ (including $\overline{\text{KEYIN}_0}$ to $\overline{\text{KEYIN}_7}$) request signal is received, the clock oscillator begins operating. After the waiting time set in the system control register (bits STS2 to STS0), clock pulses are supplied to the CPU and on-chip supporting modules. The CPU executes the interrupt-handling sequence for the requested interrupt, then returns to the instruction after the SLEEP instruction. The SSBY bit is not cleared.

See section 15.2, System Control Register: Power-Down Control Bits, for information about the STS bits.

Interrupts $\overline{\text{IRQ}_3}$ to $\overline{\text{IRQ}_5}$ and $\overline{\text{IRQ}_7}$ should be disabled before entry to the software standby mode. Clear IRQ_3E to IRQ_5E and IRQ_7E to 0 in the interrupt enable register (IER).

Recovery by $\overline{\text{RES}}$ Pin: When the $\overline{\text{RES}}$ pin goes low, the clock oscillator starts. Next, when the $\overline{\text{RES}}$ pin goes high, the CPU begins executing the reset sequence. The SSBY bit is cleared to 0.

The $\overline{\text{RES}}$ pin must be held low long enough for the clock to stabilize.

Recovery by $\overline{\text{STBY}}$ Pin: When the $\overline{\text{STBY}}$ pin goes low, the chip exits from the software standby mode to the hardware standby mode.

15.4.3 Sample Application of Software Standby Mode

In this example this LSI enters the software standby mode when NMI goes low and exits when NMI goes high, as shown in figure 15-1.

The NMI edge bit (NMIEG) in the system control register is originally cleared to 0, selecting the falling edge. When NMI goes low, the NMI interrupt handling routine sets NMIEG to 1, sets SSBY to 1 (selecting the rising edge), then executes the SLEEP instruction. This LSI enters the software standby mode. It recovers from the software standby mode on the next rising edge of NMI.

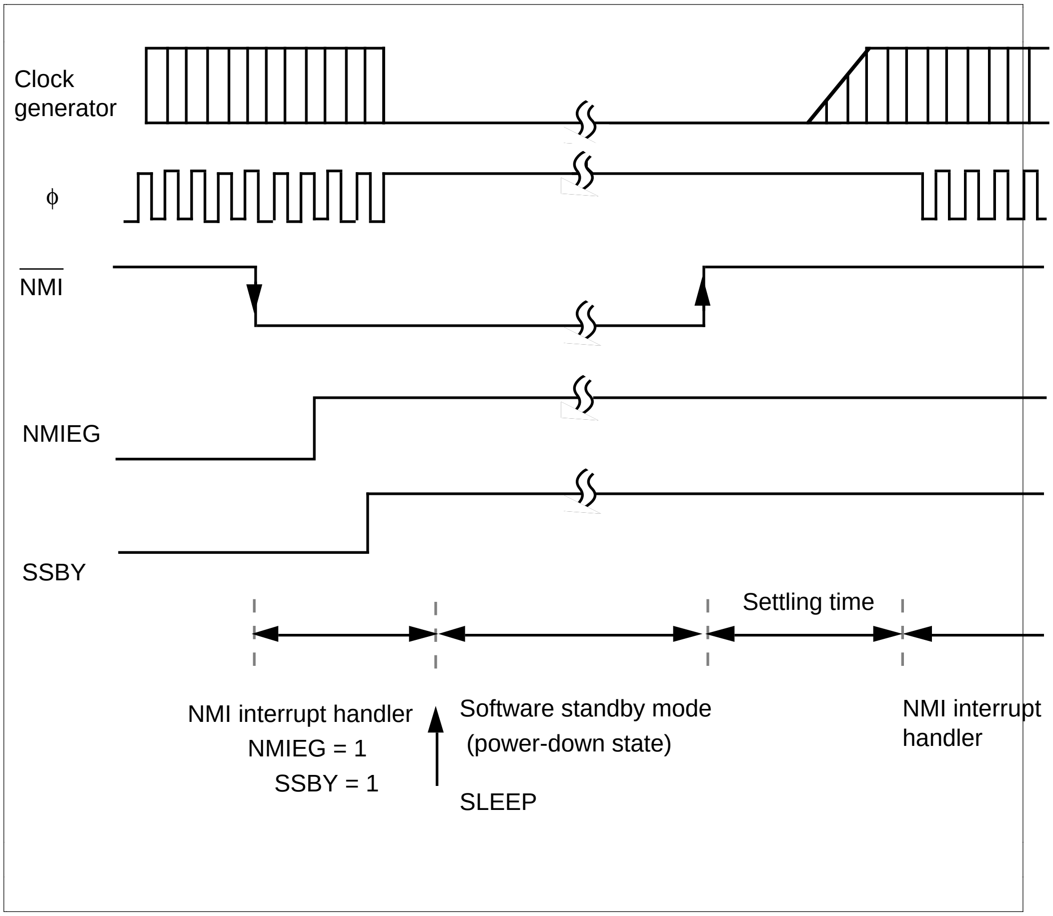


Figure 15-1 Software Standby Mode NMI Timing

15.4.4 Application Notes

I/O Ports: The I/O ports generally retain their current states in the software standby mode, depending on operation mode. See appendix C for detailed description. If a port is in the high output state, the current dissipation caused by the high output current is not reduced.

EEPMOV: The EEPMOV instruction can affect the software standby current dissipation. Specifically, if the H8/3332 enters software standby mode by executing an instruction from on-chip ROM after an EEPMOV instruction has been executed, the standby current dissipation will be greater than normal. To avoid this problem, use one of the following measures when executing from on-chip ROM:

- Do not use EEPMOV for block transfers. Use repeated MOV instructions instead.

- Use the hardware standby mode, in which there is no additional current dissipation.

15.5 Hardware Standby Mode

15.5.1 Transition to Hardware Standby Mode

Regardless of its current state, the chip enters the hardware standby mode whenever the $\overline{\text{STBY}}$ pin goes low.

The hardware standby mode reduces power consumption drastically by halting the CPU, stopping all the functions of the on-chip supporting modules, and placing I/O ports in the high-impedance state. The registers of the on-chip supporting modules are reset to their initial values. Only the on-chip RAM is held unchanged, provided the minimum necessary voltage supply is maintained (at least 2V).

Notes: 1. The RAME bit in the system control register should be cleared to 0 before the $\overline{\text{STBY}}$ pin goes low, to disable the on-chip RAM during the hardware standby mode.

2. Do not change the inputs at the mode pins (MD1, MD0) during hardware standby mode. Be particularly careful not to let both mode pins go low in hardware standby mode, since that places the chip in PROM mode and increases current dissipation.

15.5.2 Recovery from Hardware Standby Mode

Recovery from the hardware standby mode requires inputs at both the $\overline{\text{STBY}}$ and $\overline{\text{RES}}$ pins.

When the $\overline{\text{STBY}}$ pin goes high, the clock oscillator begins running. The $\overline{\text{RES}}$ pin should be low at this time and should be held low long enough for the clock to stabilize. When the $\overline{\text{RES}}$ pin changes from low to high, the reset sequence is executed and the chip returns to the program execution state.

15.5.3 Timing Relationships

Figure 15-2 shows the timing relationships in the hardware standby mode.

In the sequence shown, first $\overline{\text{RES}}$ goes low, then $\overline{\text{STBY}}$ goes low, at which point this LSI enters the hardware standby mode. To recover, first $\overline{\text{STBY}}$ goes high, then after the clock settling time, $\overline{\text{RES}}$ goes high.

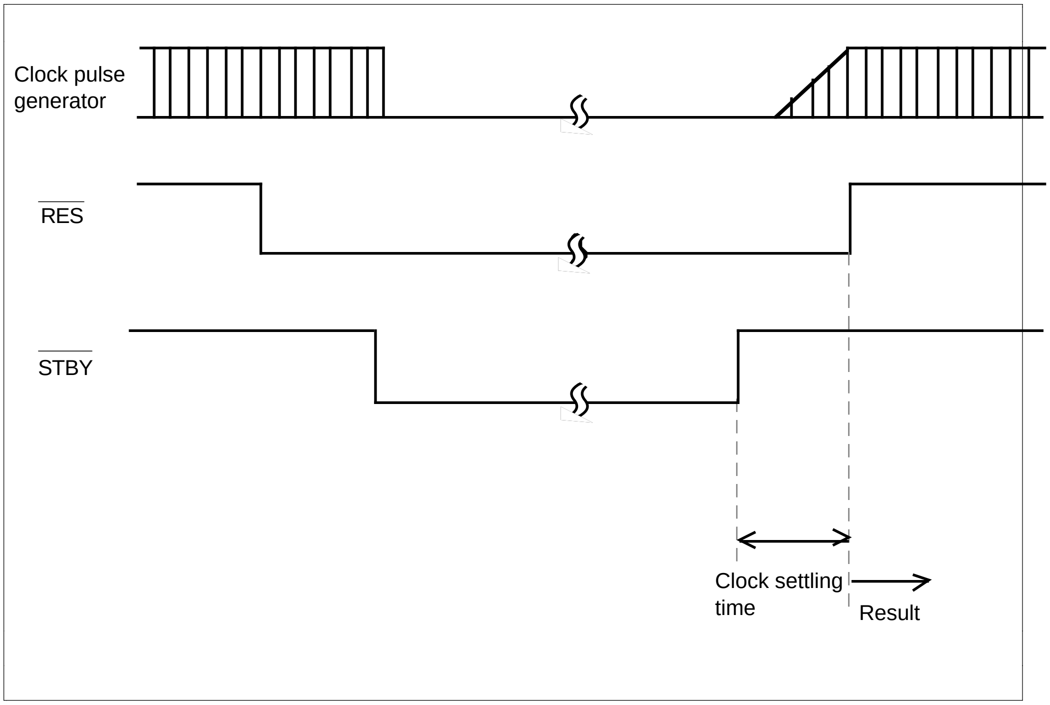


Figure 15-2 Hardware Standby Mode Timing

Section 16 Clock Pulse Generator

16.1 Overview

The H8/3332 has a built-in clock pulse generator (CPG) consisting of an oscillator circuit, a system (ϕ) clock divider, and a prescaler (figure 16-1). The prescaler generates clock signals for the on-chip supporting modules.

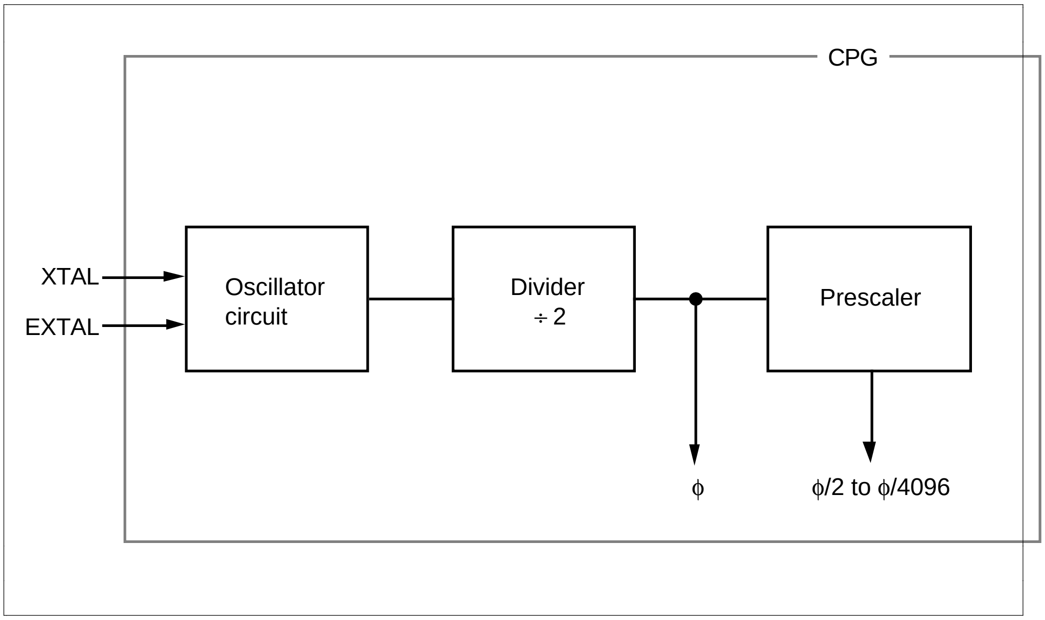


Figure 16-1 Block Diagram of Clock Pulse Generator

16.2 Oscillator Circuit

If an external crystal is connected across the EXTAL and XTAL pins, the on-chip oscillator circuit generates a clock signal for the system clock divider. Alternatively, an external clock signal can be applied to the EXTAL pin.

16.2.1 Connecting an External Crystal

Circuit Configuration: An external crystal can be connected as in the example in figure 16-2. An AT-cut parallel resonating crystal should be used. Figure 16-3 shows the external crystal equivalent circuit.

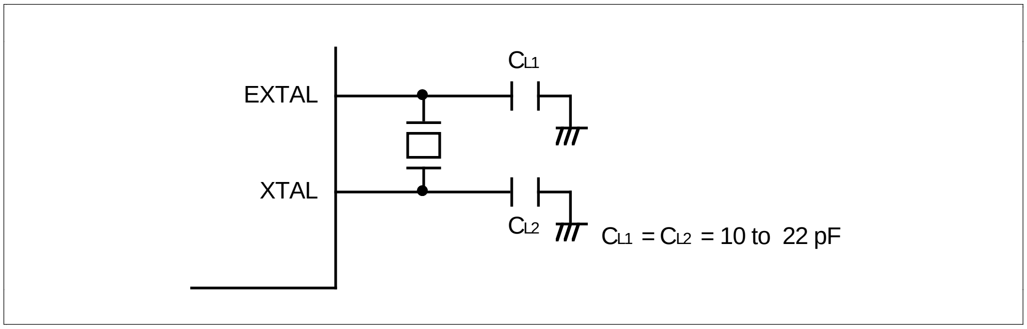


Figure 16-2 Connection of Crystal Oscillator (Example)

Crystal Oscillator: The external crystal should have the characteristics listed in table 16-1.

Table 16-1 External Crystal Parameters

Frequency (MHz)	R_S Max (Ω)	C_O (pF)
2	500	7 pF max
4	120	
8	60	
12	40	
16	30	
20	20	

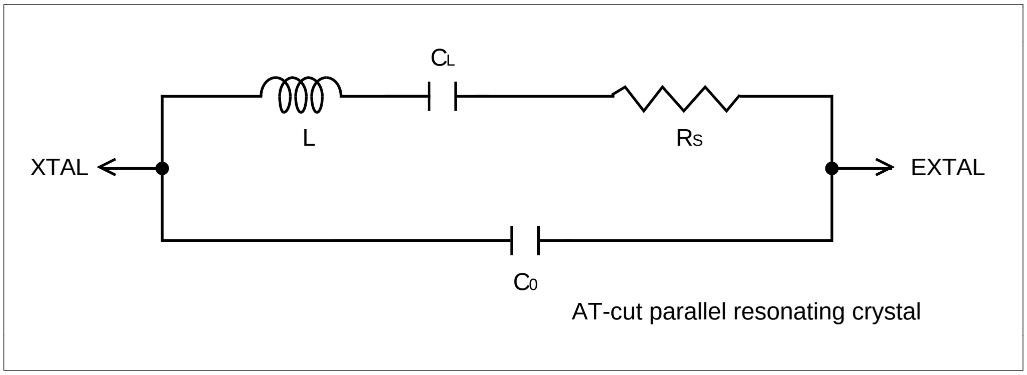


Figure 16-3 Equivalent Circuit of External Crystal

Note on Board Design: When an external crystal is connected, other signal lines should be kept away from the crystal circuit to prevent induction from interfering with correct oscillation. See figure 16-4. The crystal and its load capacitors should be placed as close as possible to the XTAL and EXTAL pins.

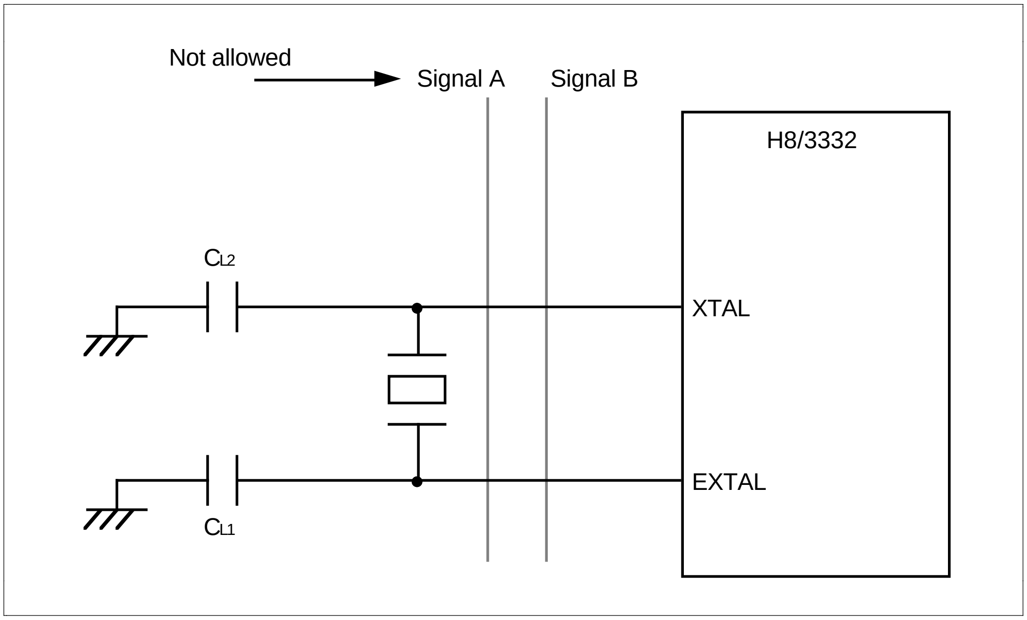


Figure 16-4 Notes on Board Design around External Crystal

16.2.2 Input of External Clock Signal

Circuit Configuration: An external clock signal can be input as shown in the examples in figure 16-5. In example (b), the external clock signal should be kept high during standby.

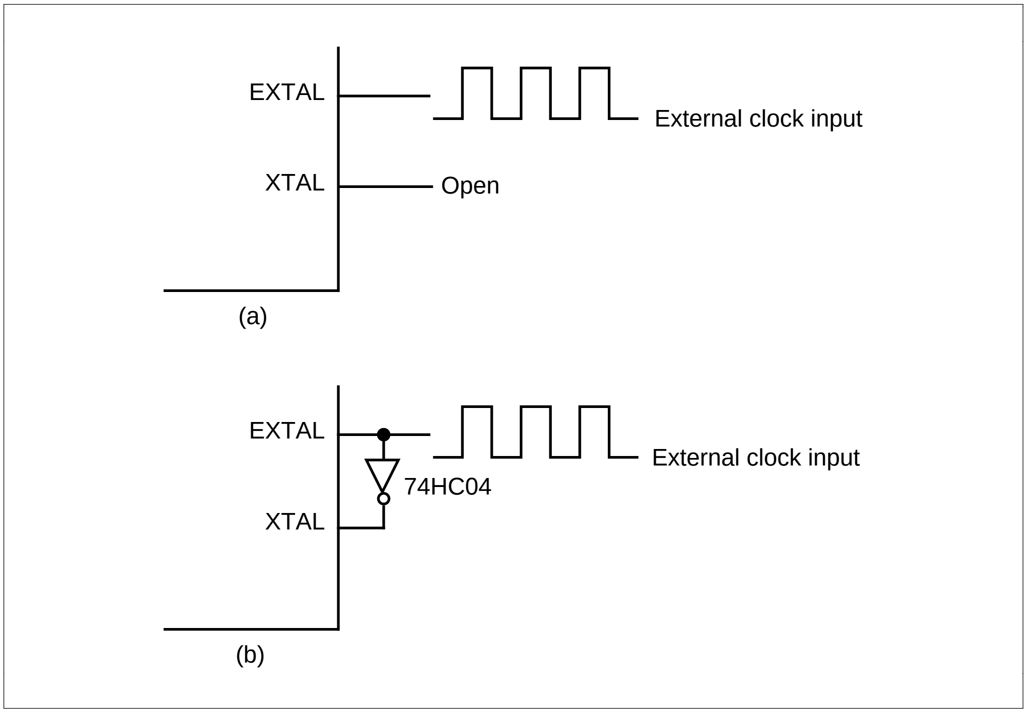


Figure 16-5 External Clock Input (Example)

External Clock Input: Table 16-2 shows the external clock specifications.

Table 16-2 External Clock

Item	Specification
Frequency	Double the system clock (ϕ) frequency
Duty factor	45% to 55%

16.3 System Clock Divider

The system clock divider divides the crystal oscillator or external clock frequency by 2 to create the system clock (ϕ).

Section 17 Electrical Specifications

17.1 Absolute Maximum Ratings

Table 17-1 lists the absolute maximum ratings.

Table 17-1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Programming voltage	V_{PP}	–0.3 to +13.5	V
Input voltage:			
Ports 1–6, 8, 9	Vin	–0.3 to V_{CC} + 0.3	V
Port 7	Vin	–0.3 to AV_{CC} + 0.3	V
Analog supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note: Exceeding the absolute maximum ratings shown in table 17-1 can permanently destroy the chip.

17.2 Electrical Characteristics

17.2.1 DC Characteristics

Table 17-2 lists the DC characteristics of the 5-V version. Table 17-3 lists the DC characteristics of the 3-V version.

Table 17-2 DC Characteristics (5-V Version)

(V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%$^{\text{Note 1}}$, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications))

							Measurement
Item		**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Schmitt trigger input voltage (1)	$P6_7$–$P6_0^{\text{Note 2}}$, $\overline{\text{IRQ}}_0$–$\overline{\text{IRQ}}_2^{\text{Note 3}}$, $\overline{\text{IRQ}}_3$–$\overline{\text{IRQ}}_5$	V_T^-	1.0	—	—	V	
		V_T^+	—	—	V_{CC} × 0.7	V	
		$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage (2)	$\overline{\text{RES}}$, $\overline{\text{STBY}}$, MD_1, MD_0, EXTAL, $\overline{\text{NMI}}$	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	$P7_7$–$P7_0$		2.0	—	AV_{CC} + 0.3	V	
Input high voltage	Input pins other than (1) and (2)		2.0	—	V_{CC} + 0.3	V	
Input low voltage (3)	$\overline{\text{RES}}$, $\overline{\text{STBY}}$, MD_1, MD_0	V_{IL}	–0.3	—	0.5	V	
Input low voltage	Input pins other than (1) and (3)	V_{IL}	–0.3	—	0.8	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1.0 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1 and 2		—	—	1.0	V	I_{OL} = 10.0 mA
Input leakage current	$\overline{\text{RES}}$	$\lvert \text{Iin} \rvert$	—	—	10.0	µA	Vin = 0.5 V to V_{CC} – 0.5 V
	$\overline{\text{STBY}}$, $\overline{\text{NMI}}$, MD_1, MD_0		—	—	1.0	µA	
	$P7_7$–$P7_0$		—	—	1.0	µA	Vin = 0.5 V to AV_{CC} – 0.5 V

Notes: 1. When the A/D converter is not in use, AV_{CC} should be connected to V_{CC} (power supply).

2. $P6_7$–$P6_0$ with auxiliary functions input

3. $\overline{\text{IRQ}}_2$ with $\overline{\text{ADTRG}}$ input

Table 17-2 DC Characteristics (5-V Version) (cont)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Leakage current in 3-state (off state)	Ports 1, 2, 3, 4, 5, 6, 8, 9	$\lvert ITSI \rvert$	—	—	1.0	µA	Vin = 0.5V to V_{CC} – 0.5V
Input pull-up current	Ports 1, 2, 3	–Ip	30	—	250	µA	Vin = 0 V
Input capacitance	$\overline{\text{RES}}$ (V_{PP})	Cin	—	—	60	pF	Vin = 0V
	$\overline{\text{NMI}}$		—	—	30	pF	
	All input pins except $\overline{\text{RES}}$ and $\overline{\text{NMI}}$		—	—	15	pF	f = 1 MHz Ta = 25°C
Current dissipation Note 1	Normal operation	I_{CC}	—	12	25	mA	f = 6 MHz
			—	16	30	mA	f = 8 MHz
			—	20	40	mA	f = 10 MHz
	Sleep mode		—	8	15	mA	f = 6 MHz
			—	10	20	mA	f = 8 MHz
			—	12	25	mA	f = 10 MHz
	Standby modes Note 2		—	0.01	5.0	µA	
Analog supply current	During A/D conversion	AI_{CC}	—	0.6	1.5	mA	
	Waiting		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes:
1. Current dissipation values assume that V_{IH} min. = V_{CC} – 0.5V , V_{IL} max. = 0.5 V, all output pins are in the no-load state, and all input pull-ups are off.
2. For these values it is assumed that $V_{RAM} \leq V_{CC} < 4.5$ V and V_{IH} min. = $V_{CC} \times 0.9$, V_{IL} max. = 0.3 V.

Table 17-3 DC Characteristics (3-V Version)

(V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 5.0 V ±10%[Note 1], V_{SS} = AV_{SS} = 0 V, Ta = –20 to 75°C)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Schmitt trigger input voltage[Note 2] (1)	$P6_7$–$P6_0$[Note 3], $\overline{\text{IRQ}}_0$–$\overline{\text{IRQ}}_2$[Note 4], $\overline{\text{IRQ}}_3$–$\overline{\text{IRQ}}_5$	V_T^-	V_{CC} × 0.15	—	—	V	
		V_T^+	—	—	V_{CC} × 0.7	V	
		$V_T^+ - V_T^-$	0.2	—	—	V	
Input high voltage[Note 2] (2)	$\overline{\text{RES}}$, $\overline{\text{STBY}}$, MD_1, MD_0, EXTAL, $\overline{\text{NMI}}$	V_{IH}	V_{CC} × 0.9	—	V_{CC} + 0.3	V	
	$P7_7$–$P7_0$		V_{CC} × 0.7	—	AV_{CC} + 0.3	V	
Input high voltage[Note 2]	Input pins other than (1) and (2)		V_{CC} × 0.7	—	V_{CC} + 0.3	V	
Input low voltage (3)	$\overline{\text{RES}}$, $\overline{\text{STBY}}$, MD_1, MD_0	V_{IL}	–0.3	—	V_{CC} × 0.1	V	
	Input pins other than (1) and (3)		–0.3	—	V_{CC} × 0.15	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –200 µA
			V_{CC} – 0.9	—	—	V	I_{OH} = –1.0 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 0.8 mA
	Ports 1 and 2		—	—	0.4	V	I_{OL} = 1.6 mA

Notes:
1. Connect AV_{CC} to V_{CC} (+2.7 V to +3.6 V) when the A/D converter is not used.
2. In the range 3.6 V < V_{CC} < 4.5 V, for the input levels of V_{IH} and V_T+, apply the higher of the values given for the 5-V and 3-V versions. For V_{IL} and V_T–, apply the lower of the values given for the 5-V and 3-V versions.
3. $P6_7$–$P6_0$ with auxiliary functions input
4. $\overline{\text{IRQ}}_2$ with $\overline{\text{ADTRG}}$ input

Table 17-3 DC Characteristics (3-V Version) (cont)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input leakage current	$\overline{RES}$	$\lvert \mathrm{Iin} \rvert$	—	—	10.0	µA	Vin = 0.5 V to V_{CC} − 0.5 V
	$\overline{STBY}$, $\overline{NMI}$, MD_1, MD_0		—	—	1.0	µA	
	$P7_7$–$P7_0$		—	—	1.0	µA	Vin = 0.5 V to AV_{CC} − 0.5 V
Leakage current in 3-state (off state)	Ports 1, 2, 3, 4, 5, 6, 8, 9	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	Vin = 0.5V to V_{CC} − 0.5V
Input pull-up current	Ports 1, 2, 3	–Ip	3	—	120	µA	Vin = 5.0 V
Input capacitance	$\overline{RES}$	Cin	—	—	60	pF	Vin = 0V
	$\overline{NMI}$		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and $\overline{NMI}$		—	—	15	pF	Ta = 25°C
Current dissipation Note 3	Normal operation	I_{CC}	—	6	—	mA	f = 3 MHz
			—	10	20	mA	f = 5 MHz
	Sleep mode		—	4	—	mA	f = 3 MHz
			—	6	12	mA	f = 5 MHz
	Standby modes Note 4		—	0.01	5.0	µA	
Analog supply current	During A/D conversion	AI_{CC}	—	0.6	1.5	mA	
	Waiting		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes (cont):

5. Current dissipation values assume that V_{IH} min. = V_{CC} – 0.5V, V_{IL} max. = 0.5 V, all output pins are in the no-load state, and all input pull-ups are off.
6. For these values it is assumed that $V_{RAM} \leq V_{CC} < 2.7$ V and V_{IH} min. = V_{CC} × 0.9, V_{IL} max. = 0.3 V.

Table 17-4 Allowable Output Current Sink Values
(5-V Version: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, Ta = –20 to 75°C (regular specifications) Ta = –40 to 85°C (wide-range specifications))
(3-V Version: V_{CC} = 2.7 V to +3.6 V, V_{SS} = 0 V, Ta = –20 to 75°C)

			5 V		3 V		
Item		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Allowable output low current sink (per pin)	Ports 1 and 2	I_{OL}	—	10	—	2	mA
	Other output pins		—	2.0	—	1	mA
Allowable output low current sink (total)	Ports 1 and 2, total	ΣI_{OL}	—	80	—	40	mA
	Total of all output pins		—	120	—	60	mA
Allowable output high current sink (per pin)	All output pins	$-I_{OH}$	—	2.0	—	2	mA
Allowable output high current sink (total)	Total of all output	$\Sigma -I_{OH}$	—	40	—	30	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 17-4. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 17-1 and 17-2.

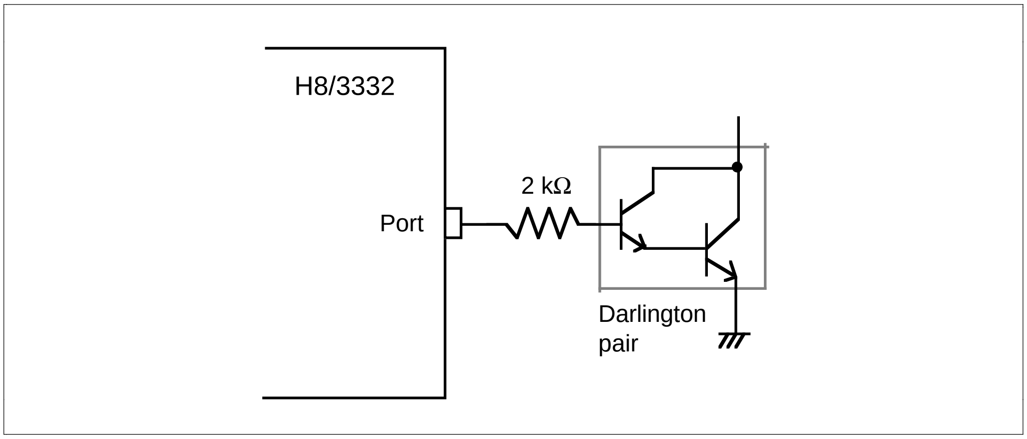


Figure 17-1 Circuit Example for Driving a Darlington Pair

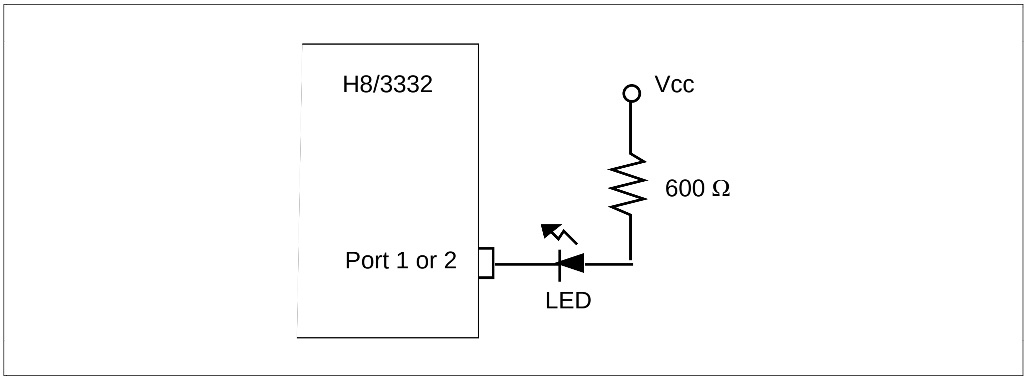


Figure 17-2 Circuit Example for Driving a LED

17.2.2 AC Characteristics

The AC characteristics are listed in tables 17-4 to 17-6. Bus timing parameters are given in table 17-4, control signal timing parameters in table 17-5, and timing parameters of the on-chip supporting modules in table 17-6.

Table 17-5 Bus Timing
(5-V Version: V_{CC} = 5.0 V ±10%, V_{SS} = 0V, ϕ = 0.5 MHz to maximum operating frequency, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications))
(3-V Version: V_{CC} = +2.7 V to +3.6 V, V_{SS} = 0V, ϕ = 0.5 to 10 MHz, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications))

		3 V		5 V							
		5 MHz		6 MHz		8 MHz		10 MHz			Measurement
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Conditions
Clock cycle time	t_{cyc}	200	2000	166.7	2000	125	2000	100	2000	ns	Fig. 17-4
Clock pulse width low	t_{CL}	70	—	65	—	45	—	35	—	ns	Fig. 17-4
Clock pulse width high	t_{CH}	70	—	65	—	45	—	35	—	ns	Fig. 17-4
Clock rise time	t_{Cr}	—	25	—	15	—	15	—	15	ns	Fig. 17-4
Clock fall time	t_{Cf}	—	25	—	15	—	15	—	15	ns	Fig. 17-4
Address delay time	t_{AD}	—	90	—	70	—	60	—	50	ns	Fig. 17-4
Address hold time	t_{AH}	30	—	30	—	25	—	20	—	ns	Fig. 17-4
Address strobe delay time	t_{ASD}	—	80	—	70	—	60	—	40	ns	Fig. 17-4
Write strobe delay time	t_{WSD}	—	80	—	70	—	60	—	50	ns	Fig. 17-4

Table 17-5 Bus Timing (cont)

		3 V		5 V							
		5 MHz		6 MHz		8 MHz		10 MHz			Measurement
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Strobe delay time	t_{SD}	—	90	—	70	—	60	—	50	ns	Fig. 17-4
Write strobe pulse width[Note]	t_{WSW}	200	—	200	—	150	—	120	—	ns	Fig. 17-4
Address setup time 1[Note]	t_{AS1}	25	—	25	—	20	—	15	—	ns	Fig. 17-4
Address setup time 2[Note]	t_{AS2}	105	—	105	—	80	—	65	—	ns	Fig. 17-4
Read data setup time	t_{RDS}	90	—	70	—	50	—	35	—	ns	Fig. 17-4
Read data hold time[Note]	t_{RDH}	0	—	0	—	0	—	0	—	ns	Fig. 17-4
Read data access time[Note]	t_{ACC}	—	300	—	270	—	210	—	170	ns	Fig. 17-4
Write data delay time	t_{WDD}	—	125	—	85	—	75	—	75	ns	Fig. 17-4
Write data setup time	t_{WDS}	10	—	20	—	10	—	5	—	ns	Fig. 17-4
Write data hold time	t_{WDH}	30	—	30	—	25	—	20	—	ns	Fig. 17-4
Wait setup time	t_{WTS}	60	—	40	—	40	—	40	—	ns	Fig. 17-5
Wait hold time	t_{WTH}	20	—	10	—	10	—	10	—	ns	Fig. 17-5

Note: Values at maximum operating frequency.

Table 17-6 Control Signal Timing
(5-V Version: V_{CC} = 5.0V ±10%, V_{SS} = 0 V, ϕ = 0.5 MHz to maximum operating frequency, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications))
(3-V Version: V_{CC} = +2.7 V to +3.6 V, V_{SS} = 0 V, ϕ = 0.5 MHz to maximum operating frequency, Ta-= –20 to 75°C)

		3 V		5 V							
		5 MHz		6 MHz		8 MHz		10 MHz			Measurement
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Conditions
$\overline{\text{RES}}$ setup time	t_{RESS}	300	—	200	—	200	—	200	—	ns	Fig. 17-6
$\overline{\text{RES}}$ pulse width	t_{RESW}	10	—	10	—	10	—	10	—	tcyc	Fig. 17-6
NMI setup time ($\overline{\text{NMI}}$, $\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_7$)	t_{NMIS}	300	—	150	—	150	—	150	—	ns	Fig. 17-7
NMI hold time ($\overline{\text{NMI}}$, $\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_7$)	t_{NMIH}	10	—	10	—	10	—	10	—	ns	Fig. 17-7
Interrupt pulse width for recovery from software standby mode ($\overline{\text{NMI}}$, $\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_2$)	t_{NMIW}	300	—	200	—	200	—	200	—	ns	Fig. 17-7
Crystal oscillator settling time (reset)	t_{OSC1}	20	—	20	—	20	—	20	—	ms	Fig. 17-8
Crystal oscillator settling time (software standby)	t_{OSC2}	10	—	10	—	10	—	10	—	ms	Fig. 17-9

Table 17-7 Timing Conditions of On-Chip Supporting Modules
(5-V Version: V_{CC} = 5.0V ±10%, V_{SS} = 0 V, ϕ = 0.5 MHz to maximum operating frequency, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications))
(3-V Version: V_{CC} = +2.7 V to +3.6 V, V_{SS} = 0 V, ϕ = 0.5 MHz to maximum operating frequency, Ta-= –20 to 75°C)

			3 V		5 V							
			5 MHz		6 MHz		8 MHz		10 MHz			Measurement
	Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Conditions
FRT	Timer output delay time	t_{FTOD}	—	150	—	100	—	100	—	100	ns	Fig. 17-10
	Timer input setup time	t_{FTIS}	80	—	50	—	50	—	50	—	ns	Fig. 17-10
	Timer clock input setup time	t_{FTCS}	80	—	50	—	50	—	50	—	ns	Fig. 17-11
	Timer clock pulse width	t_{FTCWH}, t_{FTCWL}	1.5	—	1.5	—	1.5	—	1.5	—	tcyc	Fig. 17-11
TMR	Timer output delay time	t_{TMOD}	—	150	—	100	—	100	—	100	ns	Fig. 17-12
	Timer reset input setup time	t_{TMRS}	80	—	50	—	50	—	50	—	ns	Fig. 17-14
	Timer clock input setup time	t_{TMCS}	80	—	50	—	50	—	50	—	ns	Fig. 17-13
	Timer clock pulse width (single edge)	t_{TMCWH}	1.5	—	1.5	—	1.5	—	1.5	—	tcyc	Fig. 17-13
	Timer clock pulse width (both edges)	t_{TMCWL}	2.5	—	2.5	—	2.5	—	2.5	—	tcyc	Fig. 17-13
PWM	Timer output delay time	t_{PWOD}	—	150	—	100	—	100	—	100	ns	Fig. 17-15

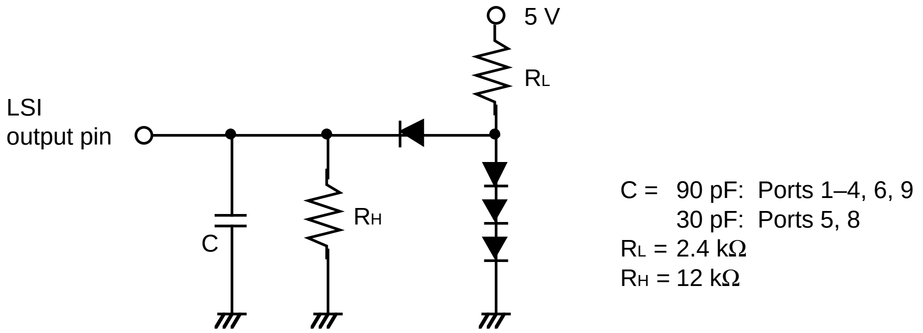
Table 17-7 Timing Conditions of On-Chip Supporting Modules (cont)

			3 V		5 V							
			5 MHz		6 MHz		8 MHz		10 MHz			Measurement
	Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Conditions
SCI	Input clock cycle (Async)	t_{scyc}	4	—	4	—	4	—	4	—	tcyc	Fig. 17-16
	(Sync)	t_{scyc}	6	—	6	—	6	—	6	—	tcyc	Fig. 17-16
	Transmit data delay time (Sync)	t_{TXD}	—	200	—	100	—	100	—	100	ns	Fig. 17-16
	Receive data setup time (Sync)	t_{RXS}	150	—	100	—	100	—	100	—	ns	Fig. 17-16
	Receive data hold time (Sync)	t_{RXH}	150	—	100	—	100	—	100	—	ns	Fig. 17-16
	Input clock pulse width	t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{scyc}	Fig. 17-17
Ports	Output data delay time	t_{PWD}	—	150	—	100	—	100	—	100	ns	Fig. 17-18
	Input data setup time	t_{PRS}	80	—	50	—	50	—	50	—	ns	Fig. 17-18
	Input data hold time	t_{PRH}	80	—	50	—	50	—	50	—	ns	Fig. 17-18
HIF read cycle	$\overline{\text{CS}}/\text{HA}_0$ to $\overline{\text{IOR}}$ ↓ setup time	t_{HAR}	10	—	10	—	10	—	10	—	ns	Fig. 17-19
	$\overline{\text{CS}}/\text{HA}_0$ hold time from $\overline{\text{IOR}}$ ↑	t_{HRA}	10	—	10	—	10	—	10	—	ns	Fig. 17-19
	$\overline{\text{IOR}}$ pulse width	t_{HRPW}	220	—	120	—	120	—	120	—	ns	Fig. 17-19
	$\overline{\text{IOR}}$ ↓ to HDB valid delay time	t_{HRD}	—	200	—	100	—	100	—	100	ns	Fig. 7-19
	$\overline{\text{IOR}}$ ↑ to HDB float delay time	t_{HRF}	0	40	0	25	0	25	0	25	ns	Fig. 7-19
	HIRQ_i delay from $\overline{\text{IOR}}$ ↑	t_{HIRQi}	—	200	—	120	—	120	—	120	ns	Fig. 7-19

Table 17-7 Timing Conditions of On-Chip Supporting Modules (cont)

			3 V		5 V							
			5 MHz		6 MHz		8 MHz		10 MHz			Measurement
	Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Conditions
HIF write cycle	$\overline{\text{CS}}/\text{HA}_0$ to $\overline{\text{IOW}}$ ↓ setup time	t_{HAW}	10	—	10	—	10	—	10	—	ns	Fig. 17-20
	$\overline{\text{CS}}/\text{HA}_0$ hold time from $\overline{\text{IOW}}$ ↑	t_{HWA}	10	—	10	—	10	—	10	—	ns	Fig. 17-20
	$\overline{\text{IOW}}$ pulse width	t_{HWPW}	100	—	60	—	60	—	60	—	ns	Fig. 17-20
	HDB valid to $\overline{\text{IOW}}$ ↑ setup time	t_{HDW}	50	—	30	—	30	—	30	—	ns	Fig. 17-20
	HDB hold time after $\overline{\text{IOW}}$ ↑	t_{HWD}	25	—	15	—	15	—	15	—	ns	Fig. 17-20
	GA_{20} delay from $\overline{\text{IOW}}$ ↑	t_{HGA}	—	180	—	90	—	90	—	90	ns	Fig. 17-20

Measurement Conditions for AC Characteristics



Input/output timing reference levels

Low: 0.8 V
High: 2.0 V

Figure 17-3 Output Load Circuit

17.2.3 A/D Converter Characteristics

Table 17-8 A/D Converter Characteristics

(Condition A: $V_{CC} = AV_{CC} = 5.0$ V ±10%, $V_{SS} = AV_{SS} = 0$ V, $\phi = 0.5$ MHz to maximum operating frequency, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications))
(Condition B1: $V_{CC} = +2.7$ V to +3.6 V, $AV_{CC} = 5.0$ V ±10%, $V_{SS} = AV_{SS} = 0$ V, $\phi = 0.5$ MHz to maximum operating frequency, Ta = –20 to 75°C)
(Condition B2: $V_{CC} = +2.7$ V to +3.6 V, $AV_{CC} = 2.7$V to 3.6V, $V_{SS} = AV_{SS} = 0$ V, $\phi = 0.5$ MHz to maximum operating frequency, Ta = –20 to 75°C)

	B2			**B1**			**A**			
	5 MHz			**5 MHz**			**10 MHz**			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	8	8	8	8	8	8	8	8	8	Bits
Conversion time (single mode)[Note]	—	—	122	—	—	122	—	—	122	tCYC
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal source impedance	—	—	10	—	—	10	—	—	10	kΩ
Nonlinearity error	—	—	±1.5	—	—	±1	—	—	±1	LSB
Offset error	—	—	±1	—	—	±1	—	—	±1	LSB
Full-scale error	—	—	±1	—	—	±1	—	—	±1	LSB
Quantizing error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±2.0	—	—	±1.5	—	—	±1.5	LSB

Note: Values at maximum operating frequency.

17.3 MCU Operational Timing

This section provides the following timing charts:

• 17.3.1 Bus Timing	Figures 17-4 to 17-5
• 17.3.2 Control Signal Timing	Figures 17-6 to 17-9
• 17.3.3 16-Bit Free-Running Timer Timing	Figures 17-10 to 17-11
• 17.3.4 8-Bit Timer Timing	Figures 17-12 to 17-14
• 17.3.5 PWM Timer Timing	Figure 17-15
• 17.3.6 SCI Timing	Figures 17-16 to 17-17
• 17.3.7 I/O Port Timing	Figure 17-18
• 17.3.8 Host interface Timing	Figures 17-19 to 17-20

17.3.1 Bus Timing

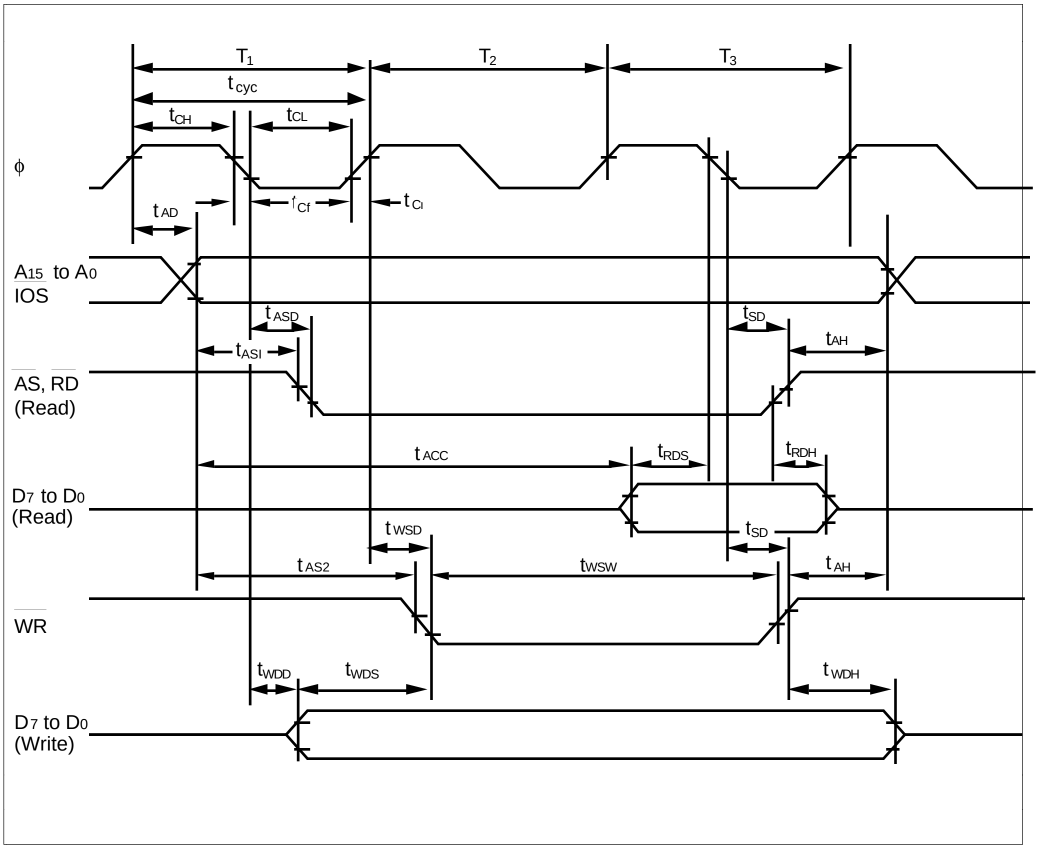


Figure 17-4 Basic Bus Cycle (Without Wait States) in Expanded Modes

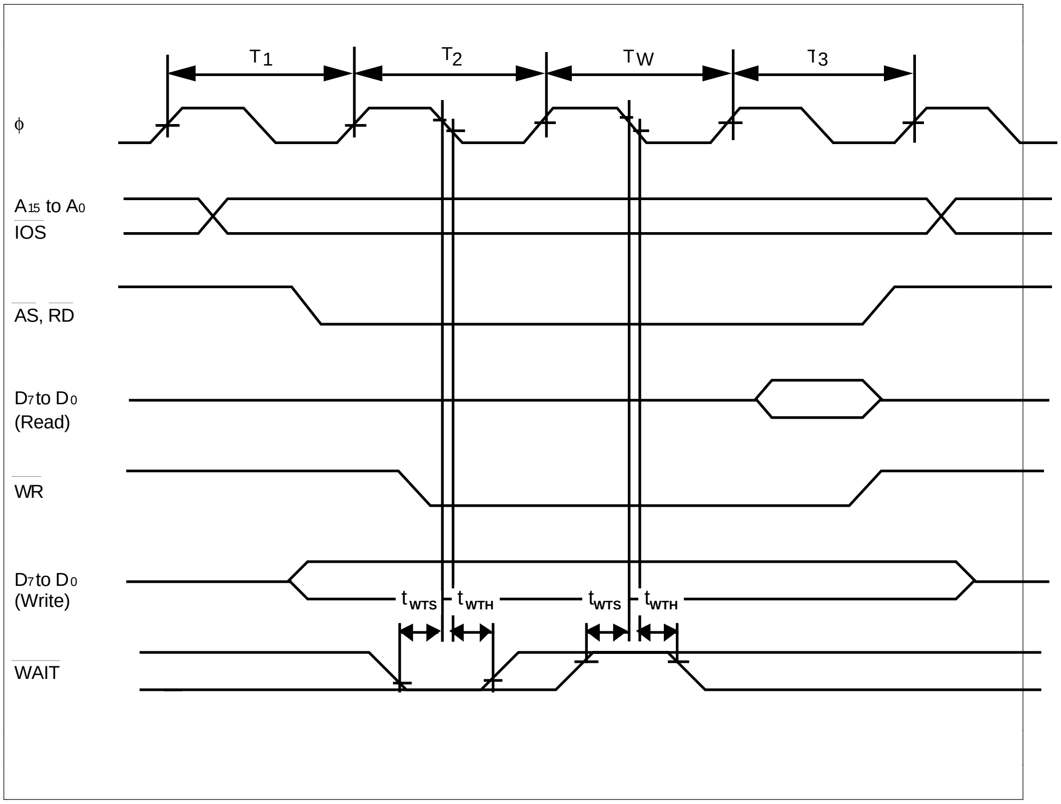


Figure 17-5 Basic Bus Cycle (With 1 Wait State) in Expanded Modes (Modes 1 and 2)

17.3.2 Control Signal Timing

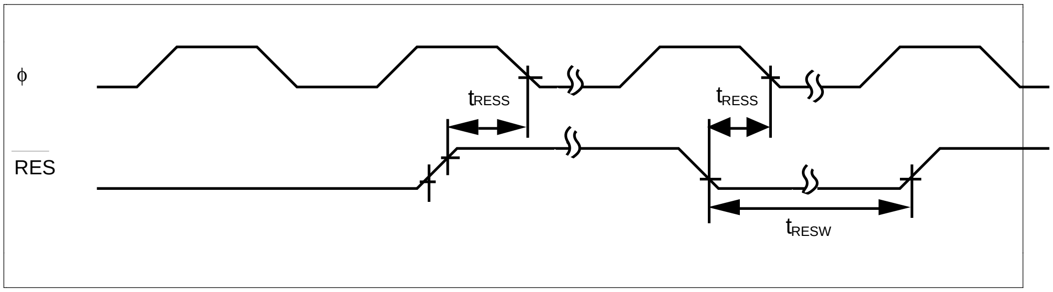


Figure 17-6 Reset Input Timing

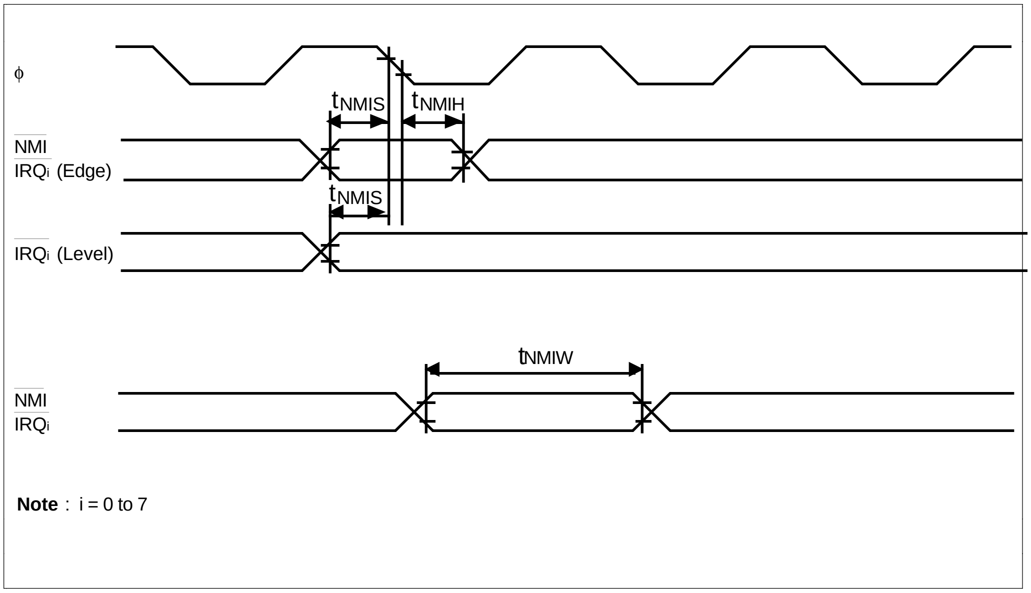


Figure 17-7 Interrupt Input Timing

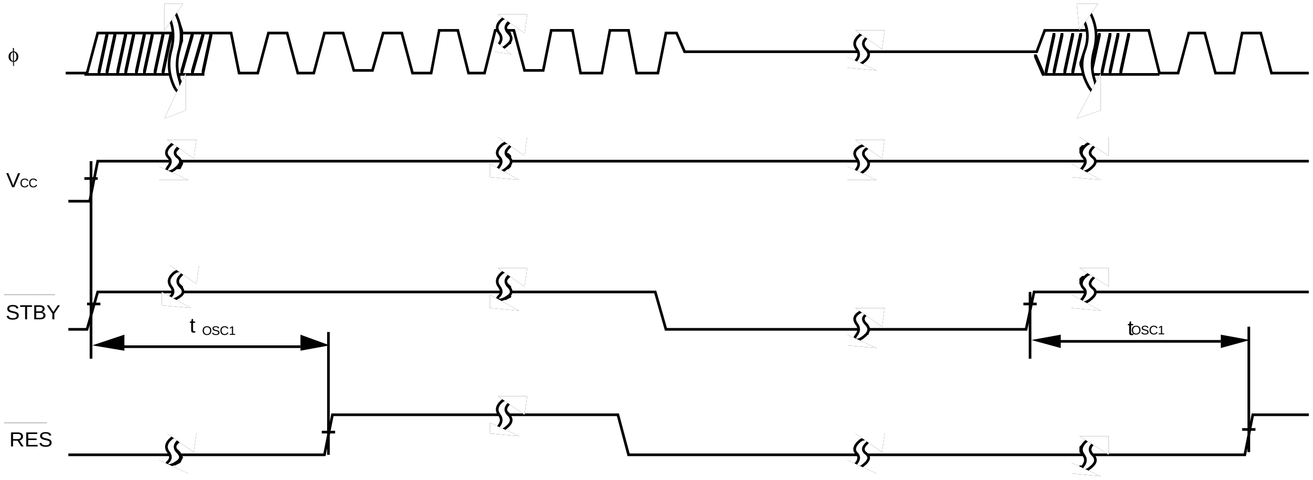


Figure 17-8 Clock Settling Timing

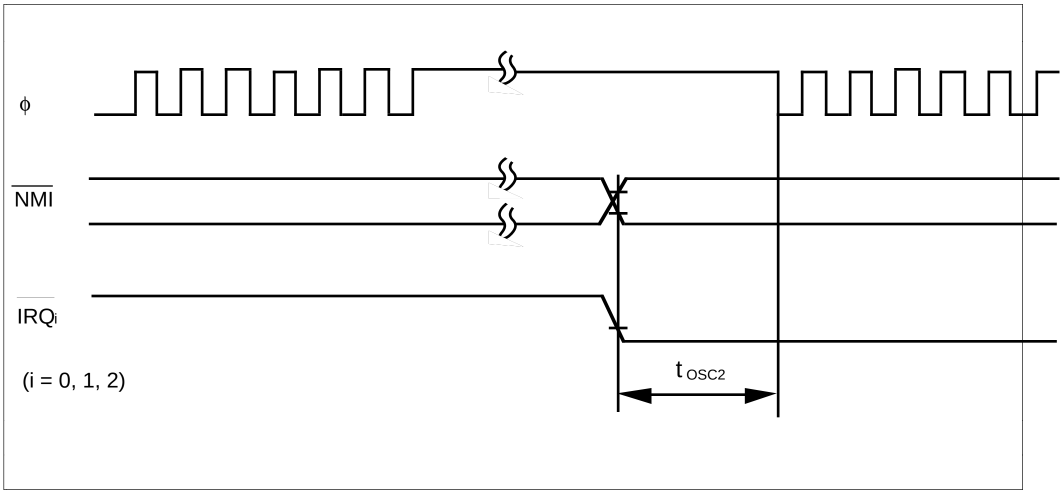


Figure 17-9 Clock Settling Timing for Recovery from Software Standby Mode

17.3.3 16-Bit Free-Running Timer Timing

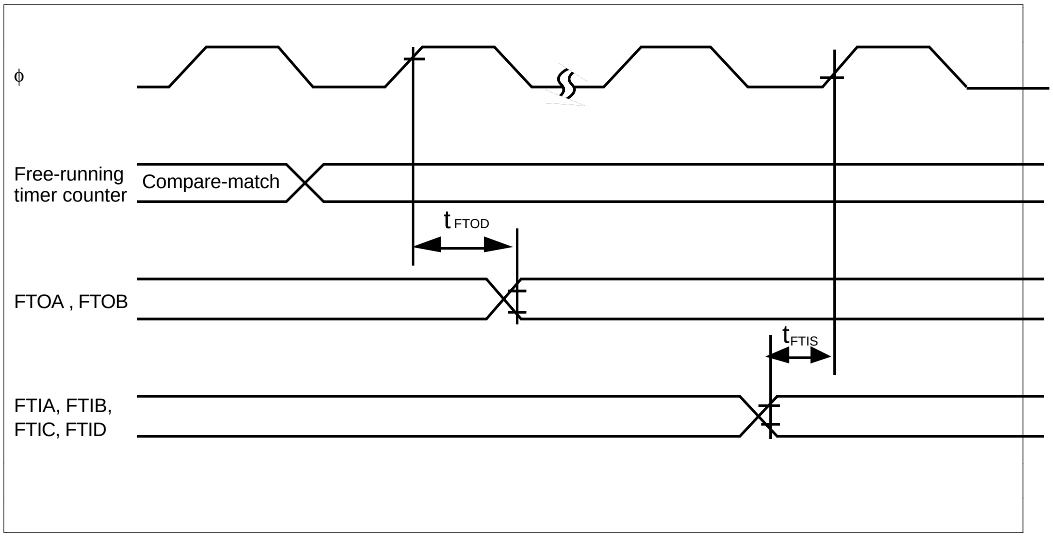


Figure 17-10 Free-Running Timer Input/Output Timing

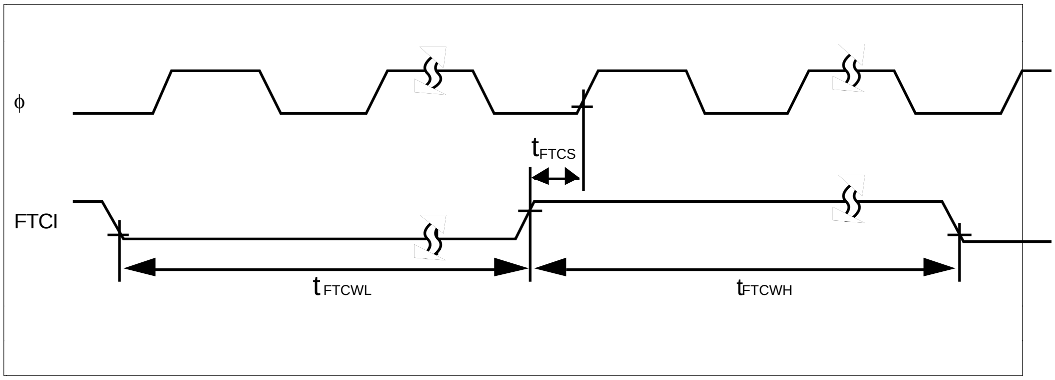


Figure 17-11 External Clock Input Timing for Free-Running Timer

17.3.4 8-Bit Timer Timing

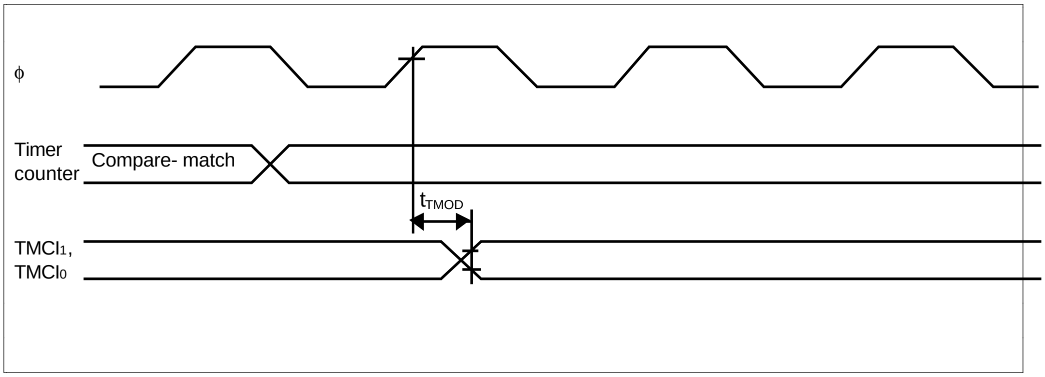


Figure 17-12   8-Bit Timer Output Timing

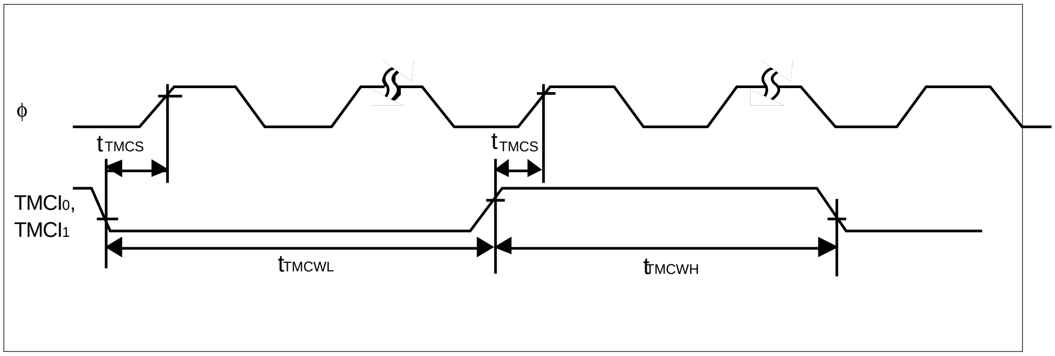


Figure 17-13   8-Bit Timer Clock Input Timing

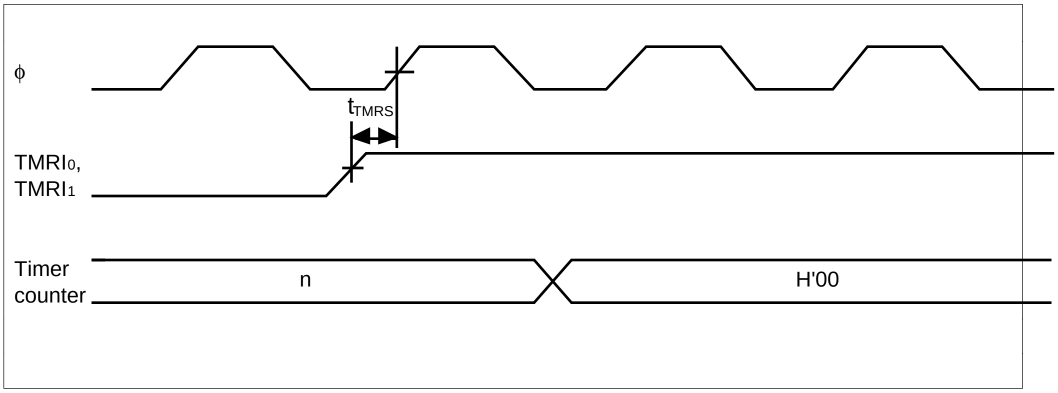


Figure 17-14 8-Bit Timer Reset Input Timing

17.3.5 Pulse Width Modulation Timer Timing

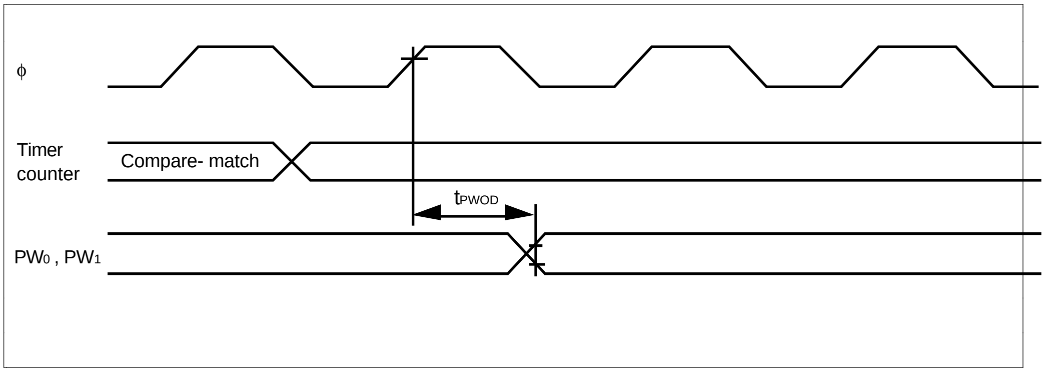


Figure 17-15 PWM Timer Output Timing

17.3.6 Serial Communication Interface Timing

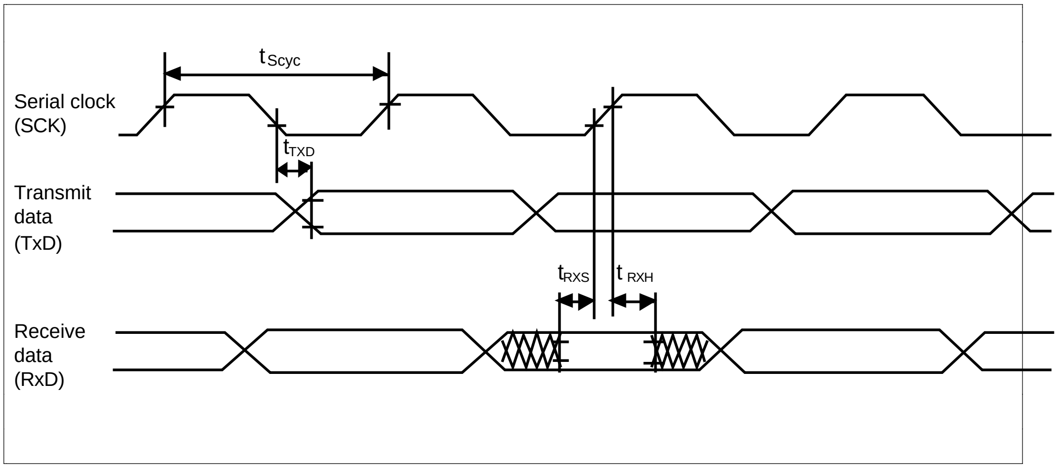


Figure 17-16 SCI Input/Output Timing (Synchronous Mode)

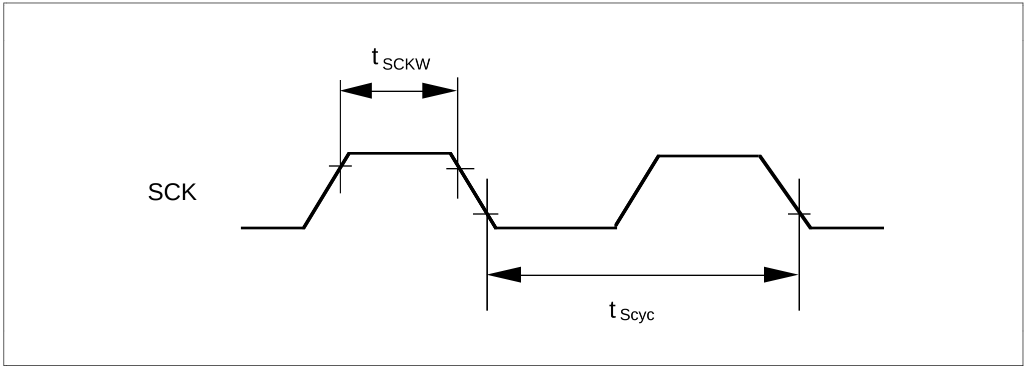


Figure 17-17 SCI Input Clock Timing

17.3.7 I/O Port Timing

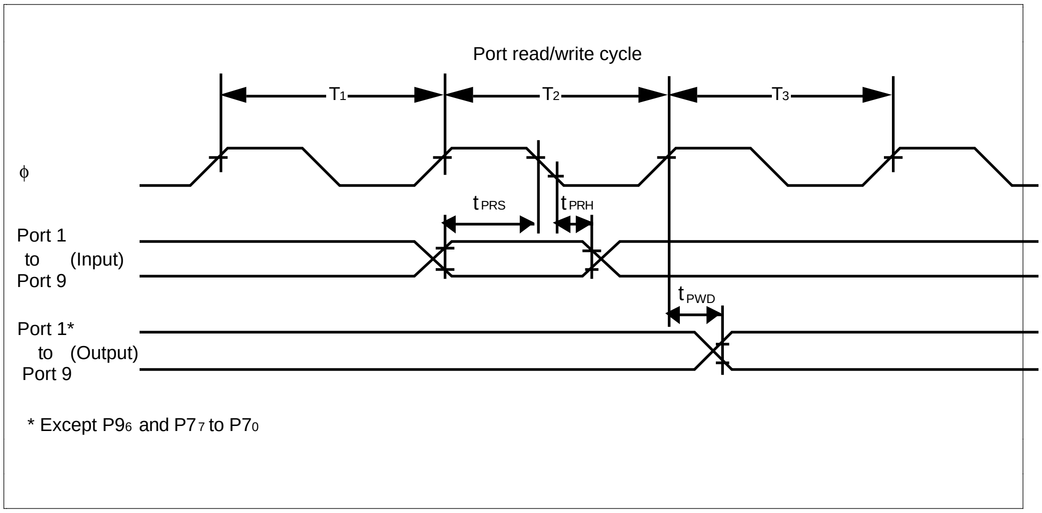


Figure 17-18 I/O Port Input/Output Timing

17.3.8 Host Interface Timing

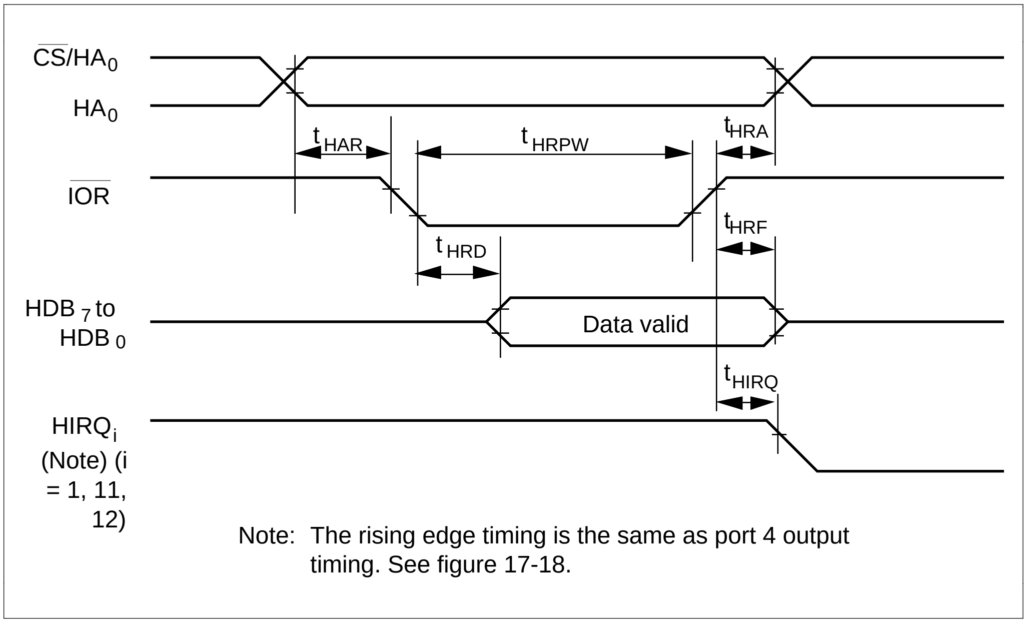


Figure 17-19 Host Interface Read Timing

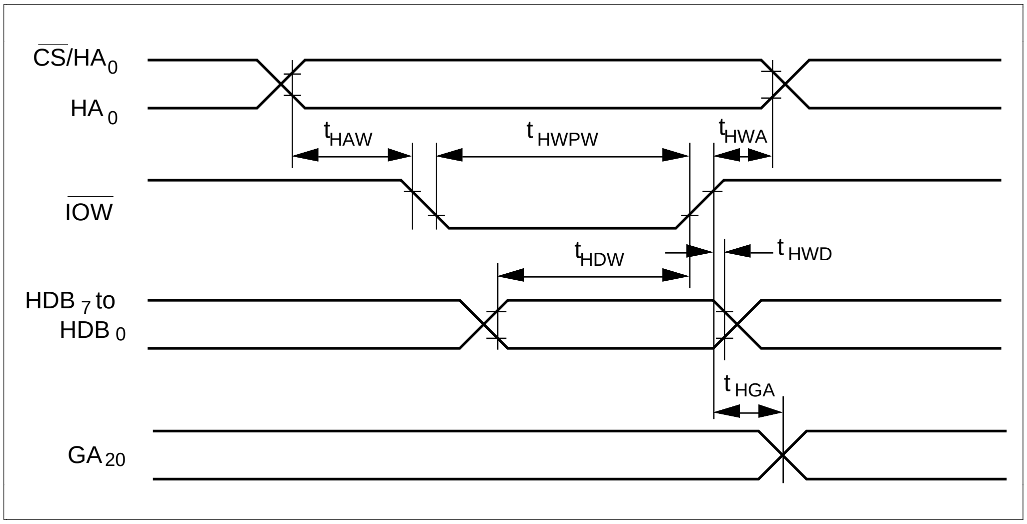


Figure 17-20 Host Interface Write Timing

Appendix A. CPU Instruction Set

A.1 Instruction Set List

Operation Notation

Rd8/16	General register (destination) (8 or 16 bits)
Rs8/16	General register (source) (8 or 16 bits)
Rn8/16	General register (8 or 16 bits)
CCR	Condition code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#xx:3/8/16	Immediate data (3, 8, or 16 bits)
d:8/16	Displacement (8 or 16 bits)
@aa:8/16	Absolute address (8 or 16 bits)
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	AND logical
∨	OR logical
⊕	Exclusive OR logical
→	Move
—	Not

Condition Code Notation

↕	Modified according to the instruction result
*	Undetermined (unpredictable)
0	Always cleared to “0”
—	Not affected by the instruction result

Table A-1. Instruction Set

Mnemonic	Operand size	Operation	Addressing mode/ instruction length									Condition code						No. of states
			#xx:8/16	Rn	@Rn	@(d:16,Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8,PC)	@@aa	Implied	I	H	N	Z	V	C	
MOV.B #xx:8,Rd	B	#xx:8 → Rd8	2									–	–	↕	↕	0	–	2
MOV.B Rs,Rd	B	Rs8 → Rd8		2								–	–	↕	↕	0	–	2
MOV.B @Rs,Rd	B	@Rs16 → Rd8			2							–	–	↕	↕	0	–	4
MOV.B @(d:16,Rs),Rd	B	@(d:16,Rs16) → Rd8				4						–	–	↕	↕	0	–	6
MOV.B @Rs+,Rd	B	@Rs16 → Rd8 Rs16+1 → Rs16					2					–	–	↕	↕	0	–	6
MOV.B @aa:8,Rd	B	@aa:8 → Rd8						2				–	–	↕	↕	0	–	4
MOV.B @aa:16,Rd	B	@aa:16 → Rd8						4				–	–	↕	↕	0	–	6
MOV.B Rs,@Rd	B	Rs8 → @Rd16			2							–	–	↕	↕	0	–	4
MOV.B Rs,@(d:16,Rd)	B	Rs8 → @(d:16,Rd16)				4						–	–	↕	↕	0	–	6
MOV.B Rs,@–Rd	B	Rd16–1 → Rd16 Rs8 → @Rd16					2					–	–	↕	↕	0	–	6
MOV.B Rs,@aa:8	B	Rs8 → @aa:8						2				–	–	↕	↕	0	–	4
MOV.B Rs,@aa:16	B	Rs8 → @aa:16						4				–	–	↕	↕	0	–	6
MOV.W #xx:16,Rd	W	#xx:16 → Rd16	4									–	–	↕	↕	0	–	4
MOV.W Rs,Rd	W	Rs16 → Rd16		2								–	–	↕	↕	0	–	2
MOV.W @Rs,Rd	W	@Rs16 → Rd16			2							–	–	↕	↕	0	–	4
MOV.W @(d:16,Rs),Rd	W	@(d:16,Rs16) → Rd16				4						–	–	↕	↕	0	–	6
MOV.W @Rs+,Rd	W	@Rs16 → Rd16 Rs16+2 → Rs16					2					–	–	↕	↕	0	–	6
MOV.W @aa:16,Rd	W	@aa:16 → Rd16						4				–	–	↕	↕	0	–	6
MOV.W Rs,@Rd	W	Rs16 → @Rd16			2							–	–	↕	↕	0	–	4
MOV.W Rs,@(d:16,Rd)	W	Rs16 → @(d:16,Rd16)				4						–	–	↕	↕	0	–	6
MOV.W Rs,@–Rd	W	Rd16–2 → Rd16 Rs16 → @Rd16					2					–	–	↕	↕	0	–	6
MOV.W Rs, @aa:16	W	Rs16 → @aa:16						4				–	–	↕	↕	0	–	6
POP Rd	W	@SP → Rd16 SP+2 → SP					2					–	–	↕	↕	0	–	6
PUSH Rs	W	SP–2 → SP Rs16 → @SP					2					–	–	↕	↕	0	–	6
MOVFPE @aa:16,Rd	B	Not supported																
MOVTPE Rs,@aa:16	B	Not supported																
EEPMOV	–	if R4L≠0 then Repeat @R5 → @R6 R5+1 → R5 R6+1 → R6 R4L–1 → R4L Until R4L=0 else next									4	–	–	–	–	–	–	[4]

Table A-1. Instruction Set (cont.)

Mnemonic	Operand size	Operation	Addressing mode/ instruction length								Condition code						No. of states
			#xx:8/16	Rn	@Rn	@(d:16,Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8,PC)	@@aa	I	H	N	Z	V	C	
ADD.B #xx:8,Rd	B	Rd8+#xx:8 → Rd8	2								–	↕	↕	↕	↕	↕	2
ADD.B Rs,Rd	B	Rs8+Rd8 → Rd8		2							–	↕	↕	↕	↕	↕	2
ADD.W Rs,Rd	W	Rs16+Rd16 → Rd16		2							–	[1]	↕	↕	↕	↕	2
ADDX.B #xx:8,Rd	B	Rd8+#xx:8 +C → Rd8	2								–	↕	↕	[2]	↕	↕	2
ADDX.B Rs,Rd	B	Rd8+Rs8 +C → Rd8		2							–	↕	↕	[2]	↕	↕	2
ADDS.W #1,Rd	W	Rd16+1 → Rd16		2							–	–	–	–	–	–	2
ADDS.W #2,Rd	W	Rd16+2 → Rd16		2							–	–	–	–	–	–	2
INC.B Rd	B	Rd8+1 → Rd8		2							–	–	↕	↕	↕	–	2
DAA.B Rd	B	Rd8 decimal adjust → Rd8		2							–	*	↕	↕	*	[3]	2
SUB.B Rs,Rd	B	Rd8–Rs8 → Rd8		2							–	↕	↕	↕	↕	↕	2
SUB.W Rs,Rd	W	Rd16–Rs16 → Rd16		2							–	[1]	↕	↕	↕	↕	2
SUBX.B #xx:8,Rd	B	Rd8–#xx:8 –C → Rd8	2								–	↕	↕	[2]	↕	↕	2
SUBX.B Rs,Rd	B	Rd8–Rs8 –C → Rd8		2							–	↕	↕	[2]	↕	↕	2
SUBS.W #1,Rd	W	Rd16–1 → Rd16		2							–	–	–	–	–	–	2
SUBS.W #2,Rd	W	Rd16–2 → Rd16		2							–	–	–	–	–	–	2
DEC.B Rd	B	Rd8–1 → Rd8		2							–	–	↕	↕	↕	–	2
DAS.B Rd	B	Rd8 decimal adjust → Rd8		2							–	*	↕	↕	*	–	2
NEG.B Rd	B	0–Rd → Rd		2							–	↕	↕	↕	↕	↕	2
CMP.B #xx:8,Rd	B	Rd8–#xx:8	2								–	↕	↕	↕	↕	↕	2
CMP.B Rs,Rd	B	Rd8–Rs8		2							–	↕	↕	↕	↕	↕	2
CMP.W Rs,Rd	W	Rd16–Rs16		2							–	[1]	↕	↕	↕	↕	2
MULXU.B Rs,Rd	B	Rd8×Rs8 → Rd16		2							–	–	–	–	–	–	14
DIVXU.B Rs,Rd	B	Rd16÷Rs8 → Rd16 (RdH:remainder,RdL:quotient)		2							–	–	[6]	[7]	–	–	14
AND.B #xx:8,Rd	B	Rd8∧#xx:8 → Rd8	2								–	–	↕	↕	0	–	2
AND.B Rs,Rd	B	Rd8∧Rs8 → Rd8		2							–	–	↕	↕	0	–	2
OR.B #xx:8,Rd	B	Rd8∨#xx:8 → Rd8	2								–	–	↕	↕	0	–	2
OR.B Rs,Rd	B	Rd8∨Rs8 → Rd8		2							–	–	↕	↕	0	–	2
XOR.B #xx:8,Rd	B	Rd8⊕#xx:8 → Rd8	2								–	–	↕	↕	0	–	2
XOR.B Rs,Rd	B	Rd8⊕Rs8 → Rd8		2							–	–	↕	↕	0	–	2
NOT.B Rd	B	$\overline{\text{Rd}}$ → Rd		2							–	–	↕	↕	0	–	2

Table A-1. Instruction Set (cont.)

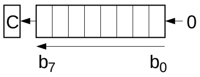
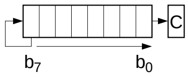
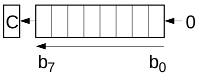
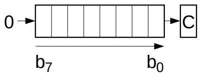
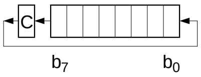
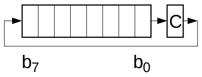
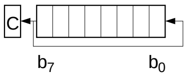
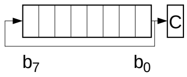
Mnemonic	Operand size	Operation	Addressing mode/ instruction length								Condition code						No. of states
			#xx:8/16	Rn	@Rn	@(d:16,Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8,PC)	@@aa	I	H	N	Z	V	C	
SHAL.B Rd	B			2							–	–	↕	↕	↕	↕	2
SHAR.B Rd	B			2							–	–	↕	↕	0	↕	2
SHLL.B Rd	B			2							–	–	↕	↕	0	↕	2
SHLR.B Rd	B			2							–	–	0	↕	0	↕	2
ROTXL.B Rd	B			2							–	–	↕	↕	0	↕	2
ROTXR.B Rd	B			2							–	–	↕	↕	0	↕	2
ROTL.B Rd	B			2							–	–	↕	↕	0	↕	2
ROTR.B Rd	B			2							–	–	↕	↕	0	↕	2
BSET #xx:3,Rd	B	(#xx:3 of Rd8) ← 1		2							–	–	–	–	–	–	2
BSET #xx:3,@Rd	B	(#xx:3 of @Rd16) ← 1			4						–	–	–	–	–	–	8
BSET #xx:3,@aa:8	B	(#xx:3 of @aa:8) ← 1						4			–	–	–	–	–	–	8
BSET Rn,Rd	B	(Rn8 of Rd8) ← 1		2							–	–	–	–	–	–	2
BSET Rn,@Rd	B	(Rn8 of @Rd16) ← 1			4						–	–	–	–	–	–	8
BSET Rn,@aa:8	B	(Rn8 of @aa:8) ← 1						4			–	–	–	–	–	–	8
BCLR #xx:3,Rd	B	(#xx:3 of Rd8) ← 0		2							–	–	–	–	–	–	2
BCLR #xx:3,@Rd	B	(#xx:3 of @Rd16) ← 0			4						–	–	–	–	–	–	8
BCLR #xx:3,@aa:8	B	(#xx:3 of @aa:8) ← 0						4			–	–	–	–	–	–	8
BCLR Rn,Rd	B	(Rn8 of Rd8) ← 0		2							–	–	–	–	–	–	2
BCLR Rn,@Rd	B	(Rn8 of @Rd16) ← 0			4						–	–	–	–	–	–	8
BCLR Rn,@aa:8	B	(Rn8 of @aa:8) ← 0						4			–	–	–	–	–	–	8
BNOT #xx:3,Rd	B	(#xx:3 of Rd8) ← ($\overline{\text{\#xx:3}}$ $\overline{\text{of}}$ $\overline{\text{Rd8}}$)		2							–	–	–	–	–	–	2
BNOT #xx:3,@Rd	B	(#xx:3 of @Rd16) ← ($\overline{\text{\#xx:3}}$ $\overline{\text{of}}$ $\overline{\text{@Rd16}}$)			4						–	–	–	–	–	–	8
BNOT #xx:3,@aa:8	B	(#xx:3 of @aa:8) ← ($\overline{\text{\#xx:3}}$ $\overline{\text{of}}$ $\overline{\text{@aa:8}}$)						4			–	–	–	–	–	–	8

Table A-1. Instruction Set (cont.)

Mnemonic	Operand size	Operation	Addressing mode/ instruction length								Condition code						No. of states
			#xx:8/16	Rn	@Rn	@(d:16,Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8,PC)	@@aa	I	H	N	Z	V	C	
BNOT Rn,Rd	B	$(\text{Rn8 of Rd8}) \leftarrow (\overline{\text{Rn8 of Rd8}})$		2							–	–	–	–	–	–	2
BNOT Rn,@Rd	B	$(\text{Rn8 of @Rd16}) \leftarrow (\overline{\text{Rn8 of @Rd16}})$			4						–	–	–	–	–	–	8
BNOT Rn,@aa:8	B	$(\text{Rn8 of @aa:8}) \leftarrow (\overline{\text{Rn8 of @aa:8}})$						4			–	–	–	–	–	–	8
BTST #xx:3,Rd	B	$(\overline{\text{\#xx:3 of Rd8}}) \rightarrow Z$		2							–	–	–	↕	–	–	2
BTST #xx:3,@Rd	B	$(\overline{\text{\#xx:3 of @Rd16}}) \rightarrow Z$			4						–	–	–	↕	–	–	6
BTST #xx:3,@aa:8	B	$(\overline{\text{\#xx:3 of @aa:8}}) \rightarrow Z$						4			–	–	–	↕	–	–	6
BTST Rn,Rd	B	$(\overline{\text{Rn8 of Rd8}}) \rightarrow Z$		2							–	–	–	↕	–	–	2
BTST Rn,@Rd	B	$(\overline{\text{Rn8 of @Rd16}}) \rightarrow Z$			4						–	–	–	↕	–	–	6
BTST Rn,@aa:8	B	$(\overline{\text{Rn8 of @aa:8}}) \rightarrow Z$						4			–	–	–	↕	–	–	6
BLD #xx:3,Rd	B	(#xx:3 of Rd8) → C		2							–	–	–	–	–	↕	2
BLD #xx:3,@Rd	B	(#xx:3 of @Rd16) → C			4						–	–	–	–	–	↕	6
BLD #xx:3,@aa:8	B	(#xx:3 of @aa:8) → C						4			–	–	–	–	–	↕	6
BILD #xx:3,Rd	B	$(\overline{\text{\#xx:3 of Rd8}}) \rightarrow C$		2							–	–	–	–	–	↕	2
BILD #xx:3,@Rd	B	$(\overline{\text{\#xx:3 of @Rd16}}) \rightarrow C$			4						–	–	–	–	–	↕	6
BILD #xx:3,@aa:8	B	$(\overline{\text{\#xx:3 of @aa:8}}) \rightarrow C$						4			–	–	–	–	–	↕	6
BST #xx:3,Rd	B	C → (#xx:3 of Rd8)		2							–	–	–	–	–	–	2
BST #xx:3,@Rd	B	C → (#xx:3 of @Rd16)			4						–	–	–	–	–	–	8
BST #xx:3,@aa:8	B	C → (#xx:3 of @aa:8)						4			–	–	–	–	–	–	8
BIST #xx:3,Rd	B	$\overline{C} \rightarrow (\text{\#xx:3 of Rd8})$		2							–	–	–	–	–	–	2
BIST #xx:3,@Rd	B	$\overline{C} \rightarrow (\text{\#xx:3 of @Rd16})$			4						–	–	–	–	–	–	8
BIST #xx:3,@aa:8	B	$\overline{C} \rightarrow (\text{\#xx:3 of @aa:8})$						4			–	–	–	–	–	–	8
BAND #xx:3,Rd	B	C∧(#xx:3 of Rd8) → C		2							–	–	–	–	–	↕	2
BAND #xx:3,@Rd	B	C∧(#xx:3 of @Rd16) → C			4						–	–	–	–	–	↕	6
BAND #xx:3,@aa:8	B	C∧(#xx:3 of @aa:8) → C						4			–	–	–	–	–	↕	6
BIAND #xx:3,Rd	B	$C\wedge(\overline{\text{\#xx:3 of Rd8}}) \rightarrow C$		2							–	–	–	–	–	↕	2
BIAND #xx:3,@Rd	B	$C\wedge(\overline{\text{\#xx:3 of @Rd16}}) \rightarrow C$			4						–	–	–	–	–	↕	6
BIAND #xx:3, @aa:8	B	$C\wedge(\overline{\text{\#xx:3 of @aa:8}}) \rightarrow C$						4			–	–	–	–	–	↕	6
BOR #xx:3,Rd	B	C∨(#xx:3 of Rd8) → C		2							–	–	–	–	–	↕	2
BOR #xx:3,@Rd	B	C∨(#xx:3 of @Rd16) → C			4						–	–	–	–	–	↕	6
BOR #xx:3,@aa:8	B	C∨(#xx:3 of @aa:8) → C						4			–	–	–	–	–	↕	6
BIOR #xx:3,Rd	B	$C\vee(\overline{\text{\#xx:3 of Rd8}}) \rightarrow C$		2							–	–	–	–	–	↕	2

Table A-1. Instruction Set (cont.)

Mnemonic	Operand size	Operation		Addressing mode/ instruction length								Condition code						No. of states
			Branching condition	#xx:8/16	Rn	@Rn	@(d:16,Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8,PC)	@@aa	I	H	N	Z	V	C	
BIOR #xx:3,@Rd	B	C∨($\overline{\text{\#xx:3}}$ $\overline{\text{of}}$ $\overline{\text{@Rd16}}$) → C				4						–	–	–	–	–	↕	6
BIOR #xx:3, @aa:8	B	C∨($\overline{\text{\#xx:3}}$ $\overline{\text{of}}$ $\overline{\text{@aa:8}}$) → C							4			–	–	–	–	–	↕	6
BXOR #xx:3,Rd	B	C⊕(#xx:3 of Rd8) → C			2							–	–	–	–	–	↕	2
BXOR #xx:3,@Rd	B	C⊕(#xx:3 of @Rd16) → C				4						–	–	–	–	–	↕	6
BXOR #xx:3, @aa:8	B	C⊕(#xx:3 of @aa:8) → C							4			–	–	–	–	–	↕	6
BIXOR #xx:3,Rd	B	C⊕($\overline{\text{\#xx:3}}$ $\overline{\text{of}}$ $\overline{\text{Rd8}}$) → C			2							–	–	–	–	–	↕	2
BIXOR #xx:3,@Rd	B	C⊕($\overline{\text{\#xx:3}}$ $\overline{\text{of}}$ $\overline{\text{@Rd16}}$) → C				4						–	–	–	–	–	↕	6
BIXOR #xx:3, @aa:8	B	C⊕($\overline{\text{\#xx:3}}$ $\overline{\text{of}}$ $\overline{\text{@aa:8}}$) → C							4			–	–	–	–	–	↕	6
BRA d:8 (BT d:8)	–	PC ← PC+d:8								2		–	–	–	–	–	–	4
BRNd:8 (BF d:8)	–	PC ← PC+2								2		–	–	–	–	–	–	4
BHI d:8	–	if condition is true then PC ← PC+d:8 else next;	C∨Z = 0							2		–	–	–	–	–	–	4
BLS d:8	–		C∨Z = 1							2		–	–	–	–	–	–	4
BCC d:8 (BHS d:8)	–		C = 0							2		–	–	–	–	–	–	4
BCS d:8 (BLO d:8)	–		C = 1							2		–	–	–	–	–	–	4
BNE d:8	–		Z = 0							2		–	–	–	–	–	–	4
BEQ d:8	–		Z = 1							2		–	–	–	–	–	–	4
BVC d:8	–		V = 0							2		–	–	–	–	–	–	4
BVS d:8	–		V = 1							2		–	–	–	–	–	–	4
BPL d:8	–		N = 0							2		–	–	–	–	–	–	4
BMI d:8	–		N = 1							2		–	–	–	–	–	–	4
BGE d:8	–		N⊕V = 0							2		–	–	–	–	–	–	4
BLT d:8	–		N⊕V = 1							2		–	–	–	–	–	–	4
BGT d:8	–		Z∨(N⊕V) = 0							2		–	–	–	–	–	–	4
BLE d:8	–		Z∨(N⊕V) = 1							2		–	–	–	–	–	–	4
JMP @Rn	–	PC ← Rn16				2						–	–	–	–	–	–	4
JMP @aa:16	–	PC ← aa:16							4			–	–	–	–	–	–	6
JMP @@aa:8	–	PC ← @aa:8									2	–	–	–	–	–	–	8
BSR d:8	–	SP–2 → SP PC → @SP PC ← PC+d:8								2		–	–	–	–	–	–	6

Table A-1. Instruction Set (cont.)

Mnemonic	Operand size	Operation	Addressing mode/ instruction length									Condition code						No. of states
			#xx:8/16	Rn	@Rn	@(d:16,Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8,PC)	@@aa	Implied	I	H	N	Z	V	C	
JSR @Rn	–	SP–2 → SP PC → @SP PC ← Rn16			2							–	–	–	–	–	–	6
JSR @aa:16	–	SP–2 → SP PC → @SP PC ← aa:16						4				–	–	–	–	–	–	8
JSR @@aa:8	–	SP–2 → SP PC → @SP PC ← @aa:8								2		–	–	–	–	–	–	8
RTS	–	PC ← @SP SP+2 → SP									2	–	–	–	–	–	–	8
RTE	–	CCR ← @SP SP+2 → SP PC ← @SP SP+2 → SP									2	↕	↕	↕	↕	↕	↕	10
SLEEP	–	Transit to sleep mode.									2	–	–	–	–	–	–	2
LDC #xx:8,CCR	B	#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
LDC Rs,CCR	B	Rs8 → CCR		2								↕	↕	↕	↕	↕	↕	2
STC CCR,Rd	B	CCR → Rd8		2								–	–	–	–	–	–	2
ANDC #xx:8,CCR	B	CCR∧#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
ORC #xx:8,CCR	B	CCR∨#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
XORC #xx:8,CCR	B	CCR⊕#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
NOP	–	PC ← PC+2									2	–	–	–	–	–	–	2

Notes: The number of states is the number of states required for execution when the instruction and its operands are located in on-chip memory.

[1] Set to “1” when there is a carry or borrow from bit 11; otherwise cleared to “0”.

[2] If the result is zero, the previous value of the flag is retained; otherwise the flag is cleared to “0”.

[3] Set to “1” if decimal adjustment produces a carry; otherwise cleared to “0”.

[4] The number of states required for execution is 4n+8 (n = value of R4L)

[5] These instructions are not supported by the H8/338 Series.

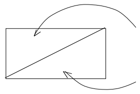
[6] Set to “1” if the divisor is negative; otherwise cleared to ”0”.

[7] Cleared to “0:”if the divisor is not zero; “1” when the divisor is zero.

A.2 Operation Code Map

Table A-2 is a map of the operation codes contained in the first byte of the instruction code (bits 15 to 8 of the first instruction word).

Some pairs of instructions have identical first bytes. These instructions are differentiated by the first bit of the second byte (bit 7 of the first instruction word).



Instruction when first bit of byte 2 (bit 7 of first instruction word) is "0."
Instruction when first bit of byte 2 (bit 7 of first instruction word) is "1."

Table A-2. Operation Code Map

HI \ LO	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SLEEP	STC	LDC	ORC	XORC	ANDC	LDC	ADD		INC	ADDS	MOV		ADDX	DAA
1	SHLL SHAL	SHLR SHAR	ROTXL ROTL	ROTXR ROTR	OR	XOR	AND	NOT NEG	SUB		DEC	SUBS	CMP		SUBX	DAS
2	MOV															
3																
4	BRA*2	BRN *2	BHI	BLS	BCC *2	BCS *2	BNE	BEQ	BVC	BVS	BPL	BMI	BGE	BLT	BGT	BLE
5	MULXU	DIVXU			RTS	BSR	RTE			JMP				JSR		
6	BSET	BNOT	BCLR	BTST				BST BIST	MOV *1							
7					BOR BIOR	BXOR BIXOR	BAND BIAND	BLD BILD		MOV		EEPMOV	Bit manipulation instruction			
8	ADD															
9	ADDX															
A	CMP															
B	SUBX															
C	OR															
D	XOR															
E	AND															
F	MOV															

*1 The MOVFPE and MOVTPE instructions are identical to MOV instructions in the first byte and first bit of the second byte (bits 15 to 7 of the instruction word). The PUSH and POP instructions are identical in machine language to MOV instructions.

*2 The BT, BF, BHS, and BLO instructions are identical in machine language to BRA, BRN, BCC, and BCS, respectively.

A.3 Number of States Required for Execution

The tables below can be used to calculate the number of states required for instruction execution. Table A-3 indicates the number of states required for each cycle (instruction fetch, branch address read, stack operation, byte data access, word data access, internal operation). Table A-4 indicates the number of cycles of each type occurring in each instruction. The total number of states required for execution of an instruction can be calculated from these two tables as follows:

Execution states = $I \times S_I + J \times S_J + K \times S_K + L \times S_L + M \times S_M + N \times S_N$

Examples: Mode 1 (on-chip ROM disabled), stack located in external memory, 1 wait state inserted in external memory access.

1. BSET #0, @FFC7
   From table A-4: $I = L = 2$, $J = K = M = N= 0$
   From table A-3: $S_I = 8$, $S_L = 3$
   Number of states required for execution: $2 \times 8 + 2 \times 3 =22$

2. JSR @@30
   From table A-4: $I = 2$, $J = K = 1$, $L = M = N = 0$
   From table A-3: $S_I = S_J = S_K = 8$
   Number of states required for execution: $2 \times 8 + 1 \times 8 + 1 \times 8 = 32$

Table A-3. Number of States Taken by Each Cycle in Instruction Execution

Execution Status		**Access Location**		
(instruction cycle)		**On-Chip Memory**	**On-Chip Reg. Field**	**External Memory**
Instruction fetch	S_I	2	6	6 + 2m
Branch address read	S_J			
Stack operation	S_K			
Byte data access	S_L		3	3 + m
Word data access	S_M		6	6 + 2m
Internal operation	S_N		1	

Notes: m: Number of wait states inserted in access to external device.

Table A-4. Number of Cycles in Each Instruction

		Instruction	Branch	Stack	Byte Data	Word Data	Internal
		Fetch	Addr. Read	Operation	Access	Access	Operation
Instruction	Mnemonic	I	J	K	L	M	N
ADD	ADD.B #xx:8, Rd	1					
	ADD.B Rs, Rd	1					
	ADD.W Rs, Rd	1					
ADDS	ADDS.W #1/2, Rd	1					
ADDX	ADDX.B #xx:8, Rd	1					
	ADDX.B Rs, Rd	1					
AND	AND.B #xx:8, Rd	1					
	AND.B Rs, Rd	1					
ANDC	ANDC #xx:8, CCR	1					
BAND	BAND #xx:3, Rd	1					
	BAND #xx:3, @Rd	2			1		
	BAND #xx:3, @aa:8	2			1		
Bcc	BRA d:8 (BT d:8)	2					
	BRN d:8 (BF d:8)	2					
	BHI d:8	2					
	BLS d:8	2					
	BCC d:8 (BHS d:8)	2					
	BCS d:8 (BLO d:8)	2					
	BNE d:8	2					
	BEQ d:8	2					
	BVC d:8	2					
	BVS d:8	2					
	BPL d:8	2					
	BMI d:8	2					
	BGE d:8	2					
	BLT d:8	2					
	BGT d:8	2					
	BLE d:8	2					
BCLR	BCLR #xx:3, Rd	1					
	BCLR #xx:3, @Rd	2			2		
	BCLR #xx:3, @aa:8	2			2		
	BCLR Rn, Rd	1					
	BCLR Rn, @Rd	2			2		
	BCLR Rn, @aa:8	2			2		

Table A-4. Number of Cycles in Each Instruction (cont.)

		Instruction	Branch	Stack	Byte Data	Word Data	Internal
		Fetch	Addr. Read	Operation	Access	Access	Operation
Instruction	Mnemonic	I	J	K	L	M	N
BIAND	BIAND #xx:3, Rd	1					
	BIAND #xx:3, @Rd	2			1		
	BIAND #xx:3, @aa:8	2			1		
BILD	BILD #xx:3, Rd	1					
	BILD #xx:3, @Rd	2			1		
	BILD #xx:3, @aa:8	2			1		
BIOR	BIOR #xx:3 Rd	1					
	BIOR #xx:3 @Rd	2			1		
	BIOR #xx:3 @aa:8	2			1		
BIST	BIST #xx:3, Rd	1					
	BIST #xx:3, @Rd	2			2		
	BIST #xx:3, @aa:8	2			2		
BIXOR	BIXOR #xx:3, Rd	1					
	BIXOR #xx:3, @Rd	2			1		
	BIXOR #xx:3, @aa:8	2			1		
BLD	BLD #xx:3, Rd	1					
	BLD #xx:3, @Rd	2			1		
	BLD #xx:3, @aa:8	2			1		
BNOT	BNOT #xx:3, Rd	1					
	BNOT #xx:3, @Rd	2			2		
	BNOT #xx:3, @aa:8	2			2		
	BNOT Rn, Rd	1					
	BNOT Rn, @Rd	2			2		
	BNOT Rn, @aa:8	2			2		
BOR	BOR #xx:3, Rd	1					
	BOR #xx:3, @Rd	2			1		
	BOR #xx:3, @aa:8	2			1		
BSET	BSET #xx:3, Rd	1					
	BSET #xx:3, @Rd	2			2		
	BSET #xx:3, @aa:8	2			2		
	BSET Rn, Rd	1					
	BSET Rn, @Rd	2			2		
	BSET Rn, @aa:8	2			2		

Table A-4. Number of Cycles in Each Instruction (cont.)

		Instruction	Branch	Stack	Byte Data	Word Data	Internal
		Fetch	Addr. Read	Operation	Access	Access	Operation
Instruction	Mnemonic	I	J	K	L	M	N
BSR	BSR d:8	2		1			
BST	BST #xx:3, Rd	1					
	BST #xx:3, @Rd	2			2		
	BST #xx:3, @aa:8	2			2		
BTST	BTST #xx:3, Rd	1					
	BTST #xx:3, @Rd	2			1		
	BTST #xx:3, @aa:8	2			1		
	BTST Rn, Rd	1					
	BTST Rn, @Rd	2			1		
	BTST Rn, @aa:8	2			1		
BXOR	BXOR #xx:3, Rd	1					
	BXOR #xx:3, @Rd	2			1		
	BXOR #xx:3, @aa:8	2			1		
CMP	CMP.B #xx:8, Rd	1					
	CMP.B Rs, Rd	1					
	CMP.W Rs, Rd	1					
DAA	DAA.B Rd	1					
DAS	DAS.B Rd	1					
DEC	DEC.B Rd	1					
DIVXU	DIVXU.B Rs, Rd	1					12
EEPMOV	EEPMOV	2			2n+2[*1]		1
INC	INC.B Rd	1					
JMP	JMP @Rn	2					
	JMP @aa:16	2					2
	JMP @@aa:8	2	1				2
JSR	JSR @Rn	2		1			
	JSR @aa:16	2		1			2
	JSR @@aa:8	2	1	1			
LDC	LDC #xx:8, CCR	1					
	LDC Rs, CCR	1					
MOV	MOV.B #xx:8, Rd	1					
	MOV.B Rs, Rd	1					
	MOV.B @Rs, Rd	1			1		
	MOV.B @(d:16,Rs), Rd	2			1		

Table A-4. Number of Cycles in Each Instruction (cont.)

		Instruction	Branch	Stack	Byte Data	Word Data	Internal
		Fetch	Addr. Read	Operation	Access	Access	Operation
Instruction	Mnemonic	I	J	K	L	M	N
MOV	MOV.B @Rs+, Rd	1			1		2
	MOV.B @aa:8, Rd	1			1		
	MOV.B @aa:16, Rd	2			1		
	MOV.B Rs, @Rd	1			1		
	MOV.B Rs, @(d:16, Rd)	2			1		
	MOV.B Rs, @–Rd	1			1		2
	MOV.B Rs, @aa:8	1			1		
	MOV.B Rs, @aa:16	2			1		
	MOV.W #xx:16, Rd	2					
	MOV.W Rs, Rd	1					
	MOV.W @Rs, Rd	1				1	
	MOV.W @(d:16, Rs), Rd	2				1	
	MOV.W @Rs+, Rd	1				1	2
	MOV.W @aa:16, Rd	2				1	
	MOV.W Rs, @Rd	1				1	
	MOV.W Rs, @(d:16, Rd)	2				1	
	MOV.W Rs, @–Rd	1				1	2
	MOV.W Rs, @aa:16	2				1	
MOVFPE	MOVFPE @aa:16, Rd	Not supported					
MOVTPE	MOVTPE.Rs, @aa:16	Not supported					
MULXU	MULXU.Rs, Rd	1					12
NEG	NEG.B Rd	1					
NOP	NOP	1					
NOT	NOT.B Rd	1					
OR	OR.B #xx:8, Rd	1					
	OR.B Rs, Rd	1					
ORC	ORC #xx:8, CCR	1					
POP	POP Rd	1			1		2
PUSH	PUSH Rd	1			1		2
ROTL	ROTL.B Rd	1					
ROTR	ROTR.B Rd	1					
ROTXL	ROTXL.B Rd	1					
ROTXR	ROTXR.B Rd	1					

Table A-4. Number of Cycles in Each Instruction (cont.)

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
RTE	RTE	2		2			2
RTS	RTS	2		1			2
SHAL	SHAL.B Rd	1					
SHAR	SHAR.B Rd	1					
SHLL	SHLL.B Rd	1					
SHLR	SHLR.B Rd	1					
SLEEP	SLEEP	1					
STC	STC CCR, Rd	1					
SUB	SUB.B Rs, Rd	1					
	SUB.W Rs, Rd	1					
SUBS	SUBS.W #1/2, Rd	1					
SUBX	SUBX.B #xx:8, Rd	1					
	SUBX.B Rs, Rd	1					
XOR	XOR.B #xx:8, Rd	1					
	XOR.B Rs, Rd	1					
XORC	XORC #xx:8, CCR	1					

Notes: All blanks are "0."

*1 n: Initial value in R4L. Source and destination are accessed n + 1 times each.

*2 Data access requires 9 to 16 states.

Appendix B. Register Fields

B.1 Register Addresses and Bit Names

Addr.										
(last	Register				Bit names					
byte)	name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
H'80										External addresses (in expanded modes)
H'81										
H'82										
H'83										
H'84										
H'85										
H'86										
H'87										
H'88										—
H'89										
H'8A										
H'8B										
H'8C										
H'8D										
H'8E										
H'8F										
H’90	TIER	ICIAE	ICIBE	ICICE	ICIDE	OCIAE	OCIBE	OVIE	—	FRT
H’91	TCSR	ICFA	ICFB	ICFC	ICFD	OCFA	OCFB	OVF	CCLRA	
H’92	FRC (H)									
H’93	FRC (L)									
H’94	OCRA (H)									
	OCRB (H)									
H’95	OCRA (L)									
	OCRB (L)									
H’96	TCR	IEDGA	IEDGB	IEDGC	IEDGD	BUFEA	BUFEB	CKS1	CKS0	
H’97	TOCR	—	—	—	OCRS	OEA	OEB	OLVLA	OLVLB	
H’98	ICRA (H)									
H’99	ICRA (L)									
H’9A	ICRB (H)									
H’9B	ICRB (L)									
H’9C	ICRC (H)									
H’9D	ICRC (L)									
H’9E	ICRD (H)									
H’9F	ICRD (L)									

Notes: FRT: Free-Running Timer

(Continued on next page)

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Addr. (last byte)	**Register name**	**Bit names**								**Module**
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	
H'A0	TCR	OE	OS	—	—	—	CKS2	CKS1	CKS0	PWM0
H'A1	DTR									
H'A2	TCNT									
H'A3	—	—	—	—	—	—	—	—	—	
H'A4	TCR	OE	OS	—	—	—	CKS2	CKS1	CKS0	PWM1
H'A5	DTR									
H'A6	TCNT									
H'A7	—	—	—	—	—	—	—	—	—	
H'A8	TCSR									WDT
H'A9	TCNT/TCSR[Note 1]									
H'AA										
H'AB										
H'AC	P1PCR	P1$_7$PCR	P1$_6$PCR	P1$_5$PCR	P1$_4$PCR	P1$_3$PCR	P1$_2$PCR	P1$_1$PCR	P1$_0$PCR	Port 1
H'AD	P2PCR	P2$_7$PCR	P2$_6$PCR	P2$_5$PCR	P2$_4$PCR	P2$_3$PCR	P2$_2$PCR	P2$_1$PCR	P2$_0$PCR	Port 2
H'AE	P3PCR	P3$_7$PCR	P3$_6$PCR	P3$_5$PCR	P3$_4$PCR	P3$_3$PCR	P3$_2$PCR	P3$_1$PCR	P3$_0$PCR	Port 3
H'AF										
H'B0	P1DDR	P1$_7$DDR	P1$_6$DDR	P1$_5$DDR	P1$_4$DDR	P1$_3$DDR	P1$_2$DDR	P1$_1$DDR	P1$_0$DDR	Port 1
H'B1	P2DDR	P2$_7$DDR	P2$_6$DDR	P2$_5$DDR	P2$_4$DDR	P2$_3$DDR	P2$_2$DDR	P2$_1$DDR	P2$_0$DDR	Port 2
H'B2	P1DR	P1$_7$	P1$_6$	P1$_5$	P1$_4$	P1$_3$	P1$_2$	P1$_1$	P1$_0$	Port 1
H'B3	P2DR	P2$_7$	P2$_6$	P2$_5$	P2$_4$	P2$_3$	P2$_2$	P2$_1$	P2$_0$	Port 2
H'B4	P3DDR	P3$_7$DDR	P3$_6$DDR	P3$_5$DDR	P3$_4$DDR	P3$_3$DDR	P3$_2$DDR	P3$_1$DDR	P3$_0$DDR	Port 3
H'B5	P4DDR	P4$_7$DDR	P4$_6$DDR	P4$_5$DDR	P4$_4$DDR	P4$_3$DDR	P4$_2$DDR	P4$_1$DDR	P4$_0$DDR	Port 4
H'B6	P3DR	P3$_7$	P3$_6$	P3$_5$	P3$_4$	P3$_3$	P3$_2$	P3$_1$	P3$_0$	Port 3
H'B7	P4DR	P4$_7$	P4$_6$	P4$_5$	P4$_4$	P4$_3$	P4$_2$	P4$_1$	P4$_0$	Port 4
H'B8	P5DDR	—	—	—	—	—	P5$_2$DDR	P5$_1$DDR	P5$_0$DDR	Port 5
H'B9	P6DDR	P6$_7$DDR	P6$_6$DDR	P6$_5$DDR	P6$_4$DDR	P6$_3$DDR	P6$_2$DDR	P6$_1$DDR	P6$_0$DDR	Port 6
H'BA	P5DR	—	—	—	—	—	P5$_2$	P5$_1$	P5$_0$	Port 5
H'BB	P6DR	P6$_7$	P6$_6$	P6$_5$	P6$_4$	P6$_3$	P6$_2$	P6$_1$	P6$_0$	Port 6
H'BC	—	—	—	—	—	—	—	—	—	—
H'BD	P8DDR	—	P8$_6$DDR	P8$_5$DDR	P8$_4$DDR	P8$_3$DDR	P8$_2$DDR	P8$_1$DDR	P8$_0$DDR	Port 8
H'BE	P7DR	P7$_7$	P7$_6$	P7$_5$	P7$_4$	P7$_3$	P7$_2$	P7$_1$	P7$_0$	Port 7
H'BF	P8DR	—	P8$_6$	P8$_5$	P8$_4$	P8$_3$	P8$_2$	P8$_1$	P8$_0$	Port 8

(Continued on next page)

Notes: PWM0: Pulse-Width Modulation timer channel 0

PWM1: Pulse-Width Modulation timer channel 1

WDT: Watchdog Timer

1. See section 11, Watchdog Timer, for register bit description.

(Continued from preceding page)

Addr. (last byte)	Register name				Bit names					Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H’C0	P9DDR	P97DDR	P96DDR	P95DDR	P94DDR	P93DDR	P92DDR	P91DDR	P90DDR	Port 9
H’C1	P9DR	P97	P96	P95	P94	P93	P92	P91	P90	
H’C2	—	—	—	—	—	—	—	—	—	
H’C3	STCR	—	—	—	—	—	MPE	ICKS1	ICKS0	—
H’C4	SYSCR	SSBY	STS2	STS1	STS0	XRST	NMIEG	HIE	RAME	System control
H’C5	MDCR	—	—	—	—	—	—	MDS1	MDS0	
H’C6	ISCR	IRQ7SC	IRQ6SC	IRQ5SC	IRQ4SC	IRQ3SC	IRQ2SC	IRQ1SC	IRQ0SC	
H’C7	IER	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E	
H’C8	TCR	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR0
H’C9	TCSR	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0	
H’CA	TCORA									
H’CB	TCORB									
H’CC	TCNT									
H’CD	—	—	—	—	—	—	—	—	—	
H’CE	—	—	—	—	—	—	—	—	—	
H’CF	—	—	—	—	—	—	—	—	—	
H’D0	TCR	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR1
H’D1	TCSR	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0	
H’D2	TCORA									
H’D3	TCORB									
H’D4	TCNT									
H’D5	—	—	—	—	—	—	—	—	—	
H’D6	—	—	—	—	—	—	—	—	—	
H’D7	—	—	—	—	—	—	—	—	—	
H’D8	SMR	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI
H’D9	BRR									
H’DA	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H’DB	TDR									
H’DC	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
H’DD	RDR									
H’DE	—	—	—	—	—	—	—	—	—	
H’DF	—	—	—	—	—	—	—	—	—	

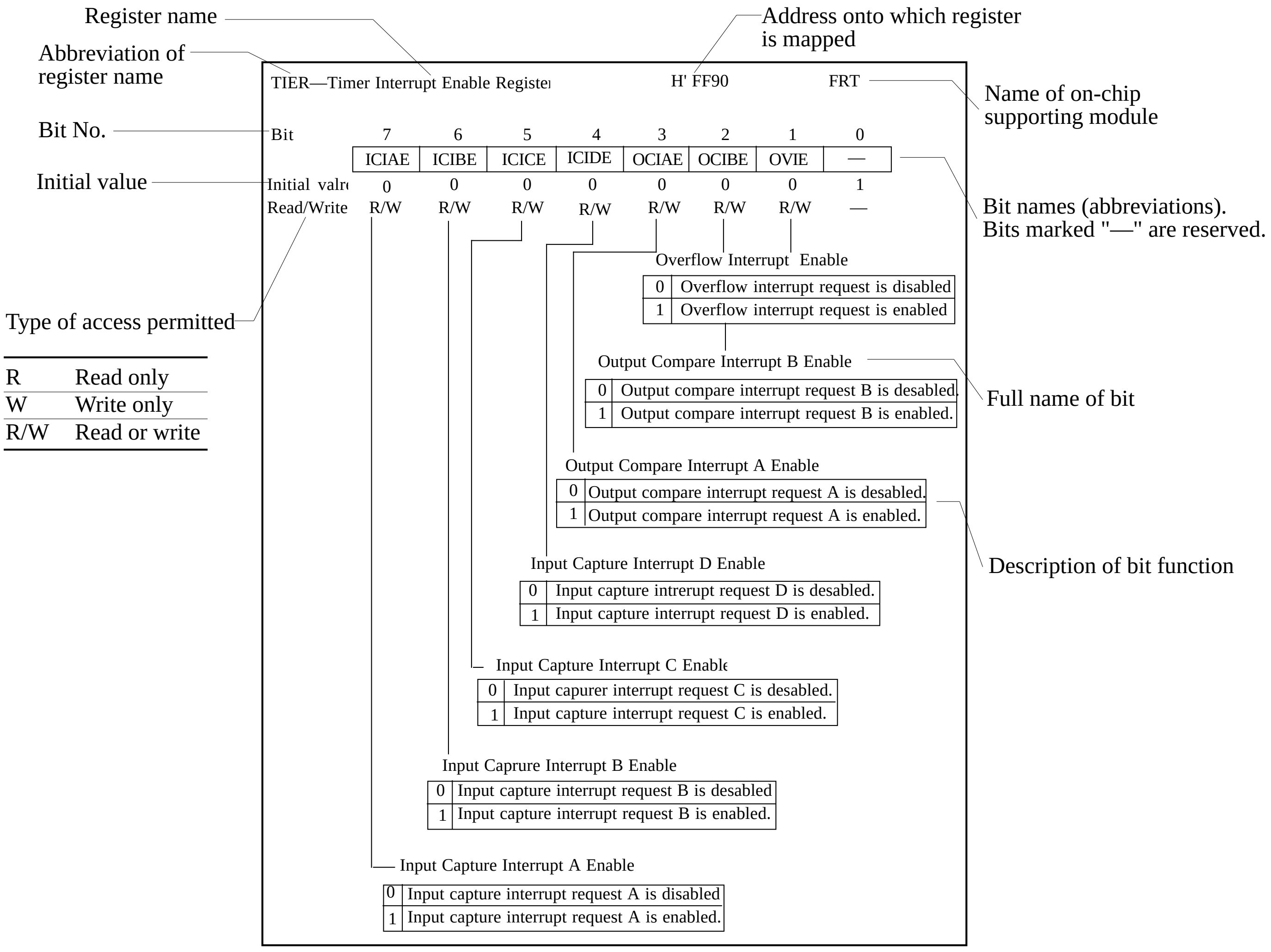
(Continued on next page)

Notes: TMR0: 8-Bit Timer channel 0
TMR1: 8-Bit Timer channel 1
SCI: Serial Communication Interface

(Continued from preceding page)

Addr. (last byte)	Register name	Bit names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H’E0	ADDRA									A/D
H’E1	—	—	—	—	—	—	—	—	—	
H’E2	ADDRB									
H’E3	—	—	—	—	—	—	—	—	—	
H’E4	ADDRC									
H’E5	—	—	—	—	—	—	—	—	—	
H’E6	ADDRD									
H’E7	—	—	—	—	—	—	—	—	—	
H’E8	ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0	
H’E9	—	—	—	—	—	—	—	—	—	
H’EA	ADCR	TRGE	—	—	—	—	—	—	CHS	
H’EB	—	—	—	—	—	—	—	—	—	
H’EC	—	—	—	—	—	—	—	—	—	
H’ED	—	—	—	—	—	—	—	—	—	
H’EE	—	—	—	—	—	—	—	—	—	
H’EF	—	—	—	—	—	—	—	—	—	
H’F0	HICR	—	—	—	—	—	IBFIE2	IBFIE1	FGA20E	HIF
H’F1	KMIMR									
H’F2	—	—	—	—	—	—	—	—	—	
H’F3	—	—	—	—	—	—	—	—	—	
H’F4	IDR1									
H’F5	ODR1									
H’F6	STR1					$C/\overline{D}$		IBF	OBF	
H’F7	—	—	—	—	—	—	—	—	—	
H’F8	—	—	—	—	—	—	—	—	—	
H’F9	—	—	—	—	—	—	—	—	—	
H’FA	—	—	—	—	—	—	—	—	—	
H’FB	—	—	—	—	—	—	—	—	—	
H’FC	IDR2									
H’FD	ODR2									
H’FE	STR2					$C/\overline{D}$		IBF	OBF	
H’FF	—	—	—	—	—	—	—	—	—	

Note: A/D: Analog-to-Digital converter
HIF: Host Interface


Register name
Abbreviation of register name
Address onto which register is mapped
Name of on-chip supporting module
Bit No.
Initial value
Bit names (abbreviations). Bits marked "—" are reserved.
Type of access permitted
Full name of bit
Description of bit function

TIER—Timer Interrupt Enable Registe H' FF90 FRT

Bit	7	6	5	4	3	2	1	0
	ICIAE	ICIBE	ICICE	ICIDE	OCIAE	OCIBE	OVIE	—
Initial valr	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Overflow Interrupt Enable

0	Overflow interrupt request is disabled
1	Overflow interrupt request is enabled

Output Compare Interrupt B Enable

0	Output compare interrupt request B is desabled.
1	Output compare interrupt request B is enabled.

Output Compare Interrupt A Enable

0	Output compare interrupt request A is desabled.
1	Output compare interrupt request A is enabled.

Input Capture Interrupt D Enable

0	Input capture intrerupt request D is desabled.
1	Input capture interrupt request D is enabled.

Input Capture Interrupt C Enabl

0	Input capurer interrupt request C is desabled.
1	Input capture interrupt request C is enabled.

Input Caprure Interrupt B Enable

0	Input capture interrupt request B is desabled
1	Input capture interrupt request B is enabled.

Input Capture Interrupt A Enable

0	Input capture interrupt request A is disabled
1	Input capture interrupt request A is enabled.

R	Read only
W	Write only
R/W	Read or write

TIER—Timer Interrupt Enable Register H’FF90 FRT

Bit	7	6	5	4	3	2	1	0
	ICIAE	ICIBE	ICICE	ICIDE	OCIAE	OCIBE	OVIE	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Overflow Interrupt Enable

0	Overflow interrupt request is disabled.
1	Overflow interrupt request is enabled.

Output Compare Interrupt B Enable

0	Output compare interrupt request B is disabled.
1	Output compare interrupt request B is enabled.

Output Compare Interrupt A Enable

0	Output compare interrupt request A is disabled.
1	Output compare interrupt request A is enabled.

Input Capture Interrupt D Enable

0	Input capture interrupt request D is disabled.
1	Input capture interrupt request D is enabled.

Input Capture Interrupt C Enable

0	Input capture interrupt request C is disabled.
1	Input capture interrupt request C is enabled.

Input Capture Interrupt B Enable

0	Input capture interrupt request B is disabled.
1	Input capture interrupt request B is enabled.

Input Capture Interrupt A Enable

0	Input capture interrupt request A is disabled.
1	Input capture interrupt request A is enabled.

TCSR—Timer Control/Status Register H’FF91 FRT

Bit	7	6	5	4	3	2	1	0
	ICFA	ICFB	ICFC	ICFD	OCFA	OCFB	OVF	CCLRA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/W

Counter Clear A

0	FRC count is not cleared.
1	FRC count is cleared by compare-match A.

Timer Overflow Flag

0	Cleared when CPU reads OVF = “1,” then writes “0” in OVF.
1	Set when FRC changes from H’FFFF to H’0000.

Output Compare Flag B

0	Cleared when CPU reads OCFB = “1”, then writes “0” in OCFB.
1	Set when FRC = OCRB.

Output Compare Flag A

0	Cleared when CPU reads OCFA = “1”, then writes “0” in OCFA.
1	Set when FRC = OCRA.

Input Capture Flag D

0	Cleared when CPU reads ICFD = “1”, then writes “0” in ICFD.
1	Set by FTID input.

Input Capture Flag C

0	Cleared when CPU reads ICFC = “1”, then writes “0” in ICFC.
1	Set by FTIC input.

Input Capture Flag B

0	Cleared when CPU reads ICFB = “1”, then writes “0” in ICFB.
1	Set when FTIB input causes FRC to be copied to ICRB.

Input Capture Flag A

0	Cleared when CPU reads ICFA = “1”, then writes “0” in ICFA.
1	Set when FTIA input causes FRC to be copied to ICRA.

* Software can write a "0" in bits 7 to 1 to clear the flags, but cannot write a "1" in these bits

FRC (H and L)—Free-Running Counter H’FF92, H’FF93 FRT

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Count value

OCRA (H and L)—Output Compare Register A H’FF94, H’FF95 FRT

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Continually compared with FRC. OCFA is set to “1” when OCRA = FRC.

OCRB (H and L)—Output Compare Register B H’FF94, H’FF95 FRT

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Continually compared with FRC. OCFB is set to “1” when OCRB = FRC.

TCR—Timer Control Register H'FF96 FRT

Bit	7	6	5	4	3	2	1	0
	IEDGA	IEDGB	IEDGC	IEDGD	BUFEA	BUFEB	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	Internal clock source: ϕ/2
0	1	Internal clock source: ϕ/8
1	0	Internal clock source: ϕ/32
1	1	External clock source: counted on rising edge

Buffer Enable B

0	ICRD is used for input capture D.
1	ICRD is buffer register for input capture B.

Buffer Enable A

0	ICRC is used for input capture C.
1	ICRC is buffer register for input capture A.

Input Edge Select D

0	Falling edge of FTID is valid.
1	Rising edge of FTID is valid.

Input Edge Select C

0	Falling edge of FTIC is valid.
1	Rising edge of FTIC is valid.

Input Edge Select B

0	Falling edge of FTIB is valid.
1	Rising edge of FTIB is valid.

Input Edge Select A

0	Falling edge of FTIA is valid.
1	Rising edge of FTIA is valid.

TOCR—Timer Output Control Register H’FF97 FRT

Bit	7	6	5	4	3	2	1	0
	—	—	—	OCRS	OEA	OEB	OLVLA	OLVLB
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Output Level B

0	Compare-match B causes “0” output.
1	Compare-match B causes “1” output.

Output Level A

0	Compare-match A causes “0” output.
1	Compare-match A causes “1” output.

Output Enable B

0	Output compare B output is disabled.
1	Output compare B output is enabled.

Output Enable A

0	Output compare A output is disabled.
1	Output compare A output is enabled.

Output Compare Register Select

0	The CPU can access OCRA at addresses H’FF94 – H’FF95.
1	The CPU can access OCRB at addresses H’FF94 – H’FF95.

ICRA (H and L)—Input Capture Register H’FF98, H’FF99 FRT

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Contains FRC count captured on FTIA input.

ICRB (H and L)—Input Capture Register H’FF9A, H’FF9B FRT

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Contains FRC count captured on FTIB input.

ICRC (H and L)—Input Capture Register H’FF9C, H’FF9D FRT

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Contains FRC count captured on FTIC input, or old ICRA value in buffer mode.

ICRD (H and L)—Input Capture Register H’FF9E, H’FF9F FRT

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Contains FRC count captured on FTID input, or old ICRB value in buffer mode.

TCR—Timer Control Register H’FFA0 PWM0

Bit	7	6	5	4	3	2	1	0
	OE	OS	—	—	—	CKS2	CKS1	CKS0
Initial value	0	0	1	1	1	0	0	0
Read/Write	R/W	R/W	—	—	—	R/W	R/W	R/W

Clock Select (Values When ϕ = 10MHz)

			Internal clock Freq.	Resolution	PWM period	PWM frequency
0	0	0	ϕ/2	200ns	50µs	20kHz
0	0	1	ϕ/8	800ns	200µs	5kHz
0	1	0	ϕ/32	3.2µs	800µs	1.25kHz
0	1	1	ϕ/128	12.8µs	3.2ms	312.5Hz
1	0	0	ϕ/256	25.6µs	6.4ms	156.3Hz
1	0	1	ϕ/1024	102.4µs	25.6ms	39.1Hz
1	1	0	ϕ/2048	204.8µs	51.2ms	19.5Hz
1	1	1	ϕ/4096	409.6µs	102.4ms	9.8Hz

Output Select

0	Positive logic
1	Negative logic

Output Enable

0	PWM output disabled; TCNT cleared to H’00 and stops.
1	PWM output enabled; TCNT runs.

DTR—Duty Register H’FFA1 PWM0

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Pulse duty factor

TCNT—Timer Counter H’FFA2 PWM0

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Count value (runs from H’00 to H’F9, then repeats from H’00)

TCR—Timer Control Register H’FFA4 PWM1

Bit	7	6	5	4	3	2	1	0
	OE	OS	—	—	—	CKS2	CKS1	CKS0
Initial value	0	0	1	1	1	0	0	0
Read/Write	R/W	R/W	—	—	—	R/W	R/W	R/W

Note: Bit functions are the same as for PWM0.

DTR—Duty Register H’FFA5 PWM1

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for PWM0.

TCNT—Timer Counter H’FFA6 PWM1

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for PWM0.

TCSR—Timer Control/Status Register H'FFA8 (Read), H'FFA9 (Write) WDT

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{\text{IT}}$	TME	—	RST/$\overline{\text{NMI}}$	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W*)	R/W	R/W	—	R/W	R/W	R/W	R/W

Clock Select

0 0 0	φ/2
00 1	φ/3
0 1 0	φ/64
0 1 1	φ/128
1 0 0	φ/256
1 0 1	φ/512
1 1 0	φ/2048
1 1 1	φ/4096

Reset or NMI Select

0	NMI function enabled
1	Reset function enabled

Timer Enable

0	TCNT is initialized to H'00 and stopped
1	TCNT runs and requests an interrupt when it overflows

Timer Mode Select

0	Interval timer mode (OVF request)
1	Watchdog timer mode (NMI request)

Overflow Flag

0	To clear OVF, the CPU must read OVF after it has been set to 1, then write a 0 in this bit
1	Set to 1 when TCNT changes from H'FF to H'00

Note: * Software can write a 0 in bit 7 to clear the flag, but cannot write a 1 in this bit.

TCNT—Timer Counter H'FFA9 WDT

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for PWM0.

P1PCR—Port 1 Pull-Up MOS Control Register H'FFAC Port 1

Bit	7	6	5	4	3	2	1	0
	P1$_7$PCR	P1$_6$PCR	P1$_5$PCR	P1$_4$PCR	P1$_3$PCR	P1$_2$PCR	P1$_1$PCR	P1$_0$PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 1 Pull-Up Control

0	Pull-up off
1	Pull-up on

P2PCR—Port 2 Pull-Up MOS Control Register H'FFAD Port 2

Bit	7	6	5	4	3	2	1	0
	P2$_7$PCR	P2$_6$PCR	P2$_5$PCR	P2$_4$PCR	P2$_3$PCR	P2$_2$PCR	P2$_1$PCR	P2$_0$PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 2 Pull-Up Control

0	Pull-up off
1	Pull-up on

P3PCR—Port 3 Pull-Up MOS Control Register H'FFAE Port 3

Bit	7	6	5	4	3	2	1	0
	$P3_7$PCR	$P3_6$PCR	$P3_5$PCR	$P3_4$PCR	$P3_3$PCR	$P3_2$PCR	$P3_1$PCR	$P3_0$PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 3 Pull-Up Control

0	Pull-up off
1	Pull-up on

P1DDR—Port 1 Data Direction Register H'FFB0 Port 1

Bit	7	6	5	4	3	2	1	0
	$P1_7$DDR	$P1_6$DDR	$P1_5$DDR	$P1_4$DDR	$P1_3$DDR	$P1_2$DDR	$P1_1$DDR	$P1_0$DDR
Mode 1								
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—
Modes 2 and 3								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 1 Input/Output Control

0	Input port
1	Output port

P1DR—Port 1 Data Register H'FFB2 Port 1

Bit	7	6	5	4	3	2	1	0
	$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P2DDR—Port 2 Data Direction Register H’FFB1 Port 2

Bit	7	6	5	4	3	2	1	0
	P2$_7$DDR	P2$_6$DDR	P2$_5$DDR	P2$_4$DDR	P2$_3$DDR	P2$_2$DDR	P2$_1$DDR	P2$_0$DDR
Mode 1								
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—
Modes 2 and 3								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 2 Input/Output Control

0	Input port
1	Output port

P2DR—Port 2 Data Register H’FFB3 Port 2

Bit	7	6	5	4	3	2	1	0
	P2$_7$	P2$_6$	P2$_5$	P2$_4$	P2$_3$	P2$_2$	P2$_1$	P2$_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P3DDR—Port 3 Data Direction Register H’FFB4 Port 3

Bit	7	6	5	4	3	2	1	0
	P3$_7$DDR	P3$_6$DDR	P3$_5$DDR	P3$_4$DDR	P3$_3$DDR	P3$_2$DDR	P3$_1$DDR	P3$_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 3 Input/Output Control

0	Input port
1	Output port

P3DR—Port 3 Data Register H’FFB6 Port 3

Bit	7	6	5	4	3	2	1	0
	P3$_7$	P3$_6$	P3$_5$	P3$_4$	P3$_3$	P3$_2$	P3$_1$	P3$_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P4DDR—Port 4 Data Direction Register H’FFB5 Port 4

Bit	7	6	5	4	3	2	1	0
	P4$_7$DDR	P4$_6$DDR	P4$_5$DDR	P4$_4$DDR	P4$_3$DDR	P4$_2$DDR	P4$_1$DDR	P4$_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 4 Input/Output Control

0	Input port
1	Output port

P4DR—Port 4 Data Register H’FFB7 Port 4

Bit	7	6	5	4	3	2	1	0
	P4$_7$	P4$_6$	P4$_5$	P4$_4$	P4$_3$	P4$_2$	P4$_1$	P4$_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P5DDR—Port 5 Data Direction Register H’FFB8 Port 5

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	P5$_2$DDR	P5$_1$DDR	P5$_0$DDR
Initial value	1	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	W	W	W

Port 5 Input/Output Control

0	Input port
1	Output port

P5DR—Port 5 Data Register H’FFBA Port 5

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	$P5_2$	$P5_1$	$P5_0$
Initial value	1	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	R/W	R/W	R/W

P6DDR—Port 6 Data Direction Register H’FFB9 Port 6

Bit	7	6	5	4	3	2	1	0
	$P6_7$DDR	$P6_6$DDR	$P6_5$DDR	$P6_4$DDR	$P6_3$DDR	$P6_2$DDR	$P6_1$DDR	$P6_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 6 Input/Output Control

0	Input port
1	Output port

P6DR—Port 6 Data Register H’FFBB Port 6

Bit	7	6	5	4	3	2	1	0
	$P6_7$	$P6_6$	$P6_5$	$P6_4$	$P6_3$	$P6_2$	$P6_1$	$P6_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P7DR—Port 7 Data Register H’FFBE Port 7

Bit	7	6	5	4	3	2	1	0
	$P7_7$	$P7_6$	$P7_5$	$P7_4$	$P7_3$	$P7_2$	$P7_1$	$P7_0$
Initial value	*	*	*	*	*	*	*	*
Read/Write	R	R	R	R	R	R	R	R

* Depends on the levels of pins $P7_7$ to $P7_0$.

P8DDR—Port 8 Data Direction Register H’FFBD Port 8

Bit	7	6	5	4	3	2	1	0
	—	P8$_6$DDR	P8$_5$DDR	P8$_4$DDR	P8$_3$DDR	P8$_2$DDR	P8$_1$DDR	P8$_0$DDR
Initial value								
Modes 1 and 2	1	0	0	0	0	0	0	1
Mode 3	1	0	0	0	0	0	0	0
Read/Write	—	W	W	W	W	W	W	W

Port 8 Input/Output Control

0	Input port
1	Output port

P8DR—Port 8 Data Register H’FFBF Port 8

Bit	7	6	5	4	3	2	1	0
	—	P8$_6$	P8$_5$	P8$_4$	P8$_3$	P8$_2$	P8$_1$	P8$_0$
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P9DDR—Port 9 Data Direction Register H’FFC0 Port 9

Bit	7	6	5	4	3	2	1	0
	P9$_7$DDR	P9$_6$DDR	P9$_5$DDR	P9$_4$DDR	P9$_3$DDR	P9$_2$DDR	P9$_1$DDR	P9$_0$DDR
Modes 1 and 2								
Initial value	0	1	0	0	0	0	0	0
Read/Write	W	—	W	W	W	W	W	W
Mode 3								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 9 Input/Output Control

0	Input port
1	Output port

P9DR—Port 9 Data Register H’FFC1 Port 9

Bit	7	6	5	4	3	2	1	0
	$P9_7$	$P9_6$	$P9_5$	$P9_4$	$P9_3$	$P9_2$	$P9_1$	$P9_0$
Initial value	0	*	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Depends on the level of pin $P9_6$.

STCR—Serial/Timer Control Register H’FFC3 8-Bit Timer

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	MPE	ICKS1	ICKS0
Initial value	1	1	1	1	1	0	0	0
Read/Write	—	—	—	—	—	R/W	R/W	R/W

Internal Clock Source

See section 7, 8-Bit Timer,
for description of these bits

Multiprocessor Enable

0	The multiprocessor communication function is disabled, regardless of the setting of the MP bit in SMR
1	The multiprocessor communication function is enabled. The multiprocessor format can be selected by setting the MP bit in SMR to 1

SYSCR—System Control Register H’FFC4 System Control

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	XRST	NMIEG	HIE	RAME
Initial value	0	0	0	0	1	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

RAM Enable

0	On-chip RAM is disabled.
1	On-chip RAM is enabled.

Host Interface Enable

0	Host interfaceis disabled.
1	Host interfaceis enabled.

NMI Edge

0	Falling edge of $\overline{\text{NMI}}$ is detected.
1	Rising edge of $\overline{\text{NMI}}$ is detected.

External Reset

0	Reset was generated by watchdog timer overflow.
1	Reset was generated by external reset input.

Standby Timer Select

0	0	0	Clock settling time = 8192 states
0	0	1	Clock settling time = 16384 states
0	1	0	Clock settling time = 32768 states
0	1	1	Clock settling time = 65536 states
1	–	–	Clock settling time = 131072 states

Software Standby

0	SLEEP instruction causes transition to sleep mode.
1	SLEEP instruction causes transition to software standby mode.

MDCR—Mode Control Register H’FFC5 System Control

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MDS1	MDS0
Initial value	1	1	1	0	0	1	*	*
Read/Write	—	—	—	—	—	—	R	R

Mode Select Bits

Value at mode pins.

* Determined by inputs at pins MD$_1$ and MD$_0$.

ISCR—IRQ Sense Control Register H’FFC6 System Control

Bit	7	6	5	4	3	2	1	0
	IRQ$_7$SC	IRQ$_6$SC	IRQ$_5$SC	IRQ$_4$SC	IRQ$_3$SC	IRQ$_2$SC	IRQ$_1$SC	IRQ$_0$SC
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ$_0$ to IRQ$_7$ Sense Control

0	IRQ$_i$ is level-sensed (active Low).
1	IRQ$_i$ is edge-sensed (falling edge).

IER—IRQ Enable Register H’FFC7 System Control

Bit	7	6	5	4	3	2	1	0
	IRQ$_7$E	IRQ$_6$E	IRQ$_5$E	IRQ$_4$E	IRQ$_3$E	IRQ$_2$E	IRQ$_1$E	IRQ$_0$E
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ$_0$ to IRQ$_7$ Enable

0	IRQ$_i$ is disabled.
1	IRQ$_i$ is enabled.

TCR—Timer Control Register H’FFC8 TMR0

Bit	7	6	5	4	3	2	1	0
	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

TCR			STCR		
CKS2	CKS1	CKS0	ICKS1	ICKS0	Description
0	0	0	—	—	Timer stopped
0	0	1	0	—	ϕ/8 internal clock, falling edge
0	0	1	1	—	ϕ/2 internal clock, falling edge
0	1	0	0	—	ϕ/64 internal clock, falling edge
0	1	0	1	—	ϕ/32 internal clock, falling edge
0	1	1	0	—	ϕ/1024 internal clock, falling edge
0	1	1	1	—	ϕ/256 internal clock, falling edge
1	0	0	—	—	Timer stopped
1	0	1	—	—	External clock, rising edge
1	1	0	—	—	External clock, falling edge
1	1	1	—	—	External clock, rising and falling edges

Counter Clear

0	0	Counter is not cleared.
0	1	Cleared by compare-match A.
1	0	Cleared by compare-match B.
1	1	Cleared on rising edge of external reset input.

Timer Overflow Interrupt Enable

0	Overflow interrupt request is disabled.
1	Overflow interrupt request is enabled.

Compare-Match Interrupt Enable A

0	Compare-match A interrupt request is disabled.
1	Compare-match A interrupt request is enabled.

Compare-Match Interrupt Enable B

0	Compare-match B interrupt request is disabled.
1	Compare-match B interrupt request is enabled.

TCSR—Timer Control/Status Register H’FFC9 TMR0

Bit	7	6	5	4	3	2	1	0
	CMFB	CMFA	OVF	—	OS3*2	OS2*2	OS1*2	OS0*2
Initial value	0	0	0	1	0	0	0	0
Read/Write	R/(W)*1	R/(W)*1	R/(W)*1	—	R/W	R/W	R/W	R/W

Output Select

0	0	No change on compare-match A.
0	1	Output “0” on compare-match A.
1	0	Output “1” on compare-match A.
1	1	Invert (toggle) output on compare-match A.

Output Select

0	0	No change on compare-match B.
0	1	Output “0” on compare-match B.
1	0	Output “1” on compare-match B.
1	1	Invert (toggle) output on compare-match B.

Timer Overflow Flag

0	Cleared when CPU reads OVF = “1,” then writes “0” in OVF.
1	Set when TCNT changes from H’FF to H’00.

Compare-Match Flag A

0	Cleared when CPU reads CMFA = “1,” then writes “0” in CMFA.
1	Set when TCNT = TCORA.

Compare-Match Flag B

0	Cleared from when CPU reads CMFB = “1,” then writes “0” in CMFB.
1	Set when TCNT = TCORB.

*1 Software can write a “0” in bits 7 to 5 to clear the flags, but cannot write a “1” in these bits.

*2 When all four bits (OS3 to OS0) are cleared to “0,” output is disabled.

TCORA—Time Constant Register A **H’FFCA** **TMR0**

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The CMFA bit is set to “1” when TCORA = TCNT.

TCORB—Time Constant Register B **H’FFCB** **TMR0**

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The CMFB bit is set to “1” when TCORB = TCNT.

TCNT—Timer Counter **H’FFCC** **TMR0**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Count value

TCR—Timer Control Register H’FFD0 TMR1

Bit	7	6	5	4	3	2	1	0
	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

TCR			STCR		
CKS2	CKS1	CKS0	ICKS1	ICKS0	Description
0	0	0	—	—	Timer stopped
0	0	1	0	—	ϕ/8 internal clock, falling edge
0	0	1	1	—	ϕ/2 internal clock, falling edge
0	1	0	0	—	ϕ/64 internal clock, falling edge
0	1	0	1	—	ϕ/128 internal clock, falling edge
0	1	1	0	—	ϕ/1024 internal clock, falling edge
0	1	1	1	—	ϕ/2048 internal clock, falling edge
1	0	0	—	—	Timer stopped
1	0	1	—	—	External clock, rising edge
1	1	0	—	—	External clock, falling edge
1	1	1	—	—	External clock, rising and falling edges

Counter Clear

0	0	Counter is not cleared.
0	1	Cleared by compare-match A.
1	0	Cleared by compare-match B.
1	1	Cleared on rising edge of external reset input.

Timer Overflow Interrupt Enable

0	Overflow interrupt request is disabled.
1	Overflow interrupt request is enabled.

Compare-Match Interrupt Enable A

0	Compare-match A interrupt request is disabled.
1	Compare-match A interrupt request is enabled.

Compare-Match Interrupt Enable B

0	Compare-match B interrupt request is disabled.
1	Compare-match B interrupt request is enabled.

TCSR—Timer Control/Status Register H’FFD1 TMR1

Bit	7	6	5	4	3	2	1	0
	CMFB	CMFA	OVF	—	OS3*2	OS2*2	OS1*2	OS0*2
Initial value	0	0	0	1	0	0	0	0
Read/Write	R/(W)*1	R/(W)*1	R/(W)*1	—	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for TMR0.

*1 Software can write a “0” in bits 7 to 5 to clear the flags, but cannot write a “1” in these bits.

*2 When all four bits (OS3 to OS0) are cleared to “0,” output is disabled.

TCORA—Time Constant Register A H’FFD2 TMR1

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for TMR0.

TCORB—Time Constant Register B H’FFD3 TMR1

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for TMR0.

TCNT—Timer Counter H’FFD4 TMR1

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for TMR0.

SMR—Serial Mode Register H'FFD8 SCI

Bit	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	1	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ϕ clock
0	1	ϕ/4 clock
1	0	ϕ/16 clock
1	1	ϕ/64 clock

Multiprocessor Mode

0	Multiprocessor function is disabled
1	Multiprocessor function is enabled

Stop Bit Length

0	One stop bit
1	Two stop bits

Parity Mode

0	Even parity
1	Odd parity

Parity Enable

0	Transmit: No parity bit added. Receive: Parity bit not checked.
1	Transmit: Parity bit added. Receive: Parity bit checked.

Character Length

0	8-Bit data length
1	7-Bit data length

Communication Mode

0	Asynchronous
1	Synchronous

BRR—Bit Rate Register H’FFD9 SCI

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Constant that determines the bit rate

SCR—Serial Control Register **H'FFDA** **SCI**

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	1	1	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable 0

0	Asynchronous serial clock not output
1	Asynchronous serial clock output at SCK pin

Clock Enable 1

0	Internal clock
1	External clock, input at SCK pin

Transmit-End Interrupt Enable

0	The TSR-empty interrupt request (TEI) is disabled.
1	The TSR-empty interrupt request (TEI) is enabled.

Multiprocessor Interrupt Enable

0	The multiprocessor receive interrupt function is disabled.
1	The multiprocessor receive interrupt function is enabled.

Receive Enable

0	Receive disabled
1	Receive enabled

Transmit Enable

0	Transmit disabled
1	Transmit enabled

Receive Interrupt Enable

0	Receive interrupt request (RxI) is disabled.
1	Receive interrupt request (RxI) is enabled.

Transmit Interrupt Enable

0	Transmit interrupt request (TxI) is disabled.
1	Transmit interrupt request (TxI) is enabled.

TDR—Transmit Data Register H'FFDB SCI

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Transmit data

SSR—Serial Status Register H’FFDC SCI

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor Bit Transfer

0	Multiprocessor bit = “0” in transmit data.
1	Multiprocessor bit = “1” in transmit data.

Multiprocessor Bit

0	Multiprocessor bit = “0” in receive data.
1	Multiprocessor bit = “1” in receive data.

Transmit End

0	Cleared when CPU reads TDRE = “1”, then writes “0” in TDRE.
1	Set to “1” when TE = “0,” or when TDRE = “1” at the end of character transmission

Parity Error

0	Cleared when CPU reads PER = “1,” then writes “0” in PER.
1	Set when a parity error occurs (parity of receive data does not match parity selected by $O/\overline{E}$ bit).

Framing Error

0	Cleared when CPU reads FER = “1,” then writes “0” in FER.
1	Set when a framing error occurs (stop bit is “0”).

Overrun Error

0	Cleared when CPU reads ORER = “1,” then writes “0” in ORER.
1	Set when an overrun error occurs (next data is completely received while RDRF bit is set to “1”).

Receive Data Register Full

0	Cleared when CPU reads RDRF = “1,” then writes “0” in RDRF.
1	Set when one character is received normally and transferred from RSR to RDR.

Transmit Data Register Empty

0	Cleared when CPU reads TDRE = “1,” then writes “0” in TDRE
1	Set when: 1. Data is transferred from TDR to TSR. 2. TE is cleared while TDRE = "0."

* Software can write a “0” in bits 7 to 3 to clear the flags, but cannot write a “1” in these bits.

RDR—Receive Data Register H’FFDD SCI

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Receive data

ADDRn—A/D Data Register n (n = A, B, C, D) A/D
H’FFE0, H’FFE2, H’FFE4, H’FFE6

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

A/D conversion result

Note: The least significant bit of the register address is ignored.

ADCSR—A/D Control/Status Register H’FFE8 A/D

Bit	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel Select

CH2	CH1	CH0	Single mode	Scan mode
0	0	0	AN0	AN0
	0	1	AN1	AN0, AN1
	1	0	AN2	AN0 to AN2
	1	1	AN3	AN0 to AN3
1	0	0	AN4	AN4
	0	1	AN5	AN4, AN5
	1	0	AN6	AN4 to AN6
	1	1	AN7	AN4 to AN7

Clock Select

0	Conversion time = 242 states (max)
1	Conversion time = 122 states (max)

Scan Mode

0	Single mode
1	Scan mode

A/D Start

0	A/D conversion is halted.
1	1. Single mode: One A/D conversion is performed, then this bit is automatically cleared to “0.” 2. Scan mode: A/D conversion starts and continues cyclically on all selected channels until “0” is written in this bit.

A/D Interrupt Enable

0	The A/D interrupt request (ADI) is disabled.
1	The A/D interrupt request (ADI) is enabled.

A/D End Flag

0	Cleared from “1” to “0” when CPU reads ADF = “1,” then writes “0” in ADF.
1	Set to “1” at the following times: 1. Single mode: at the completion of A/D conversion 2. Scan mode: when all selected channels have been converted.

* Software can write a “0” in bit 7 to clear the flag, but cannot write a “1” in this bit.

ADCR—A/D Control Register **H’FFEA or H’FFEB** **A/D**

Bit	7	6	5	4	3	2	1	0
	TRGE	—	—	—	—	—	—	CHS
Initial value	0	1	1	1	1	1	1	0
Read/Write	R/W	—	—	—	—	—	—	R/W

Channel Select

Trigger Enable

0	ADTRG is disabled.
1	ADTRG is enabled. A/D conversion can be started by external trigger, or by software.

HICR—Host Interface Register **H’FFF0** **HIF**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	IBFIE2	IBFIE1	FGA20E
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	R/W	R/W	R/W

Fast GATE A_{20} Enable

0	Disables fast GATE A_{20} function
1	Enables fast GATE A_{20} function

Input Data Register 1 Full Interrupt Enable

0	Input data register IDR1 full interrupt is disabled
1	Input data register IDR1 full interrupt is enabled

Input Data Register 2 Full Interrupt Enable

0	Input data register IDR2 full interrupt is disabled
1	Input data register IDR2 full interrupt is enabled

IDR1—Input Data Register 1 H’FFF4 HIF

Bit	7	6	5	4	3	2	1	0
	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

Input Data

Commands and data input from the host processor.

ODR1—Output Data Register 1 H’FFF5 HIF

Bit	7	6	5	4	3	2	1	0
	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
Initial value	—	—	—	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output Data

Commands and data output to the host processor.

STR1—Status Register 1 H’FFF6 HIF

Bit	7	6	5	4	3	2	1	0
	DBU	DBU	DBU	DBU	C/$\overline{\text{D}}$	DBU	IBF	OBF
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R	R

Output Data Register Full

0	Output data register (ODR1) empty
1	Output data register (ODR1) full

Input Data Register Full

0	Input data register (IDR1) empty
1	Input data register (IDR1) full

Defined by User

Command or Data

0	Contents of IDR1 are data
1	Contents of IDR1 are a command

Defined by User

IDR2—Input Data Register 2 H’FFFC HIF

Bit	7	6	5	4	3	2	1	0
	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
Initial value	—	—	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R

Input Data

Commands and data input from the host processor.

ODR2—Output Data Register 2 H’FFFD HIF

Bit	7	6	5	4	3	2	1	0
	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
Initial value	—	—	—	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output Data

Commands and data output to the host processor.

STR2—Stauts Register 2 H’FFFE HIF

Bit	7	6	5	4	3	2	1	0
	DBU	DBU	DBU	DBU	C/$\overline{D}$	DBU	IBF	OBF
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R	R

Output Data Register Full

0	Output data register (ODR2) empty
1	Output data register (ODR2) full

Input Data Register Full

0	Input data register (IDR2) empty
1	Input data register (IDR2) full

Defined by User

Command or Data

0	Contents of IDR2 are data
1	Contents of IDR2 are a command

Defined by User

Appendix C. Pin States

C.1 Pin States in Each Mode

Table C-1. Pin States

Pin name	MCU mode	Reset	Hardware standby	Software standby	Sleep mode	Normal operation
$P1_7$ to $P1_0$	1	Low	3-State	Low	Prev. state	A_7 to A_0
A_7 to A_0	2	3-State		Low if DDR = 1, Prev. state if DDR = 0	(Addr. output pins: last address accessed)	Addr. output or input port
	3			Prev. state		I/O port
$P2_7$ to $P2_0$	1	Low	3-State	Low	Prev. state	A_{15} to A_8
A_{15} to A_8	2	3-State		Low if DDR = 1, Prev. state if DDR = 0	(Addr. output pins: last address accessed)	Addr. output or input port
	3			Prev. state		I/O port
$P3_7$ to $P3_0$	1	3-State	3-State	3-state	3-State	D_7 to D_0
D_7 to D_0	2					
	3			(note 5)	Prev. state	I/O port
$P4_7$ to $P4_0$	1	3-State	3-State	Prev. state	Prev. state	I/O port
	2			(note 3)		
	3					
$P5_2$ to $P5_0$	1	3-State	3-State	Prev. state	Prev. state	I/O port
	2			(note 3)		
	3					
$P6_7$ to $P6_0$	1	3-State	3-State	Prev. state	Prev. state	I/O port
	2			(note 3)		
	3					
$P7_7$ to $P7_0$	1	3-State	3-State	3-State	3-State	Input port
	2					
	3					
$P8_6$ to $P8_0$	1	3-State	3-State	Prev. state	Prev. state	I/O port
	2			(note 3)		
	3			(note 6)		

Table C-1. Pin States (cont.)

Pin name	MCU mode	Reset	Hardware standby	Software standby	Sleep mode	Normal operation
P9$_7$/$\overline{\text{WAIT}}$	1	3-State	3-State	3-State	3-State	$\overline{\text{WAIT}}$
	2					
	3			Prev. state	Prev. state	I/O port
P9$_6$/ϕ	1	Clock output	3-state	High	Clock output	Clock output
	2					
	3	3-State		High if DDR = 1, 3-state if DDR = 0	Clock output if DDR = 1, 3-state if DDR = 0	Clock output if DDR = 1, input port if DDR = 0
P9$_5$ to P9$_3$, $\overline{\text{AS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$	1	High	3-State	High	High	$\overline{\text{AS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$
	2					
	3	3-State		Prev. state	Prev. state	I/O port
P9$_2$ to P9$_0$,	1	3-State	3-State	Prev. state	Prev. state	I/O port
	2					
	3					

Notes:

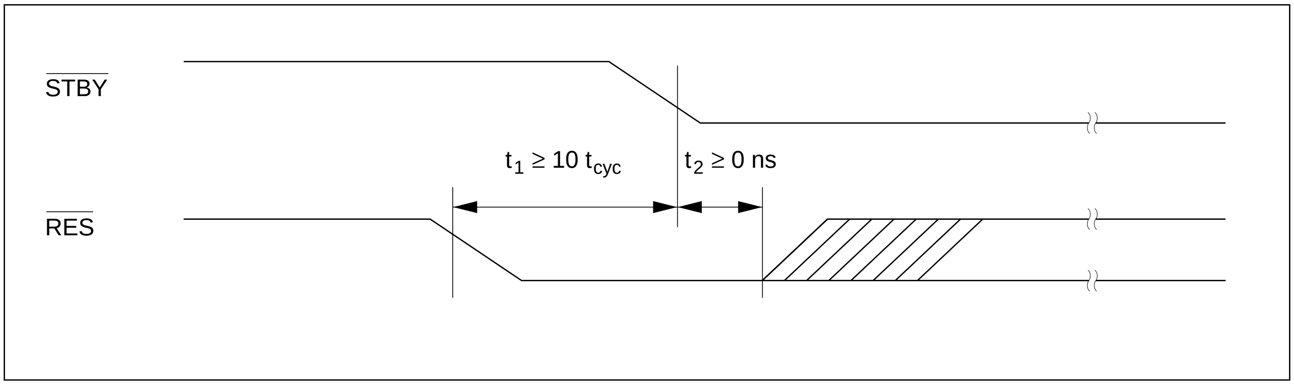
1. 3-state: High-impedance state
2. Prev. state: Previous state. Input ports are in the high-impedance state (with the MOS pull-up on if DDR = 0 and DR = 1). Output ports hold their previous output level.
3. On-chip supporting modules are initialized, so these pins revert to I/O ports according to the DDR and DR bits.
4. I/O port: Direction depends on the data direction (DDR) bit. Note that these pins may also be used by the on-chip supporting modules.
5. In master mode operation, these pins maintain their previous state. However, in slave mode operation, these port pins (P3$_7$–P3$_0$) will output 1 if the corresponding DDR bit is set to 1. Otherwise, they will be high-impedance.
6. In slave mode operation, P8$_0$–P8$_5$ are used as the host interface I/O port. During software standby, P8$_0$ to P8$_6$ will maintain their previous state.

See section 5, “I/O Ports” for further information.

Appendix D. Timing of Transition to and Recovery from Hardware Standby Mode

Timing of Transition to Hardware Standby Mode

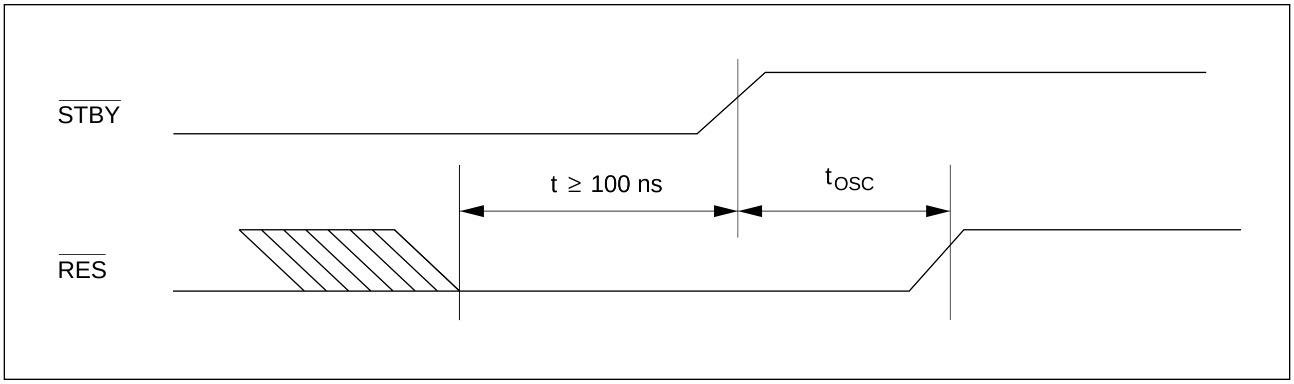
(1) To retain RAM contents, set the RAME bit to 1 and drive $\overline{\text{RES}}$ signal low for 10 system clock cycles before the $\overline{\text{STBY}}$ signal goes low, as shown below. $\overline{\text{RES}}$ must remain low until $\overline{\text{STBY}}$ goes low (minimum delay from STBY low to $\overline{\text{RES}}$ high: 0 ns).



(2) When it is not necessary to retain RAM contents, or when RAM content should be retaind while the RAME bit is set to 0, $\overline{\text{RES}}$ does not have to be driven low as in (1).

Timing of Recovery From Hardware Standby Mode

Drive the $\overline{\text{RES}}$ signal low approximately 100 ns before $\overline{\text{STBY}}$ goes high.



Appendix E. Package Dimensions

Figure E-1 shows the dimensions of the CP-84 package. Figure E-2 shows the dimensions of the FP-80A package. Figure E-3 shows the dimensions of the CG-84 package.

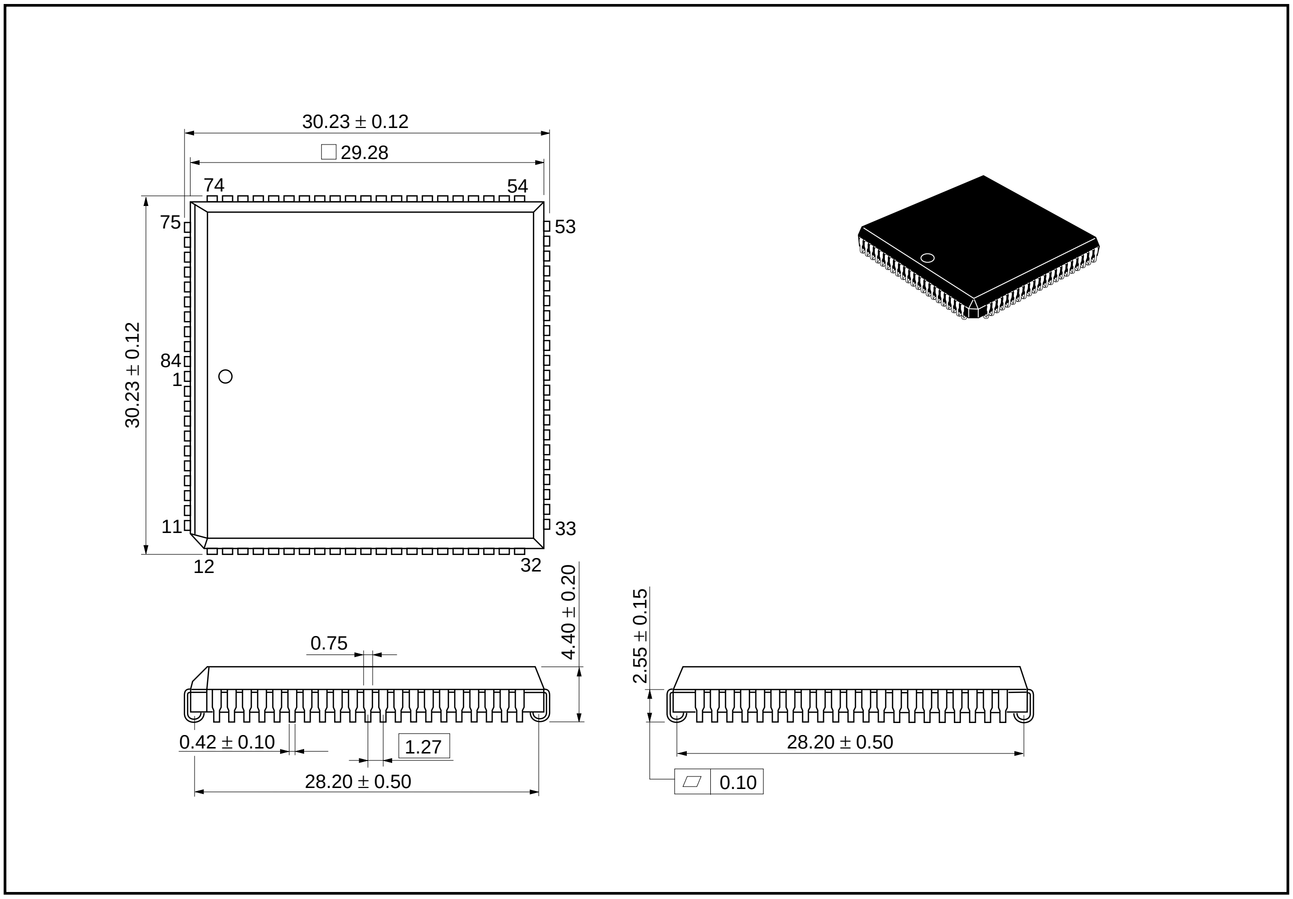


Figure E-1. Package Dimensions (CP-84)

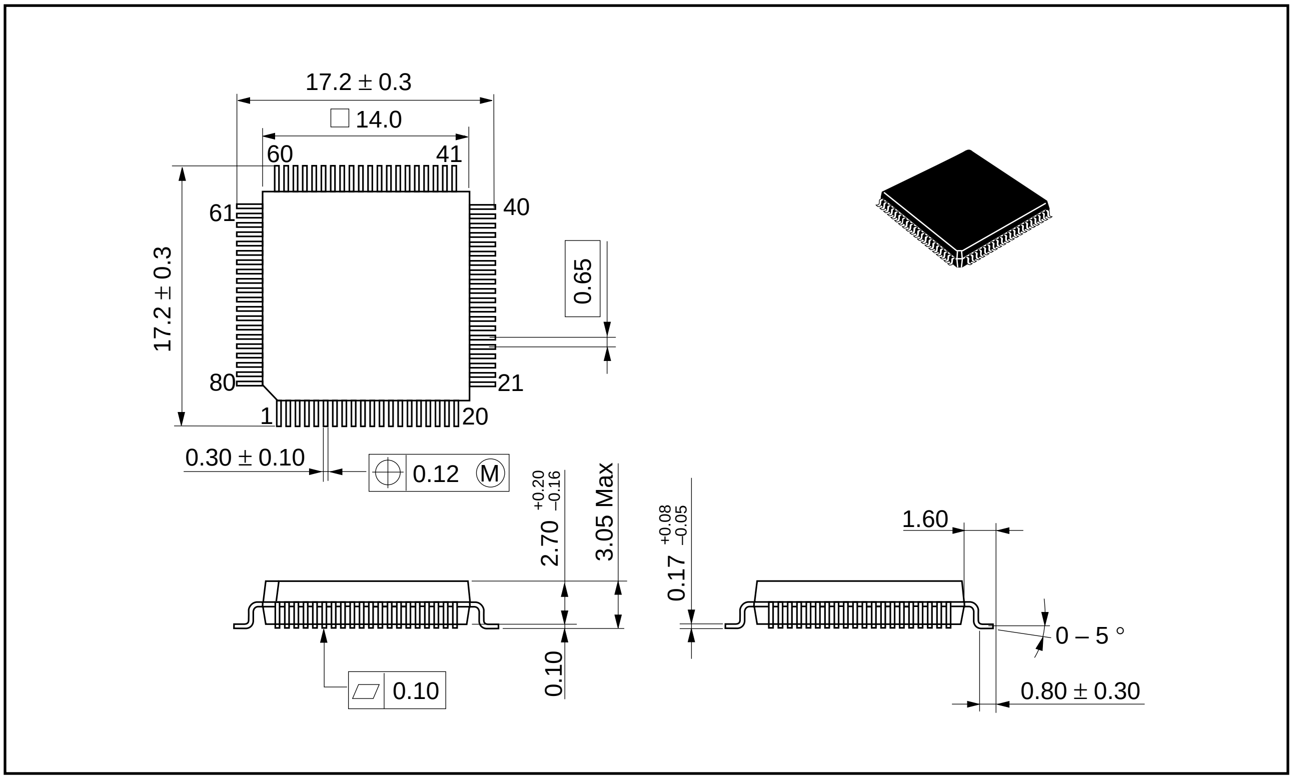


Figure E-3. Package Dimensions (FP-80A)

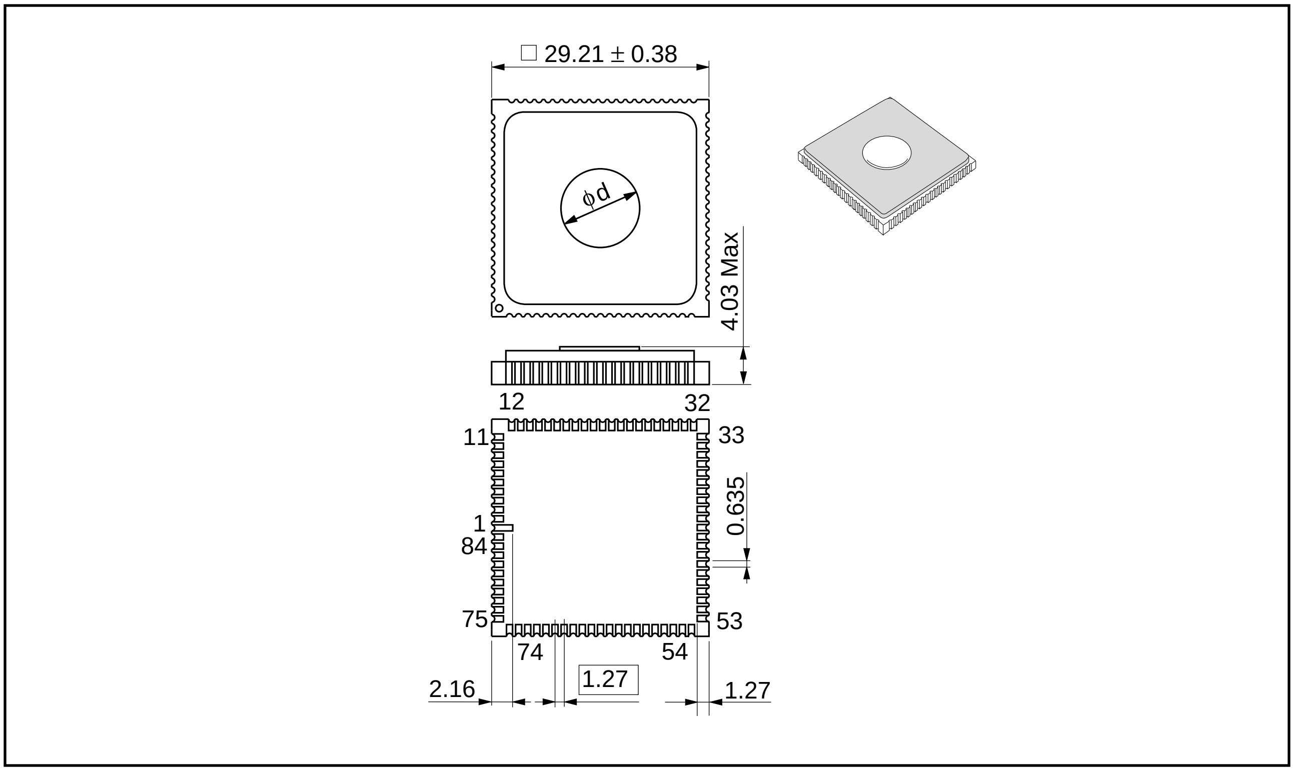


Figure E-3. Package Dimensions (CG-84)