

## Design Tips for I/O Port Pins

This technote focuses on two design tips that should be of use to the hardware design engineer. Although the discussion will focus on the H8/53x microcontrollers, by no means is the discussion limited to these devices.

The H8/53x input port pins are designed to accept either TTL or CMOS signal inputs. The input characteristics are very similar to that found in HCT logic. That is, its input logic levels are TTL-compatible, and its output characteristics are like standard high-speed CMOS.

### Design Tip 1

By convention unused input port pins are normally tied to Vcc or Gnd (See Fig: 1). This is done to prevent excessive current draw from the forward biasing of the P-channel and N-channel transistors. Although this is a commonly used method to protect the CMOS input gate, by no means is it the best method. In fact, connecting a port pin to either Vcc or ground could lead to unexpected results under certain conditions.

If an unused port pin is connected to Vcc and by accident (glitch or software error) the port pin is configured as an output and pulled low, excessive current will flow since there is no current limiting resistor. This can deteriorate the performance and reliability of the system. To be on the safe side, we recommend a pull-up or pull-down resistor (See Fig: 2) be connected to all unused I/O port pins as a safety precaution. Although this may add a few extra cents to the cost of design, the added safety protection is well worth the cost.

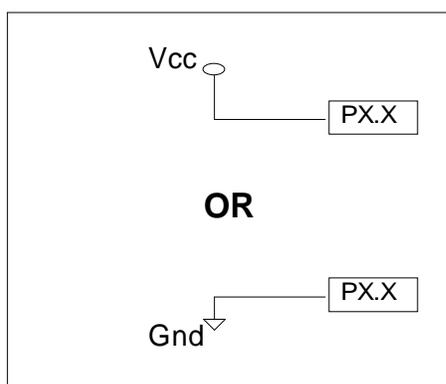


Figure 1

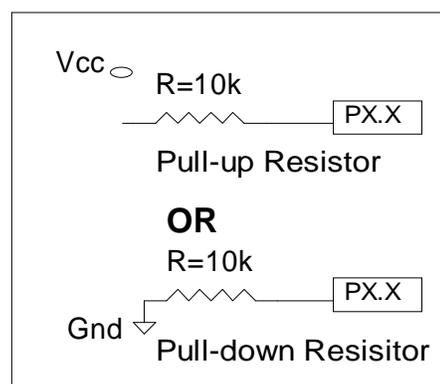


Figure 2

### Design Tip 2

For applications with I/O port pins terminating at edge connectors, a pull-down resistor along with a series resistor should be connected as shown in Figure 3. The pull down resistor R2 forces the pin to a known state in the absence of a signal being applied to the port pin and it helps eliminate static charges that may build up on the PCB. Series resistor R1 provides static and current limiting protection. See Figure 3 for details.

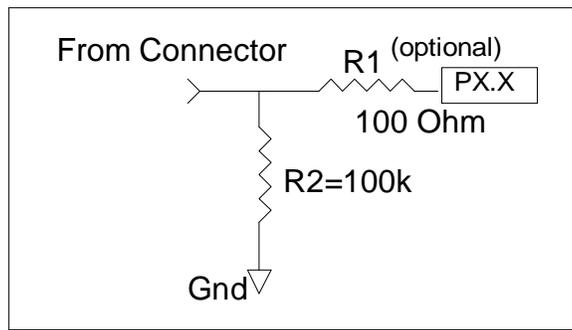


Figure 3

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