APPENDIX A: FAILURE RATE CALCULATION

Thermal Acceleration Factors

Acceleration factors (AF) for thermal stresses (High Temperature Operating Life, Data Retention and High Temperature Steady State Life) are calculated from the Arrhenius equation.

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

While there is no substitute for experimentally determining the activation energy, obtaining this information is very difficult because few devices fail stress tests. In the absence of experimental data, the following literature values are used.

Table I - Activation Energies

Failure Mechanism	Activation Energy (eV)
Charge Gain	0.3 - 0.6
Charge Loss (defects)	0.6
Charge Loss (Ionic contamination, edge bits)	1.2
Charge Loss (intrinsic wear out)	1.4
Contact Metallurgy	0.9
Electromigration	0.6 - 1.0
Intermetallic Growth (Gold)	1.0
Ionic Contamination	1.0 - 1.4
Metal Particles	0.7
Micro-cracks	1.3
Non-Visual Bits	0.6
Oxide Defects	0.3
Polarization	1.0
Silicon Bulk Defects	0.5
Surface Charge	0.5 - 1.0
Slow Trapping	1.0 - 1.3
Fabrication Defects	0.45
Unknown/Non-Visual Defect (NVD)	0.45

For example, for charge loss defects (E_A = 0.6 eV), the thermal acceleration factor between a stress junction temperature of 165°C and a use junction temperature of 70°C is:

APPENDIX A: FAILURE RATE CALCULATION (CONT.)

$$AF = \exp\left[\frac{0.6}{8.62x10^{-5}}\left[\frac{1}{343} - \frac{1}{438}\right]\right] = 82$$

Temperature-Humidity Acceleration Factors

We estimate acceleration factors for temperature-humidity stresses (Pressure Cooker Test and HAST) from a model developed by Hallberg and Peck ("Quality and Reliability Engineering International", Vol. 7, 1991.). In this paper, the authors pooled all published HAST data between 1979-1987 into one model.

The Hallberg and Peck model requires the stress junction temperature and relative humidity as well as the use temperature and relative humidity. To estimate the use relative humidity, we assume that the device room temperature is 35°C (95°F) and the room relative humidity is 100%. From any Handbook of Chemistry and Physics, the vapor pressure of water (VP(water)) at 35°C is 41.175 mm Hg. If we also assume that the device will operate with a junction temperature of 70°C (VP(water) at 70°C of 233.7 mm Hg), the junction relative humidity (RH_j) is

$$RH_j = 100\left(\frac{41.175}{233.7}\right) = 17.6\%$$

The operating conditions of the devices are then 70°C and 17.6% relative humidity.

Our Pressure Cooker Test (PCT) submits the devices to a temperature of 121°C and 100% relative humidity. Using the Hallberg and Peck model, the acceleration factor for the PCT stress can be calculated.

$$t_f = A\,(\%RH)^{-3}\exp\left(\frac{0.9}{kT}\right)$$

$$AF = \left(\frac{17.6}{100}\right)^{-3}\exp\left[\frac{0.9}{k}\left[\frac{1}{343} - \frac{1}{394}\right]\right] = 9433$$

The acceleration factor for HAST is calculated similarly, except junction temperature heating effects must be included when estimating the relative humidity at the die surface. Assuming an average junction temperature rise of 5°C, the relative humidity at the die surface during 140°C HAST testing can be calculated.

VP(140°C) = 2710.92 mm Hg
VP(145°C) = 3116.76 mm Hg

APPENDIX A: FAILURE RATE CALCULATION (CONT.)

$$RH_j = 85\% \left(\frac{2710.92}{3116.76}\right) = 73.9\%$$

Temperature-Humidity Acceleration Factors

Finally, the acceleration factor for HAST, AF_{HAST}, can be calculated.

$$AF\ (140°C) = \left(\frac{17.6}{73.9}\right)^{-3} \exp\left[\frac{0.9}{k}\left[\frac{1}{343} - \frac{1}{418}\right]\right] = 17{,}433$$

Similarly, for 130°C HAST testing,

VP(130°C) = 2026.10 mm Hg
VP(135°C) = 2347.26 mm Hg

$$RH_j = 85\% \left(\frac{2026.10}{2347.26}\right) = 73.4\%$$

$$AF\ (130°C) = \left(\frac{17.6}{73.4}\right)^{-3} \exp\left[\frac{0.9}{k}\left[\frac{1}{343} - \frac{1}{408}\right]\right] = 9{,}261$$

Failure Rate Calculation

For all but the High Temperature Operating Life (HTOL) test, the failure rate is calculated by dividing the number of fails by the product of the acceleration factor and the number of stress device-hours. For example, two FAMOS Technology devices failed during the equivalent of 110,129 device-hours of 140°C HAST. The failure rate, FR, in FIT (failures in one billion device hours) is

$$FR = \left(\frac{2}{110{,}129\ x\ 17{,}433}\right) 10^9 = 1\ FIT$$

For HTOL tests, a 60% chi-squared approximation of the failure rate is made.

$$\text{FR (Chi-squared)} = \chi^2_{2n+2} / (2 \text{ x AF x \# device-hours}) \text{ x } 10^9$$

where n is the number of failures.

For example, during the equivalent of 698,223 device-hours of 150°C HTOL stress testing, no FAMOS technology devices failed (assumed activation energy = 0.6 eV). The 60% chi-squared estimate of the failure rate is (from statistical tables, $\chi^2_2(60\%) = 1.83$)

$$\text{FR (Chi-squared)} = [1.83/(2 \text{ x } 82 \text{ x } 698{,}223)] \text{ x } 10^9 = 16 \text{ FIT.}$$

APPENDIX B: TEMPERATURE CYCLING STRESS TEST MODELS

Two acceleration factor (AF) models are used to model temperature cycling failures. The model proposed by Zelenka [1] and others uses the epoxy molding temperature (T_{mold} = 170°C) and the minimum temperature reached during temperature cycling, (T_{min}).

$$AF_{brittle} = \left(\frac{T_{mold} - T_{min,stress}}{T_{mold} - T_{min,use}} \right)^{m}$$

The model constant, 'm', is experimentally calculated for each failure mechanism. The acceleration factor is labeled `brittle' because the derivation of this equation assumes brittle fracture mechanics. Basically, the model assumes that cracks advance a little every time the maximum stress is reached. The maximum stress is assumed to be proportional to the difference in temperature between the minimum and maximum stress temperatures. For plastic-encapsulated devices, the stress is a minimum during molding, (T_{mold}), and a maximum during the lowest temperature reached during temperature cycling, (T_{min}).

The model constant, m, is a function of the failure mechanism.

Thin Film Cracking	m = 12 (Blish and Vaney [2])
Al/Au Intermetallic Fractures	m=4
Chip-Out (Cratering) Bond Failures	m=7 (Dunn and McPherson [3])

For ductile materials, dislocation movement dominates the fracture mechanics and a different model is used.

The second, and most widely accepted model, uses the difference between the minimum and maximum temperatures during temperature cycle testing (T_{min} and T_{max}) to calculate an acceleration factor.

$$AF_{ductile} = \left(\frac{T_{max,stress} - T_{min,stress}}{T_{max,use} - T_{min,use}} \right)^{m}$$

The model constant, 'm', is again experimentally calculated for each failure mechanism.

Coffin and Manson [4] developed this model from empirical observations of metal fatigue. In ductile materials, if the applied stress is high enough, dislocations are produced. At the high temperature condition of the temperature cycling stress, dislocations are forced towards one metal surface. At the low temperature, the dislocations try to glide back to their original position, but many cannot because they became entangled with other dislocations. After many cycles, these tangles grow until cracking, and finally failure, occurs. Both minimum and maximum temperatures are important, because both contribute to dislocation movement and entanglement. This model is recommended for any failures involving ductile materials. Model constants for ductile failure mechanisms follow.

Wire Bond Breakage	m=5.16 (Cypress Experimentation. See Appendix D)
Solder Fatigue	m=2 (Blish and Vaney [2])

APPENDIX B: TEMPERATURE CYCLING STRESS TEST MODELS (CONT.)

Failure Rate Calculations

By combining acceleration factor models with a few conservative assumptions, the temperature cycling failure rate can be estimated.

Our commercial devices are specified to operate between 0°C and 70°C. Using this information, the acceleration factor, AF, between use and Military Condition C stress testing (-65 to 150°C) for the brittle, thin film cracking failure mechanism and ductile, wire bond breakage failure mechanism can be calculated.

$$AF_{brittle} = \left(\frac{170 - (-65)}{170 - 0}\right)^{12} = 49$$

$$AF_{ductile} = \left(\frac{150 - (-65)}{70 - 0}\right)^{5.16} = 327$$

Failure rate calculations are best explained with an example. In 1995, five BiCMOS technology devices failed during 1,063,256 stress device-temperature cycles for thin film cracking. Assuming 365 use temperature cycles per year (0.04166 cycles/hour), the failure rate, FR, is simply

$$FR = \frac{(5)\ 0.04166}{1{,}063{,}256\ (49)}\ 10^9 = 4\ FIT$$

All temperature cycling failure rates in this report were calculated using the above methodology.

References

[1] R. L. Zelenka, **IEEE/IRPS**, pp. 30-34, 1991.
[2] R. C. Blish and P. R. Vaney, **IEEE/IRPS**, pp. 22-29, 1991.
[3] C. F. Dunn and J. W. McPherson, **IEEE/IRPS**, pp. 252-258, 1990.
[4] S. S. Manson, **Thermal Stress and Low-Cycle Fatigue**, (Robert Krieger: Malabar, Florida), 1981.

APPENDIX C: EQUIVALENCE OF DIFFERENT STRESS TEST CONDITIONS

During stress testing, more than one set of test conditions were used. To account for this difference, stress test hours or cycles at the lower stress condition were derated and then added to the total for the most severe stress test condition.

Dynamic (HTOL) and Static (HTSSL) Burn In

HTOL and HTSSL tests were performed at 150°C, 140°C, and 125°C. Using the Arrhenius equation (Appendix A) and an activation energy of 0.6 eV, the derating factor, DF, between 140°C and 150°C and can be calculated.

$$DF\ (between\ 140°C\ and\ 150°C) = \exp\left[\frac{0.6}{k}\left[\frac{1}{150 + 15 + 273} - \frac{1}{140 + 15 + 273}\right]\right] = 0.690$$

The derating factor between 125°C and 150°C can be similarly calculated.

$$DF\ (between\ 125°C\ and\ 150°C) = \exp\left[\frac{0.6}{k}\left[\frac{1}{150 + 15 + 273} - \frac{1}{125 + 15 + 273}\right]\right] = 0.382$$

These derating calculations assume a 15°C rise due to junction heating.

Temperature Cycling

Two different temperature cycling conditions were used to measure reliability, -65 to 150°C and -40 to 125°C. Using the brittle failure mechanism model with m = 12, the derating factor between -65 to 150°C and -40 to 125°C is calculated.

$$DF = \left(\frac{170 - (-40)}{170 - (-65)}\right)^{12} = 0.26$$

Amazingly, using the ductile failure mechanism model with m = 5.16, the same value for the derating factor between -65 to 150°C and -40 to 125°C temperature cycling is obtained.

$$DF = \left(\frac{125 - (-40)}{150 + (-65)}\right)^{5.16} = 0.26$$

HAST

The derating factor between the two HAST conditions, 140°C / 85% R.H. and 130°C / 85% R.H. is simply the ratio of the acceleration factors (See Appendix A).

$$DF = \frac{9,261}{17,433} = 0.531$$

APPENDIX D: TEMPERATURE CYCLING MODELLING EXPERIMENTS

A study was performed to calculate the temperature cycling model constant, 'm', for material with a severe wire bond breakage problem.

Test Conditions:

Machines Used:	Blue M Corp.	
	WSP-109BMP3	(-65°C to 150°C)
	TABAI TSV-40	(-10°C to 110°C)
Test Parameters:	Temperature:	Condition C (-65°C to 150°C) Commercial Range (-10°C to 100°C)
	Cycle time:	Condition C = 30 min/cycle Commercial Range = 25 min/cycle
Samples Used:	Device:	7C433 (4096 x 6 FIFO)
	Tech:	FAMOS
	Assy. Lot:	49559
	Fab. Lot:	2005302
	Package:	28.3 PDIP
	Die Size:	139 x 360 mil^2
Sample Size:	100 devices for each condition	

APPENDIX D: TEMPERATURE CYCLING MODELLING EXPERIMENTS (CONT.)

Table D.1: Temperature Cycling Experiment Raw Data

	Cumulative Number of Units failed	
Number of Temp. Cycles	Condition C (-65°C to 150°C)	Commercial Condition (-10°C to 100°C)
100	0	0
200	1	0
300	1	0
400	11	0
500	16	0
600	22	0
700	33	0
800	44	0
900	57	0
1000	60	0
6500		0
7000		0
7500		0

Because failures occurred at several different read points, the log normal distribution [1] can be used to model the Military C test condition. In log normal distribution analyses,

$$Z = (\ln N - \mu)/\sigma$$

where N is the number of cycles,
μ is the mean of the distribution, and
σ is the standard deviation.

The cumulative probability, Φ, is a function of Z and is obtained from standard normal distribution tables.

APPENDIX D: TEMPERATURE CYCLING MODELLING EXPERIMENTS (CONT.)

Table D.2: Probability Data From Temperature Cycling Experiment (Condition: -65°C - 150°C)

Total # Cycles	Total # of Fails	Cum. Probability	Z
100	0	0	------
200	1	0.01	-2.327
300	1	0.01	-2.327
400	11	0.11	-1.226
500	16	0.16	-0.995
600	22	0.22	-0.772
700	30	0.30	-0.524
800	44	0.44	-0.151
900	57	0.57	+0.176
1000	60	0.60	+0.253

The linear regression correlation coefficient for the log-normal fit is R = 0.98. From this fit,

$$\sigma = 0.571 \quad \text{and} \quad \mu = 6.787.$$

The mean number of cycles to failure, (MCTF), is [1]

$$MCTF = \exp(\mu)\ \exp(\sigma^2/2).$$

$$MCTF_{\text{Cond. C}} = \exp(6.787)\ \exp(0.571^2/2) = 886\ (1.18) = 1043 \text{ cycles}$$

For commercial conditions, since no failures have occurred in 7500 cycles, we assume that one fail occurred at 7501 cycles which gives Z = -2.327. If we assume that the failure mechanism is the same for both conditions, then the standard deviations are also the same. The mean for this distribution is then

$$-2.327 = (\ln(7501) - \mu)/0.571; \quad \mu = 10.252$$

$$MCTF_{\text{Cond. I}} = \exp(10.252)\ \exp(0.571^2/2) = 28{,}340\ (1.18) = 33{,}440 \text{ cycles}$$

APPENDIX D: TEMPERATURE CYCLING MODELLING EXPERIMENTS (CONT.)

The Manson-Coffin [2] equation will be used to estimate the acceleration factors.

$$MCTF = \tfrac{1}{2}(\gamma/(2\,\varepsilon))^{1/c}$$

where γ is the cyclic shear strain,
ε is the fatigue ductility,
and c is the fatigue ductility exponent.

For gold wire fatigue, an internal Cypress report showed,

c = -0.673 [2] (usually $-0.7 < c < -0.5$ [3]) and
ε = 3.09 (ε is used in the following calculations but its value does not affect the results)

$$\gamma_{\text{Cond. C}} = 2(3.09)(2(1043))^{-0.673} = 3.61 \times 10^{-2}$$
$$\gamma_{\text{Commercial Range}} = 2(3.09)(2(33{,}440))^{-0.673} = 3.50 \times 10^{-3}$$

The cyclic shear strain is clearly a function of stress conditions.

To extrapolate the temperature effect, the following assumptions are made.

1) The strain rate is proportional to the strain.
2) The stress is proportional to the maximum temperature difference during a cycle.
3) A power law creep relation exists (i.e. the strain rate is proportional to the stress raised to a power).

Given the above assumptions, we can fit our data to an equation of the form,

$$\gamma = \eta(\Delta T)^{\zeta}$$

where ΔT is the temperature difference per cycle in °C and η and ζ are constants calculated from the above tests. From our experimental data, $\zeta = 3.482$, and $\eta = 2.728 \times 10^{-10}$.

Assume that during actual operating conditions, the device will experience a temperature rise equivalent to the difference in the specified maximum operating temperatures 0°C and 70°C. Including a 15°C temperature rise due to junction heating, one use cycle spans 85°C.

$$\gamma_{use} = 2.728 \times 10^{-10}\,(85)^{3.482} = 1.426 \times 10^{-4}$$

$$MCTF_{use} = \tfrac{1}{2}(1.426 \times 10^{-3}/(2(3.09))^{-1.483} = 1.237 \times 10^{5} \text{ cycles}$$

The acceleration factor, AF, between Condition C and use conditions is then

$$AF = 1.237 \times 10^{5}/1043 = 119$$

APPENDIX D: TEMPERATURE CYCLING MODELLING EXPERIMENTS (CONT.)

Finally, by combining the exponents, m is found to equal 5.16 and the acceleration factor equation for this ductile failure mechanism can be written.

$$AF_{ductile} = \left(\frac{T_{max,stress} - T_{min,stress}}{T_{max,use} - T_{min,use}} \right)^{5.16}$$

References

[1] W. Hines and D. Montgomery, "Probability and Statistics in Engineering and Management Science", (New York: John Wiley), 1980.
[2] N. V. Chidambaram, "A Numerical and Experimental Study of Temperature Cycle Wire Bond Failure", CHMT/IEEE Conference, May 13-15, 1991.
[3] S. Manson, "Thermal Stress and Low Cycle Fatigue", (New York: McGraw-Hill), 1966.

APPENDIX E: HAST VERSUS 85°C/85% R.H. TEMPERATURE HUMIDITY BIAS TESTING

Cypress substitutes HAST testing (140°C/85% R.H. - JEDEC Test Method A110) for 85°C/85% R.H., because HAST produced more reliability data in less time. To certify the change, a comparison was made between the THB test conditions on two lots with known moisture sensitivity. The following table summarizes our qualification of the HAST stress test.

Table E.1: Summary of Cypress Internal HAST Qualification

Device Type: 7C168 (SRAM)						
Assy. Lot:	HAST 120°C, 85% R.H.[1]			85°C/85% R.H.		
	Sample Size	Readpoint 96 hr	Readpoint 200 hr	Sample Size	Readpoint 1000 hr	Readpoint 2000 hr
12954	50	49 fails	N/A	50	1 fail	1 fails
12710	51	1 fail	0 fails	50	0 fails	0 fails

The results from the two conditions can be directly compared, because failure analysis revealed that all failures were due to the same failure mode (i.e. moisture penetrating through topside passivation cracks). This experiment showed that 200 hours of HAST is far more effective at inducing failures than 2000 hours of 85°C/85% R.H. testing. From our 120°C/85% R.H. - 85°C/85% R.H. experimental data, we estimate that the acceleration factor between 140°C/85% R.H. and 85°C/85% R.H. is at least 21. This estimation completely discounts the 20°C temperature increase between the qualification test and our current HAST stress conditions.

Comparisons between HAST and 85°C/85% R.H. testing are difficult because devices typically do not fail at 85°C/85% R.H. conditions. Several investigators, though, have collected enough data to calculate and publish acceleration factors between HAST (130°C/85% R.H.) and 85°C/85% R.H. temperature-humidity-bias testing.

[1]Since we first introduced HAST testing, we have increased our test conditions from 120°C / 85% R.H. to our present 140°C / 85% R.H.

APPENDIX E: HAST VERSUS 85°C/85% R.H. TEMPERATURE HUMIDITY BIAS TESTING (CONT.)

Table E.2. Acceleration Factors between HAST (130°C/85% R.H.) and 85°C/85% R.H.

Source of Data	AF between HAST and 85°C/85% R.H.
Matsushita Electronics [1]	30
Intel [2]	32
I.B.M. [3]	52
Hallberg and Peck [4]	27

Cypress uses the Hallberg and Peck model to calculate acceleration factors because it combines all published HAST data between 1979-1987 into one model and is the most conservative. HAST testing has been accepted

$$t_f = A(\%RH)^{-3}\exp\left(\frac{0.9}{kT}\right)$$

by all the electronic industry associations. The following table summarizes the electronic industry association requirements.

Table E.3: Electronic Industry Associations' HAST Requirements

Source	Conditions	Duration (hours)
JEDEC (USA)	130°C - 85% R.H.	50
IEC (Europe)	130°C - 85% R.H.	96 max.
EIAJ (Japan)	120°C - 85% R.H.	10

All our information supports the conclusion that the acceleration factor between 140°C/85% R.H. and 85°C/85% R.H. is at least 20. Consequently, our 128 hour HAST test is equivalent to at least 2560 hours of 85°C/85% R.H. testing

References

[1] T. Wada, N. Maeda, M. Sugimoto, H. Higuchi, and T. Ajiki, "Moisture-Resistance Test Using Unsaturated Pressure Cooker Equipment", ISTFA, pp. 189-194, 1986.
[2] D. Danielson, G. Marcy, E. Babb and S. Kudua, "HAST Applications: Acceleration Factors and Results for VLSI Components", IEEE/Proc. IRPS, pp. 114-121, 1989.
[3] J. Gunn, R. Camenga, and S. K. Malik, "Rapid Assessment of the Humidity Dependence of IC Failure Modes by Use of HAST", IEEE/IRPS, pp. 66-72, 1983.
[4] Hallberg and Peck, "Quality and Reliability Engineering International", Vol. 7, 1991.

APPENDIX F: VOLTAGE ACCELERATION FACTORS

Time Dependent Dielectric Breakdown

The operating voltage of a device is often increased during accelerated reliability testing. The time dependent dielectric breakdown induced by the reliability test over-voltage is most often quantified with the following equation that combines both an Arrhenius temperature term and a voltage term.

$AF = \exp[\{1/(E_{EF}t_{OX})\}(V_2-V_1)] \exp[(E_A/k)\{(1/T_1)-(1/T_2)\}]$,

where t_{OX} is the oxide thickness, V_2 and V_1 are voltages, E_A is the activation energy, k is Boltzmann's constant, T_1 and T_2 are temperatures and E_{EF} is the electric-field model constant. For the above model equation only, E_{EF} is related to the often cited γ parameter through the equation,

$E_{EF} = 1/\ln 10^{\gamma}$.

The following table summarizes acceleration factor calculations for our standard 5.75 V dynamic bias burn-in conditions. The calculations assume a stress junction temperature equal to 150°C + 15°C = 165°C and a use junction temperature equal to 55°C + 15°C = 70°C.

Table F.1: Acceleration Factor Calculations of Cypress Burn-in Using Constants Derived from Different Studies

Model Constants	E_A (eV)	E_{EF} (MV/cm)	AF 28 nm gate	AF 19.5 nm gate
Crook [1]	0.3	0.062	677	4,444
Hokari [2]	1.0	0.26	4,298	6,719
Anolick and Nelson [3]	0.6	0.0724	3,298	16,500
Berman [2]	2.0*	0.0987	3.6×10^7	1.2×10^8

* The oxide breakdown voltages (~20 V for 195 Å gate technology and ~25 V for 280 Å technology) is needed for the Berman model.

Recently, a new model has been suggested [4]. This model uses a different acceleration factor equation and yields acceleration factors, for our 195 Å gate technologies, in excess of a billion.

APPENDIX F: VOLTAGE ACCELERATION FACTORS (CONT.)

Inter-oxide Defects

Cypress performed an engineering experiment to determine the voltage acceleration factor for inter-oxide defects. We determined that the voltage acceleration factor, AF_{VOLT} can be approximately modeled with the following equation.

$$AF_{VOLT} = \exp [\, 2.083 \, (V_2 - V_1)]$$

where V_2 and V_1 are in volts.

All acceleration factors used in this report do not include any voltage acceleration.

References

[1] D. L. Crook, "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown", IEEE/IRPS, pp. 1-7, 1979.

[2] J. W. McPherson and D. A. Baglee, "Acceleration Factors for Thin Gate Oxide Stressing", IEEE/IRPS, pp. 1-5, 1985.

[3] E. S. Anolick and G. R. Nelson, "Low Field Time Dependent Dielectric Integrity", IEEE/IRPS, pp. 8-12, 1979.

[4] I. C. Chen and Chenming Hu, "Accelerated Testing of Time-Dependent Breakdown of SiO_2", IEEE/Electron Dev. Lett., Vol EDL-8, No.4, pp. 140-142, 1987.

APPENDIX G: EVALUATION OF ESD PERFORMANCE OF COMPETITOR PRODUCT

A comparison study was made between Cypress Semiconductor 256k SRAMs (CY7C199) Human Body Model (HBM) ESD performance and two of our competitors, Company H and Company T. The units were tested in accordance with Mil-STD-883, Method 3015.7. The voltage level was incrementally increased until the maximum passing voltage was determined, with new devices being tested at each voltage level. The results are summarized below.

Company H

Although Company H uses a very complicated ESD structure, the performance of their structure was not extraordinary. The maximum pass voltage was 2200 volts. At 3300 V, 14 out of the 28 pins failed. The use of three different polysilicon resistors may have a major effect on the reliability of Company H's structure. Polysilicon resistors are thermally insulated with oxide layers. During the heating associated with an ESD event, these resistors can evaporate causing failure.

Company T

Company T's structure has a grounded gate FET for input protection. The maximum pass voltage is approximately 5000 volts. The V_{CC} pin fails at 5500 V.

Cypress Semiconductor

CY7C199 employs a grounded gate FET connected to the bond pad and a Field FET connected to the bond pad through a diffused resistor. Our ESD pass voltage levels are high, ranging from 5,500 to 10,000 volts, 7000 V is typical.

Table G.1 Summary of Competitor ESD Study

Company	H	T	Cypress Semi. Assy. date 1992
Protection Scheme	Complex structure with Field FETs and ThinOx FETs	Grounded Gate FET	Grounded Gate FET and Field FET
Area (mil^2)	75	56	44
Input Resistance	8 squares of poly	Unavailable	80 ohms
Max ESD Pass Voltage	2,200 V	5,000 V	5,500 to 10,000 V

APPENDIX H: BRIEF DESCRIPTIONS OF TECHNOLOGY FAMILIES

BiCMOS

Our BiCMOS process is a 0.8 micron, 17 mask, single-poly, double-metal technology. This process features twin buried layers and wells, an advanced LOCOS isolation, $TiSi_2$ poly, dual LDD FETs, and planarized double layer metal. The NPN transistors contain deep N+ (sinker) implants, intrinsic and extrinsic bases, and polysilicon emitters. First metal contacts (1.2 x 1.2 μm^2) are made to NPN poly emitters, FET gates and resistors, silicon bases, collectors and FET source/drains. First layer metallization consists of a highly reliable composite of Ti-TiW-AlSi (600 nm) - Ti. This approach insures excellent electromigration resistance, eliminates contact spiking, and minimizes hillocks. First layer metal contacts second layer metalization through conventional vias (1.6 x 1.6 μm^2). Second layer metal consists of 150 nm of Ti and 900 nm of Al(Si 1%). Metal pitches are 2.6 µm for first layer metal and 3.6 µm for the second.

FLASH

Our FLASH technology is a twin-well CMOS process with a grounded p-substrate, standard LOCOS isolation, double poly, and double metal. Excellent planarization is obtained from our chemical mechanical polished interlayer dielectric process. The design rules are similar to our 0.8 µm FAMOS technology with the addition of fast 0.65 µm LDD transistors for performance. The FLASH cell uses a conventional floating-gate transistor to program a cell while cell erase is achieved by Fowler-Nordheim tunneling through the 10 nm floating gate oxide. Our cell avoids the reliability risks of other FLASH approaches, over-erase and disturb, by using a unique 2 1/2 transistor cell architecture. Metal 1 is composed of 600 nm of Al(Si 1%) with a 120 nm TiW cap. Metal 2 is composed of a 150 nm TiW layer followed by 900 nm of Al(Si 1%) and a 32 nm TiW cap.

FAMOS

Our FAMOS technology uses LOCOS isolation, LDD junctions for optimum reliability and performance, double poly, and double metal layers. The minimum transistor dimension for this CMOS process is 0.65 µm; the control gate oxide thickness is 16.5 nm; and the floating gate oxide is 22.5 nm thick. Metal 1 is composed of 50 nm of Ti, 120 nm of TiW, 600 nm of Al(Si 1%) followed by a 120 nm thick TiW cap. Our Metal 2 stack contains 150 nm of Ti, 120 nm of TiW, 900 nm of Al(Si 1%) followed by 32 nm of TiW.

SRAM/LOGIC

Second Generation

Our SRAM/LOGIC technology uses a back-bias substrate CMOS process with standard LOCOS isolation, LDD junctions for optimum reliability and performance, double poly, and single metal layers. A chemical-mechanical-polished interlayer dielectric process is used to obtain superior planarization. The minimum transistor dimension is 0.8 µm and the gate oxide thickness is 19.5 nm. Metal 1 is composed of 50 nm of Ti, 120 nm of TiW, 600 nm of Al(Si 1%) followed by a 12 nm TiW cap with a minimum width of 1.3 µm and a minimum pitch of 2.6 µm. Metal 2 consists of a 150 nm TiW barrier layer followed by 1000 nm of Al(Si 1%).

APPENDIX H: BRIEF DESCRIPTIONS OF TECHNOLOGY FAMILIES (CONT.)

Third Generation

Our SRAM/LOGIC technology uses a CMOS process with standard LOCOS isolation, LDD junctions for optimum reliability and performance, double poly, double metal layers. The minimum transistor dimension is 0.50 µm and the gate oxide thickness is 16.5 nm. Metal 1 is composed of 50 nm of TiW, and 600 nm of Al(Cu), and 120 nm of TiW. Metal 2 is composed of 50 nm of TiW, 1 µm of Al(Cu), and 30 nm of Ti.

APPENDIX I: ESD DATA SUMMARY

CYPRESS PART #	PASSING HBM (V)	PASSING CDM (V)	CYPRESS PART #	PASSING HBM (V)	PASSING CDM (V)
CY100E383	Class 2	2000	CY7B139	-----	2000
CY100E474	Class 2	2000	CY7B145	Class 3	1500
CY100EL474	Class 2	2000	CY7B166	Class 2	1500
CY10E422	Class 3	2000	CY7B166	Class 3	-----
CY10EL484	Class 2	2000	CY7B173	Class 2	2000
CY2028	Class 1	-----	CY7B180	Class 2	-----
CY2061	Class 3	-----	CY7B923	Class 3	2000
CY2063	Class 1	-----	CY7B933	Class 3	2000
CY2071	Class 2	2000	CY7B9392	Class 3	2000
CY2093	Class 2	-----	CY7B951	Class 3	2000
CY2254	Class 2	500	CY7B991	Class 3	2000
CY2255	Class 1	200	CY7B9910	-----	2000
CY2260	Class 2	500	CY7B992	Class 3	2000
CY2291	Class 3	2000	CY7C025	Class 2	1000
CY2292	Class 2	-----	CY7C068	Class 1	-----
CY27C010	Class 2	1000	CY7C1009	Class 2	-----
CY2907	Class 3	2000	CY7C1031	Class 2	1000
CY2954	Class 1	-----	CY7C106	Class 1	1500
CY2955	Class 1	-----	CY7C108	-----	1500
CY2958	Class 2	-----	CY7C109	Class 2	1000
CY6233	Class 3	-----	CY7C1199	Class 2	2000
CY74FCT138	Class 3	-----	CY7C122	Class 2	-----
CY74FCT16244	Class 2	2000	CY7C123	Class 2	200
CY74FCT162543	Class 2	2000	CY7C128	Class 2	2000
CY74FCT244	Class 2	-----	CY7C135	Class 3	1500
CY74FCT273	Class 3	-----	CY7C136	Class 2	1500
CY74FCT3384	Class 2	-----	CY7C1399	Class 2	200
CY74FCT373	Class 3	-----	CY7C147	Class 2	-----
CY74FCT374	Class 3	-----	CY7C148	Class 2	-----
CY74FCT377	Class 3	-----	CY7C150	Class 2	-----
CY74FCT480	Class 3	-----	CY7C152	Class 3	-----
CY74FCT521	Class 3	-----	CY7C162	-----	2000
CY74FCT540	Class 1	-----	CY7C164	-----	2000
CY74FCT541	Class 3	-----	CY7C166	-----	2000
CY74FCT543	Class 2	-----	CY7C168	-----	500
CY74FCT548	Class 3	-----	CY7C171	-----	500
CY74FCT573	Class 3	-----	CY7C172	-----	2000
CY74FCT574	Class 3	-----	CY7C178	-----	500
CY74FCT646	Class 3	-----	CY7C182	-----	1000
CY74FCT818	Class 3	-----	CY7C185	Class 2	2000
CY74FCT825	Class 3	-----	CY7C187	-----	2000
CY74FCT827	Class 3	-----	CY7C188	Class 2	1500
CY7B1099	Class 2	1500	CY7C190	Class 2	-----
CY7B138	Class 3	-----	CY7C198	Class 2	2000

APPENDIX I: ESD DATA SUMMARY

CYPRESS PART #	PASSING HBM (V)	PASSING CDM (V)	CYPRESS PART #	PASSING HBM (V)	PASSING CDM (V)
CY7C199	Class 2	2000	CY7C971		
CY7C225	-----	1000	CY82C691	Class 2	1000
CY7C2291	Class 3	-----	CY82C692	Class 1	1000
CY7C235	-----	1000	CY82C693	Class 2	1000
CY7C243	Class 2	-----	CY9159	Class 2	-----
CY7C251	Class 1	-----	PAL16L8	Class 3	-----
CY7C256	Class 3	1000	PAL22V10	Class 2	-----
CY7C258	Class 3	-----	PAL22V10C	Class 1	-----
CY7C266	Class 2	-----	PAL22V10D	Class 3	2000
CY7C270	Class 1	-----	PALC22V10B	Class 2	-----
CY7C271	Class 3	-----	PALCE16V8	Class 2	1000
CY7C274	Class 3	500			
CY7C279	Class 2	-----			
CY7C286	Class 3	-----			
CY7C287	Class 2	-----			
CY7C291	Class 1	-----			
CY7C331	Class 1	1000			
CY7C335	Class 3	1000			
CY7C341	Class 1	500			
CY7C342	Class 2	1000			
CY7C346	Class 1	-----			
CY7C371	Class 3	2000			
CY7C372	Class 3	1000			
CY7C373	Class 2	1000			
CY7C374	Class 2	1000			
CY7C375	Class 3	-----			
CY7C382	Class 3	2000			
CY7C384	Class 3	1000			
CY7C386	Class 3	2000			
CY7C387	Class 3	1500			
CY7C388	Class 3	1500			
CY7C404	-----	2000			
CY7C409	-----	500			
CY7C421	Class 2	-----			
CY7C4245	Class 3	1000			
CY7C425	Class 2	2000			
CY7C429	-----	1000			
CY7C433	Class 2	2000			
CY7C455	Class 2	1500			
CY7C457	Class 1	-----			
CY7C464	-----	1500			
CY7C470	Class 3	-----			
CY7C474	-----	500			
CY7C517	Class 1	-----			

APPENDIX J: PRODUCT RELIABILITY FAMILIES

The following table can be used to determine the product reliability family for each product. To assist with grouping like products, two short-hand symbols have been used.

* Signifies that any number of alpha-numeric characters can follow.
? Signifies that any single alpha-numeric character can be substituted.

PART NUMBER	PRODUCT RELIABILITY FAMILY
CY7C0*	SRAM/LOGIC
CY7C1*, EXCEPT CY7C10E* OR CY7C101E*	SRAM/LOGIC
CY7C4*	SRAM/LOGIC
VIC* OR VAC*	SRAM/LOGIC
CY7C9*	SRAM/LOGIC
CY54FCT*	SRAM/LOGIC
CY74FCT*	SRAM/LOGIC
ICD*	SRAM/LOGIC
CY????	SRAM/LOGIC
CY7C10E* OR CY7C101E*	BiCMOS
CY7B*	BiCMOS
CYM*	MODULE
CY27*	FAMOS
CY7C2*	FAMOS
CY7C3*, EXCEPT CY7C37*	FAMOS
PAL*	FAMOS
PLD*	FAMOS
CY7C37*	FLASH

APPENDIX K: CYPRESS RELIABILITY TEST DATA

Stress Test Description

TEST	DESCRIPTION
BNDPL	Bond Pull
CONST	Constant Acceleration
DRET	Plastic Data Retention Test
DRET2	Ceramic Data Retention Test
EOS	Electronic Overstress Failure Test
ESD	Electronic Static Discharge Failure Test
LDFAT	Lead Fatigue Test
LDFIN	Adhesion of Lead Finish Test
PCT	Pressure Cooker Test
HAST	Highly Accelerated Saturation Test
H2OVA	Water Vapor Test
HTOL	High Temperature Operating Life Test
HTS	High Temperature Storage Test
HTSSL	High Temperature Steady State Life Test
MARKP	Mark Permanence Test
MECHS	Mechanical Shock Test
MOISR	Moisture Resistance Test
PHYSD	Physical Dimension Test
SALTA	Salt Atmosphere Test
SOLDE	Solderability Test
TC	Temperature Cycling Test
THRMS	Thermal Shock Test
VIBR	Vibration Test