CYPRESS UNVEILS CPLDs AT FPGA DENSITIES™

Delta39K™ CPLDs Offer Ease-of-Use, Performance, and Non-Volatility at up to 350,000 Gates

SAN JOSE, Calif., May 24, 1999 -- Cypress Semiconductor (NYSE:CY) today announced the world's largest complex programmable logic devices (CPLDs). Cypress's new Delta39K™ CPLDs will reach 350,000 usable gates, approximately ten times the size of today's largest CPLD. The family offers more embedded memory (240 Kbits for the 100,000-gate Delta39K100) than any other programmable logic device, including even the largest field-programmable gate arrays (FPGAs). Delta39K is also the first programmable logic device to embed FIFO control and dual-port memory arbitration logic into each specialty memory block. This significantly reduces the logic required, increases the system performance, and speeds the design cycle of any application utilizing FIFO or dual-port memory.

Delta39K CPLDs offer blazing performance with a 6.5 ns pin-to-pin propagation delay and 300 MHz system performance – more than fast enough to implement a fully synthesizable, 64-bit, 66-MHz PCI core. A programmable, spread-aware PLL, with unparalleled multiply, divide, and clock edge control options, provides four global clocks to all logic clusters, memories, and I/O cells to maintain precise on and off-chip timing.

The Delta39K family also maintains Cypress's highly regarded In-System Reprogrammability (ISR™). ISR gives designers the flexibility to add to and change a design with the confidence that speed and pinout will not be altered. With FPGAs, designers can't be sure of a design's performance until after place and route is complete. Unlike FPGAs, Delta39K's CPLD architecture allows all pin-to-pin delays to be specified in the data sheet, regardless of where logic is placed or which routing path through the device is used.

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The devices are manufactured on a 0.18-micron, six-layer metal process at TSMC. This is the most aggressive process ever used for a programmable logic device, and provides high performance with very low power consumption (less than 100 microamps at 1.8 V). In addition to using an aggressive process technology, Cypress is also offering innovative packaging options that embed a non-volatile flash memory die in the same package as the Delta39K die. This creates a unique non-volatile solution and eliminates the need for an external boot PROM. This package option provides In-System Reprogrammability via a standard JTAG hardware interface using the recently approved STAPL programming language.

“Cypress is bringing the well-recognized advantages of our CPLDs, namely speed, ISR, ease-of-use, and non-volatility, to FPGA densities,” said Dan McCranie, Cypress’s executive vice president of sales and marketing. “These features along with an abundance of memory, built-in FIFOs, a library of cores, and very low power consumption, create a winning combination unlike any other on the market today.”

Delta39K Architecture

The Delta39K architecture consists of logic block clusters (LBCs), each of which has 128 macrocells (eight, 16-macrocell logic blocks) connected by a Programmable Interconnect Matrix (PIM™). Each LBC has 16 Kbits of single-port SRAM cluster memory (two 8 Kbit blocks) configurable as synchronous or asynchronous and as x1, x2, x4, or x8. The cluster memory can be cascaded with other cluster memory blocks to implement larger memory functions. If a cluster memory block is not specifically utilized by the designer, Cypress’s *Warp*™ software will automatically use it to implement large clusters of logic. This increases the effective density of a Delta39K device by more than 20%.

In addition to the cluster memory blocks, each LBC also has a "channel" memory block associated with it. The 4 Kbit channel memory uses Cypress’s true-dual-ported cell to offer optimized dual-port and FIFO memory with completely independent write and read clocks. Each channel memory block also includes FIFO control (programmable flags) and dual-port arbitration logic required to

implement extremely fast and powerful specialty memory functions. In FPGA devices, implementing a simple FIFO can utilize as much as 25% of a device's logic capacity, and results in a much slower circuit. The Delta39K100 device will offer FIFO performance as high as 250MHz. The channel memory, like the cluster memory, is configurable as x1, x2, x4, or x8, and can be width and/or depth expanded.

The LBCs and the channel memory blocks communicate via abundant vertical and horizontal routing channels. Each channel of interconnect carries signals across the entire length of the device without adding any delays. These channels also connect to a block of I/O pins at each end to provide maximum pinout flexibility and true In-System-Reprogrammability.

The Delta39K family offers an array of voltage options. The core operates at 1.8-V, and Cypress uses an on-chip voltage regulator to support 2.5-V and 3.3-V power supplies as well. The Delta39K family also supports 3.3-V, 2.5-V, and 1.8-V I/O voltages. Delta39K also offers support for a broad array of I/O standards, including LVTTL, LVCMOS, 3.3V PCI, HSTL (I-IV), SSTL-2 (I, II), SSTL-3 (I, II), and GTL+.

"The Delta39K family showcases the breadth of Cypress's intellectual property," said Christopher Norris, vice president of Cypress's Programmable Logic Division. "We have combined our programmable logic design experience of over 10 years with our PLL, SRAM, and specialty memory expertise to deliver a highly differentiated, market leading CPLD family."

Software Support

The Delta39K CPLDs will be supported by Cypress's industry-leading *Warp* design tools. The *Warp* tools accept VHDL and Verilog HDL as input, and perform synthesis, technology mapping, and fitting all in one easy-to-use design environment. Cypress will also offer an architecture viewer, graphic timing analyzer, and full LPM support for implementing custom memory blocks. In addition to *Warp*'s powerful logic synthesis capability (specifically tuned to the Delta39K architecture), it will employ advanced mapping algorithms that automatically fit appropriate logic equations into RAM blocks significantly increasing the overall logic density of the device.

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Price and Availability

The Delta39K family includes eight device densities ranging from 50,000 to 350,000 gates. Software support and samples of the 100,000-gate Delta39K100 are planned for the fourth quarter. The Delta39K50, Delta39K75, Delta39K130, Delta39K165, and Delta39K200 will sample in Q1 2000, with 250,000 and 350,000 gate devices slated for the second half of 2000. Volume pricing for the 50,000-gate Delta39K50 is projected to be below $10. Customers can call Cypress at (800) 858-1810 in the U.S. or (408) 943-2600, or visit www.cypress.com.

Cypress Semiconductor Corporation, headquartered in San Jose, California, provides a broad range of integrated circuits for leading computer, networking, and telecommunications companies worldwide. Cypress's products include static RAM and specialty memories, programmable logic devices (PLDs), data communications products, timing devices, and USB microcontrollers. Its shares are listed on the New York Stock Exchange under the symbol CY, and its web site is http://www.cypress.com.

"Safe Harbor" Statement under the Private Securities Litigation Reform Act of 1995: Statements herein that are not historical facts are "forward-looking statements" involving risks and uncertainties. Please refer to Cypress's Securities and Exchange Commission filings for a discussion of such risks.

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