

CYPRESS ROLLS OUT ENTIRE Ultra37000™ CPLD FAMILY

All 14 Devices from 32 to 512 Macrocells Supported by *Warp*™ Software Rel. 5.1

SAN JOSE, Calif., January 18, 1999 -- Cypress Semiconductor (NYSE:CY) today announced that it is accepting samples orders for the entire family of Ultra37000™ Complex Programmable Logic Devices (CPLDs), and that all of the devices will be in full production by the end of this quarter. The entire family of devices is supported by Release 5.1 of Cypress's \$99 *Warp2*® design tools.

Cypress's Ultra37000 CPLD family consists of 14 devices, ranging from 32 to 512 macrocells. It offers a simple, fixed timing model that guarantees pin-to-pin propagation delays as fast as 5 ns for the 32-macrocell device, and 7.5 ns for the 256-macrocell device. Available in both 3.3-V and 5-V versions (the 3.3-V devices are 5-V tolerant), the family also offers Cypress's In-System Reprogrammability (ISR™), which assures that logic changes won't affect pinouts or critical timing.

"We introduced the first device in mid 1998, and have rolled out the rest of the family in only 6 months," said Christopher Norris, vice president of Cypress's programmable logic division. "Today, 3.3V and 5V versions of both the 256- and 192-macrocell devices are in full production, and the entire family will be in production by the end of this quarter."

Cypress's ISR Advantage

In many CPLDs, changes in logic often cannot fit into original pinouts and/or alter critical timing paths--rendering design changes useless without a new board layout. This is especially true at high densities where other CPLD vendors have implemented hierarchical interconnect, which compromises performance and introduces variable delays. Cypress has extended its unique pin-locking and "speed-locking" to 512 macrocells. Users benefit from faster real-world system performance, and true ISR from fixed timing and abundant routing resources.

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Software and Programming Support

The Ultra37000 CPLDs are supported by Cypress's industry-leading *Warp* design tools. Cypress is the leading supplier of VHDL-based programming tools with over 20,000 installed *Warp* seats worldwide. Cypress is offering Jam programming support for the new family as well. The Jam programming language is an open standard that allows automated test equipment (ATE) and on-board microcontrollers to program the devices.

The Ultra37000 CPLDs' ISR function is implemented through a JTAG-compliant serial interface. They also feature full JTAG boundary-scan for system testing. The devices are fully compliant with the PCI Local Bus specification, meeting all electrical and timing requirements.

The Ultra37000 family includes 5-V and true 3.3-V versions of the 32-macrocell CY37032(V), the 64-macrocell CY37064(V), the 128-macrocell CY37128(V), the 192-macrocell CY37192(V), the 256-macrocell CY37256(V), the 384-macrocell CY37384(V), and the 512-macrocell CY37512(V).

Price and Availability

Cypress is accepting sample requests for every member of the Ultra37000 family now, and will have all devices in full production by the end of this quarter. Pricing ranges from \$1.25 for the Ultra37032 to \$49.00 for the Ultra37512, both in high-volume quantities. Customers can contact Cypress at (800) 858-1810 in the U.S. or (408) 943-2600 elsewhere, or visit www.cypress.com.

Cypress Semiconductor Corporation is an international supplier of high-performance integrated circuits with worldwide headquarters in San Jose, California. The company provides a broad range of products for leading computer, networking, and telecommunications companies worldwide. Cypress's product line includes static RAM and specialty memories; programmable logic devices (PLDs); data communications products; FCT logic; and personal computer timing devices and USB microcontrollers. Its shares are listed on the New York Stock Exchange under the symbol CY. The company's worldwide web site is <http://www.cypress.com>.

"Safe Harbor" Statement under the Private Securities Litigation Reform Act of 1995: Statements herein that are not historical facts are "forward-looking statements" involving risks and uncertainties. Please refer to Cypress's Securities and Exchange Commission filings for a discussion of such risks.

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