AddressingModes

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Chapter 1

AddressingModes

1.1 M68000 Family Addressing Modes

```
      M68000 Family Addressing Modes
      ------------------------------
```

The M68000 Family knows 18 different addressing modes.

ASM-One supports all of them, but there are possibilities to surpress elements in addressing modes. So here's an complete list of all possible addressing modes.

Special symbols are used. Here is an explenation of them.

```
   Data Register Direct Mode
   Address Register Direct Mode
   Address Register Indirect Mode
   Address Register Indirect with Postincrement Mode
   Address Register Indirect with Predecrement Mode
   Address Register Indirect with Displacement Mode
   Address Register Indirect with Index (8-bit Displacement) Mode
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   Immediate Data
```

1.2 Data Register Direct Mode

```
    Data Register Direct Mode
```

```
    -------------------------

Assembler Notation :  Dn
ASM-One Notation   :  Dn
Processor          :  All

Example:

  MOVE.L  D0,D1
```

1.3 Address Register Direct Mode

```
    Address Register Direct Mode
    ----------------------------

Assembler Notation :  An
ASM-One Notation   :  An
Processor          :  All

Example:

  SUB.L A1,A2
```

1.4 Address Register Indirect Mode

```
    Address Register Indirect Mode
    ------------------------------

Assembler Notation :  (An)
ASM-One Notation   :  (An)
Processor          :  All

Example:

  ADDI.W  #1,(A3)
```

1.5 Address Register Indirect with PostincrementMode

```
    Address Register Indirect with Postincrement Mode
    -------------------------------------------------

Assembler Notation :  (An)+
ASM-One Notation   :  (An)+
Processor          :  All

Example:

  MOVE.B  (A5)+,D0
```

1.6 Address Register Indirect with Predecrement Mode

```
    Address Register Indirect with Predecrement Mode
    ------------------------------------------------

Assembler Notation :  -(An)
ASM-One Notation   :  -(An)
Processor          :  All

Example:

  MOVEM.L D0-A6,-(A7)
```

1.7 Address Register Indirect with Displacement Mode

```
    Address Register Indirect with Displacement Mode
    ------------------------------------------------

Assembler Notation :  (d16,An)
ASM-One Notation   :  d16(An)
      (d16,An)
Processor          :  All

Example:

label:  MOVE.L  $7FFF(A2),D0
  MOVE.L  label(A6),D2
  MOVE.L  [begin-end](A4),D5


begin:  DC.L  0
end:  DC.L  0
```

1.8 Address Register Indirect with Index (8-bit Displacement) Mode

```
    Address Register Indirect with Index (8-bit Displacement) Mode
    --------------------------------------------------------------

Assembler Notation : (d8,An,Xn.SIZE*SCALE)
ASM-One Notation   : (d8,An,Xn.SIZE*SCALE)
Processor          : Without SCALEing: All
         With SCALEing: 68020 and up
Remark       : Default SIZE is W (Word)
         Default SCALE is 1

Example:

label:  MOVE.L  $7FFF(A2),D0
  MOVE.L  label(A6),D2
  MOVE.L  [begin-end](A4),D5
```

```
begin:  DC.L  0
end:  DC.L  0
```

1.9 Address Register Indirect with Index (Base Displacement) Mode

```
    Address Register Indirect with Index (Base Displacement) Mode
    -------------------------------------------------------------

Assembler Notation   : (bd,An,Xn.SIZE*SCALE)
ASM-One Notation     : (An,Xn,bd)
           (An,Xn.SIZE,bd)
           (An,Xn*SCALE,bd)
           (An,Xn.SIZE*SCALE,bd)
Processor            : 68020 and up
Surpressable Elements: An, Xn and bd
Remark         : Default SIZE is W (Word)
           Default SCALE is 1

Example:

label:  MOVE.L  (A2,D2,label),D0
  MOVE.L  (A6,A3.W*4),D2
  MOVE.L  (A4,D5.L,[end-begin]),D5


begin:  DC.L  0
end:  DC.L  0
```

1.10 Memory Indirect Postindexed Mode

```
    Memory Indirect Postindexed Mode
    --------------------------------

Assembler Notation   : ([bd,An],Xn.SIZE*SCALE,od)
ASM-One Notation     : ([bd,An],Xn.SIZE*SCALE,od)
Processor            : 68020 and up
Surpressable Elements: An, Xn, bd and od
Remark         : Default SIZE is W (Word)
           Default SCALE is 1

Example:

label:  MOVE.L  ([$7FFFFF,A2],D2,$7FFFFF),D0
  MOVE.L  ([A6],A3.W*4),D2
  MOVE.L  ([A4],D5.L,$7FFF.W),D5
```

1.11 Memory Indirect Preindexed Mode

```
    Memory Indirect Preindexed Mode
    -------------------------------

Assembler Notation   : ([bd,An,Xn.SIZE*SCALE],od)
ASM-One Notation     : ([bd,An,Xn.SIZE*SCALE],od)
Processor            : 68020 and up
Surpressable Elements: An, Xn, bd and od
Remark         : Default SIZE is W (Word)
           Default SCALE is 1

Example:

label:  MOVE.L  ([$7FFFFF,A2,D2],$7FFFFF),D0
  MOVE.L  ([A6,A3.W*4]),D2
  MOVE.L  ([A4,D5.L],$7FFF.W),D5
```

1.12 Program Counter Indirect with Displacement Mode

```
    Program Counter Indirect with Displacement Mode
    -----------------------------------------------

Assembler Notation   : (d16,PC)
ASM-One Notation     : (d16,PC)
         : d16(PC)
Processor            : All

Example:

label:  MOVE.L  (label,PC),D0
  RTS
```

1.13 Program Counter Indirect with Index (8-bit Displacement) Mode

```
    Program Counter Indirect with Index (8-bit Displacement) Mode
    -------------------------------------------------------------

Assembler Notation   : (d8,PC,Xn.SIZE*SCALE)
ASM-One Notation     : (d8,PC,Xn.SIZE*SCALE)
Processor            : Without SCALEing: All
           With SCALEing: 68020 and up
Remark         : Default SIZE is W (Word)
           Default SCALE is 1

Example:

label:  MOVE.L  ($7F,PC,D2.W*4),D0
  RTS
```

1.14 Program Counter Indirect with Index (Base Displacement) Mode

```
    Program Counter Indirect with Index (Base Displacement) Mode
    ------------------------------------------------------------

Assembler Notation   : (bd,PC,Xn.SIZE*SCALE)
ASM-One Notation     : (bd,PC,Xn.SIZE*SCALE)
Processor            : 68020 and up
Surpressable Elements: An, Xn, and bd
Remark         : Default SIZE is W (Word)
           Default SCALE is 1
Note         : A PC of ZERO is represented by the ZPC symbol

Example:

label:  MOVE.L  (label,PC,D2.W*4),D0
  MOVE.L  (label,ZPC,D2.W*4),D0
  RTS
```

1.15 Program Counter Memory Indirect Postindexed Mode

```
    Program Counter Memory Indirect Postindexed Mode
    ------------------------------------------------

Assembler Notation   : ([bd,PC],Xn.SIZE*SCALE,od)
ASM-One Notation     : ([bd,PC],Xn.SIZE*SCALE,od)
Processor            : 68020 and up
Surpressable Elements: An, Xn, bd and od
Remark         : Default SIZE is W (Word)
           Default SCALE is 1
Note         : A PC of ZERO is represented by the ZPC symbol

Example:

label:  MOVE.L  ([label,PC],D2.W*4,$7FFFFF),D0
  MOVE.L  ([label,ZPC],D2.W*4,$7FFFFF),D0
  RTS
```

1.16 Program Counter Memory Indirect Preindexed Mode

```
    Program Counter Memory Indirect Preindexed Mode
    -----------------------------------------------

Assembler Notation   : ([bd,PC,Xn.SIZE*SCALE],od)
ASM-One Notation     : ([bd,PC,Xn.SIZE*SCALE],od)
Processor            : 68020 and up
Surpressable Elements: An, Xn, bd and od
Remark         : Default SIZE is W (Word)
           Default SCALE is 1
Note         : A PC of ZERO is represented by the ZPC symbol

Example:
```

```
label:  MOVE.L  ([label,PC,D2.W*4],$7FFFFF),D0
  MOVE.L  ([label,ZPC,D2.W*4],$7FFFFF),D0
  RTS
```

1.17 Absolute Short Addressing Mode

```
    Absolute Short Addressing Mode
    ------------------------------

Assembler Notation   : (xxx).W
ASM-One Notation     : (xxx).W
Processor            : All

Example:

label:  MOVE.L  ($7FF).W,D0
  RTS
```

1.18 Absolute Long Addressing Mode

```
    Absolute Long Addressing Mode
    -----------------------------

Assembler Notation   : (xxx).L
ASM-One Notation     : (xxx).L
Processor            : All

Example:

label:  MOVE.L  (label).L,D0
  RTS
```

1.19 Immediate Data

```
    Immediate Data
    --------------

Assembler Notation   : #xxx
ASM-One Notation     : #xxx
Processor            : All

Example:

label:  MOVE.L  #label,D0
  RTS
```

1.20 Explenation of Used Symbols

Symbol	Explenation
Dn	Data Register, n = 0-7
An	Address Register, n = 0-7
PC	Program Counter
ZPC	Zero Program Counter
Xn	Index Register, X = A or D, n = 0-7
d8	8-bit Displacement
d16	16-bit Displacement
bd	Base Displacement
od	Outer Displacement
SIZE	Index Register Size, could be nothing, W or L
SCALE	Index Register Scaling, could be nothing, 1, 2, 4, or 8